Appendix A - Errata

Errata 1 – Correction to Figure 12 in [P.III].

Figure 12 is now depicted as:

It should be shown as:

Fig. 12 The equivalent Logic circuit for determining the faulty phase.
Errata 2 – Correction to equation (6) in [P.V] and equation (8) in [P.VI].

The equation (6) in [P.V] now reads:

\[ P_{u(\text{Feeder}_j)}(k) = \sum_{n=k-2N+1}^{k} |d3_{u_a}(n) \times d3_{la(\text{Feeder}_j)}(n)| \]  

It should be written as:

\[ P_{u(\text{Feeder}_j)}(k) = \sum_{n=k-2N+1}^{k} d3_{u_a}(n) \times d3_{la(\text{Feeder}_j)}(n) \]  

(6)

The equation (8) in [P.VI] now reads:

\[ P_{d3}(k) = \sum_{n=k-2N+1}^{k} |d3_{u_r}(n) \times d3_{i_r}(n)| \]  

It should be written as:

\[ P_{d3}(k) = \sum_{n=k-2N+1}^{k} d3_{u_r}(n) \times d3_{i_r}(n) \]  

(8)