Integrated Radio Frequency LO Circuits for Beamforming Receivers

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Abstract

5th generation (5G) New Radio (NR) demands high data-rate connections for wireless channels that are crowded by interference signals, especially the frequency range 1 (FR1). On the other hand, the desire to integrate more functionality on the same integrated circuit (IC) calls for receivers to operate over a band of several GHz without off-chip channel filters. Beamforming is one effective way to reduce interference and improve the signal-to-noise ratio to enable higher data-rate connections. The choice of beamforming approach impacts the footprint of the receiver’s signal chain, and the required dynamic range for blocks before summation. Analog beamforming is a strong candidate for the 5G NR either as a standalone solution or as part of hybrid beamforming, because it reduces the footprint and dynamic range requirements, particularly for the analog-to-digital converters (ADCs). This thesis concentrates on the design of local oscillator (LO) circuits for phase-tuning and true-time-delay beamforming receivers. This is because it can maintain orthogonal gain and phase-tuning, simplify the calibration procedure as well as conserve the linearity and noise figure of the radio frequency (RF) signal path.

The research presented in this thesis is based on three receiver front-ends, the focus being the development of LO circuits to enable beamforming. Design 1 is a 2-5.5 GHz 4-element beamforming receiver front-end that applied LO phase-tuning with a >7-bit phase-resolution and 360° tuning range. The developed delay line provides divider-less I/Q generation and a compact design (0.008 mm²) with moderate power consumption (2.23-5.6 mW for the reported range) favoring integration of a higher number of beamforming elements. The phase calibration scheme includes pilot-signal generation and baseband detection, being able to measure phase mismatches up to 1° (detection through external devices).

Design 2 introduces a new true-time-delay (TTD) beamforming architecture that applies RF resampling to generate time-delay through discrete-time signal processing. The pulse-skipped LO concept was developed to empower TTD beamforming for large arrays. The implemented LO chain’s delay-tuning range with pulse-skipping extends to 3 carrier cycles suitable for an 8-element TTD array. The receiver, operating in 0.6-4 GHz, achieved squint-free beamforming for modulation bandwidth as large as 40% of the LO frequency. Design 3 concentrates on developing LO circuits with mixed-signal techniques for operation at 12-25 GHz to drive the Gilbert cell mixer of the first stage of a heterodyne receiver. The LO chain comprises pulse generation and varactor based phase-tuning blocks. The measurements demonstrate that rail-to-rail LO signalling can be generated, processed and propagated up to 25 GHz in deep submicron processes.

Keywords Integrated circuits, RF, CMOS, receivers, beamforming, LO, phase-tuning, true-time-delay.
Preface

In the name of God, the Merciful, the Beneficent.

This dissertation is the result of research work conducted between 2017 and 2021 in the department of Electronics and Nanoengineering, School of Electrical Engineering, Aalto University. The research conducted for this thesis was funded by the Academy of Finland, Business Finland, and Aalto University.

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This dissertation could not have been completed without the encouragement of my parents, friends and siblings. The dictionary falls short of words to thank you for supporting me throughout these years.

Espoo, January 14, 2022,

Mahwish Zahra
# Contents

**Preface**  
i

**Contents**  
iii

**List of Publications**  
v

**Author's Contribution**  
vii

## 1. Introduction  
1.1 Background  
1.2 Objective of This Work  
1.3 Contents of This Dissertation  
1.4 Main Scientific Merits  
3

## 2. Beamforming for Radio Receivers  
2.1 Radio Receivers  
2.2 Tuning in Phased Arrays  
2.2.1 Beam Squint  
2.2.2 Phase/Time-Delay Tuning Resolution  
2.2.3 Calibration  
2.3 Beamforming Approaches  
2.3.1 Analog Beamforming  
2.3.2 Digital Beamforming  
2.3.3 Hybrid Beamforming  
2.4 Analysis of Analog Beamforming  
2.4.1 RF Phase-tuning  
2.4.2 LO Phase-tuning  
2.4.3 Baseband Phase-tuning  
2.4.4 True-time-delay Beamforming  
2.5 Summary  
9

## 3. LO Circuits for Beamforming Receivers  
3.1 Overview  
25

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iii
List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.


Author’s Contribution

Publication I: “A 2–5.5 GHz Beamsteering Receiver IC With 4-Element Vivaldi Antenna Array”

The author participated in the system-level design of the beamforming receiver and LO phase-tuning block. The idea for the delay line was originally proposed by M.Sc. Yury Antonov, but the author is responsible for putting it on silicon. The author also designed, verified and implemented the pilot-signal generator and part of the RF-ADC interface. The author conducted measurements for the receiver front-end (partly) and beamforming presented in the paper. She is one of the three main contributors to the manuscript.

Publication II: “A Delay-Based LO Phase-Shifting Generator for a 2-5GHz Beamsteering Receiver in 28nm CMOS”

The author worked on the final implementation and verification of the proposed delay line for LO phase-tuning. During measurements, she characterized the delay lines and phase mismatches between beamforming elements through the baseband calibration method. She also performed 2-element beamforming measurements presented in the paper. She is one of the main contributors to the manuscript.

Publication III: “A 3-43ps time-delay cell for LO phase-shifting in 1.5-6.5GHz beamsteering receiver”

The author analyzed the time-delay cell and conducted the verification simulations that are presented in the paper. She is one of the main contributors to the manuscript.
Publication IV: “True-Time-Delay Beamforming Receiver With RF Re-Sampling”

The author participated in the development of the proposed true-time-delay beamforming technique, LO generation requirements and the pulse-skipped LO concept. The TTD receiver front-end was designed by M.Sc. Kalle Spoof, he was mainly responsible for preparing the manuscript. The author designed the underlying pulse-skipped LO generation technique that supports the TTD receiver. A circuit-level presentation of the LO generator is presented in publication V.

Publication V: “A 0.6–4.0 GHz RF-Resampling Beamforming Receiver With Frequency-Scaling True-Time-Delays up to Three Carrier Cycles”

The author designed, verified and implemented the pulse-skipped LO generator. The author conducted part of the measurements, and is one of the main contributors to the manuscript.
List of Abbreviations

1G 1st generation.
4G 4th generation.
5G 5th generation.

ADC analog-to-digital converter.
AM/AM amplitude-to-amplitude modulation.
AM/PM amplitude-to-phase modulation.

BB baseband.
BF beamforming.

CMOS complementary metal-oxide semiconductor.

DAC digital-to-analog converter.
DBF digital beamforming.
DCDL digitally-controlled delay line.
DSP digital signal processing.

ESD electrostatic discharge.

FE front-end.
FFT Fast Fourier transform.
FR1 frequency range 1.
FR2 frequency range 2.

HB hybrid beamforming.
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>HPBW</td>
<td>half-power beamwidth.</td>
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<tr>
<td>I-V</td>
<td>current-voltage.</td>
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<tr>
<td>I/Q</td>
<td>in-phase/quadrature.</td>
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<td>IC</td>
<td>integrated circuit.</td>
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<td>IF</td>
<td>intermediate frequency.</td>
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<tr>
<td>ILO</td>
<td>injection locked oscillator.</td>
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<tr>
<td>IoT</td>
<td>Internet of Things.</td>
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<tr>
<td>LNA</td>
<td>low noise amplifier.</td>
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<tr>
<td>LNTA</td>
<td>low noise transconductance amplifier.</td>
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<tr>
<td>LO</td>
<td>local oscillator.</td>
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<tr>
<td>MIMO</td>
<td>multiple-input-multiple-output.</td>
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<tr>
<td>MOS</td>
<td>metal-oxide semiconductor.</td>
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<tr>
<td>NR</td>
<td>New Radio.</td>
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<tr>
<td>PCB</td>
<td>printed circuit board.</td>
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<tr>
<td>PLL</td>
<td>phase-locked loop.</td>
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<td>PS CTRL</td>
<td>pulse-skip control.</td>
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<tr>
<td>PSG</td>
<td>pilot-signal generator.</td>
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<tr>
<td>PVT</td>
<td>process-voltage temperature.</td>
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<tr>
<td>RC</td>
<td>resistor-capacitor.</td>
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<tr>
<td>RF</td>
<td>radio frequency.</td>
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<tr>
<td>RTPS</td>
<td>reflection-type phase-shifter.</td>
</tr>
<tr>
<td>Rx</td>
<td>receiver.</td>
</tr>
<tr>
<td>SAR</td>
<td>successive approximation register.</td>
</tr>
<tr>
<td>SAW</td>
<td>surface acoustic wave.</td>
</tr>
<tr>
<td>SH</td>
<td>sample-and-hold.</td>
</tr>
<tr>
<td>SNR</td>
<td>signal-to-noise ratio.</td>
</tr>
<tr>
<td>SPI</td>
<td>serial peripheral interface.</td>
</tr>
<tr>
<td>TTD</td>
<td>true-time-delay.</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>--------------</td>
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<tr>
<td>VCO</td>
<td>voltage-controlled oscillator.</td>
</tr>
<tr>
<td>VGA</td>
<td>variable-gain amplifier.</td>
</tr>
<tr>
<td>W/L</td>
<td>width-over-length ratio.</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
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<td>-------------</td>
</tr>
<tr>
<td>$\Delta_N$</td>
<td>total coarse delay for a signal path</td>
</tr>
<tr>
<td>$\Delta t$</td>
<td>relative time-delay</td>
</tr>
<tr>
<td>$\Delta t_D$</td>
<td>delay between received signals for antenna 1 and N</td>
</tr>
<tr>
<td>$\Delta \theta$</td>
<td>beam squint, deviation from desired angle-of-arrival</td>
</tr>
<tr>
<td>$\Delta \tau$</td>
<td>relative time-delay</td>
</tr>
<tr>
<td>$\Delta \phi_D$</td>
<td>phase-shift between received signals at antenna 1 and N</td>
</tr>
<tr>
<td>$\theta$</td>
<td>beamforming angle-of-arrival</td>
</tr>
<tr>
<td>$\theta_{max}$</td>
<td>maximum beamforming angle-of-arrival</td>
</tr>
<tr>
<td>$\theta_o$</td>
<td>desired angle-of-arrival</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>signal wavelength</td>
</tr>
<tr>
<td>$\tau_N$</td>
<td>time-delay added by circuit or block</td>
</tr>
<tr>
<td>$w_{BB}$</td>
<td>angular baseband frequency</td>
</tr>
<tr>
<td>$w_C$</td>
<td>angular carrier frequency</td>
</tr>
<tr>
<td>$A$</td>
<td>amplification factor</td>
</tr>
<tr>
<td>$A(t)/B(t)/C(t)$</td>
<td>output response of time-delay cell</td>
</tr>
<tr>
<td>$BW$</td>
<td>modulation bandwidth of baseband signal</td>
</tr>
<tr>
<td>$C$</td>
<td>node capacitance</td>
</tr>
<tr>
<td>$C[: \in {0; 1}$</td>
<td>static control signal</td>
</tr>
<tr>
<td>$C_N$</td>
<td>clock signal for sampling stage</td>
</tr>
</tbody>
</table>
List of Symbols

\( d \) \quad \text{distance between consecutive antenna elements}

\( f \) \quad \text{instantaneous frequency point (across modulation bandwidth)}

\( f_c \) \quad \text{carrier frequency}

\( f_{LO} \) \quad \text{LO frequency}

\( f_{max} \) \quad \text{maximum oscillation frequency}

\( f_T \) \quad \text{transit frequency}

\( G_m \) \quad \text{transconductance}

\( K_N \) \quad \text{discrete-time baseband signal}

\( L \) \quad \text{inductance}

\( LO_N \) \quad \text{LO negative (180° phase-shifted) signal for mixer}

\( LO_P \) \quad \text{LO positive (0° phase-shifted) signal for mixer}

\( M \) \quad \text{number of skipped pulses}

\( N \) \quad \text{total number of beamforming elements in an array}

\( R \) \quad \text{on-resistance of a switch}

\( S_{RF} \) \quad \text{RF signal}

\( t_{DL_{max}} \) \quad \text{maximum delay tuning range}

\( t_{DL} \) \quad \text{delay introduced by a delay line}

\( T_{LO} \) \quad \text{time period of the LO signal}

\( T_{samp.} \) \quad \text{total tracking time for LO signal of a sampling stage}

\( T_{trN} \) \quad \text{tracking time for LO signal of a sampling stage}

\( V_N \) \quad \text{node voltage}

\( V_{DD} \) \quad \text{supply voltage}

\( Z \) \quad \text{node impedance}
1. Introduction

1.1 Background

Today, we live in a global village which is shrinking with the ever-increasing demand for higher connectivity to share information and ideas as well as to socialize. In the past decades wireless communication systems have evolved from the analog 1G standard to 4G, addressing the demand for connecting a larger volume of mobile phone users through higher data-rate connections mainly intended for multimedia applications. However, researchers are exploring new avenues including Internet of Things (IoT), e-healthcare and Financial Technology, that require larger user and traffic capacity in mobile broadband communications.

The target of 5G NR is to increase wireless data rates, bandwidth, coverage and connectivity while reducing latency and energy consumption [1–4]. The primary methods to address these 5G requirements include increasing the density of existing cellular networks, utilizing full-duplex communication, multiple-input multiple-output radios, beamforming, millimeter-wave spectrum, energy-aware communication and energy harvesting [5, 6]. These research themes are broad and multidisciplinary; demanding comprehensive studies. From the perspective of hardware design, beamforming can benefit the deployment of 5G NR through spatial filtering of interference signals and increasing the signal-to-noise ratio (SNR).

The integration of multiple radio transceivers in the same device calls for hardware to have a small form factor and lower power consumption. CMOS technology reduces the manufacturing cost, and the scaling trend favors higher integration while reducing the power consumption to perform the same task. Front-end receiver design has seen a shift from narrowband operation, with off-chip high-Q channel filters, to operating frequency spanning several GHz [7–10]. On the other hand, the wireless propagation channel is crowded by in-band and out-of-band interference signals. These and other harmful signals create non-linear distortion in
the receiver that can lead to desensitization. The trade-off between operating frequency range and filtering interference can be alleviated by incorporating beamforming architecture.

In a beamforming architecture, an array of antennas and associated front-ends (receiver/transmitter) generate and steer the beam across the spatial domain. This architecture not only improves the signal-to-noise ratio (SNR) but also reduces interference through spatial filtering. The data rate depends on the baseband (BB) modulation bandwidth, modulation order and coding rate; a higher modulation order requires a higher SNR as closer symbols require better SNR for acceptable bit error rates [11]. 5G envisions to incorporate higher modulation bandwidth to meet the demand for higher data-rate transmission [6].

The hardware required for 5G NR transceivers should operate over a frequency band spanning several gigahertz from 400 MHz to 7 GHz. The maximum modulation bandwidth for the transceivers is set to be 100 MHz. The noise figure (NF) is lower than the 4G standard, to achieve the target link budget. Techniques to improve spectral efficiency including carrier aggregation constrict the in-band (IB) linearity, moreover, blockers located close to the wanted signal place stringent linearity requirements on the receivers [1–4]. The initial deployment of 5G has addressed these requirements to some extent, leaving room for developing the receiver hardware. In 5G, a differentiating factor for the transceiver design will be the extensive employment of phased arrays because it is one of the effective means to reduce blockers and improve the SNR. Hence, this work focuses on developing receiver front-ends with the beamforming architecture.

The beamforming architecture can be divided into three approaches, namely analog, digital and hybrid beamforming. It can be further classified into phase-tuning and true-time-delay (TTD) beamforming. The optimum choice for the beamforming approach and architecture depends on the frequency band and target specifications. The choice of beamforming approach impacts the footprint of the receiver’s signal chain, and the required dynamic range for the blocks before beamforming summation.

Analog beamforming is a strong candidate for 5G NR either as a standalone solution or as part of hybrid beamforming because it reduces the footprint and dynamic range requirements of the ADC. This thesis concentrates on the local oscillator (LO) phase-tuning architecture. The design of LO chain circuits for the sub-6 GHz beamforming receivers requires further study. In the future, phased arrays will be developed mostly for the millimeter-wave and circuit design techniques similar to the low GHz range cannot be used here. This work also presents an LO circuit design for greater than 6 GHz operation.
1.2 Objective of This Work

The objective of this dissertation is developing beamforming receiver front-ends with LO phase-tuning architecture. The main focus is the design and implementation of LO-path circuits for phase-tuning and true-time-delay beamforming for the sub-6 GHz band. This work also aims to study LO circuit design with mixed-signal techniques to operate above 10 GHz. These topics are examined with methods including theoretical analysis, system-level and circuit simulations, the design of integrated circuits as well as measurements of the fabricated prototype.

1.3 Contents of This Dissertation

This dissertation consists of a summary of the research work and five scientific articles (referred to as Publications I-V) that have been published in peer-reviewed journals and conference proceedings.

Chapter 2 presents an overview of the topic, providing background information for the new research discussed in the subsequent chapters. The chapter begins with an overview of the recent developments in receiver design. It is followed by beamforming theory and circuit design aspects that can contribute towards deviating the beam characteristics from the desired targets, to identify the major limitations coming from the signal blocks in the beamforming elements. Section 2.3 discusses merits and challenges associated with beamforming approaches, namely analog, digital and hybrid beamforming. The presented research in this dissertation is about analog beamforming techniques, therefore Section 2.4 closely examines the trade-offs linked with analog beamforming architectures, combined with a presentation of literature related to these topics.

Chapter 3 covers the implementation of two sub-6 GHz beamforming receivers and one >10 GHz heterodyne receiver. The research contributions related to these topics are detailed in Publications I - V. This chapter is divided into four parts. Section 3.1 discusses trade-offs for the applicable LO phase-tuning techniques in the sub-6 GHz band and motivation for the adopted choice. Section 3.2 presents the details for the beamforming receiver applying LO phase-tuning; it is linked to Publications I - III. Here, system-level design details for the receiver are followed by block-level implementation details for the proposed delay-line, time-delay cell and phase calibration, presented with supporting simulation and measurement results.

Section 3.3 presents the details for the proposed true-time-delay beamforming receiver, linked to Publications IV and V. The requirements for multiphase LO generation are derived from system-level design and a novel solution based on pulse-skipped LO is presented. These are then
followed by supporting simulation and measurement results. In Section 3.4 performance of the two CMOS beamforming receivers for the sub-6 GHz band are compared to state-of-the-art receivers.

Section 3.5 presents the design of the LO circuit that applied mixed-signal techniques for operation above 10 GHz. The measurement and simulation results for the receiver prototype are presented alongside discussion of the implementation challenges and LO circuit design details.

Chapter 4 summarizes the outcomes of the research work.

### 1.4 Main Scientific Merits

The original research work conducted as part of this dissertation has been presented in Publications I-V, containing the most detailed description of the results. An overview of the outcome is also provided in Chapter 3, the most significant scientific achievements of this work being summarized as follows:

- The system-level, block-level design and performance details for a beamforming receiver, with LO phase-tuning architecture, were presented including RF, LO, and phase calibration paths, and the antenna assembly. The 4-element beamforming receiver prototype was characterized through measurements for 2 - 5.5 GHz [I].

- A delay line was developed for LO phase-tuning and divider-less I/Q generation. 2-element beamforming measurements produced through the baseband calibration method were presented [II].

- The analysis, design and verification simulations of the proposed time-delay cell to generate coarse and fine delays for the delay line as a phase-tuning element was presented [III].

- The pulse-skipping LO concept that enables true-time-delay beamforming was developed and presented in the paper [IV].

- The circuit-level design of the LO generator that enables true-time-delay beamforming receiver in 0.6 - 4 GHz was presented along with the receiver measurement results [V].

- An LO circuit was developed applying mixed-signal techniques for operation at 12 - 25 GHz; the circuit design details, supporting simulation for the LO block and measurement results for the receiver are presented in Chapter 3. This implementation demonstrated that rail-to-rail LO signalling can be generated and propagated up to 25 GHz in deep submicron
CMOS processes.
2. Beamforming for Radio Receivers

This chapter on beamforming discusses the background information and motivation for the research work summarized in Chapter 3. First, Section 2.1 motivates the need for beamforming while discussing wideband receiver design and development. Section 2.2 presents an overview of the beamforming theory and the parameters which affect the performance of phased arrays. Section 2.3 introduces analog, digital and hybrid beamforming approaches. As the main topic of the thesis is LO circuits for phase-tuning and true-time-delay beamforming, the final section compares different analog beamforming techniques alongside the literature review of state-of-the-art techniques.

2.1 Radio Receivers

The need for high data rates requires that the transceiver hardware can cope with large modulation bandwidth [12]. And the demand for tunable operation frequency in transceivers necessitate that the front-end can operate over a wide frequency band. Consequently, the band-select filter, positioned between the antenna and the front-end, allows the reception of signals from a wider spectrum. There is a good chance that a stronger signal at a close-by frequency, known as interference or blocker, from the signal-of-interest can distort the useful information either by saturating the RF front-end or desensitizing it. In the past, heterodyne receivers [13] have been widely adopted due to their high selectivity, thanks to high-Q filters constructed with discrete components. It is, however, absent in direct-conversion receiver architecture which is well-suited for an integrated wideband radio [14–17]. In the absence of channel-select filters, spectral filtering can also be accomplished with n-path filters [7–10, 18]. In the thesis, ‘wideband’ refers to a wide operating frequency band.

Several techniques are presented in literature to optimize the design of wideband receivers for wireless communication systems [19–22]. This topic encompasses several subtopics for research, including self-interference...
cancellation [23,24] to enable full-duplex operation, and the reduction of LO harmonics leaking to the RF-path [25]. Extensive research has also been carried out to explore techniques to alleviate noise-bandwidth trade-off for the low-noise amplifier (LNA) [26–32], as well as the analog-to-digital converter (ADC) trade-offs including resolution, throughput and power consumption [33–35]. Wideband receivers can operate with high linearity to reduce the impact of interference in the absence of voltage amplification through passive mixers and transconductance amplifiers [36–38].

Studies have been conducted to push the digital circuit boundary close to the antenna through direct delta-sigma receivers [39–41]. Phased arrays can also address some receiver design challenges; they generate directive beams, increasing the signal-to-noise ratio (SNR) to improve channel capacity, and introduce spatial filtering to reduce interference [42]. The focus of the thesis is the design and implementation of LO phase-tuning for phased-array receivers; next, a brief section about beamforming theory and approaches is presented, followed by phase-tuning techniques in the later sections.

2.2 Tuning in Phased Arrays

Phased arrays employ an antenna array to generate and electronically steer the signal beam by applying the appropriate gain weights and time-delay or phase-shift in each signal path, typically consisting of a transceiver [42–44]. Figure 2.1 depicts a generic beamforming scheme with $N$ number of linearly-spaced antenna elements along one dimension radiating a beam at 45° from the antenna boresight. A simplified scenario is presented here by assuming that the radiating source is located in the far-field region; the received signal wavefront is a straight line and its incidence angle is equal
for each element. The time-delay $\Delta t_D$ between the received signals at the $N^{th}$ element with respect to the $1^{st}$ element is expressed as

$$\Delta t_D = \frac{d(N - 1)\sin(\theta)}{c}, \quad c \approx 300,000 \text{Km/s}$$

(2.1)

where $\theta$ is the angle of arrival of the beam, $d$ is the distance between two consecutive antenna elements, and $N$ is the total number of array elements as depicted in Fig. 2.1.

Delay compensation in each path results in coherent signal summation for all received signals, improving the SNR and channel capacity for the same transmit power. Theoretically, the SNR increases by 3 dB for the doubling elements of the array because uncorrelated noise from the receiver paths adds up in power while the correlated desired signal adds up in voltage [45]. Phased arrays exhibit higher directivity than single antennas and filter interference in the spatial domain. Implementation of time-delay tuning in transceivers is challenging, with many design trade-offs; this point is expanded in Section 2.4.

Alternatively, if the modulation bandwidth of a signal is smaller than the carrier frequency ($f_c$), it is narrowband. Delay in time equals phase-shift for a point frequency; this approximation is also viable for narrowband signals. Equation 2.1 can be modified for relative phase-shift as

$$\Delta \phi_D = \frac{2\pi d(N - 1)\sin(\theta)}{\lambda} = 2\pi f_c \Delta t_D$$

(2.2)

$f_c$ and $\lambda$ is the received signal frequency and wavelength respectively. Phase-tuning techniques are presented in Sections 2.4.1 and 2.4.2. Most antennas are reciprocal, the same beamforming equations apply to the transmitter antenna array as well. Beamforming and beamsteering are interchangeable terms used to describe the formation and steering of a signal beam in antenna arrays. The term beamforming will be used in this thesis to maintain uniformity.

The overall array’s pattern is determined by the element factor (the pattern produced by an individual antenna) and array factor (beamforming in an array of isotropic elements). Figure 2.2 shows the normalized array factor for an ideal case: a uniform array with linear phase-shift progression between the elements. The ideal radiation pattern shows the dependence of the beam’s characteristics including the mainlobe, half-power beam-width, sidelobe levels, grating lobes, and the beam’s nulls depend on the array geometry including array size $N$, spacing between the elements $d$ and the beam weights [42,46].

Figure 2.2(a) presents the radiation patterns for different array sizes, the spacing between the elements is set to $\lambda/2$. Enlarging the antenna array reduces the beamwidth, and the number of sidelobe nulls increases. Figure 2.2(b) presents radiation patterns for different spacing between the elements of a 16-element array. The spacing between the elements
Figure 2.2. (a) Normalized array factor of linear array as a function of array size, \( d = \lambda/2 \), \( \theta_o = 0^\circ \). (b) Normalized array factor for different spacing between elements, \( \theta_o = 27^\circ \), \( d > \lambda/2 \) can introduce a grating lobe, in this case at \(-65^\circ\).

Figure 2.3. (a) Beam squint for a signal with 50% modulation bandwidth of \( f_c \), \( \theta_o = 27^\circ \), \( N = 16, d = \lambda/2 \). The center band represents the target direction. (b) Array factor for different phase-tuner resolutions \( \theta_o = 35^\circ \), \( N = 16, d = \lambda/2 \).

determines not only the beamwidth and number of sidelobes, but spacing > 0.5\( \lambda \) can introduce grating lobes, present at \(-65^\circ\) in the illustrated case. The peak-to-null ratio is important for reducing the blocker signal in the spatial domain. The phased array parameters that a circuit designer can influence will be discussed in the following sections.

### 2.2.1 Beam Squint

Figure 2.3(a) presents an array factor where the modulation bandwidth \( BW \) is half of the carrier frequency, the maximum gain of the beam shifting away from the target direction \( \theta_o \) (represented by black color) across the bandwidth. The approximation of the time-delay as the phase-shift degrades array performance for wideband signals through a phenomena...
called beam squint \([44,47]\): a spatial error that quantifies the angular shift of the mainlobe of a beam versus frequency. Phase-shift beamforming leads to a change in the target direction \(\theta_o\) of the beam according to the ratio of the carrier frequency \((f_c)\) to instantaneous frequency \((f)\), resulting in the beam pointing towards different angles across the modulation bandwidth. Beam squint is also a function of the target beam angle \(\theta_o\), and can be calculated from \([48]\)

\[
\Delta \theta = \arcsin \left( \frac{f_c}{f} \sin \theta_o \right) - \theta_o
\]  

(2.3)

Beam squinting can be avoided if the transceiver replaces the phase-shifting block by a time-delay block \([47]\).

### 2.2.2 Phase/Time-Delay Tuning Resolution

Figure 2.3(b) shows that coarse resolution (without tapering) results in an increase in sidelobe levels and a lower peak-to-null ratio for a 16-element array and 35\(^0\) angle-of-arrival. Finite resolution also affects the steering of a beam across its angular range. If the phase gradient applied across the array is uniform (i.e. a linearly progressing phase-shift) the beamforming resolution can be calculated from Equation 2.2. If a non-uniform phase gradient is applied across a large array, then a smaller beamforming resolution can be achieved \([49]\).

The finite resolution of a phase or time-delay element results in quantization sidelobes, analogous to a time-sampled system. The level of quantization sidelobes is determined by many factors including phase/delay resolution, the phase/delay gradient applied across the array, the angle-of-arrival and tapering \([43,50]\). Tapering is the gain adjustment of phased array elements in accordance to a windowing function, such as a Taylor or Hamming window function. Tapering results in sidelobe suppression at the cost of widened beam width \([49]\). \([50]\) demonstrated through system-level simulations that 6-bit resolution \((5.6\%\) maintains sidelobe levels within \(~1\) dB of an ideal tuning element for a 64-element array with a 20 dB Taylor window applied.

Phase-tuning resolution, alongside the phase detector’s accuracy, also determines the maximum allowed value for random mismatches between the beamforming elements. These random mismatches also increase the sidelobe levels and decrease the peak-to-null ratio, as can be seen from Figure 2.4. The peak-to-null ratio is important for interference reduction in phased arrays \([51,52]\). The range for a time-delay \((\Delta t_D)\) or phase-shift \((\Delta \phi_D)\) tuning element should cover the time-period of the radiated signal for wide beamforming angles in large arrays.
Figure 2.4. Normalized array factor for $N = 8, d = \lambda/2$ demonstrating the effect of gain and phase mismatches between the phased array elements: (a, c) $0^\circ$ angle-of-arrival. (b, d) $32^\circ$ angle-of-arrival.

2.2.3 Calibration

IC characteristics can contribute to random errors in phased arrays due to process variations, signal-path non-linearity and AM/AM or AM/PM effects. Static path mismatches can be introduced by asymmetry in the antenna feeding path and signal distribution path on the PCB; these are related to fabrication tolerances and depend on the implementation. Calibration can improve the robustness of the transceiver against performance variation over its lifespan, by monitoring and optimizing its key parameters [53]. It also addresses other issues generated from process variations such as, for instance, LO feedthrough or IQ imbalance in direct-conversion architecture [54]. Likewise, calibration can also optimize the beam’s properties (i.e. sidelobe suppression [55] or improving the peak-to-null ratio [56]) by rectifying gain and phase mismatches between the transceiver elements in phased arrays [57, 58]. The beam’s characteristics can be transformed for interference reduction [52].

Orthogonal gain and phase/delay tuning (i.e. gain independent phase-
tuning and vice-versa) is important from a system design perspective because the phased array should maintain sidelobe levels below a threshold while steering the beam, and the beam’s target direction should be maintained while attempting to keep the levels of the sidelobes below a certain threshold. Non-orthogonal phase and gain-tuning requires a dedicated complex calibration procedure. Furthermore, it can also limit the gain that is practically achievable and the phase accuracy [50].

Figure 2.4 shows the effect of gain and phase mismatches on beamforming, the sidelobes levels increasing by 2-5 dB owing to the mismatches. Lower gain and phase-tuning resolution results in higher sidelobe levels. The effect of non-orthogonal phase-tuning can also be seen from the presented results. Phase-dependent gain variation, if modeled as random gain variation in the beamforming elements, leads to an increase in sidelobe levels and a poorer peak-to-null ratio for the phased array [59]. On-chip calibration can reduce the testing and optimization cost for a phased array, which is beneficial for mass production [57,58].

Transmission and reception requires two signal paths (i.e. RF and LO); the on-chip calibration procedure can address both independently. RF-path calibration can also be called data synchronization, and LO-path calibration can be termed as carrier synchronization. In general, the data calibration block is composed of 3 segments: coupling the RF signal to the calibration path, down-conversion and low-pass filtering, and amplitude/phase detection and conversion to digital control codes by the ADC or phase-to-digital converter (PDC) [53–58]. The digital codes serve as control signals for tuning variable-gain amplifiers or phase/time-delay tuning blocks. Carrier or LO synchronization is performed in each element with phase or delay locked loops [14].

2.3 Beamforming Approaches

Beamforming weights can be applied in the analog, digital or both domains (hybrid beamforming). Various beamforming techniques can be evaluated on the basis of tuning range, resolution, signal-chain linearity, gain and phase-tuning orthogonality, die area and power consumption, insertion loss, flexibility and calibration complexity.

2.3.1 Analog Beamforming

Figure 2.5 shows a block diagram of a direct-conversion receiver that applies RF phase-tuning, a sub-category of analog beamforming. In this approach, tunable weights for delay and gain compensation are implemented in the analog domain. Every antenna element reserves dedicated weight-tuning hardware to ensure coherent signal summation, and the
received copies are summed before analog-to-digital conversion. Low-noise amplifier (LNA) is assumed to have gain-tuning capability for tapering or mismatch calibration. Analog beamforming can employ phase-shifting or true-time-delay techniques either in the radio frequency (RF), local oscillator (LO) or baseband domain.

Analog beamforming requires the least amount of front-end hardware in a phased array thanks to early summation, and relaxes the dynamic range requirement of all blocks after summation. The presence of strong and weak received signals at the input of an ADC requires a high instantaneous dynamic range that leads to high power consumption [60]. However, schemes for spectral efficiency such as spatial multiplexing cannot be accommodated here. The thesis topic is a part of analog beamforming, thus the design, implementation advantages and challenges for state-of-the-art beamforming techniques will be discussed in detail in Section 2.4.

2.3.2 Digital Beamforming

Figure 2.5(b) shows a digital beamforming (DBF) receiver, where the digital signal processing (DSP) unit represents all digital domain operations including phase and delay-tuning. In this approach, signals from different antennas are digitized independently, each element reserving a transceiver front-end (FE) and data converter. Phase/time-delay tuning, gain tuning and signal summation are implemented through digital operations. DBF executes precise phase-shifting by complex-weight multiplication or delay-tuning with fractional rate interpolation. This approach can achieve high computational flexibility and accurate beamforming with the possibility to transmit and receive multiple independently steered beams for spatial multiplexing [61]. Phased arrays also benefit from digital signal processing (DSP) algorithms for null steering and phased array calibration. However, the number of signal chains, composed of the front-end and most of the back-end components, increases proportionally with the array size. This results in a demanding dynamic range requirement for most of the signal chain components to combat the blockers.

In [62–65], digital beamforming for phase-shifting and true-time-delay
Figure 2.6. Hybrid beamforming receiver: (a) partially connected hybrid beamforming (b) fully connected hybrid beamforming.

has been demonstrated. And several techniques presented in [51, 52, 60, 66, 67] propose solutions for spatial interference rejection to alleviate the high dynamic range requirement for the ADC. Designs [51, 52] presented solutions for spatial filtering of interference signals, accomplished by steering beamforming nulls through analog phase-tuning techniques. Digital beamforming exhibits higher energy efficiency (defined as spectral efficiency over power consumption) through digital precoding of multiple data streams. Nonetheless, purely digital beamforming has not yet become a viable option for low-cost on-chip implementation, especially for transceivers operating at the millimeter-wave frequencies.

2.3.3 Hybrid Beamforming

Figure 2.6 shows two types of hybrid beamforming architectures, the DSP unit encloses all digital beamforming functions. This approach combines analog beamforming and digital precoding to form beam patterns that benefit from higher beamforming gain, and flexibility to execute spatial multiplexing and interference rejection. The phased array antennas are not connected to the transceiver’s front-end or back-end components in a one-to-one fashion, employing a few signal chains compared to DBF. This adaptable architecture can be broadly divided into two types: sub-connected or partially-connected and fully-connected hybrid beamforming (HB). As shown in Figure 2.6(a), a partially-connected hybrid beamforming receiver consists of multiple independent sub-arrays. Each sub-array reserves a dedicated signal chain from front-end to back-end, while each
antenna has independent analog gain and phase-tuning blocks for increasing the directivity of the sub-arrays. Generally, the first stage in partially-connected hybrid beamforming is a PA or LNA [68–70].

In fully-connected HB, each signal chain (highlighted by different colors in Figure 2.6(b)) is connected to all antennas through a signal combiner or splitter. This approach enables higher array gain, a narrower beam, larger beamsteering range and better energy efficiency than partially-connected HB, though the signal distribution from the antenna poses a challenge for large arrays, especially at higher frequencies [68–70].

Hybrid beamforming addresses the issues related to purely analog and digital beamforming to reduce blocker-induced non-linearity and increase channel capacity through spatial multiplexing. Although [71–73] have presented hybrid beamforming ICs, the optimum solution for different frequency bands requires further study.

2.4 Analysis of Analog Beamforming

IC hardware enables analog beamforming through implementation of electronic phase-tuning in either RF, LO or BB domains, as shown in Figure 2.7. There are also analog beamforming approaches that do not fall into any of these categories [74–76]. Since the first demonstration of beamforming on Silicon [77], researchers have extensively investigated this topic. In the following subsections, analog phase-tuning methods will be discussed in detail. The most important characteristics that must be achieved with the phase-tuning circuitry will be highlighted. As the focus of this work is LO phase-tuning, a literature review of state-of-the-art analog beamforming techniques including phase-tuning and true-time-delay will therefore also be presented.
2.4.1 RF Phase-tuning

In RF phase-tuning architecture, the received/transmitted signal phase is adjusted in the RF path, usually accompanied by variable-gain amplifiers (VGAs) and power combiners before a shared down-conversion stage. This architecture relaxes the dynamic range requirement for the signal blocks following beamforming summation because interferers can be filtered in the spatial domain. Early summation and low-voltage amplification reduces the probability of signal chain compression or desensitization in the presence of strong in-band blockers [78]. Most of the blocks in the signal chain, including the down-conversion mixer and LO signal distribution network, are shared between the phased-array front-ends (FEs), reducing the LO footprint. However, RF path phase-tuning increases design complexity as the phase-tuner is required to maintain high linearity, low NF and a wide frequency band.

Several implementations have employed RF phase-tuning architecture, focusing on beamforming in the millimeter-wave frequency band. These implementations can be classified into passive phase-tuning [79, 80] based on reflection-type (RTPS) [59, 81], switch-type LC [82, 83] or transmission-line based implementations [50, 84], and active phase-tuning based on vector modulation [85–90]. Passive phase-tuning techniques such as switch-type LC or reflection-type can introduce a phase-shift dependent insertion loss, which if unaddressed can cause sidelobe re-growth [50]. Cascading multiple LC networks can lead to a large occupied area [89]. In some of the reported implementations, the phase resolution is either limited to lower resolution/range or trade-offs with other performance parameters [82, 83].

Vector modulators exhibit lower insertion loss and a fine phase-shift of 7-bit or higher resolution [85, 86, 90] while covering the full phase-tuning range. However, Cartesian vector modulators require variable transconductance amplifiers that can introduce gain-dependent phase errors. Besides careful design, this scheme requires isolation at the input and output of the transconductance stage [74].

Overall, most RF phase-tuning techniques [59, 81–83, 85, 86, 90] exhibit non-orthogonal phase-tuning, requiring careful design and more complex calibration to reduce phase errors. Phase-dependent gain variation increases the cost of calibration, measured through the time and power consumption required for data synchronization.

2.4.2 LO Phase-tuning

To overcome the limitations presented by RF phase-tuning including phase-dependent gain variation [59, 81–83, 85, 86, 90], phase-tuning can also be performed in the LO path, shown in Figure 2.7. The phase of the signals can be tuned during up-conversion/down-conversion by phase-shifting the
LO signals. This architecture reduces the linearity and NF requirements for the phase-tuner in comparison to RF phase-tuning. If the mixer is driven to saturation by rail-to-rail LO signals, the gain of the RF signal in each beamforming element is unaffected while phase-tuning and careful design choices mitigate gain-dependent phase variation for the phase-tuner. This not only maintains gain/phase-tuning orthogonality for optimal beamforming performance, but also provides a degree of freedom in the choice of the applied technique. In the LO domain, the phase-tuning block can be implemented by passive-less techniques, without bulky inductors or transmission-lines, to profit most from the downscaling trend in phased arrays.

Figure 2.8 shows different phase-tuning techniques, the reference LO (REF) can be operating at different frequencies for these cases. LO phase-tuning designs have been reported in [91, 92] comprising either injection-locked oscillators [93–95], injection-locked frequency dividers [96] or phase-locked loops (PLL) [97, 98]. There are also several reported techniques utilizing vector modulators [52, 99, 100], or passive phase-tuning formed with a reflection-type phase shifter [101, 102], poly-phase filters, switching capacitors and varactors [103]. LO phase-tuning architecture increases the power consumption as the mixers and driving LO buffers increase proportionally with the array size.

LO phase-tuning can facilitate integration of large arrays by lowering the calibration complexity and reducing the number of steps required for optimum beamforming performance [50]. Moreover, LO phase-tuning can incorporate a localized calibration loop in addition to the conventional RF-path calibration. LO-path calibration can reduce phase mismatches arising from random variations in this path and maintain phase-tuning accuracy over PVT variations. Injection-locking oscillators or phase-locked loops are an integral part of transceivers. If equipped with phase-tuning capability, they can be utilized for phase-tuning as well as carrier synchronization. The switching speed for tuning and calibration is high in phase-tuners that incorporate MOS transistors with digital controls, which is usually the case for LO phase-tuning. The phase-tuning range is limited to 360° but LO phase-tuning can be extended to a higher number of clock cycles. This concept and details of the beamforming receiver implementation will be discussed in Section 3.3 of Chapter 3.
2.4.3 Baseband Phase-tuning

Phase-tuning can also be applied in the baseband domain before analog-to-digital conversion. In this case, the signal chain hardware multiplies with the array size; increasing power consumption and the required area for the phased array. Since down-conversion lowers the frequency, a longer range is required for phase and delay-tuning elements. It is, however, simpler to implement these blocks in the baseband domain. However, large dynamic range is required for the signal chain blocks up to the ADC input. Phased array implementations for this approach are presented in [104–106].

2.4.4 True-time-delay Beamforming

Figure 2.9 shows different schemes for true-time-delay beamforming. In this approach, the time-delay experienced by the arriving signals is compensated instead of the phase-shift. The signal generating from beamforming summation does not exhibit beam squinting, the modulation bandwidth being extendable up to half of the carrier frequency, making it suitable for high data-rate applications. Figure 2.9(a) shows that true time-delay can be applied in the RF path. There are several implementation challenges involved in true-time-delay beamforming in the RF-path; for example, the passive delay-tuning element occupies a large area [50,107–110]. Other implementations have applied all-pass Gm-C based delay lines [111,112] that consume higher power and demonstrate narrower operation frequency.

Figure 2.9(b) shows another approach for implementing TTD beamforming. An RF delay-tuning block is replaced by two blocks to implement the same functionality: phase-tuning and time-delay tuning added to the LO or BB path. Phase-tuning can be applied to the LO path or baseband domain, and time-delay tuning is added in the baseband domain [113]. Two blocks replace the true-time-delay tuning block in the RF path because time-delaying a baseband signal $\sin(w_{BB}t)$ when up-conversion results in
the RF signal $S_{RF}$

$$S_{RF} = \sin \left( (w_{BB} + w_C) \left( t - \Delta t_D + \frac{w_C}{w_{BB} + w_C} \Delta t_D \right) \right) \quad (2.4)$$

$$= \sin \left( (w_{BB} + w_C)(t - \Delta t_D) + w_C \Delta t_D \right) \quad (2.5)$$

A delay smaller than the required $\Delta t_D$ is generated in the baseband domain; it can be made equal to the desired value by phase-shifting the up-converted/down-converted signal by $w_C \Delta t_D$ [64]. The concept of true-time-delay beamforming was developed further, and the architecture and receiver implementation details will be discussed in Section 3.3 of Chapter 3.

### 2.5 Summary

This chapter discussed system-level design aspects for phased arrays and compared different beamforming techniques. The performance of a phased array is impacted by the choice of phase-tuning versus time-delay technique, the phase resolution and calibration. The choice of beamforming approach impacts the footprint of the receiver’s signal chain, and the required dynamic range for the blocks before beamforming summation.

An analog beamforming approach can be deployed as a standalone solution, or as part of hybrid beamforming. Hybrid beamforming is an attractive approach, because it preserves the advantages of analog beamforming (including a relaxed ADC dynamic range through spatial filtering and reduced signal-block footprint), and incorporates the higher computational flexibility of digital beamforming for spatial diversity. Analog beamforming can be classified mainly into four phase-tuning architectures: RF, LO, BB and analog, and three architectures that support true-time-delay: RF, LO-BB or BB. These architectures have their own set of advantages, most popular among them being RF, LO and analog phase-tuning, and RF true-time-delay.

This thesis investigated the application of LO phase-tuning architecture as it has the potential to address key requirements for beamforming. It helps preserve RF-path linearity and noise performance by applying phase-tuning in the LO path, maintains orthogonal gain and phase-tuning capability, and requires simpler phase-calibration. RF-path linearity and the location of beamforming summation in the signal chain determine the impact of blocker-induced non-linearity in SAW-less receivers, and the noise performance determines the receiver’s sensitivity. Gain and phase-tuning orthogonality is important to achieve simultaneously the desired beam direction across the beamforming angular range and sidelobe suppression.

In LO phase-tuning architecture, phased arrays can have two indepen-
dent calibration loops in the RF and LO paths for reducing phase mismatches arising from PVT variations over the lifetime of the device. On-chip calibration provides a cost-effective means for factory calibration as well as calibration of drift from the desired behavior due to PVT variations over the lifetime of the device. LO phase-tuning architecture has been adopted for two receivers presented in this thesis, encompassing phase-tuning and true-time-delay beamforming for the sub-6 GHz band. The design and implementation details for the mixed-signal techniques applied to the LO circuits operating above 10 GHz will also be presented in the following chapter.
3. LO Circuits for Beamforming Receivers

3.1 Overview

FR1 5G receivers require hardware that can operate over the sub-6 GHz band to enable backward compatibility to existing 3G and 4G networks [1]. The fundamental design parameters for a wideband receiver include input matching to minimize power loss between the antenna and IC interface, gain, linearity for tolerating blockers, compression and inter-modulation performance [14]. Phased arrays can be deployed to filter interference in the spatial domain and improve the channel capacity by increasing the SNR [42]. The choice of phase-tuning architecture impacts the overall phased array receiver performance. Digital beamforming is flexible, accurate and computationally efficient but introduces a stringent dynamic range requirement for the ADC because interference signals are filtered in the digital domain. The presence of strong and weak received signals at the ADC input requires a high instantaneous dynamic range that leads to high power consumption in the ADC [60].

To ease the dynamic range requirement for the ADC, [51, 52] present spatial filtering of interference signals through analog phase-tuning techniques. In the big picture, analog beamforming can be present in phased arrays as part of a hybrid beamformer or multiple-input multiple-output (MIMO) receiver, because it helps address the requirements for energy efficient operation by relaxing the ADC dynamic range requirement and reducing the number of ADCs in a phased array.

Figure 3.1 shows a phased array that applied RF and LO phase-tuning architecture. RF and LO phase-tuning are good candidates for analog beamforming with their own set of advantages and challenges. The early summation of beamforming branches in RF phase-tuning architecture supports the conservation of hardware and eases the dynamic range requirement for following signal chain blocks including mixers. However, RF-path phase-shifting requires careful design for maintaining the signal
path’s linearity and noise figure. Ideally, it should not contribute to distortion by introducing gain-dependent phase variation or phase-dependent gain variation. Passive techniques in the sub-6 GHz range may occupy a large area if inductors, transformers or transmission-lines are employed. Switched-capacitor techniques [45, 114] increase the receiver’s noise figure. Cartesian vector modulators [51] require variable transconductance to generate variable length of vectors for generating a constellation point. This non-orthogonal phase-tuning technique requires careful design and relatively complex calibration as the varying transconductance can introduce phase errors for a beamforming element. It also requires isolation at the input and output of the transconductance stage [74, 75].

A constant-Gm vector modulator needs the same amount of transconductance to create a constellation point. It has a fixed set of N binary-scaled transconductance stages and the associated I/Q waveform generator, the output current of these stages being summed at baseband (BB). In the case of constant-Gm vector modulators, higher resolution requires a larger number of slices. A slice contains a fixed Gm stage, passive mixers with driving LO buffers, and associated baseband switches for connecting/disconnecting a slice to the relevant I or Q branch. The reported constant-Gm vector modulators [51, 74] achieved 44 phase steps (5.5 bit) with 15 slices for one beamforming element.

Figure 3.1(b) shows an N-element phased array with LO phase-tuning. The implementation-related challenges for RF and analog phase-tuning can be evaded simply by incorporating LO phase-tuning architecture. It maintains gain-tuning and phase-tuning orthogonality if the mixers are driven by rail-to-rail signals. Orthogonal operation is necessary for concurrent beamforming and sidelobe suppression across the range of the beam’s angle-of-arrival. This also reduces the complexity of the calibration procedure [50], and thereby its cost. Since the phase-tuner’s performance does not directly affect the RF signal path, it provides a degree of freedom in the choice of the applied phase-tuning technique. LO signal-path calibration
can be conducted independently while the receiver is operating in order to optimize the phased array performance. This architecture increases the LO footprint in comparison to Cartesian vector modulators employed for RF phase-tuning because the mixers and driving LO buffers increase in proportion to the phased array size.

At low GHz frequencies, beamforming arrays can benefit most from technology node scaling if a delay line is employed for phase-tuning. The propagation delays for minimum-sized devices in advanced CMOS processes equals tens of picoseconds, sufficient to cover the time-period of the LO signal with a relatively small component overhead. Target resolution higher than the propagation delay of the device size, ranging around a picosecond, can be achieved through interpolation. Delay lines are digital friendly, taking most advantage from CMOS technology scaling to achieve the highest integration and lower power consumption. Design considerations for LO phase-tuning include: the delay-tuning range determined by the receiver’s operation frequency, 6-bit resolution (sufficient for suppressing sidelobes) [50], power consumption, size, phase error margin and calibration.

A central part of the original research conducted for this dissertation is the design and implementation of LO phase tuning circuits for wideband RF beamforming receivers in the sub-6 GHz frequency band. Two receiver front-end designs, implemented in a 28-nm CMOS process, are discussed in the following sections. Each design is introduced by an overview of the requirements for phase-tuning, the implemented circuit for multiphase LO signals, plus the simulation and measurement results for the overall receiver. The implemented beamforming receivers are referred to as design 1 and 2 in this chapter, these designs being reported in Publications I-V. The beamforming solutions presented in this chapter take advantage of technology scaling by incorporating digitally compatible delay-tuning designs.

Design 1 is a sub-6 GHz wideband beamforming receiver that applies LO phase-tuning by implementing a digitally-controlled delay line. The design also includes on-chip calibration with pilot-signal generation and delay mismatch detection with FFT units. The beamforming functionality for the prototype that included a 4-element Vivaldi antenna array was verified for the 2 - 5.5 GHz range. Publication I expanded the discussion about the overall receiver and antenna prototype design and verification. Publication II dived into the delay line designed for LO phase-tuning with supporting measurement results, and Publication III discussed the time-delay cell and presented its simulation results.

In design 2, we proposed a beamforming technique that extends LO phase-tuning to true-time-delay (TTD) by incorporating discrete-time signal processing. The proposed technique achieved TTD beamforming for modulation bandwidths as large as 40% of the LO frequency by
RF re-sampling and pulse-skipped LO signaling. Integrated in a direct-conversion receiver operating in the 0.6 - 4 GHz range, the implemented design realized TTD with a relatively small area and power overhead. Publication IV introduced the concept for the proposed true-time-delay beamforming technique, and discussed the design considerations with supporting simulation results for the receiver front-end. Publication V reported the measurement results for the implemented 2-element true-time-delay receiver front-end.

Design 3 concentrates on developing the LO signal chain to operate between 12 - 25 GHz. This design concentrates on answering the question: can the digital domain be pushed close to the antenna interface for receivers operating above 10 GHz? As a first step to answering this question, the LO chain was designed with mixed-signal techniques. The design and implementation details, simulation and measurement results are discussed in Section 3.5.

3.2 Design 1: LO Phase-tuning

In this implementation we focused on designing a sub-6 GHz receiver with LO phase-tuning architecture, targeting NR FR1. This section summarizes the key research findings from the original work detailed in Publications I-III. The beamforming receiver architecture is presented first, followed by the system-level requirements for the delay-based LO phase-tuner, its implementation details including the delay line and delay cell structure and simulation results. This section is concluded with over-the-air measurement results for the antenna array and IC prototype.

3.2.1 Receiver Architecture

The receiver architecture is shown in Figure 3.2. The overall objectives of this receiver included designing a wideband front-end with LO phase-tuning: building the RF, LO and digital signal paths and their interfaces, having phase calibration capability and co-designing the antenna array with the IC. The implementation includes a 4-element beamforming receiver and Vivaldi antenna array operating in the 2 - 5.5 GHz range. The receiver front-end targets to provide 50Ω input matching for 2 – 5.5 GHz, compact design, moderate 5-dB amplification before signal summation, and a modulation bandwidth of 200 MHz.

In a wideband receiver, blocker-induced distortion can be reduced by circumventing voltage amplification and incorporating a transconductance amplifying stage and passive mixers [115]. This also leads to current summation for beamforming elements which is easier to implement. The modulation bandwidth is 10% of the carrier frequency at best, beam squint-
Figure 3.2. Receiver architecture for a 4-element beamforming receiver.

Figure 3.2 shows that a single-receiver path consists of a low-noise transconductance amplifier (LNTA), 4-phase passive mixers and an LO phase-tuner. The LNTA exhibits a 3-dB gain-tuning capability with a 1-dB step size for tapering. The proposed delay line provides gain-independent and passive-less LO phase-tuning functionality for the 2-5.5 GHz band. Beamforming is realized by summing the phase-shifted signals at the BB filter input, supporting up to a 200-MHz modulation bandwidth. The BB amplifier has a resistor-capacitor feedback network that exhibits a 3-8 dB gain-bandwidth tuning capability.

A pilot signal, for the built-in self-test, is generated on-chip and distributed across the receiver front-ends through directional couplers present on the printed circuit board (PCB). The pilot signal is employed for delay characterization through back-end circuits (FFT units) or baseband signal detection. Delay characterization between the beamforming signal paths is implemented with sensing ADCs combined with FFT computations; any of the four antennas can be connected to either of the sensing ADCs through a switch-matrix amplifier. The switch-matrix amplifier consists of a chain of buffers to isolate the RF path and drive the high capacitance load presented by the SAR-ADC. Delay characterization with the FFT units provides delay mismatch information for beamforming implemented with digitally-controlled delay lines. The design details for the implemented beamforming receiver and Vivaldi antenna array can be found in Publication I.

3.2.2 Phase-tuning

This section presents the design and simulation results for the delay line and the time-delay cell.
Figure 3.3. A detailed view of implemented LO phase-tuning architecture. The LO chain includes a feeding network consisting of input buffers (IBF) and a clock tree (CT), digitally-controlled delay lines, quadrature passive mixers, baseband summation and amplification (OBF), and pilot signal generator (PSG).

**Delay Line**

In phased arrays, the required phase-shift for an element depends on three factors; the angle-of-arrival of the beam, the element’s position in the array with respect to the reference element, and the applied phase gradient across the array (linear or non-linear). 360° phase-shift is required to steer the beam across the desired steering range. The delay line’s range covered the time-period for the 2 GHz signal, the lowest target frequency, with a margin for shrinkage across the process corners. The phase tuner’s resolution directly translates to the beamsteering resolution, for example, 1.4° phase-tuning resolution can steer the beam with < 1° steps. 6-bit or higher resolution suppresses the sidelobes within ~1 dB of an ideal phase-shifter with the same resolution, while tapering is also applied [50]. Moreover, higher phase-tuning resolution leads to a higher calibration accuracy, given that the precision of detection matches the resolution of the phase tuning element. The delay line was designed for ~1 ps accuracy because the phase step changes with frequency 1°–2.4° at 2 GHz and 5 GHz respectively. Secondly, the resolution is greater than 6-bits to allow ample phase error margin (for PVT variations) without limiting the beamforming performance for an open-loop phase tuner. The occupied area and power consumption of a phase tuner are important parameters for phased arrays because these parameters increase proportionally with the array size. The proposed phase tuner occupies a small area, so it can be placed in proximity to the mixer switches. The proposed design consumes lower power thanks
Figure 3.3 shows the LO chain driving the quadrature passive mixers. An external reference clock signal is fed and distributed across the IC through the input buffers (IBFs) and the clock tree (CT). The clock tree buffers are designed to provide rail-to-rail signals for four delay lines and the capacitive load of the long wires that spread across the chip. This buffer stage also features positive feedback for faster settling to static voltage levels. Publication II provides detailed information about the design and measurement results for the proposed delay line. It is built by chaining together identical time-delay cells that can produce both coarse and fine delays through a 4-bit digital control word. The length of the delay line depends on the application: the LO phase-tuner required delays of varying lengths for phase mismatch calibration, beamforming and divider-less I/Q signal generation. The delay line is divided into three functional domains: beamforming delays, path calibration delays and 4-phase pulse generation. As the name suggests, the beamforming and path calibration sections are responsible for beamforming and compensating the delay mismatches due to the asymmetry or PVT variations between the receiving paths, respectively.

Figure 3.4(a) shows the delay-tuning range of the delay line through simulation results for coarse steps versus control settings. Here, the x-axis represents the number of coarse steps required for 360° phase-tuning across 2 - 5.5 GHz. The simulation results show that the time period of the lower range of operating frequency (2 GHz) is covered by 13 coarse delay jumps. The lowest frequency determined the length of the delay line, since each time-delay cell is capable of producing one coarse or fine delay which can be used for phase-tuning or pulse generation. These results
demonstrate the range of the delay line. Its resolution and relevant results are discussed in the next section.

The designed delay line has a passive-less and divider-less structure to generate LO signals to drive the I/Q mixers. The 4-phase 25% duty-cycle pulses are generated by branching the delay line into four independently tuned paths, each passing 50% duty-cycle waveforms. These paths are combined through the AND operation to create four $90^\circ$ phase-shifted outputs. Pulse-generation is arranged to be the last stage to decrease power consumption and reduce the chance of pulse-swallowing which is usually higher for 25% duty-cycle pulses especially at higher frequencies. The boundary between the different functional domains depends on the calibration and pulse-generation requirements at each carrier frequency. Since the time-delay cells are identical, the control codes determine delays at the input of the mixers. Coarse jumps are enabled towards the end of the line to maintain signal integrity.

Figure 3.4(b) shows the time domain waveforms for I/Q generation at 2 GHz. According to Figure 3.3, out2 /out2_n /out1 /out1_n represent the input waveforms for pulse generation. Their rise and fall instants contribute towards the rising edge and pulse width of the output I/Q waveforms, e.g. the AND operation for out2 (reference) and the $90^\circ$ phase-shifted out1 waveforms results in a 25% duty cycle IP waveform. Similar logic is applied to out2_n and out1_n waveforms to generate the IM waveform. The delay line is branched into four paths, the last stage of each path possess an independently tuned time-delay cell. The last delay cell equalizes the propagation delay of non-inverted (out2 and out1) and inverted waveforms (out2_n and out1_n). The delay required for a $90^\circ$ phase-shift varies over the operating frequency, in practice requiring two dedicated time-delay cells in the last segment of the delay line. Up to $\sim1$ ps accuracy in delay difference can be achieved for I/Q generation, thanks to the fine delay-tuning range of the designed time-delay cell. Publication II presents the design for the proposed digitally-controlled delay line for LO phase-tuning and the measurement results for 2-element beamforming.

**Time-Delay Cell**

The presented time-delay cell is the basic building block for the proposed delay line, which is composed by chaining together identical time-delay cells to create delays for beamforming, path calibration and 4-phase 25% duty-cycle pulses. The time-delay cell (shown in Figure 3.5) is composed of coarse delays and fine delays. In the context of a stand-alone time-delay cell, coarse delays are generated through the propagation delay of a small-sized unit inverter. The uniformity of coarse delay jumps is maintained by changing the number of unit-inverters in each path. In the sub-6 GHz frequency band, delay lines can benefit most from technology scaling to create delays of tens of picosecond with reduced DC power consumption.
The implemented time-delay cell has 3 parallel branches that can be increased to create a diverse profile for the coarse delays.

The switchable delay block shown in Figure 3.5 is a multiplexer with asymmetric transmission gates. These blocks generate fine delays through a current-blending regime for delay interpolation. Fine delays are controlled by the on-resistance of the slow (S) and fast (F) transmission gates. The impact of interpolation on fine delay generation depends on the rise time of the pulses, the delay difference between them, and the time constant of the summing node. The sizing for the employed devices, especially the summing node inverter, is comparable to the minimum size to have a small RC time constant; enabling a small difference in gate length to produce the desired picosecond accuracy. The fine delay block sums only two nodes to avoid excessive loading and to maintain signal integrity.

The time-delay cell is designed to have uneven delays with a 4-bit control word to enable a broad delay profile for beamforming as well as 4-phase generation. The output response for an ideal model of the presented time-delay cell (in Figure 3.5) can be obtained by applying a unit step excitation $L(u(t)) = U(s) = 1/s$ to the delay cell’s transfer functions and then taking the inverse Laplace transform to return to the time domain [116]

$$V_0 = V_2 = V_{IN} \times e^{-s\tau_0} \times A, \quad V_1 = V_{IN} \times e^{-3s\tau_0} \times A$$  (3.1)
Table 3.6: Control word and delay settings for the time-delay cell.

<table>
<thead>
<tr>
<th>TD mode</th>
<th>Control word</th>
<th>Delay (ps) @<a href="mailto:1V@3.5GHz">1V@3.5GHz</a></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C[3:0]</td>
<td>Abs., τ</td>
</tr>
<tr>
<td>Fine</td>
<td>1011</td>
<td>83.75</td>
</tr>
<tr>
<td></td>
<td>1010</td>
<td>84.53</td>
</tr>
<tr>
<td></td>
<td>1110</td>
<td>84.62</td>
</tr>
<tr>
<td></td>
<td>0110</td>
<td>86.51</td>
</tr>
<tr>
<td></td>
<td>1111</td>
<td>86.73</td>
</tr>
<tr>
<td></td>
<td>0010</td>
<td>87.23</td>
</tr>
<tr>
<td>Coarse</td>
<td>0111</td>
<td>98.81</td>
</tr>
<tr>
<td></td>
<td>1001</td>
<td>101.82</td>
</tr>
<tr>
<td></td>
<td>1101</td>
<td>107.68</td>
</tr>
<tr>
<td></td>
<td>0101</td>
<td>129.18</td>
</tr>
<tr>
<td>No passage</td>
<td>0000</td>
<td>∞</td>
</tr>
</tbody>
</table>

Figure 3.6. The simulated delay profile for a time-delay cell, consisting of coarse and fine delays.

\[
V_{INT1} = \left( \frac{C[3]V_0}{R_0} + \frac{C[2]V_1}{R_1} \right) \left( \frac{C[3]}{R_0} + \frac{C[2]}{R_1} + \frac{1}{Z} \right)^{-1} \tag{3.2}
\]

\[
V_3 = V_{INT1} \times e^{-st_3} \times A,
\]

\[
V_4 = V_2 \times e^{-st_3} \times A \tag{3.3}
\]

\[
V_{INT2} = \left( \frac{C[0]V_3}{R_1} + \frac{C[1]V_4}{R_0} \right) \left( \frac{C[1]}{R_0} + \frac{C[0]}{R_1} + \frac{1}{Z} \right)^{-1} \tag{3.4}
\]

\[
V_{OUT} = V_{INT2} \times e^{-st_3} \times A \times e^{-st_5} \times A \tag{3.5}
\]

\[
A(t) = \left( 1 - e^{-\frac{t-\Delta A}{\tau_0 R_0 C}} \right) u(t - \Delta A) \tag{3.6}
\]

\[
B(t) = \left( 1 - \left( \frac{1}{R_0 - R_1} \right)(R_0 e^{-\frac{t-\Delta A}{\tau_0 C}} - R_1 e^{-\frac{t-\Delta A}{\tau_1 C}}) \right) u(t - \Delta A) \tag{3.7}
\]

\[
C(t) = \left( 1 - e^{-\frac{t-\Delta C}{\tau_1 R_1 C}} \right) \left( 1 + \frac{t - \Delta C}{R_1 C} \right) u(t - \Delta C) \tag{3.8}
\]

\[
\Delta B = \Delta A = \tau_0 + 2\tau_3 + \tau_5, \quad \Delta C = 3\tau_0 + 2\tau_3 + \tau_5 \tag{3.9}
\]

where \( V_{IN} \) is the input signal. \( V_0, V_1, V_2, V_3, V_4, V_{INT1}, V_{INT2} \) represent internal node signals for the time-delay cell. \( A = -1 \) symbolizes the inversion operation and \( C[\cdot] \in \{0; 1\} \) are the static control signals for path selection. \( R_N \) is the switch on-resistance, \( C_N \) is the node capacitance and \( Z = \frac{1}{j\omega C} \) is the node impedance. An inverter’s propagation delay is represented by \( \tau_N \) and the total coarse delay for different control settings is represented by \( \Delta_N \). The internal node voltages are used to derive the output response \( A(t), B(t), C(t) \) of the delay cell for unit step excitation, corresponding to the control codes 0010, 1001, 0101 respectively. The output response shows that the coarse delays are determined by the number of inverters in a path. The fine delays are determined by the threshold crossing point (\( V_{DD}/2 \)) which is regulated by the node impedance and switch on-resistance. The implemented time-delay cell provides frequency-
LO Circuits for Beamforming Receivers

Figure 3.6 shows the absolute and relative delay profile of the time-delay cell. Relative delays are important as they enable LO phase-tuning and I/Q generation; while absolute delays determine the upper frequency of operation in the presented design which utilizes minimum-sized devices. The delay profile consists of coarse and fine delays as a function of the control codes. Uneven delays provide an effective means to cover the LO signal’s time-period for $360^\circ$ phase-tuning and I/Q generation with minimum device overhead. Control code 1011 represents the by-pass mode since it exhibits the shortest absolute delay, and code 0000 disables the time-delay cell which switches off down-conversion. Details for the time-delay cell design and simulation results are presented in Publication III.

3.2.3 Phase Calibration

Relative gain and phase mismatches between the beamforming elements can arise due to process variations, signal-path non-linearity, the fabrication tolerance of the antenna feeding path and the asymmetric distribution network on the PCB. These mismatches create random errors that impact the characteristics of the beam, including an increase in the sidelobe level and a decrease in the peak-to-null ratio [59]. In the sub-6 GHz range, asymmetric signal paths between the antenna and the IC are unavoidable for large arrays because of the difference in sizes. Calibration can optimize the beam’s properties, i.e. sidelobe suppression or increase peak-to-null ratio by rectifying gain and phase mismatches between the beamforming elements [55–58].

Figure 3.7. (a) RF IC block diagram with pilot-signal generator and phase calibration scheme. (b) Pilot-signal distribution network highlighted on the PCB.
Pilot-Signal Generator

The pilot-signal generator (PSG) is shown in Figure 3.7(a). It is generated on-chip through the XOR operation of the reference LO and the down-converted LO signal (divide-by-32 block is constructed with a flip-flop based divider). Simulation results show that the PSG output buffer pushes -19 dBm to the load while consuming a measured power of 11.4 mW. The received copies for the pilot-signal generate an approximately 100 MHz baseband signal (within the baseband amplifier bandwidth) upon down-conversion from a 3 GHz reference LO signal.

Figure 3.7(b) highlights the coupler-based distribution network present on the PCB. In the receiver’s idle-mode, it can deliver the pilot-signal to the receiver input for phase calibration. The directional couplers exhibit 25-dB coupling, which is low enough to not attenuate the received RF signal while allowing the pilot-signal to be detected at the receiver inputs.

Figure 3.8(a) shows the time-domain simulation results for the pilot signal, and Figure 3.8(b) shows the measured frequency response at the baseband output, displaying the down-converted peak at ~100 MHz. Figure 3.8(a) shows the simulated time-domain waveforms for the full receiver chain, down-converting the pilot-signal for the two cases: 1 receiver is operational, and 4 receivers are operational. The simulated s-parameters for the distribution network exhibits small mismatches (< 10 ps) between the signal paths. Because the signal paths between the antenna and IC are symmetric, phase calibration was not required for these simulations. The ‘Rx bb’ waveforms represent the voltages at the summation-node capacitors after the down-conversion mixers.
Figure 3.9. (a) Measured gain for 2-element array versus phase-shift. (b) Measurements for calibration: delay-line settings are changed for element 2 to identify the null point.

**Baseband Detection**

The presented receiver can detect phase mismatches through two schemes: delay detection with two on-chip FFT units and baseband signal detection. The first method is presented in Publication I and measurement results for the second method are presented here. The baseband detection method was utilized to detect phase mismatches and characterize the delay lines. The phase mismatches are measured in relation to a reference receiver path. Two receiver paths are powered on at one point to measure their summed baseband gain. The measurements are limited to two beamforming elements in order to extract meaningful information about relative mismatches between the paths.

Figure 3.9(a) shows that the summed gain for the two elements exhibiting a wide beam and the null is the only exclusive point in the gain versus phase-shift graph which represents out-of-phase signals. Ideally, if path mismatches are non-existent, the beamforming null should appear at the 180° phase-shift point on the x-axis. The measured data shows that path mismatches move this point away by $\Delta t = t_{DL1} - t_{DL2}$ (delay introduced by DL1 and DL2). This null point can be steered by changing the delay-line settings of the second element. Secondly, this null point was also steered to estimate the delay versus control code for each beamforming element. These two sets of measurements and simulations for the delay line provided sufficient information to estimate relative phase mismatches between the two elements. The gain of one receiver is presented as a reference in the graph. Four beamforming elements in $2 \times 2$ configuration generate a wide beam; the phase tuner’s resolution ($1^0$ at 2 GHz) was measured through null steering.

Figure 3.9(b) shows that a calibration algorithm scans through different delay-line settings to search for out-of-phase received signals for 3 and
Figure 3.10. (a) Maximum gain achieved from summation of two beamforming elements versus phase-shift, dashed line shows single channel gain at 5 GHz. (b) Chip micrograph.

4 GHz LO input frequency, because they accurately indicate the delay-line settings for one state. The calibration algorithm tunes the delay-line settings based on simulated results for the time-delay cell and takes into account the previous measurement result.

The baseband phase calibration technique measures the mismatches arising from the PCB and IC assembly; it can be employed at initial power-up of the IC for a built-in self-test without the requirement of extra hardware. The demonstrated search for control codes can be performed by the back-end hardware. Antenna-generated mismatches can only be calibrated if a transmitter is present on-chip, this pilot-signal and distribution assembly providing a close approximation of the errors generated in a standalone beamforming receiver array. The baseband phase calibration accuracy is defined by the gain-tuning capability of the LNTA (1 dB steps up to 3 dB) and the phase-tuning resolution of the delay line (1° - 2.4° at 2 - 5 GHz). LNTA gain-tuning was utilized to equalize the receiver gain during phase calibration, but its 1 dB steps are designed to implement tapering.

Figure 3.10(a) demonstrates the gain invariant phase-tuning capability for the beamforming receiver with LO phase-tuning. All data points represent maximum achievable gain versus phase-shift between the two beamforming elements. These points are measured by tuning the delay-line settings of the second element after introducing a phase-shift at the RF ports. The detection was performed by external devices, a time-saving calibration algorithm being implemented resulted in a 0.7 dB variation between the measured points. The control sequence for the delay line has $2^{15}$ options for phase-tuning. The search for the control sequence at maximum gain is paced up by first hopping between coarse delay settings to find the trend i.e. maxima and minima. Then, based on the results from the coarse code sweep, a search for fine control codes is initiated to discover the minima/maxima control sequence. Since the delay values
for the time-delay cell are uneven, search time is reduced by examining previous gain values to predict if the delay jump should be longer, shorter or equal to the previous control sequence change.

### 3.2.4 Beamforming Measurements

The chip micrograph is shown in Figure 3.10(b), 4 delay lines (DLs) are located close to the receiver front-ends (Rx 1, 2, ...). The delay lines and pilot-signal generator are driven by an external reference clock.

Figure 3.11 presents over-the-air measurement results for 2 GHz and 5 GHz in both the E- and H-planes. The initial phase control settings were acquired through calibration and delay-line characterization measurements. The far-field beam patterns for the prototype, containing a $2 \times 2$ Vivaldi antenna array and 4 beamforming elements, were measured in the anechoic chamber. The RF and LO signals for the measurements were produced with a dual-channel vector signal generator, and the receiver BB signal was measured with a vector network analyzer. At 2 GHz, beamforming is demonstrated for approximately a $-30^\circ, 0^\circ$, and $30^\circ$ angle-of-arrival. At 5 GHz operating frequency, beamforming is demonstrated for approximately a $-13^\circ, 0^\circ$, and $13^\circ$ angle-of-arrival. The far-field patterns are not identical at all frequencies because of the wide operating frequency; the spacing between the antennas is optimized to $\lambda/2$ for the 3 GHz input frequency. The beamwidth and sidelobe level increase as the antenna
spacing decreases. On the other hand, the grating lobes may appear if the antenna spacing is greater than $\lambda/2$. The antenna separation is set to $\lambda/2$ to compromise between the desired beamwidth and sidelobe levels, and the grating lobes [48]. The width of the main beam is known as half-power beamwidth (HPBW), being determined by the angle between the points where the power is reduced by $3\,\text{dB}$. The far-field pattern at 2 GHz has a wide HPBW, which becomes narrow at 5 GHz. However, grating lobes appear because the antenna array spacing for 5 GHz reception was larger than $\lambda/2$. These graphs demonstrate the LO phase-tuning capability of the receiver prototype over a wide frequency range.

### 3.3 Design 2: True-Time-Delay Beamforming

This section summarizes the key research findings from the original work detailed in Publications IV and V. In Publication IV, the concept of the proposed true-time-delay beamforming and pulse-skipped LO is presented with supporting simulation results for a receiver front-end. Publication V reported the measurement results for the implemented 2-element true-time-delay receiver front-end that can achieve squint-free beamforming for up to 40% modulation bandwidth of the carrier frequency in the 0.6 - 4 GHz range. This is the first time a pulse-skipping LO mechanism has been proposed and implemented on silicon. The implemented TTD concept has been summarized in the following paragraphs followed by details for the required LO signals.

This section has been organized in the following way: first the approach adopted for implementing true-time-delay beamforming and the system-level details are presented. Then, the requirements for the LO signals are discussed, followed by the implementation details and simulation results. Finally, the measurement results for the beamforming receiver IC are presented as the proof-of-concept.

#### 3.3.1 Receiver Architecture

Figure 3.12(a) illustrates the operating principle for delay generation through discrete-time signal processing. The sampling stages sample or re-sample the continuous-time signal ($K_0$) at distinct time instants. Delay-tuning $\Delta \tau$ the re-sampling clock $C_2$ generates a delayed version ($K_2$) of the output of the first sampling stage ($K_1$).

Figure 3.12(b) shows the receiver architecture that implements the time-delay through sampling during down-conversion. The LO phase-tuning architecture was extended to enable true-time-delay beamforming by means of RF re-sampling. The arrival delay between the received signals for antenna 1 and antenna N is compensated by the delay-tuning LO signals,
\( \tau_N \) with respect to \( \tau_1 \). In the illustrated timing diagram, LO pulses are assumed to be impulses (Samp.), delayed according to arrival delay. The sampled values (Rx_1 and Rx_N) are stored on capacitors following the down-conversion mixers. The summation of signals (BF\textsubscript{COMB}) from different beamforming elements is conducted by an op-amp with capacitive feedback. The sampled signals (Rx_1 and Rx_N) are summed in-phase at the beamforming summation stage (BF\textsubscript{COMB}). Similarly, CMOS switches can re-sample the baseband signal. A re-sampling stage is added to define the instants when the sample values are updated at the baseband output (BB\textsubscript{OUT}).

In earlier discussions, the point of reference for beamforming was the incoming signal at the reference antenna, but in the presented case the common re-sampling clock (LO\textsubscript{REF}) can also be taken as a reference point. The delay difference of sampling times for different receivers with respect to the re-sampling signal compensates the time-delay between the received copies. The time-delay applied through RF sampling implements true-time-delay beamforming.

The re-sampling stage can precede the beamforming summation, but it follows the summation stage to reduce the hardware overhead and associated power consumption. Since the LO delays for the sampling mixers are measured in relation to the re-sampling clock, the delay difference is preserved in both configurations between the beamforming element’s
3.3.2 LO Requirements and Polyphase Structure

Figure 3.13(a) illustrates the limitation for the proposed TTD beamforming approach. The range for the delay-tuning element is determined by the difference in the time-of-arrival for the received RF signals. In practice, $\Delta \tau$ is set by the angle-of-arrival, the spacing between the antennas and the array size. The required delay range increases for larger arrays, in practice requiring delays longer than one clock (LO) cycle. However, the presented architecture limits the available tuning range, as can be seen from Figure 3.13(a). The output of a passive mixer ($Y_1$) is re-sampled by a clock signal $C_2$. The passive mixer consists of two switches driven by the positive and negative phase LO signals ($LO_P$ and $LO_N$). The track time ($T_{tr}$) refers to the 'on-time' for the LO signals. The re-sampling clock is added to define the instants when the sample values are updated at the baseband output (BB$_{OUT}$). The mixer and re-sampling LO signals should not overlap because the sample values at the mixer outputs should be defined before the re-sampling operation. The LO signals driving the mixers are tracking the input $Y_0$ for a good fraction of the time period $T_{LO}$. The duty cycle for the LO signals is set to be 25% for quadrature generation. The minimum delay-tuning range is limited by the tracking time of the re-sampling stage $T_{tr}$. If the LO signals are considered to be 25% duty-cycle pulses, the minimum delay range is limited by $T_{LO}/4$. This is the time required to allow the output $Y_2$ to settle. And the maximum
allowed delay is limited by the time period of the LO signals minus the track time of both sampling and re-sampling signals. The total tracking time for the sampling mixer clock \( T_{\text{samp.}} \) and achievable delay-tuning range \( t_{DL} \) is

\[
T_{\text{samp.}} = T_{LOp} + T_{LOn} + 0.25^*T_{LO} \quad (3.10)
\]

\[
T_{\text{samp.}} = 0.75^*T_{LO} \quad (3.11)
\]

\[
t_{DL} = [0 \quad ... \quad 0.25(T_{LO}) - T_{tr,2}] \quad (3.12)
\]

Figure 3.13(a) illustrates this point, the top set of signals \( Y_1, Y_2, LO_{P/N}, C_2 \) (white background) representing a conventional LO signaling case. The maximum allowed delay range is less than a quarter of one LO period. This tuning range is insufficient for implementing the TTD operation because the delay range should be equal to the time-of-arrival delays for the received copies from the edge antennas in linear arrays. This limitation can be alleviated either by decreasing the clock frequency or skipping the LO signal pulses to extend the delay-tuning range. In Figure 3.13(a), for the second set of signals, the \( LO_{P/N}, C_2 \) (with yellow background) represent the 2 pulse-skipped case, the delay range is extended up to \( 2^*T_{LO} \). In the later case, there are two additional RF paths (compensation branches) included for polyphase combination.

For the proposed TTD architecture, the required number of skipped LO pulses \( M \) can be derived from the maximum time-of-flight delay \( \Delta t_{D_{\text{max}}} \) experienced by the signals arriving at the \( N^{th} \) antenna with respect to the reference. Then, the maximum delay-tuning range \( t_{DL_{\text{max}}} \) is determined by

\[
\Delta t_{D_{\text{max}}} = \frac{d(N - 1)\sin(\theta_{\text{max}})}{c} \quad (3.13)
\]

\[
t_{DL_{\text{max}}} \geq \Delta t_{D_{\text{max}}} \quad (3.14)
\]

\[
t_{DL_{\text{max}}} = (M)T_{LO}, \quad T_{LO} \geq 1/(2BW) \quad (3.15)
\]

\[
M = \frac{2d}{\lambda_{LO}} (N - 1) \left( \frac{BW}{f_{LO}} \right) \sin(\theta_{\text{max}}) \quad (3.16)
\]

\[
M = \frac{2d}{\lambda_{LO}} (N - 1) \left( \frac{BW}{f_{LO}} \right) \sin(\theta_{\text{max}}) \quad (3.17)
\]

\( N \) is the size of a linear array, \( d \) is the spacing between the antennas and \( T_{LO} \) is the time period of the LO signal. The maximum steering angle-of-arrival is represented by \( \theta_{\text{max}} \), and the modulation bandwidth is written as \( BW \).

For the LO signal chain, pulse-skipping means that if every other pulse is skipped, a compensating branch is added to the receiver. The skipped pulses drive the compensating branch’s mixer. In the presented design, pulse-skipping extends the delay-tuning range by 3 LO cycles to enable
TTD for an array of 8 antennas. The inter-element antenna spacing is set to $\lambda/2$ and the maximum angle-of-arrival is assumed to be $60^\circ$.

Figure 3.13(b) shows the proposed TTD beamforming receiver with 4 polyphase branches and pulse-skipped LO signaling. These branches are added because down-conversion with pulse-skipped LO signals leads to spectral aliasing at multiples of $f_{LO}/N$. The noise and interference signals present at multiples of $f_{LO}/N$ are also down-converted along the desired signal. Spectral aliasing can be evaded if the sample rate is restored to $f_{LO}$; this is accomplished by a polyphase structure. It restores the sample rate by incorporating $N$ independent down-conversion branches that are combined after re-sampling. Each compensation branch is driven by LO signals operating at $f_{LO}/N$. The LO signals for each compensation branch are shifted by the $T_{LO}$ relative to adjacent branches.

An advantage of this technique is that it can enable TTD beamforming for a modulation bandwidth as large as the Nyquist criterion allows i.e. $f_{LO}/2$.

### 3.3.3 LO Generation

Figure 3.13(b) shows the implemented TTD receiver architecture that comprises four polyphase branches. Each polyphase branch operates with the pulse-skipped non-overlapping I/Q signals. The LO signals provide the pulse-skipped sampling and re-sampling clock signals for TTD operation. In the presented case, the LO pulses are skipped by 1-3 LO cycles. The architecture for LO generation is slightly different from the receiver, a slice of LO generator is providing the mixer driving signals for all delay compensation branches associated with an antenna.
Figure 3.14(a) shows that the implemented LO generation can be divided into three parts: delay-tuning, 4-phase generation and pulse-skipping. The delay line is responsible for coarse phase-tuning; it precedes I/Q signal generation to save power. It can be classified as a tapped delay line constructed with inverters, the required coarse delay being selected by the multiplexers with a step size of 35 ps. The delay line executes only coarse delays because pulse-skipped LO distribution across the chip will cause a timing mismatch between the mixer inputs for different compensation branches.

25% duty-cycle I/Q signals are generated by the latch-based frequency divider [117]. The master-slave latch topology requires the setting of initial node voltages during start-up to initiate the correct order of I/Q pulses. This is accomplished by introducing pull-up and pull-down control switches in the latch output nodes \( \varphi_1 \) and \( \varphi_3 \). The control transistors set the nodes through minimum size NMOS and PMOS transistors, which are 25 times smaller than pull-up and regenerative loop transistors which helps reduce their impact on the output after start-up. The I/Q generator is followed by a multiplexer to generate coarse delays of \( T_{LO}/2 \) to cover one LO cycle. The delay line operating at \( 2 \times f_{LO} \) can only cover the delay range of \( T_{LO}/2 \).

A pulse-skipping slice is shown in Figure 3.14(b). It is made up of 4-bit ring counters that act as control signals for pulse-skipping. The ring counters were constructed with TSPC logic D flip-flops. The LO signal driving the mixers serves as a clock signal for the ring counter. TSPC logic was chosen because it requires a single-ended clock, and the implementation is a ratio-less device. The LO signals from the frequency divider drives the mixers and ring counters. In path P, a buffer was added to drive \( 4 \times 4 \) transistors present in the D flip-flops of the ring counters to ensure fast transition time. Since the propagation delay for the asymmetric paths P and Q is different, and the path P provides the control signal for the multiplexer, synchronization of the signals is critical. The control signal delay stems from the propagation delay for the buffer and delay element, the setup time and CLK-to-Q for the D flip-flops. As the LO signals are trapezoidal in nature, their spectral content at \( f_{LO} \) is affected by the rise-time. The control pulse should arrive before the Q path signal to preserve the pulse-skipped LO signal’s integrity. Given the longer path delay in the ring counter, it is driven by an inverted clock and a chain of buffers is added for additional delay and synchronization.

The ring counters are set/reset initially by a trigger pulse generated from their input clock. The trigger circuit is composed of an XOR gate based pulse generator for the initial setting of internal nodes. Current-starved inverters are integrated in the feedback loop to allow flexibility of skipping any number of pulses within the range from 1 to 3. The second multiplexer, controlled by a 4-bit synchronous counter, realizes both pulse-skipping and delay-tuning with a step size of \( T_{LO} \) between the polyphase branches.
Pulse-skipping is the last stage before mixer buffering.

PVT variations can affect the delay-line tuning range and resolution. The implemented design is robust against process variations mainly because of the sizing of buffers, it being 10 times the minimum allowed size. The details of pulse-skip control synchronization are discussed in the following paragraphs. Buffering between the stages ensures that the rise time is restored throughout the chain. In the implemented IC with two beamforming elements, certain LO signals of receiver 1 (reference path) are reused as the re-sampling clock.

The time-domain LO and re-sampling waveforms for TTD beamforming with the 3 pulse-skipping case (PS) are shown in Figure 3.15 (a) and (b). The presented design has two beamforming elements that are represented by Ant_1 and Ant_2. Here, Br_A or Br_B represent the polyphase branches utilized in the pulse-skipping mode. The re-sampling signal for each branch is represented by Resamp.

Figure 3.15(a) shows LO and re-sampling waveforms for one delay compensation branch. The simulation results show that a maximum delay between the LO signals of $3^*T_{LO}$ can be achieved. This delay range requirement is derived from the array spacing for a linear array and maximum angle-of-arrival. If the two beamforming elements (Ant_1 and Ant_2) represent the outermost antennas of an 8-element array with $\lambda/2$ spacing between the elements, the two antennas will have a distance of 3.5 $\lambda$. From Equation 3.17, the delay-tuning range needs to cover delays up to $3 T_{LO}$, if the maximum desired angle-of-arrival is set to be 60°.
Figure 3.16. Timing diagram for LO and re-sampling waveforms for beamforming elements Ant_1 and Ant_2, pulse-skip (PS) mode= 3: (a) timing diagram for LO and control signals. (b) Delay-tuning range versus control codes.

Figure 3.15(b) shows the LO and re-sampling signals for the full receiver, following a similar delay arrangement as Figure 3.15(a). Pulse-skipping increases the delay range in proportion to the number of skipped pulses. The window of interest is highlighted in red; it moves by one clock cycle for each delay compensation branch. Because the sample rate has been decreased to $f_{LO}/4$, the compensation branches sample the received signal by a delay of $T_{LO}$. These are added to restore the sample rate to $f_{LO}$. The LO signals are re-used for the re-sampling clock, the I path LO signals functioning as the re-sampling clock for the Q path and vice versa.

Figure 3.16 (a) and (b) shows the simulations results for the LO generator’s delay-tuning capability in two formats: the timing diagram and the delay range versus control code simulations. Figure 3.16(a) shows mostly the I path waveform IP for different stages of the designed LO generator. The delay line operates at $2^*f_{LO}$ of the mixer input signals introducing a coarse delay step of 35 ps to cover a range of $T_{LO}/2$. Two stages of multiplexers extend this range to one $T_{LO}$ and $3^*T_{LO}$ (depending on the number of skipped LO pulses) respectively. The timing of the pulse-skip control signal (PS CTRL) is synchronized with the falling edge of the input clock signal. The pulse-skipping window is generated by a ring counter, path delays between the IP and PS CTRL are unequal, so synchronization of the pulse-skip control is important. It is carried out by the falling edge of the IP signal, which also serves as the clock for the ring counter. Additional buffers are added in the clock path for the ring counters to control $\Delta \tau_{CTRL}$.

Figure 3.15 (b) shows the simulation results for the range of achievable delays for one compensation branch operating at 1 - 4 GHz. The results are presented for the 3 pulse-skipped scenario, where the * marks in the graph
represent the time period of one clock cycle ($T_{LO}$). The achieved delay-tuning range is three clock cycles, it being limited by the non-overlapping condition of the sampling and re-sampling signals. The delay range scales with the frequency in this scheme.

3.3.4 Beamforming Measurements

Figure 3.17(a) shows the chip micrograph; the LO pulse-skipping block is present between the mixers and the baseband summation plus the re-sampling stage. Figure 3.17(b) shows the measured performance of the 2-element TTD receiver, operating in the 0.6 - 4 GHz range. It was fabricated in 28-nm CMOS process. To prove the presented TTD concept, the measurement results for the 2-element beamforming are presented for the following case: beamforming elements (Ant$_1$ and Ant$_2$) represent the outermost antennas of an 8-element array, with $\lambda/2$ spacing between them. A far field signal will experience a delay of $3.5 \lambda$ for the antenna 2 with respect to a reference antenna. If the maximum desired angle-of-arrival is set to be 60°; the maximum delay compensation required is $3 \times T_{LO}$. The results shown depict this scenario, the presented LO generator achieved a relative delay of 3 clock cycles with respect to the reference branch. True-time-delay beamforming means that the beam points towards the target direction over the modulation bandwidth. In the presented case, the modulation bandwidth is set to be 800 MHz with the center frequency of
2.001 GHz.

Figure 3.17 (i) shows the measured directivity at 1.600 GHz, 2.001 GHz and 2.400 GHz. The main lobe of the beam points towards 60° exhibiting a squint-free beam. These measurement results conform with the simulation results presented in Figure 3.17 (ii). For the same test setup, the LO phase-shifting simulations lead to beam-squinting and a loss of 9 dB gain across the modulation bandwidth, as shown in Figure 3.17 (iii). The grating lobes, visible in the beam patterns, and wide beamwidth are a consequence of the large spacing presumed between the antennas and the small number of elements. The null depth of the array gain is limited by the bandwidth of the summation amplifier (70 MHz baseband bandwidth). The receiver front-end implementation details are discussed more fully in Publication IV.

3.4 Performance Summary for Designs 1 and 2

In this section, two comparison tables are presented comparing the performance of design-1 (LO phase-tuning) and design-2 (true-time-delay) with state-of-the-art beamforming receivers. Design-1 targets included wideband receiver front-end design, beamforming based on LO phase-tuning, phase calibration with the back-end and baseband circuits, interfacing of the LO, RF and digital paths keeping in view the scalability of the beamforming array, and antenna+IC co-design.

The implemented 4-element beamforming receiver achieved 2 - 5.5 GHz operation applying LO phase-tuning through a digitally-controlled delay line. Additionally, the design incorporated on-chip phase calibration with pilot-signal generation and baseband detection. The phase-tuning functionality was measured for the prototype including the 4-element Vivaldi antenna array. In design-2, LO phase-tuning was extended to true-time-delay (TTD) through RF re-sampling and the pulse-skipped LO. The implemented receiver achieved TTD beamforming for a modulation bandwidth as large as 40% of the LO frequency. The proposed RF re-sampling and pulse-skipping LO was integrated in a direct-conversion receiver operating in the 0.6 - 4 GHz range.

Table 3.1 summarizes the performance of design-1 and compares it with the state-of-the-art sub-6 GHz beamforming receivers that have applied phase-tuning techniques. The overall receiver comparison and measurements show that the LO phase-tuning methods implemented by the author enable state-of-the-art performance. In fact, the applied technique achieves higher phase resolution with lower power consumption per beamforming element.
Table 3.1. Comparison of sub-6 GHz CMOS beamforming receivers employing phase-tuning techniques.

<table>
<thead>
<tr>
<th>Reference</th>
<th>JSSC’20 [51]</th>
<th>ISSCC’16 [118]</th>
<th>JSSC’18 [119]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beamforming Elements</td>
<td>4 (4×4 MIMO)</td>
<td>4 (4×4 MIMO)</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>Antenna array</td>
<td>N/A</td>
<td>2×2</td>
<td>N/A</td>
<td>2×2 Vivaldi</td>
</tr>
<tr>
<td>Calibration</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Phase</td>
</tr>
<tr>
<td>Phase-tuning domain</td>
<td>Analog</td>
<td>LO</td>
<td>Digital</td>
<td>LO</td>
</tr>
<tr>
<td>RF Freq. (GHz)</td>
<td>0.7 - 5.7</td>
<td>0.1 - 1.7</td>
<td>1</td>
<td>2 - 5.5</td>
</tr>
<tr>
<td>CMOS Tech. (nm)</td>
<td>22</td>
<td>65</td>
<td>40</td>
<td>28</td>
</tr>
<tr>
<td>Power Supp. (V)</td>
<td>0.8</td>
<td>1.2</td>
<td>N/A</td>
<td>1 - 1.2</td>
</tr>
<tr>
<td>Power Cons. (mW)</td>
<td>77 - 139 (0)</td>
<td>83 (analog)</td>
<td>312 (2)</td>
<td>18 (3)</td>
</tr>
<tr>
<td>Active area (mm²)</td>
<td>0.52</td>
<td>1.69</td>
<td>0.22 (2)</td>
<td>0.62 (4)</td>
</tr>
<tr>
<td>Phase-tuning Technique</td>
<td>Const. Gm VM</td>
<td>Cartesian VM</td>
<td>Complex Weight Multiplication</td>
<td>Delay line</td>
</tr>
<tr>
<td>Resolution</td>
<td>5.5 bits</td>
<td>6 bits</td>
<td>6 bits</td>
<td>&gt;7 bits</td>
</tr>
<tr>
<td>1 Phase-tuner Power Cons. (mW)</td>
<td>N/A</td>
<td>N/A</td>
<td>68 (6)</td>
<td>2.23 - 5.6 (5)</td>
</tr>
</tbody>
</table>

(0) for 4 beamforming elements.
(1) at 500 MHz.
(2) ADC + digital down-conversion + digital beamforming entity.
(3) 1 beamforming element for 3 GHz LO, consisting of 1 RF front-end + DL + shared baseband I and Q amplifiers and LO buffers (divided by element count).
(4) 4 front-ends and DL + baseband I/Q amplifiers + 2 SAR-ADC + 2 FFT units.
(5) Scales with frequency: 2 - 5 GHz.
(6) Digital beamforming (DBF) entity.

The designed LO phase-tuning and phase calibration blocks enable > 7-bit (1⁰-2.4⁰) phase resolution. 6-bit or higher resolution can suppress the sidelobes within ~1 dB of an ideal phase-shifter [50], achieve higher calibration accuracy and phase error margin for PVT variations. The implemented delay line benefits from technology node scaling, consuming moderate power: 2.23 - 5.6 mW for 2 - 5 GHz. The wide beamforming capability was verified with a 2×2 Vivaldi antenna array. Phase calibration was demonstrated through delay detection with FFT units to detect phase mismatches of 1.44⁰ and 3.96⁰ for 2 GHz and 5.5 GHz signals accordingly. Phase mismatches were also measured through baseband detection (1⁰) with the aid of an external calibration loop.

Increasing the number of antennas improves the receiver sensitivity at the expense of increased power consumption. This, however, requires a power efficient front-end. This beamforming architecture can be expanded to a larger array size because the phase-tuning element occupies an active
Table 3.2. Comparison of sub-6 GHz CMOS beamforming TTD techniques.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Beamforming</td>
<td>RF</td>
<td>RF</td>
<td>RF</td>
<td>Digital</td>
<td>BB</td>
<td>LO</td>
</tr>
<tr>
<td>Time-delay Technique</td>
<td>LC</td>
<td>Gm-C</td>
<td>Gm-C</td>
<td>DDL and CWM</td>
<td>BB re-sampling</td>
<td>RF re-sampling</td>
</tr>
<tr>
<td>No. of Elements</td>
<td>N/A</td>
<td>4</td>
<td>N/A</td>
<td>16</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>RF Freq. (GHz)</td>
<td>1 - 20</td>
<td>1 - 2.5</td>
<td>0.1 - 2</td>
<td>1</td>
<td>N/A</td>
<td>0.6 - 4</td>
</tr>
<tr>
<td>Range (ps)</td>
<td>400</td>
<td>550</td>
<td>250 - 1700</td>
<td>0 - 7500</td>
<td>15000</td>
<td>750 - 5000(5)</td>
</tr>
<tr>
<td>Resolution (ps)</td>
<td>5.6+0.2(1)</td>
<td>13</td>
<td>10(1)</td>
<td>10 bit</td>
<td>5</td>
<td>35</td>
</tr>
<tr>
<td>Amplitude Variation vs Freq (dB)</td>
<td>N/A</td>
<td>± 1.4</td>
<td>± 0.7</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>CMOS Tech. (nm)</td>
<td>130</td>
<td>140</td>
<td>130</td>
<td>40</td>
<td>65</td>
<td>28</td>
</tr>
<tr>
<td>Power Supp. (V) by 1 Delay Element</td>
<td>1.2</td>
<td>1.5</td>
<td>1.4</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Power Consumed (mW) by 1 Delay Element</td>
<td>2.2 - 5</td>
<td>90</td>
<td>112 - 364</td>
<td>196(2)</td>
<td>47(3)</td>
<td>5 - 13(4)</td>
</tr>
<tr>
<td>Active area (mm²) by 1 Delay Element</td>
<td>4</td>
<td>0.15</td>
<td>0.29</td>
<td>0.13(2)</td>
<td>0.57(3)</td>
<td>0.13(3)</td>
</tr>
</tbody>
</table>

(0) Scales with f_{LO}.
(1) Continuous tuning.
(2) Digital beamforming entity.
(3) 4-input baseband beamformer.
(4) multiphase LO generator and passive mixer’s power consumption for one antenna, it scales with F_{LO}.
(5) 1 beamforming element + shared front-end.

area, 0.008 mm² (1 DL) and 0.005 mm² (shared input buffer and clock-tree). It can be placed close to the mixers to reduce mismatches. These characteristics suggest that the architecture can be suitable for larger array sizes.

Articles presenting constant-Gm vector modulators [51, 74] have not addressed LO signal mismatches for inter-element or intra-element I/Q signals, these mismatches possibly stemming from distribution asymmetry or process variations. Moreover, the phase resolution of constant-Gm vector modulators is proportional to the number of slices, the design implementing 44 phase steps with 15 slices per antenna for beamforming. A slice contains a transconductance stage and a passive I/Q mixer requiring a proportional amount of driving LO buffers, increasing the power consumption for higher resolution. Similar to all analog beamforming approaches, LO phase-tuning relaxes the required dynamic range for the ADC (in comparison to digital beamforming) because the interference signals from all receiving directions are filtered [119]. In [118], the interference signals can be filtered from two directions.

Table 3.2 summarizes the measured performance of different TTD techniques and compares them to the state-of-the-art architectures in the literature. Passive structures in the RF path occupy a large area especially in the low GHz range, rendering it impractical. Moreover Gm-C cells consume higher power when compared to other techniques. [113] has...
adopted a similar TTD beamforming architecture, however the novelty in our design is that the LO phase-tuning has been extended to TTD operation through RF re-sampling to achieve the desired functionality with the least hardware (re-cycling blocks).

The presented technique suits wideband low-GHz beamforming implementation for true-time-delay because of its implementation ease, lower power and area consumption. Pulse-skipping and multiplexing extends the delay range to $3 T_{LO}$ which scales with the LO frequency. To extend the proposed TTD beamformer to larger arrays, the pulse-skipping range needs to be extended to a higher number of LO cycles. This can be accomplished with a small increase in power or occupied area, by incorporating a higher bit ring or a mod-2n ring counter.

### 3.5 Design 3: LO Chain for 12-25 GHz

This section concentrates on designing LO chain blocks for frequencies above 10 GHz. Here, circuits are designed with mixed-signal techniques to benefit from the CMOS scaling trend. Deep submicron CMOS processes offer transistor performance with transit frequencies ($f_T$) and maximum oscillation frequencies ($f_{max}$) exceeding several hundreds of gigahertz [121]. These metrics of transistor speed when combined with innovative architecture and circuit-level design can open opportunities to design the millimeter-wave CMOS transceivers. In the future, phased arrays will be developed mostly for the millimeter-wave to establish higher data-rate communication links.

LO circuits for transceiver applications above 10 GHz are often designed using analog techniques [94,103]. This leaves the question of pushing the
digital boundary close to the antenna interface largely unaddressed, especially for high-frequency reception. The presented LO circuit attempts to address this need by migrating mixed-signal techniques to receive signals above 10 GHz. The implemented receiver and LO signal chain is part of a transceiver, which, due to delayed measurements, the full transceiver characterization is yet to be completed.

The receiver and LO block diagram is shown in Figure 3.18. The receiver implementation consists of the first stage of heterodyne architecture with an output frequency of up to 7 GHz. This receiver front-end can be integrated with the direct-conversion receiver presented as design-1 for heterodyne reception to IF frequency. It is composed of a single-to-differential transformer, cross-coupled common-gate LNA, Gilbert cell mixer and an IF amplifier. The input transformer serves a dual purpose: single-to-differential conversion and ESD protection. The LO chain aims to drive the mixers through hard switching in the range of 12 - 25 GHz. At these frequencies, rail-to-rail signal generation and propagation requires special design considerations. The RC time-constant contributed by the load, interconnect and transistor parasitics limits the driving capability of the circuits. Logic circuits with more than two transistors require higher drive strength that cannot be provided easily at these frequencies. Given these constraints, the circuits for pulse-generation and phase-tuning are implemented with inverters, that present the smallest possible load.

3.5.1 Implementation

Figure 3.18, illustrates the LO signal chain, the reference LO signal being fed in through a single-to-differential transformer and the distribution buffers. The pulse generation is the first block in the LO chain responsible for generating pulse-like waveforms. It consists of an inverter chain, each inverter driving 1.5 times its size. The inverter sizing has been limited to a ratio of 1.5 because the driving inverters could not amplify a 25 GHz LO signal greater than this load. Amplification is required here to create rail-to-rail pulse-like waveforms. The pulse generator is followed by a phase-tuning element consisting of 10 inverter-varactor pairs. The varactors are driven by a 2.3 times minimum-sized inverter to maintain the signal integrity up to 25 GHz; digital controls (0,1) enable the varactor-tuning. The varactor-tuning block can calibrate phase mismatches between the LO_F and LO_N signals (mixer inputs) to optimize performance or can serve as phase-tuning for beamforming applications.

The simulation results in Figure 3.19(a) show the post-layout simulation results for the LO signal chain at 16 GHz and 21 GHz respectively. The waveforms in the sub-figures (i) and (ii) are the differential signals at the input of the double-balanced mixer. The interconnect and via resistance, the interconnect capacitance to the substrate, the coupling capacitance
between the interconnects and the intrinsic parasitic capacitance of the transistors contribute to the RC time-constant that limits the rise and fall time of the LO signals. The minimum transistor sizes for millimeter-wave transistor models in the CMOS process are restricted, allowed W/L ratio for millimeter-wave model being 10 times minimum process W/L, exhibiting higher load capacitance.

Figure 3.19(b) shows the post-layout time-domain waveforms to illustrate the phase-tuning capability of the LO chain at 18 GHz. Here, one of the differential input signal LO\(_P\) is phase-tuned by progressively changing the varactor controls from V\(_{DD}\) to ground. The simulated phase-tuning range of the varactor-inverter chain is ~85\(^0\); eight stages exhibit ~8\(^0\) step size and the last two stages are designed to have four steps of ~2.5\(^0\). Varactor-based phase-tuning is suitable for a wide LO operating range of 13 GHz.

### 3.5.2 Measurements

A part of the chip micrograph is shown in Figure 3.20(a) that shows the LO and mixer blocks. The chip consisting of a transceiver was fabricated on 22-nm CMOS process. However, due to delay in conducting measurements, only the receiver has so far been characterized. An LO block takes up an area of 400um x 150um, which is mostly occupied by the supply routing to support large instantaneous currents flowing during the switching operation of inverters. The overall power consumption for the LO signal chain is 176 mW at 25 GHz for three independent LO blocks associated with two on-chip transmitters and one receiver, and the distribution buffers. If this power consumption is equally divided among each LO block, it consumes ~60 mW, and each differential signal path (LO\(_P\) and LO\(_N\)) consumes ~30 mW. The power consumption for the LO block is dominated by the phase-tuning block, which consists of 10 inverter-varactor pairs. The trapezoidal shape (I-V overlap) of the waveforms increases the power loss
Figure 3.20. (a) Part of chip micrograph showing LO and mixer blocks. (b) Frequency response of receiver versus LO frequency with each plot scaled to 0 dB.

during the switching operation of the inverters.

Figure 3.20(b) shows the measured frequency response of the receiver versus LO frequency; the LO transformer limits the lower end of the operating range, and the upper range is limited by the performance of the LO chain. The LO transformer exhibits a variation in loss of about 3 dB (simulation results) in the reported range. The measured receiver gain varies by 5 dB over the operating receiver band: 13 - 26 GHz. The IF frequency was set to 1 GHz for these measurements. The receiver’s gain variation trend for the measured results conforms with the simulation results up to a LO frequency of 21 GHz, the LO chain losses decreasing the gain for higher frequency operation.

Overall, the presented LO signal chain is functional from 12 - 25 GHz with phase-tuning capability. The presented design drives the mixers of the first stage of a heterodyne receiver. This implementation demonstrated that rail-to-rail LO signaling can be generated, processed and propagated up to 25 GHz in deep submicron processes.
4. Conclusions

This thesis explored the design and development of beamforming receivers and LO circuits for phase-tuning and true-time-delay operating in the sub-6 GHz band. The choice of beamforming approach impacts the footprint of the receiver's signal chain, and the required dynamic range for the blocks before beamforming summation. The research is motivated by the fact that analog beamforming can be deployed in transceivers either as a standalone solution or as part of hybrid beamforming. Hybrid beamforming is an attractive approach because it preserves the advantages derived from analog beamforming including a relaxed ADC dynamic range and reduced signal-block footprint, and incorporates the higher computational flexibility from digital beamforming for spatial diversity. This thesis concentrates on LO phase-tuning, extending it to true-time-delay beamforming, because it can outperform RF or analog phase-tuning architectures in some respects. LO phase-tuning is able to maintain orthogonal gain and phase-tuning, it can simplify the calibration procedure with the possibility of integrating two independent calibration loops, and it can conserve the linearity and NF performance of the RF signal path.

The original research presented in this thesis is based on three receiver implementations, the focus being on the development of an LO chain for beamforming in the sub-6 GHz band. Design-1 is a 2-5.5 GHz 4-element beamforming receiver that employed LO phase-tuning. The achieved targets include higher than 7-bit phase-resolution with $360^\circ$ phase-tuning and an on-chip calibration capability with two different detection methods: baseband and FFT. Baseband detection measured the phase mismatches up to $1^\circ$, the calibration loop having external detectors. The proposed delay line aids orthogonal phase-tuning, divider-less I/Q generation and compact design ($0.008 \text{mm}^2$) with moderate power consumption (2.23-5.6 mW for reported range) favoring the integration of a higher number of beamforming elements in comparison to other analog beamforming techniques. The wide beamforming capability was verified with a $2 \times 2$ Vivaldi antenna array. Publications I-III present the design details and results for the receiver and LO phase-tuning block.
Design-2 extended the LO phase-tuning architecture to true-time-delay (TTD) through RF re-sampling of discrete-time signals. This scheme requires delays longer than one LO cycle, which was accomplished by introducing a pulse-skipping LO mechanism. The designed and implemented pulse-skipping LO circuit can extend the delay range up to 3 carrier cycles, appropriate for an 8-element beamforming. The delay-tuning range scales with the LO frequency. The proposed RF re-sampling and pulse-skipping LO were integrated in a direct conversion receiver operating in the 0.6-4 GHz range. The receiver achieved beam-squint-free TTD beamforming for modulation bandwidths as large as 40% of the LO frequency. The multiphase LO generator and passive mixers consume 5 - 13 mW for one beamforming element in the reported range. Publications IV-V present the design details and results for the TTD receiver and LO block.

Design-3 concentrates on developing a LO signal chain operational between 12 - 25 GHz. The presented LO chain drives the first stage of the heterodyne receiver with IF frequency up to 7 GHz. This design concentrates on answering the question: can the digital domain be pushed close to the antenna interface for receivers operating above 10 GHz? As a first step to answering this need, the LO chain was designed with mixed-signal techniques. This implementation, with pulse-generation and phase-tuning capability, demonstrated that rail-to-rail LO signaling can be generated, processed and propagated up to 25 GHz in the deep submicron processes. Some key requirements for beamforming receivers were addressed in this dissertation. However, there is room for improvement; for instance, power optimized was largely unaddressed due to strict tape-out deadlines. Distribution buffers consume a good portion of LO power; including adaptive supply voltage through low-dropout regulators for inverters can reduce the consumed power. A localized LO-path calibration block can speed up phase calibration for mismatches stemming in the LO path; moreover calibration can be performed during reception. Duty-cycle control circuits present close to the mixers might be required to produce 25% duty-cycle waveforms. The pulse-skipped LO implementation can also be based on the time-interleaving concept. A low frequency signal with coarse delay tuning and duty-cycle control can mimic the pulse-skipping function with a reduced reference LO frequency.

Beamforming is a vast subject, this study could be extended to include beamforming transmitters and high frequency phased arrays. At the millimeter-wave band, the trade-offs for a beamforming architecture and circuit design of the LO distribution, phase-tuning and calibration requires an in-depth investigation. The LO distribution lines are comparable to the signal wavelength; routing and matching are critical design aspects, and circuit design procedure is different from the low GHz circuits. Built-in self-test can reduce the cost of calibration for the millimeter-wave phased arrays against PVT variations. The LO generator needs careful archi-
architecture planning for power/area consumption versus LO synchronization trade-offs. An LO block may consist of phase-locked loops, frequency doublers/triplers and calibration blocks. The design of the calibration scheme and detection circuits is an interesting topic for further study.

In summary, this dissertation addressed some 5G requirements by presenting receivers that operate over several GHz in the FR1 and support up to 100 MHz modulation bandwidth. The work also addressed the optimization of beam pattern and beamsteering through accurate phase-tuning with $360^\circ$ range, and deployment related challenges including area and power consumption, calibration and true-time-delay beamforming. It also studied the challenges of implementing mixed-signal techniques for the LO chain operating above 10 GHz. As a whole, the thesis provided a deeper perspective into beamforming receiver design by addressing a wide set of sub-topics, and presented LO phase-tuning as a competitive choice among other architectures.
References


References


5th generation (5G) demands high data-rate connections for wireless channels that are crowded by interference signals. Beamforming is one effective way to reduce interference and improve the signal-to-noise ratio to enable higher data-rate connections. The presented work concentrates on the design of local oscillator (LO) circuits for beamforming receivers, addressing some challenges in hardware development for 5G.