Carbon nanotube thin film transistors based on aerosol methods

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Abstract

We demonstrate a fabrication method for high-performance field-effect transistors (FETs) based on dry-processed random single-walled carbon nanotube networks (CNTNs) deposited at room temperature. This method is an advantageous alternative to solution-processed and direct CVD grown CNTN FETs, which allows using various substrate materials, including heat-intolerant plastic substrates, and enables an efficient, density-controlled, scalable deposition of as-produced single-walled CNTNs on the substrate directly from the aerosol (floating catalyst) synthesis reactor. Two types of thin film transistor (TFT) structures were fabricated to evaluate the FET performance of dry-processed CNTNs: bottom-gate transistors on Si/SiO2 substrates and top-gate transistors on polymer substrates. Devices exhibited on/off ratios up to 105 and field-effect mobilities up to 4 cm2 V−1 s−1. The suppression of hysteresis in the bottom-gate device transfer characteristics by means of thermal treatment in vacuum and passivation by an atomic layer deposited Al2O3 film was investigated. A 32 nm thick Al2O3 layer was found to be able to eliminate the hysteresis.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Impressive progress has been achieved over the last decade in the development of organic thin film transistors (TFTs), which in combination with large-area printing methods provide a low-cost alternative to hydrogenated amorphous silicon TFTs for the fabrication of flexible, lightweight and large-area electronic devices [1, 2]. However, the performance of organic electronics is limited by the low charge-carrier mobility. In addition, organic semiconductors may exhibit processing difficulties due to their insolubility or air sensitivity under ambient conditions [2, 3]. Recently, the application of random carbon nanotube networks (CNTNs) as a semiconducting material for TFTs has been the subject of profound research interest owing to their higher performance in comparison to organic TFTs and potentially low-cost fabrication [4–6]. The uniformity of CNTN properties is achieved by statistical averaging over a number of individual tubes comprising the network. This allows one to attain reproducible electrical behavior over larger length scales in comparison to individual carbon nanotubes (CNTs), where tube to tube variations in chirality, position, and orientation constitute a major fabrication obstacle [4, 7]. Various devices and components based on CNTNs have been successfully demonstrated, including field-effect transistors (FETs), diodes, logic circuit elements, solar cells, displays, and sensors [5, 6].

Typically, prior to the actual device fabrication, random CNTNs are produced either by localized synthesis processes on the catalyzed substrates or by remote synthesis processes, depositing CNTs from suspensions using spray- and dip-coating [8], spin-coating [9, 10], vacuum filtration [7, 11], airbrushing [12], or electrophoretic deposition [13]. Localized
growth of CNTNs directly on the substrate gives a possibility to achieve well-aligned long nanotubes with selective spatial growth and dense packing; however, it requires high growth temperatures (>600 °C) and reactive environment, and there may be undesirable by-products deposited on the substrate surface during the growth process. Deposition of pre-synthesized CNTs from liquids in ambient conditions is nowadays the most widespread technique. However, it involves additional time-consuming processing steps like purification and dispersion of CNTs. Due to their inert nature, non-functionalized CNTs show low solubility and tend to aggregate into bundles owing to strong van der Waals forces, which makes CNT dispersions unstable in time. In order to prepare a homogeneous dispersion of single-walled CNTs (SWCNTs), various techniques involving dispersing agents like surfactants or polymers with thorough ultrasonication or shear mixing [14], as well as CNT solubilization by means of chemical functionalization [15] have been used. Moreover, the adhesion of the nanotubes to the substrates can be improved by functionalizing the substrate itself with, for instance, polyimide or a self-assembled monolayer of 3-aminopropyltriethoxysilane (APTS) before the CNT deposition (e.g. [16]). Some methods have been developed in order to avoid the CNT length reduction or chemical modification: for example, dissolving polyelectrolyte CNT salts in polar organic solvents [17]. However, an inert non-oxygen-containing atmosphere is needed to keep the solution stable. Still all these methods constitute solution-based tedious multi-step preparation processes that require removing the excess surfactant after the deposition, which influences the inter-tube contact and thus the electrical performance of the network [18].

We have developed an alternative technique for the fabrication of CNTN devices based on a simple and dry deposition of CNTs directly after the aerosol (floating catalyst) synthesis reactor. This essentially single-step deposition occurs at room temperature instantaneously after the CNT growth, enabling scalable fabrication of electronic devices using various substrates including lower-heat-tolerant plastic substrates. Thus, this method is potentially applicable for the realization of low-cost, flexible, and transparent electronics. Moreover, this technique allows a precise CNTN patterning for transistor channels using standard photolithography and lift-off. The network consists of small bundles of high-quality pristine SWCNTs, and the density of the network can be controlled in a wide range by varying the deposition time. FETs prepared from as-deposited CNTNs showed good and reproducible performance. The electrical characteristics of the fabricated bottom-gate devices on silicon and top-gate devices on polymer (kapton) are presented and discussed. The bottom-gate devices exhibited hysteresis that is typical for CNT-based FETs when sweeping the gate voltage back and forth. In addition, we have investigated the suppression of the hysteresis by means of thermal treatment in vacuum and subsequent atomic layer deposition of an Al2O3 coating.
positively charged SWCNT bundles towards the substrate surface (or positive potential to attract negatively charged SWCNT bundles). Without the application of an electric field, CNTs in a gas flow tend to go around the substrate, leaving very few nanotubes that have landed on the surface due to diffusion, while the application of an electric field significantly improves the collection, as seen in figure 2. The CNTN density can be controllably adjusted by varying the electric field strength and collection time (see figure 3(b)). In order to obtain low-density CNTNs close to the percolation threshold (≈1–5 CNT bundles μm−2), the collection time was varied between 30 and 120 s when an electric field of ≈300 kV m−1 was applied to ensure the most efficient deposition, as can be seen from figure 3(a). The density of the CNTN was estimated by means of a condensation particle counter (CPC, TSI Model 3775) connected to the ESP. On the basis of the aerosol measurements of the CNT bundle concentration in the ESP before and after application of an electric field, the CNTN density was estimated according to the following formula:

\[ \rho_{\text{calc}} = \frac{t \cdot \Delta C \cdot Q}{S} \]

where \( t \) is the collection time; \( \Delta C \) is the CNT concentration change in the ESP taking into account the ratio between the positively and negatively charged SWCNT bundles at certain synthesis temperatures as shown in [20]; \( Q \) is the particle flow rate; and \( S \) is the substrate area. The estimated average CNTN density was in a good agreement with the direct CNT density measurements using a scanning electron microscope (SEM, Leo Gemini 982). Therefore, this method allows control of the CNTN density during the collection process by simply adjusting the collection time.

The fact that the D-band (typically associated with disordered carbon) is almost absent in the Raman spectra, measured for various samples with CNTs grown in the temperature range between 800 and 1000 °C, shows the high quality of the material with respect to amorphous carbon. Figure 4(a) shows characteristic Raman spectra measured with 633 and 488 nm laser excitations from CNTs synthesized at a reactor temperature of 800 °C and deposited directly from the aerosol synthesis reactor at room temperature. Hereinafter, only the results obtained with SWCNTs synthesized at 800°C will be used if not specified otherwise. The presence of the strong G-band and radial breathing mode (RBM), characteristic for a SWCNT, in the Raman spectra shows the SWCNT formation, which was confirmed by the transmission electron microscope (TEM, Philips CM200 FEG).
observations. From the frequency of the RBM it was calculated that the diameters of SWCNTs, that are in resonance with the lasers used, lay in the range 0.9–1.7 nm for the 633 nm laser (that excites metallic nanotubes in that diameter range) and 0.8–1.2 nm for the 488 nm laser (that excites semiconducting nanotubes). Individual SWCNTs with an average length of 1.2 μm (800 °C) and 300 nm (1000 °C) entangle with each other in the cooling zone of the reactor, forming bundles of CNTs with a few tubes in a bundle (from 2 to 7 SWCNTs in a bundle), as seen from the TEM image in figure 4(b). A typical SEM image of a network of CNTs synthesized at 800 °C and deposited at room temperature on a Si/SiO₂ substrate is displayed in figure 4(c). SWCNTs synthesized by a HWG method with an average length of an individual CNT ~1 μm and average diameter of ~1 nm were used for the fabrication of transistors on a polymer substrate [22]. Both bottom-gate and top-gate FET structures have been fabricated to measure the performance of as-deposited CNTNs.

2.2. Bottom-gate transistors on silicon

Bottom-gate transistors were fabricated by depositing CNTNs on a highly boron-doped Si substrate (resistivity 0.01–0.05 Ω cm) coated with a thermally grown SiO₂ (100 nm), acting as a gate dielectric. A 200 nm layer of Al was sputtered on the back-side to provide a better contact for the back-gate electrode. For the precise alignment of the subsequent lithography steps for the channel and source–drain formation, thin Al alignment marks were prepared on the front-side of the substrate. Prior to the CNTN deposition a photolithography step was performed to define the transistor channel areas. This allows an accurate post-growth patterning of CNTNs by lift-off after the CNTN deposition, since the adhesion between the dry-deposited carbon nanotubes and the silicon dioxide surface was found to be sufficient so that lift-off in acetone could be successfully applied. Thus no etching processes for CNT removal were needed to electrically separate individual devices from each other.

Source and drain electrodes (20 nm Ti/100 nm Au) contacting the CNTN transistor channels were deposited using an electron-beam evaporator (IM9912) by standard photolithography and lift-off techniques. The geometry of the fabricated devices was varied with the source–drain channel length L (2–50 μm) and channel width W (10–200 μm). Schematics of a typical CNTN FET with a CNTN along the transistor channel can be seen in figure 5(a). As an additional step, an aluminum oxide (Al₂O₃) passivation layer was deposited on top of the device by the atomic layer deposition (ALD) technique. This step is described in more detail in section 2.4.

2.3. Top-gate transistors on a polymer

Kapton 200 HN, as a widely used flexible and mechanically strong polymer, was chosen as a substrate material for the top-gate FET structure. The thickness of the polymer sheet

Figure 4. (a) Raman spectra of SWCNTs using 633 nm (red) and 488 nm (blue) laser excitations. (b) TEM image of a typical SWCNT bundle. (c) SEM image of a CNTN on a Si/SiO₂ substrate with an average density of ~5–6 CNT bundles μm⁻² deposited at room temperature using the ESP.

Figure 5. Schematics of typical (a) bottom-gate and (b) top-gate CNTN FET structures with source and drain electrodes patterned on top of the CNTN channel area.
was 50.8 μm. CNTNs were deposited onto the polymer substrate and the source and drain electrodes (20 nm Ti/50 nm Au, deposited by an electron-beam evaporator) were patterned by standard photolithography and lift-off. For the gate dielectric, 100 nm of Al₂O₃ was deposited by ALD on top of the structures. This step also provided an effective device passivation. Finally, the top-gate electrode (50 nm Al, deposited by an electron-beam evaporator) was defined by another step of photolithography and lift-off. The schematics of this device structure are shown in figure 5(b).

### 2.4. Atomic layer deposition (ALD) of alumina (Al₂O₃)

In this work, Al₂O₃ layers were grown in a Beneq TFS-500 reactor using trimethyl aluminum (TMA) and deionized water as precursors for aluminum and for oxidation, respectively. The deposition was conducted at 190–200 °C with a deposition rate of 1.1 Å per cycle, and the pressure in the reactor was kept at about 5 mbar. The ALD process temperature in this range was chosen in order to perform thermal treatment of the devices so as to remove the possible water residuals, which might be present on the device surface after lift-off and subsequent rinsing processing steps. Nitrogen was used both as a carrier and purging gas. The ALD growth process is described in more detail elsewhere [25].

An important parameter for the ALD growth is the layer thickness. Initially, it was calculated from the known growth per cycle value for the ALD of Al₂O₃. The thickness of the grown layer was also confirmed by ellipsometer measurements (PLASMOS SD 2300). To get more information about the thickness and conformality of the ALD Al₂O₃ coating of CNTs, TEM studies were performed.

### 3. Experimental results and discussion

An HP 4155A semiconductor parameter analyzer was used for the electrical measurements of the devices at ambient conditions. Figure 6(a) shows that a typical bottom-gate FET with a lower CNTN density (∼1–5 CNT bundles μm⁻²) exhibits a p-type unipolar behavior at room temperature when sweeping the gate voltage from −10 to 10 V, with the ON/OFF ratio of up to 10⁵ and effective device mobility of ∼4 cm² V⁻¹ s⁻¹. This linear-regime mobility was evaluated by a commonly used formula:

\[
\mu_{\text{eff}} = \frac{dI_{\text{sd}}}{dV_{\text{g}}} \frac{t_{\text{ox}} L}{\varepsilon V_{\text{sd}} W},
\]

where \(dI_{\text{sd}}/dV_{\text{g}}\) is the transconductance; \(t_{\text{ox}}\) and \(\varepsilon\) are the thickness and the dielectric constant of the gate dielectric, respectively; \(L\) and \(W\) are the channel length and width, respectively; and \(V_{\text{sd}}\) is the source–drain voltage. This calculated value of the average mobility of a CNTN is somewhat underestimated since the gate capacitance is calculated as a full parallel plate gate capacitance, as discussed in [26]. Figure 6(b) demonstrates the scaling behavior of the ON and OFF currents, \(I_{\text{on}}\) and \(I_{\text{off}}\), of a random CNTN with a low coverage (∼2–3 CNT bundles μm⁻²), showing a rapid increase of the ON/OFF ratio with increasing channel length in the range between ∼3 and 10⁵, in agreement with the stick-percolation model of completely random networks when the probability of CNTs to form new percolating paths between the source and drain electrodes is increased with the decreasing channel length (effectively increasing the channel width), thus increasing the current, as discussed in [27].

Large hysteresis was observed in the transfer characteristics of our bottom-gate CNTN FETs in air when sweeping the gate voltage from the negative direction to positive and back, as seen from figure 7(a). This phenomenon has been attributed to various charge-trapping mechanisms, such as adsorbed water molecules or oxygen from air on or near SWCNTs. Contaminations like photoresist residues adsorbed on the CNT surface during the device fabrication process might also affect the electrical performance of CNT FETs [28–30]. The hysteresis is one of the major obstacles in the practical development of CNTN transistors.

Surface passivation of CNT FETs can be performed in order to protect and isolate the devices from the surrounding environment. A silicon nitride (SiNₓ) film or polymethylmethacrylate (PMMA) polymer have been widely used for CNT device passivation and hysteresis suppression.
Figure 7. Characteristics of a typical p-type CNTN FET before coating (a) and after coating by ALD with Al₂O₃ layers of various thicknesses: 5 nm (b), 10 nm (c), and 32 nm (d). \( L = 50 \mu m \) and \( W = 100 \mu m \). \( V_g \) was kept 0.1 V while the \( V_d \) was swept from -10 to 10 V and back, as shown by the arrows. (e) Hysteresis width change, quantified with respect to the threshold voltage shift at half of \( I_{sd} \), with various thicknesses of the ALD Al₂O₃ passivation layer.

It was, however, reported that SiNₓ film deposition by electron cyclotron resonance (ECR) sputtering or thermal chemical vapor deposition (CVD) induces surface damages in the CNT channel leading to current degradation [31], while the PMMA protection of a CNT channel from the ambient atmosphere’s humidity is not sufficiently effective [32]. ALD has been shown to be an attractive technique for non-destructive passivation of SWCNTs with a possibility to grow thin films at low processing temperatures [33, 34]. Recently it has been demonstrated that the utilization of an ALD Al₂O₃ film as a gate dielectric and passivation layer for top-gate SWCNT transistors leads to the reduction of interface trap densities around CNTs according to the small noise spectrum of the passivated devices [35]. We have studied the suppression of hysteresis in the transfer characteristics of our CNTN FETs depending on the thickness of the ALD Al₂O₃ layer by means of electrical characterization of the passivated devices after each subsequent increase in the Al₂O₃ film thickness. Also, TEM observations of the ALD-coated SWCNT bundles were carried out.
TEM images of SWCNT bundles, synthesized at 1000 °C and coated with various ALD Al2O3 thicknesses, can be seen in figure 8. From these TEM studies it can be seen that amorphous Al2O3 material conformally coats the SWCNT bundles with controlled uniform thickness along the full bundle length, in agreement with the previous reports on the ALD Al2O3 coating of individual multi-walled CNTs [36, 37]. The following Al2O3 thicknesses have been deposited: 2, 5, 10, 20 and 32 nm. The ALD layer thickness, measured with an ellipsometer and calculated from the ALD growth per cycle value, agrees very well with the thickness measured from the TEM images. This shows that the ALD growth on CNT bundles starts from the initial cycles, without any delay (known as an incubation period) which is characteristic for hydrogen-terminated silicon surfaces [38]. ALD Al2O3 was deposited using TMA and H2O precursors, as described in section 2.4. The bonding mechanism of ALD Al2O3 on SWCNT bundles can be explained by taking into account that TMA is known to react with such functional groups as alcohols, carbonyl, and carboxyl groups which, according to the measured Fourier transform infrared (FT-IR) spectra of pristine CNT films (not shown here), are present in small amounts on the surface of our samples.

The effect of the Al2O3 coating on the electrical characteristics of CNTN FETs was studied by measuring the electrical performance of CNTN FETs at room temperature in air after each subsequent increase of the ALD Al2O3 thickness. The $I_{sd}$–$V_g$ characteristics of the bottom-gate CNTN FET with the channel length 50 μm and channel width 100 μm coated with 5, 10, and 32 nm ALD Al2O3 layers can be seen in figures 7(b)–(d). We can state that the Al2O3 coating monotonically suppresses the hysteresis after each step of the Al2O3 thickness increase starting with 2 nm, and leads to its disappearance at the layer thickness of ~32 nm. Here, the hysteresis was quantified with respect to the threshold voltage shift at half of $I_{sd}$ (see figure 7(a)). Figure 7(e) shows the hysteresis width as a function of ALD Al2O3 thickness for a typical CNTN FET. We believe that water molecules absorbed on the substrate surface near the CNT or on the nanotube itself in air, acting as a major source of charge traps [28], have desorbed during the growth of the ALD Al2O3 at 200°C in vacuum, reducing the interface trap density. Thus the Al2O3 serves as a passivation layer, preventing the adsorption of contaminant molecules from the surrounding atmosphere. Oxygen/moisture and other impurities also play a role of doping molecules of the uncapped devices in air. Their charge transfer effect is reduced upon the ALD passivation, which results in a reduction of the maximum current value over the measured $V_g$ sweep [29, 39]. This conjecture was confirmed by performing electrical measurements of the bottom-gate CNTN FETs in vacuum (~10⁻⁹ bar), in which the same level of $I_{on}$ reduction was observed (figure 9). The fact that the on-state current reduction occurs in the case of ALD passivation similarly as in vacuum shows again that the ALD process is benign to CNTs, and so does not destroy their electrical properties [40]. In comparison, the degradation of electrical properties of polymer transistors upon the ALD-deposited Al2O3 encapsulation layer constitutes a considerable problem due to the fact that AlOx can be included in the polymeric semiconductor layer during the ALD precursor nucleation process, as discussed in [39]. Note that the hysteresis was somewhat reduced in the bottom-gate CNTN FETs in vacuum but was not fully eliminated even after 7 days of keeping in vacuum. This result agrees with [28], where it was shown that
pumping in vacuum removes only the water molecules weakly adsorbed to the CNT surface and heating at $\geq 200\, ^{\circ}\mathrm{C}$ is needed in order to remove the hydrogen-bonded water remains from the surface of SiO$_2$ that cause the residual hysteresis.

Finally, our top-gate transistors fabricated on a polymer substrate (kapton) using dry-processed CNTNs showed characteristic p-type transistor behavior with an ON/OFF ratio of up to $10^5$ and the mobility reaching $\sim 1\, \text{cm}^2\, \text{V}^{-1}\, \text{s}^{-1}$, as can be estimated from figure 10. Though this performance is superior to that of most organic TFTs, our current work is targeted towards the improvement of the effective device mobilities of our top-gate TFTs by means of optimizing the device structure. In general, this study represents a new step forward towards the development of SWCNT network-based flexible electronics.

4. Conclusions

A novel fabrication technique for CNT TFTs based on dry-processed pristine SWCNTs efficiently deposited at room temperature directly downstream of the aerosol synthesis reactor is presented. This technique offers a simple way of CNTN deposition with controllable CNT density and allows the utilization of low-cost, flexible, and heat-sensitive substrate materials as well as conventional silicon substrates. Bottom-gate (on silicon) and top-gate (on polymer) transistors were fabricated. The CNTN FETs exhibited high performance, with an ON/OFF ratio of up to $10^5$ on both silicon and polymer substrates. Passivation by an ALD Al$_2$O$_3$ layer was used to suppress the hysteresis in the transfer characteristics of as-fabricated CNTFETs. It was shown that the ALD Al$_2$O$_3$ layer conformally and uniformly coats SWCNT bundles, and that an Al$_2$O$_3$ thickness of 32 nm was enough for the elimination of the hysteresis.

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References