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STUDY OF STATIC TRANSFER SWITCHES  

This thesis has been submitted for official examination for the degree of Master of Science in Electrical and Communications Engineering in Espoo Finland on February 26th, 2008  

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ABSTRACT of the Master’s Thesis

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Quality and reliability of electrical power have become a must for many industries and applications. Airports, hospitals, data centers and financial institutions are just a few of the locations where an unexpected loss of power could bring fatal consequences ranging from massive economic losses to life casualties. The risk of not having such power calls for electrical equipment capable of assuring the quality and reliability of the power source under the hardest conditions and in the most unpredictable events. One of those equipments is a power electronics-based switch called Static Transfer Switch (STS).

This document analyzes the technical design of such a switch focusing on the power electronics of the device. For this purpose, a thorough study of semiconductors is carried out. Additionally, the report addresses the STS applications and market niches. The breakdown of the report is as follows: Chapter 2 reviews the background, applications and market niches of the STS. Chapter 3 is a theoretical study on the semiconductors that are applicable for the STS, and Chapter 4 presents an in-depth analysis of the STS design, stressing its limitations and giving guidelines of how to design it in the case that is required as a further project.

The main conclusion of this work is that the most cost-efficient design of an STS should be based on Silicon Controlled Rectifiers (SCRs). Even when other power semiconductors like Gate Turn Off Thyristors (GTOs) and Integrating Gate Commutated Thyristors (IGCTs) can provide a solution for high power requirements, and better in terms of commutation times, the limitations that they impose in other areas like thermal management, availability and cost make them commercially unsellable at the moment. Maybe with the advent of new semiconductor materials and the consequent improvement of semiconductor devices in a near future this landscape could change, but at the moment the SCR still stands out as the ultimate solution for the STS.

Keywords: STS, Critical Power, Thyristor, SCR, GTO, IGCT
PREFACE

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LIST OF ABBREVIATIONS

ABB  Asea Brown Boveri
AC    Alternating current
AGTO  Asymmetrical Gate Turn Off Thyristor
ANSI  American National Standards Institute
BBM   Break Before Make
BJT   Bipolar Junction Transistor
C     Capacitance
CBEMA Computer Business Equipment Manufacturers Association
CF    Correction Factors
$C_j$ Junction Capacitance
$C_s$ Snubber capacitance
CSI   Current Source Inverters
DC    Direct current
$di/dt$ rate of current change
$dq/dt$ Direct and quadrature axes
$dv/dt$ rate of voltage change
DUPS  Dynamic Uninterruptible Power Supplies
DVR   Dynamic Voltage Restorer
EMI   Electromagnetic Interference
GCT   Gate Commutated Thyristor
GTO   Gate Turn Off Thyristor
GU    Gate Unit
$I_{AK}$ Anode current
$I_D$  Off-state current
IEC   International Electrotechnical Commission
IEEE  Institute of Electrical and Electronic Engineers
$I_f$  Forward current
IGBT  Insulated Gate Bipolar Transistor
IGCT  Integrated Gate Commutated Thyristor
I_{GT}  
Gate current at trigger

I_{H}  
Holding current

I_{L}  
Latching current

ISO  
International Standarization Organization

i_{rr}  
reverse current

I_{RRM}  
Maximum reverse reverse current

I_{RSM}  
Reverse leakage current

I_{SH}  
Short circuit current

I_{T}  
Current thyristor

I_{TAVM}  
Maximum average on-state current

ITIC  
Information Technology Industry Council

I_{TQRM}  
Maximum turn-off current

I_{TRMS}  
Maximum RMS on-state current

J_{1}  
Junction 1

J_{2}  
Junction 2

J_{3}  
Junction 3

L_{C}  
Commutating inductance

L_{s}  
Stray inductance

MATLAB®  
MATrix LABoratory

MBB  
Make Before Brake

MCCB  
Molded Case Circuit Breaker

MOSFET  
Metal Oxide Semiconductor Field Effect Transistor

NC  
Normally Close

NO  
Normally Open

NEC  
National Electric Code

PDU  
Power Distribution Unit

Pu  
Per Unit

Q_{RR}  
Reverse recovery charge

RMS  
Root Mean Square

R_{on}  
On-state resistance

R_{S}  
Snubber resistance
$R_{JC}$ Junction to-case-thermal resistance

$R_{JC}$ Case-to-sink-thermal resistance

$R_{SA}$ Sink-ambient thermal resistance

SCR Silicon Controlled Rectifier

SGTO Symmetrical Gate Turn Off Thyristor

STS Static Transfer Switch

UL Underwrites Laboratories

T Thyristor

td delay time

tf fall time

$t_{gg}$ GTO turn-off period

$T_{on}$ turn-on period

$T_{r}$ rise time

$tr_{rr}$ reverse recovery time

$T_{jmax}$ Maximum temperature section

TVSS Transient Voltage Suppression Systems

tw Pulse width

$t_{wg}$ GTO gate reverse bias time

UL Underwrite Laboratories

UPS Uninterruptible Power Supply

$V_{AK}$ Voltage anode to cathode

$V_{BO}$ Forward breakdown voltage

$V_{C}$ Commutating voltage

$V_{DRM}$ Peak repetitive off-state forward voltage

$V_{DSP}$ Over voltage spike

$V_{DRM}$ Maximum Forward Voltage

$V_{on}$ Voltage on-state drop

$V_{RRM}$ Peak repetitive off-state voltage

$V_{R}$ Reverse Voltage

$V_{RSM}$ Non-repetitive peak reverse voltage

VSI Voltage Source Inverter
Chapter 1

Introduction

1.1 Introduction

Critical power is a concept that has come to the light as a consequence of technology development throughout the years. Quality and reliability of power supply for electrical devices have become a must for many industries and applications. Airports, hospitals and health care facilities, financial institutions and data centers demand 100% of clean and reliable power 24 hours per day during 365 days per year. One instant of failure could bring fatal consequences ranging from huge amounts of money losses to life casualties.

During the last decades, different equipments and configurations have been used in order to cope with this problem. Generator Sets, Uninterruptible Power Supplies (UPS), transfer switches, etc. All of them have been evolving in parallel with power electronics to the point where it is almost possible to achieve 100% reliability of power supply to the critical load even in the hardest conditions.

Critical power applications and energy demand will increase worldwide in the following decades. Moreover, power generation capacity won’t be able to grow at the same pace. Therefore, the critical power looms as a very interesting segment within the electrical switchgear business. The potential development of a low voltage Static Transfer Switch (STS) could give electromechanical switchgears companies the possibility of exploring new market segments and expand its customer base considering than there is already one for its electromechanical transfer switches.

1.2 Research objective

The aim of this work is to find out the most convenient design for a STS from the technical point of view. There are different issues to analyze in such a design; power semiconductors like Silicon Controlled Rectifiers (SCRs), Gate Turn Off Thyristors
(GTOs) and Integrated Gate Commutated Thyristors (IGCTs), transfer times, fault detection and control algorithms, power losses and heat dissipation, simulation and computer aid solutions, and standards.

For that purpose the STS has been divided into its three main blocks: (1) static switches, (2) control scheme and (3) bus bar assembly. Stress is given on the first block, addressing several configurations and comparing them from a static switch perspective. The other two blocks are analyzed just from one scope regardless of the semiconductor configuration. The study also gives an overview of STS applications, manufacturers and potential markets in order to provide the reader with a “wide picture” that goes beyond the technical features of these devices.

It is also an important goal of this thesis to provide the basic knowledge on semiconductors for the future development of static or hybrid switches. For that, Chapter 2 provides a thorough study addressing the semiconductor theory while Chapter 3 focuses on more practical matters concerning the specific application.

Finally, examples on how to protect, control, and specify semiconductors for STS applications are given if a prototype is sought to be built as a further project following this document.

1.3 Scope of research

The project scope includes the following:

- Applications, markets and manufacturers of STSs
- Study of thyristors: basic theory, comparison, state of the art and trends
- Technical study of commercially available STS
- Control requirements for thyristors within STS applications
- Protection of semiconductors within STS applications
- Thermal constraints on thyristors and their available solutions
1.4 Standards

The STS is an automatic transfer switch and for that reason it has to comply with its standards. For Europe, the automatic transfer switch standard is IEC 60947-6-1 while for North America is UL1008.

Additionally, there are other standards applicable to electrical devices that also must be complied. Here are some of those:

- IEC 62310, Static transfer systems
- EN 50091-2, Uninterruptible power systems (UPS). EMC requirements
- EN 61000-6, Electromagnetic Compatibility
- ANSI/NFPA70, National Electrical Code (NEC)
- IEEE/ANSI C62.41, IEEE Guide on Surge Voltages in AC Power Circuits Rated up to 600V
Chapter 2
Transfer Switches and Power reliability

2.1 Power Availability and Reliability

The quality of electric power and the assurance that it will always be available are extremely important in a society that is relying more and more on electricity. Critical mission applications are increasing and many businesses are becoming every day more heavily dependent on their information systems and processes.

The modus operandi of a power system is extremely complicated and even if there are investments and technology development ongoing on the issue, it is impossible for a utility to provide an end-user with 100% of clean and reliable power. From the improbable falling of a tree over an overhead line to a thunder strike, electric grids are susceptible to many unexpected events. The blackout stands out as the worst of all of them, taking businesses and industries to extreme situations due to the complete loss of electric power.

Power protection has become a must in most businesses and industries around the globe. Equipments like UPSs, Transient Voltage Surge Suppression systems (TVSS) and Power Distribution Units (PDU) are widely known and used along with generator sets in order to achieve high reliability of power.

Protection and availability in an electrical installation can be classified in four levels [1]: (1) Basic protection, (2) Operational support, (3) High availability and (4) Continuous availability. Basic protection prevents damage to sensitive electronics by means of a TVSS and a PDU but provides not protection against interruption of incoming power. It delivers 99.9 percent reliability depending upon the utility power source.

Operational support adds a UPS to the basic protection configuration. This protects the systems against short power outages and also provides the system with the ability of a
controlled shutdown if the outage exceeds the UPS battery capacity. A 99.99 percent of reliability is expected.

High availability (99.999 to 99.99999 percent of reliability) allows a downtime of equipment between five minutes and three seconds per year [1]. When compared to the operational support configuration it adds redundancy at the UPS level (connecting them in parallel to a common distribution network) by either 1+1 or N+1 configuration. Nevertheless, this is not enough in some cases, especially when the cost of downtime is very expensive.

Continuous availability provides the highest protection level. It consists of two independent UPS running in synchronism and connected to two independent input power sources. The two UPS are capable of carrying the entire load. The STS is used between the UPSs and the load for a seamlessly transfer of power when needed.

2.2 Vulnerability of Power Grids

The power grid is an immense electrical network connecting substations, overhead lines and generation plants across huge areas, which in many cases can be as big as entire countries or even continents. It allows the flow of electricity through thousands of kilometers from generation stations to end-users, providing the energy for most of the human and industrial processes.

They work under the premise that the power flow should be balanced, i.e. the amount of power generated shall equal the amount of power consumed. Furthermore, the grid needs to be synchronized at the same frequency, meaning that all the generating machines should be rotating at the same speed. If these two conditions fail to be achieved then power disturbances (voltage sag, swells, frequency deviation, etc.) appears imposing risks on the systems’ operation.
Electric grids are not a new technology; most of them have been developed many decades ago and still rely on old equipment and outdated technology [10]. On the other hand increase on the energy demand worldwide has led to their massive growth in size and complexity—having thousands of electrical devices interconnected between each other—and also have also pushed their capabilities to their physical limits bringing the vulnerability issue to the forefront.

The operation of an electric grid is a very cumbersome process that relies in knotty computer and communications systems. The operation of these systems is not error-free and is subjected to external factors like human mistakes, natural disasters and even terrorist attacks. What would happen if somebody hacks the control center of a transmission utility and starts disconnecting lines at will? Consequences could be of catastrophic dimensions.

The blackout of 2003 in North America affected 50 million people and brought losses of around 6 billion USD while the one in Italy during the same year affected 54 million people [5,6,8]. Both were declared to be initiated by natural events like overgrown trees and thunderstorms respectively and followed by systems and operators mistakes [7]. They left entire cities for many hours without energy for even the most basic services bringing chaos in airports, train stations and banks among other places with critical loads.

Such events highlighted the importance of the reliability of electric power and its adequate protection. One of the main conclusions of these events was that electric grids need monumental investments in order to improve the reliability of the power grid [9]. Obviously, this is difficult and if done will take several years due to the nature and amount of players in the utility business. Until then, private sectors need to protect themselves from those occurrences by all possible means.

Power disturbances of such extent showed that even protected systems are vulnerable and that in many cases redundancy of redundancy is required. For example, during the transients before the 2003 North American blackout, frequency and voltage fluctuations
were extremely high leading to UPSs failures and thus leaving protected installations without electric power. The ones which had redundancy at the UPS level where able to ride-through the event.

2.3 Transfer switches

Transfer switches or load transfer equipments are devices which are intended to remove electrical loads from a primary source of supply and to connect it to an alternate one with the aim of providing reliability to the electrical installation. They are mainly used with generator sets in applications where the loads need, if not a fully continuous, at least a steady supply of electric power.

The transfer switch allows switching from utility power to backup power or vice versa in different anomalies/situations set by the end-user. Anomalies like voltage sags, surges or power outages will most likely cause some malfunctions on the critical load; therefore the switch should perform the transfer under these situations.

The switching process can be either done manually, automatically or a combination of both. Contactors, load break switches, circuit breakers and solid state devices can provide the solution for the transfer switch depending on the technology chosen by the manufacturer and/or end-user. Electromechanical switches can be operated manually or automatically with the aid of an electric motor. Static transfer switches are electronically controlled switches based on power semiconductor devices which allow the automatic triggering for the transfer procedure.

2.4 STSs

A STS is an automatic device without moving parts for transferring one or more loads from one power source to the other. The switching is made by means of power semiconductor devices which make or break the current according to their conductivity properties; therefore there is no mechanical wear or tear and no contact bouncing on the
transfer process. An intelligent unit within the switch carries out the metering and control processes for transferring loads under abnormal conditions. In addition, several circuit breakers or mechanical switches can also be used for the bus bar assembly. Figure 2.1 shows the basic configuration of a thyristor-based STS.

![Diagram of thyristor-based STS](image)

Figure 2.1: Basic configuration of a thyristor-based STS [33]

STSSs can be divided in two groups: low voltage static STSSs and medium voltage STSS. The former is usually rated up to 1000 V while the latter goes up to 35 kV. However, it depends on the manufacturer when it comes to define the boundaries on the voltage and current range. The main difference between these two is the application in which they are used. While low voltage switches are often used in data centers, hospital or airports; medium voltage switches are useful for larger industrial installations (semiconductors, automotive, pharmaceutical). This document focuses on the low voltage group.
The main purpose of a STS is to allow virtually uninterrupted transfer of the critical load from primary to back-up power supply. The word “virtually” means in this case that there is a transition time which depends upon thyristor gating scheme, load type parameters and characteristics, fault disturbances and voltage detection logic. This time is so small (around ¼ of cycle or 5 ms) that it is invisible for the load. It is important to mention that the total transfer time is given by the detection time of the anomaly plus the transfer time itself. These concepts are further explained in Chapter 4.

The STS is constantly monitoring the quality of the power supplies (preferred and back-up) and the status of its power electronics switches. Power supplies are monitored for failure detection while semiconductor devices to check if they are ready for transfer. Once a failure is detected the control circuit will send the gate signals to the power semiconductor device for the respective commutation. It is worth to address that source paralleling should be avoided as it affects the overall transfer time. Delays for the commutation process are available as it is usual that common failures like voltage sags may appear and disappear within 1 ms, which doesn’t harm the load at all.

Another important feature of the STS is its ability to detect load current faults [2]. In that case the transfer switch must be able to block the transfer process; otherwise both sources could experience failure. This is usually accomplished by a protective device which sends a transfer inhibiting signal when a downstream fault is detected.

The STS works under the premise that both independent sources are synchronized. A transfer process under unsynchronized sources could produce undesired overvoltages and overcurrents that may damage the load. Moreover, the semiconductor devices must be rated according to desired load voltage and currents. Short circuit currents should be also taken into account in order to prevent device’s failure. Additionally, heat dissipation is an issue which should be carefully analyzed considering that solid state devices have high on-state losses.
STS applications

STSs have gained popularity and market segments during last years due to improvement of power semiconductors technical ratings and control means. They are used synergistically with UPS although sometimes they also compete against each other for some applications. STS are used inside UPSs, as an internal component of the final product. They are also used outside UPSs as separate units in different configurations for backing up critical loads and with two power supplies running in parallel and synchronized. For medium voltage applications STSs act as a replacement for electromechanical switches considering that their transfer time is considerably faster for commutation between feeders. The following paragraphs address in detail the special applications in which STSs are used.

The static switch is used within a UPS in order to maintain electric supply to the critical load during fault or overload conditions. Its main task is to provide a very fast, break-free transfer between the inverter output and the bypass. The load can be either fed from the UPS inverter output or from the mains (by means of a static bypass).

![Diagram of UPS online configuration](image)

**Figure 2.2: UPS online configuration [3]**

A UPS with a typical online configuration is showed in Figure 2.2. In this scheme the inverter provides clean and reliable power to the critical load through the static switch
during normal operation (red arrows). The static switch is continuously monitoring the state of the UPS main and bypass supply. It is an “intelligent” device, which can decide when to start the transfer process based on its control inputs (supplies and the UPS inverter output). For example, if there is an internal failure inside the rectifier/charger of the UPS, the static switch commutates to the bypass line in such a short time that the critical load doesn’t see this change (gray arrows). Once the fault is cleared on the mains supply path, the static switch starts the transfer process back to the inverter operation.

![Diagram](image)

Figure 2.3: UPS offline configuration with standby generator [48]

Figure 2.3 refers to another UPS configuration. Here the system works in offline mode, i.e. the normal power flow to the load goes through the bypass branch. This type of configuration is more efficient since it doesn’t have the continuous losses of the rectifier and inverter of the online UPS. However, it fails to provide clean and continuous power to the load during normal operation.

In the event of a fault on the utility side, the STS immediately changes the load to the inverter output of the UPS. If the fault is cleared within a reasonable time, the static switch transfers back the load to the utility supply. In case that the fault lasts longer than certain limit, the generator starts up and the transfer switch starts the transfer process once the genset has stabilized. Afterwards, the static switch waits until both inverter...
output and genset are synchronized and then transfers seamlessly the load to the genset. It is worth to mention that sometimes these types of configurations are sold as a whole solution and not just as a single UPS [48].

A third configuration is shown in Figure 2.4. Here the static switch is used with two UPS running in parallel and synchronized. It could also be any source as long as both are synchronized (e.g. transformers or two feeders from the same utility). According to customer’s choice, the critical loads can be isolated or shared between the two sources. This kind of configuration is usual in extremely critical applications where there is always a need of processed power feeding the load.

![Figure 2.4: STS with synchronized UPSs [49]](image)

A similar configuration can also be used for bigger loads; for example at the substation or service entrance of large industrial plants. This configuration is sometimes required when critical processes cannot be separated; hence, the whole plant needs to be backed up in case of a fault. For these applications, it is usual that the sources come from the utility and not from UPSs. These switches are usually manufactured for voltages above 1000 V.

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There are several types of static transfer switches and their features vary according to manufacturers, especially when it comes to its control logic. Several parameters can be controlled and even synchronization logic can also be included within the unit. In some cases the control logic is within the static transfer switch module while in others, all the control is carried out by the internal UPS processor. Chapter 4 explains in detail the semiconductor operation of the static switch.

STS markets and opportunities

Low voltage static transfer switches market has been increasing during the last years. This growth is expected to continue mainly because of the boost of data centers and other mission critical applications in military, government and healthcare facilities. Figure 2.5 shows an overview of the market revenues along with a prognosis.

![Low Voltage Static Transfer Switch Market](image)

Figure 2.5: Low Voltage STS market revenues [11]

Data centers are expected to keep growing —mainly because of the installation of new Information Technology (IT) and telecom equipment— and with an ever-increasing appetite for electric power. They doubled their power consumption worldwide between
2000 and 2005 and are expected to increase to 40% up to 2011 according to a report for the U.S. congress [4]. This provides a considerable market niche for the STS.

Another major factor contributing to market growth is the awareness of end-users of the need to protect equipment and processes from catastrophic events like the blackout of 2003 in North America. Total losses were calculated in the range of 6 to 10 billion USD [5]. The US electric grid is a clear example of the strain to which electric grids are under at the moment as a consequence of an increase in the energy demand and an aging infrastructure of transmission systems. Transition economies countries—with buoyant industry hungry for reliable power—are facing similar problems with their electric systems; hence, providing an underlying potential of growth.

Static switches based solutions are not yet as widely known as other solutions like UPS and PDU for the critical power segment. Chances of increasing the market may be higher with proper customer education about the product and its benefits. Moreover, new applications may arise as for example the possibility of using it for peak shaving purposes without having to interrupt the process in an industrial plant.

The static switch market is dominated by manufactures like Liebert (part of the Emerson group), Cyberex and Socomec. Liebert and Cyberex dominate the scene in North America while Socomec does it in Europe and Asia [11]. There are other manufactures like MGE UPS (belongs to Schneider group) and Piller that are becoming very aggressive and most likely may come to the forefront in a near future. Markets in other parts of the world still remain a question mark.
Chapter 3
Power Semiconductor devices

3.1 Overview

Power semiconductors devices exploit the electronic properties of semiconductor materials as Silicon, Germanium and Silicon Carbide. The principal characteristic of these materials are the possibility of manipulating their electronic behavior by inserting into them impurities such as atoms of phosphorus or boron. These impurities increase the number of free electrons and holes in the material, which gives the device the possibility to conduct whenever a suitable energy is applied. The energy applied can be in the form of current, voltage or light.

The revolution of power semiconductor devices started in 1958 when General Electric Company started to commercialize the first thyristor, the Silicon Controlled Rectifier (SCR)\(^1\). This was the beginning of a new era in power electronics that until that time had been based in vacuum tubes, ignitrons and phanotrons [31]. During the second half of the 1970’s, two controllable non-latching type devices, the bipolar transistor module and the GTO, were developed and introduced on the market, starting a second era on the evolution of power semiconductor devices [15].

The introduction of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) led to the development of the so-called third stage of power semiconductors. This happened through the end of the 80’s and the beginning of the 90’s with the combination of the best features of the MOS (Metal Oxide Semiconductor) and bipolar devices, resulting in the revolutionary IGBT (Insulated Gate Bipolar Transistor). During the last years a new type of thyristor has been inserted to the market, the IGCT, representing the state of the art and probably opening a new era the filed. Figure 2.1 shows an up to date chart classifying the devices in three types.

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\(^1\) Some sources define SCRs and thyristors as synonyms. However, throughout this document, SCRs refers to a type of thyristor.
Figure 3.1: Power Semiconductor devices classification [31]

A power diode is a two terminal electrical component which vary its electrical properties according to the flow of electrical carriers through it. It allows the flow of current when it is positive biased (anode at higher potential than cathode) or block it when it is reverse biased. During the conduction of the diode, there is a forward voltage drop. Additionally, during the turn-off of the device, there is a negative current flowing through it during a certain period of time (recovery time). This is an undesirable effect that can be avoided or at least diminished by the use fast-recovery diodes

Power transistors’ realm comprises Bipolar Junction Transistors (BJTs), Power MOSFETS and IGBTs. A bipolar transistor is a three terminal device that can have either a NPN or PNP configuration. For high power applications it is usually used in the common-emitter configuration and within its saturation region. This means that an NPN transistor will behave almost as an ideal on-off switch as long as it has a higher potential in its base than in its emitter and that there is enough current flowing through the base-emitter junction. Once the base to emitter positive potential is withdrawn, the transistor will leave its saturated state and go to its non-conductive state. At the moment the BJT
has been largely superseded by the IGBT at higher power levels and the power MOSFET at lower power levels [21].

Power MOSFETs are unipolar, majority carrier and voltage-controlled devices. They are superior to bipolar devices (BJTs and IGBTs) in faster switching speeds, lower switching losses, and simpler gate drives [15]. However, in conduction losses MOSFET are not so attractive since they have higher on-state resistance. That is that while the transistor is conducting there are considerable losses in the form of heat. Moreover, there is the fact that the breakdown voltage of the device is directly proportional to the on-state resistance. With all these features is logic that the MOSFET is more suitable for high switching speeds and low power application, usually up to 1000V and 100A [31].

The IGBT is a three terminal component developed in the early 80’s. It combines the power handling capability of bipolar transistors and thyristors with the simple gate drive characteristics of the MOSFET. This means that it can be controlled with the simplicity of a MOSFET and it withstands the high power ratings of thyristors and BJTs. Large IGBT modules that contain many IGBTs connected in parallel can withstand ratings of 6.5 kV/4 kA, it is expected that their ratings will keep increasing.

Thyristors are the last group of power semiconductor devices. The basic model of the thyristor (SCR) have four layers of alternating N and P-type material and it acts like a switch conducting when its gate receives a current pulse, and continue to conduct for as long as it is forward biased. Once it has been triggered (conduction mode), the gate has no more control over the device. There are other types of thyristors (GTOs and IGCTs) which can be turned on and off at will by means of controlling the current on their gates. These types will be explained in the subsequent pages. SCRs have been the workhorses for utility-scale power electronics for more than 30 years; presently they are available with impressive power handling capabilities (12 kV/4 kA) and often represent a cost-efficient alternative for the highest power levels [15]. Figure 3.2 shows an overview of the applications per power rating of the power semiconductors.
3.2 PN junction

Semiconductor materials like silicon have the feature that if they are combined (doped) with different types of atoms they change their electrical properties. If silicon is doped with atoms that provides it with free electrons (usually group V elements of the periodic table such as phosphorus, arsenic or antimony), then the material has an excess of electrons and it is said to be of N-type. Conversely, if the material is doped with atoms that absorbs electrons (usually group III elements such as boron, gallium or Indium), then the material has a deficit of electrons (excess of holes) and is it said to be of P-type.

When P and N-type elements are put together in very close contact they form the PN junction. This combination provides the basis for the functioning of every power semiconductor device. A diode for example is a single PN junction, whereas more complicated devices, like transistors and thyristors use several combinations of these junctions. The excess holes in the P-type are attracted by some of the excess electrons of the N-type material near their boundary area; therefore, they diffuse to the N layer. The situation is the same for the excess electrons in the N-type, and thus they also diffuse to the P layer. As a consequence, a small layer is formed in the limit between the elements
with an electrical polarity. It is called the depletion layer. Figure 3.3 illustrates this phenomenon.

![PN junction diagram](image)

**Figure 3.3: PN junction**

The depletion layer imposes an electrical potential that opposes to the flow of electrons from the N-material to the P-material. If a voltage source is connected to the material then the thickness of the layer either increases or decreases according to the polarity of the source. Figure 3.4a depicts a voltage source with its positive polarity connected to the P element. As voltage increases the layer decreases, reaching a point where the layer is too thin to block the flow of electrons. When this point is reached, the device enters its conduction state.

![PN junction diagrams](image)

a) Forward-biased PN junction  
b) Negative-biased PN junction

**Figure 3.4: Polarized PN junction**

When a negative voltage is applied to the PN junction, then the situation is opposed as the one explained in the last paragraph. The depletion layer increases providing even further blocking. However, there is a limit dictated by the strength of the electric field
applied. If the voltage is too high then the electrons in the depletion layer start colliding against each other, releasing energy that destroys the layer and allowing the flow of electrons.

![Graph of PN junction recovery](image)

**Figure 3.5: Recovery process of the PN junction [45]**

Once a PN junction (or diode) is conducting and the forward current ($I_F$) is diminished to zero (either due to the natural behavior of the electrical circuit or application of reverse voltage), the diode continues to conduct due to the time that the excess carriers need to recombine and form the depletion layer again. Figure 3.5 shows this phenomenon. The negative current continues to increase until it reaches a peak, and then it decreases until reaching a steady state. The steady current is the leakage current $I_{rr}$, while the time needed for this process is the reverse recovery time $t_{rr}$. These two values are very important as they play a major role on the transient behavior of semiconductors.

### 3.3 Modeling of power semiconductor devices

As explained before, the main characteristic of semiconductor materials are to act as switching devices, i.e. to break or make the current in an electric circuit. In order to understand the modeling of these devices it is useful to provide a comparison between their ideal and real characteristics. An ideal switching device should be able to carry forward current $I_t$ tending to infinite, with a low on-state voltage drop $V_{on}$ and on-state resistance $R_{on}$ tending to zero. However, this is not the case with the devices under study. There is a limit for the forward current given by the current density of the material used.
(in this case silicon) and the thermal conductivity. Additionally \( R_{on} \) exists and it is proportional to the thickness of the depletion layer of the device.

During off state, semiconductors should withstand a forward voltage tending to infinite \( V_{DRM} \), a leakage current \( I_{RR} \) tending to zero and a high off-state resistance tending to infinite. In practice this doesn’t exist, \( V_{DRM} \) is limited by the narrow band gap of silicon. A way of overcoming this limitation is to increase the thickness of the active layer of the device; however, this increases \( R_{on} \) which leads to higher losses. Therefore, a trade-off should be made when designing the device.

The turn-on and turn-off processes should be instantaneous for high frequency and efficient operation. There are no instantaneous processes in real life and semiconductors are not the exception. A rise time \( t_r \) and a fall time \( t_f \) exists due to the inertia of the carriers and their duration varies according to the device. Other issues related to switching times are \( di/dt \) and \( dv/dt \) ratings. When turning on, the device needs a minimum amount of time before all its area starts conducting the full current. If the current rises too fast, it is probable that just one part of the area will conduct the full current with the subsequent damage of the device. When it comes to the voltage all semiconductors have an internal junction capacitance \( C_j \); hence, a rapid increase in the voltage could produce a very high current with negative consequences.

The ideal thermal impedance \( R_{JA} \), (between junction and ambient) should tend to zero for letting all the heat generated within the material to be transmitted to the ambient considering that it can be significant. However, in practical designs the thermal impedance is far from zero and it is composed by three internal impedances; Junction to-case-thermal resistance \( R_{JC} \), case-to-sink-thermal resistance \( R_{CS} \) and sink-ambient thermal resistance \( R_{SA} \). All of them should be taken in account for proper device designing and circuit modeling in order to avoid reaching temperature limits which affects the conductivity of the material.
3.4 SCRs

The SCR is a solid-state semiconductor device with four layers of alternating N and P-type material. It has three terminals: anode, cathode and gate. Figure 3.6 shows the SCR symbol and its configuration layer.

![SCR diagram]

Figure 3.6: Thyristor symbol and configuration layer

When the device is forward biased, i.e. positive voltage applied from anode to cathode ($V_{AK}>0$) then junctions $J_1$ and $J_3$ will be forward biased while junction $J_2$ will be reverse biased. In this state the SCR is said to be in the forward blocking condition and it has a very small leakage current (off-state current $I_{D}$) due to the $J_2$ juncture. If $V_{AK}$ is increased, it reaches a point in which the reverse biased juncture $J_2$ will break down and as the other two junctures $J_1$ and $J_3$ are forward biased, carriers will move across the three junctures resulting in a large anode current and taking the device to its conduction state. This voltage is called the forward breakdown voltage $V_{BO}$. When $V_{AK}$ is negative, the thyristor behaves like two reverse biased diodes connected in series, this leads to a leakage current $I_{RR}$.

A minimum current known as the latching current $I_L$ should flow when the device is taken to its conducting state in order to keep the amount of carriers flowing across the junction, otherwise the device reverts to its blocking state. Once the thyristor is conducting, it behaves like a diode since there is no depletion layer on $J_2$. It will not be
possible to turn the thyristor off, unless the forward current decreases to a value where it is not enough to keep the carriers free at J2. This value is called holding current $I_{H}$, is of the order of milliamps and definitely smaller than $I_{L}$. Another important feature is that during conduction there will be a voltage drop in the device, this is mainly because of the ohmic behavior of the layers and it is usually about 1 V between anode and cathode.

As stated before, the SCR can be turned on by increasing $V_{AK}$ but this could lead to the device destruction. Usually the $V_{BO}$ voltage is maintained below breakdown levels and a positive current pulse is applied between gate and cathode (normal triggering). This lowers the breakdown voltage of J2 and therefore the device enters its conducting condition with a lower $V_{AK}$. Figure 3.7 shows a graphic of the thyristor behavior.

![Figure 3.7: Electrical behavior of SCR](image)

Apart from applying a higher $V_{AK}$ than the $V_{BO}$ and inserting a current pulse between gate and cathode, there are two other different ways of turning the thyristor on. The first one is related to thermal issues. When $T_{j}$ reaches a certain limit, it can cause a thermal runaway in the device. The second one deals with the rate of rise of the anode to cathode voltage, if it is too high then high currents are produced due to $C_{j}$. These currents will trigger the SCR.
SCRs are regenerative devices and this can be explained from Figure 3.8. When they are modeled as two complementary bipolar transistors, one NPN and other PNP, it is clearly shown that there is a positive feedback on the system (i.e. part of the output of the system is inserted into the input). Positive feedback usually causes instability and tends to saturate amplifiers; however, in the case of an SCR it allows it to reach high anode currents $I_{AK}$ with very small gate currents $I_G$.

![Two transistor model of the thyristor](image)

**Figure 3.8 Two transistor model of the thyristor**

**Operating waveforms and parameters**

As stated in the last section, within normal operation the SCR needs a gate current pulse to turn on when $V_{AK}$ is positive. This pulse should be long enough to allow $I_{AK}$ to reach the holding current and latch. The gate current should be removed before the SCR starts conducting in order to avoid additional power losses in the gate cathode juncture. Moreover, the pulse should also comply with the fact that the minimum triggering current should be greater than the noise level of the circuit. Figure 3.9 shows the operating waveforms during turn-on.
The turn on period $t_{on}$ may be divided into two phases: the initial delay time $t_d$ and the $t_r$. $t_d$ is defined as the time interval between 10% of the gate current and 10% of SCR on-state current. It is inversely proportional to the gate current. $t_r$ is the time interval required for the principal current to rise from 10 to 90% of its maximum value. It is directly proportional to $V_{AK}$.

It is important to mention that even when it is possible to turn off the thyristor by means of reducing $I_a$ or by applying a negative voltage between anode and cathode at any time; it is not so common that it is controlled in such a way. In AC applications it is naturally turned off on the negative part of the wave while in DC application it needs some additional circuitry. During the off state the SCR behaves like a diode because of its internal junctures, and hence it has a $I_{BR}$.

**Snubber circuits**

Snubber circuits are electrical networks usually composed by capacitors, resistors and inductances that control the voltage and current transients on the thyristors. They have very simple configurations, providing a reliable solution for high rise of rate voltage $dv/dt$ and rise of rate current $di/dt$. Snubber design involves compromises; they include cost, voltage rate, peak voltage, and turn-on stress [40]. Practical solutions depend on device and circuit physics, improper device selection for snubber circuits could lead to the device or circuit destruction.
The main application of snubber circuits is the protection of \(dv/dt\) during turn-off. When the circuit is inductive and \(I_{AK}\) goes below \(I_{Ht}\), there is a high voltage that starts rising across the terminals. This \(dv/dt\) induces currents on the junctures of the thyristors, which if are too high, takes the device into conduction again. In order to control the voltage rate, a capacitor is connected in parallel. Additionally, a resistor connected in series to the capacitor is connected for limiting the current discharge when the thyristor is conducting. Refer to Figure 3.10.

![Figure 3.10: SCR with RC-snubber](image)

The rate of \(I_{AK}\) is related to the current density of the material. When the SCR starts conducting, it should do it uniformly throughout all its material and not just in some “hot spots”. If this is the case, high currents are concentrated in certain parts while in others there is still voltage remaining. This leads to high power dissipation with the subsequent temperature rise and probably the device destruction. In order to counter this, it is advisable to increase the cross sectional area of the SCR that it is initially turned on by applying a gate current pulse that rises rapidly to a high value suitable for the adequate turn-on. In addition, a small inductor connected in series can be used.

**Heat dissipation and losses**

Power losses that arise during SCR operation are transformed into heat. These losses must be dissipated sufficiently and effectively in order to operate the device within its
upper temperature limit. Excessive losses could lead to the device malfunction (a raise on the temperature increases the leakage current of a negative biased PN junction and leads to the degradation or even destruction of the device due to thermal runaway and thermal breakdown).

Losses are composed by the turn-on, turn-off and on-state losses. For the specific application of a STS, switching losses (turn-on and turn-off) are not relevant since the frequency of operation is either 50 Hz or 60 Hz. They are of a great deal in converters where the frequency of operation is above 1 kHz. On-state losses depend on the on-state voltage drop and the operational current of the device. The on-state voltage drop strongly depends on the resistance imposed by the N and P layer of the semiconductor device [21].

There are several techniques to dissipate the heat from the device; conduction, natural or forced air convection and radiation [31]. The most popular one for power semiconductors in industrial applications is convection cooling. Usually a heat metal sink is attached to the device in order to transfer the heat to the ambient. The following parameters must be taken in account when designing the cooling system for SCRs: (1) $R_{JC}$, (2) $R_{CS}$ and the (3) $T_j$. Once the power loss is known, the required thermal resistance for the heat sink can be obtained for a chosen ambient temperature following the given equation [31]:

$$T_j - T_A = P_A (R_{JC} + R_{CS} + R_{sa}) \quad (3.1)$$

The cooling medium may be gas (air) or liquid (water or oil). If air is used as a cooling medium then the heat sink is required to have a large surface area. They are mainly done of aluminum and used for low and medium power applications. Conversely, if water or oil is used there is a gain in efficiency; however, the systems become much more complicated. These kinds of solutions are mainly used for high power applications.
3.5 GTO

The GTO is a four layer PNP device with similar behavior to the SCR. The main difference is that it is able to turn off the main current by means of applying a high negative current between its gate and cathode. This avoids the need of commutation circuits for turning off conventional thyristors, meaning that the application systems can be downsized and used more efficiently.

The basic layout and symbol of a GTO is showed in Figure 3.11. When a GTO is in its conducting state all the layers are filled with holes supplied from the anode and electrons supplied from the cathode. When a reverse voltage is applied between gate and cathode, a certain amount of the holes of the P base layer are extracted producing a decrease in the injection of electrons from the cathode. Further, in response to this suppression, more holes go through the gate causing again more electron suppression. As a consequence of this process the juncture J₃ becomes reverse biased and the thyristor enter its off state.

![GTO Diagram]

Figure: 3.11 GTO basic layout [41]

Another way of understanding the turn-off process is by means of the two model transistor in Figure 3.12. When $I_{GO}$ is greater than $I_B$, transistor $T_1$ turns off, turning off transistor $T_2$.  

28
Operating waveforms and parameters

The anode voltage and current waveforms and gate voltage and current waveforms are similar in the SCR and GTO during turn-on. A current pulse from gate to cathode is needed to turn on the device ($I_G$), the nature of this pulse varies according to the anode voltage. When the latter is very high, the pulse should have a peak and then come to a steady state. Whereas when the anode voltage is relatively low, the peak of the pulse can be avoided and the device is can be turned on with a step current. $I_G$ is inversely proportional to $T_j$, i.e. the lower $T_j$ the higher gate current that is needed to turn on the device. Figure 3.13 shows the GTO’s turn-on and turn-off.
There is one important difference between the conventional SCR and the GTO after the turn-on. While the SCR has a very small $I_L$, the GTO has a large one, and what is more dangerous that it depends considerable on the temperature. This could turn the device off undesirably. To counter this effect, it is necessary to inject a DC current (backporch current) between gate and cathode during the on-state time. The backporch current should be at least 20% higher than the gate trigger current $I_{GT}$ at the lowest $T_j$ (worst scenario) [20].

In order to turn off a GTO, a high negative current should flow between gate and cathode. The gate drive circuit should be able to provide this current with a high enough $di/dt$ to assure a homogeneous turn-off. A 30 A/us is considered a high $di/dt$. There is no upper limit for this parameter and the higher it is, the better for the turning off process. In fact very high rates improve considerably the switching characteristics of the devices as it is mentioned later with the description of the IGCT. When the GTO is switching off, the anode current will be shifted to the snubber circuit generating a spike voltage $V_{DSP}$ that will be proportional to the stray inductance $L_s$ and the snubber capacitance $C_s$ [41]. If this
voltage is high enough, this could lead to an avalanche effect considering that there is still a high anode current flowing.

When the GTO is turned off, the anode voltage increases at a $dv/dt$ that is proportional to $I/C$ reaching a peak voltage $V_{DM}$ and then stabilizing in the main circuit voltage level. In the meantime the anode current will be abruptly decreased. After the turn-off period $t_{so}$ a tail current flows until all the excess carriers are completely gone in the silicon. The gate voltage (negative polarity between gate and cathode) also decreases after the $t_s$ period and eventually becomes equal to the gate power supply gate voltage. It is also important to mention that $t_{so}$ is the time required to turn off the GTO, during this period the impedance between cathode and gate should be kept as low as possible in order to allow the total extraction of the excess carriers.

**Snubber circuits:**

The snubber circuit in the GTO more or less accomplishes the same function than the commutation circuit in a SCR. It should be capable of withstanding large amount of currents providing a low inductance path and an adequate capacitance. This is achieved by means of a RCD circuit. Figure 3.14 illustrates a typical circuit.

![GTO RCD-snubber diagram](image)

**Figure 3.14: GTO RCD-snubber [41]**
The total value of the inductance of the snubber circuit $L_s$ is extremely important since it affects several parameters that lead to device failure. It is composed of the diode $D_s$, capacitor $C_s$ and wiring parasitic inductances. In order to obtain its value, the following procedure can be followed [41]: Remove the snubber resistance $R_s$ from the circuit. Replace the GTO thyristor with switch SW (A fast switching SCR is recommended). Apply DC voltage to snubber capacitor CS. When switch SW is closed, a discharge waveform is obtained. $L_s$ can be obtained using Eq. (3.2) based on the pulse width ($t_w$) of this current waveform:

$$L_s = \left(\frac{t_w}{2\pi}\right) \frac{2}{C_s}$$

(3.2)

The magnitude of $V_{DSP}$ (from Figure 3.13) depends on $L_s$ and on the $di/dt$ of the current that shifts to the snubber during turn-off. The larger the inductance, the higher $V_{DSP}$ gets, which could lead to a turn-off.

The capacitance of the snubber circuit $C_s$ is inversely proportional to $dv/dt$, this comes from the fact that $I/C_s$ (I=turn off current) is proportional to $dv/dt$. Hence, if $C_s$ is too low, a big $dv/dt$ is produced causing big turn-off losses and the decreasing the maximum turn-off current $I_{TORM}$ of the device.

The snubber resistance $R_s$ is linked to the turn-on time of the SCR. When $R_s$ is high, the discharge constant $\tau = C_sR_s$ is high as well, allowing the capacitor $C_s$ to discharge completely in approximately $5\tau$. If the turn-on finishes within $5\tau$, the capacitor is not completely discharged, so the remaining capacitor’s voltage is applied to the GTO. This will increase the spike voltage and could destroy the GTO. A small value of $R_s$ increases the turn-on losses due to the high currents that flow from the capacitor discharge current. A typical value for $R_s$ is around 5 to 10 $\Omega$.

For selecting the snubber diode, the forward recovery voltage and reverse recovery time $t_{rr}$ of the device should be taken in account. $t_{rr}$ reverse recovery time is linked to the voltage drop after $V_{DM}$ (See figure 3.13). A too long time could result in a negative voltage applied between anode and cathode. Recommended values are that the forward
current $I_f$ of the diode should be one tenth of the maximum turn-off current $I_{QRM}$ of GTO and the diode $V_{RRM}$ should be equal to $V_{DRM}$ of the GTO.

**Losses and Heat Dissipation**

The power losses generated in a GTO are composed by the turn-off, turn-on and steady state losses. Turn-on losses are directly linked to the $di/dt$ rate whereas turn-off losses are to the snubber capacitance of the gate circuit. However, these losses are not relevant and will be neglected for the purpose of this document since there is no frequency of operation in the natural operation of a STS.

Steady state losses are very important for the STS since there is a steady flow of current through the semiconductor during normal operation, which leads to high losses that are be proportional to the current flowing $I_{AK}$ and $R_{on}$. The cooling techniques used are the same as the ones explained for SCRs.

**3.6 IGCTs**

The IGCT or also sometimes called HD-GTO (Hard driven GTO) is composed by a Gate Commutated thyristor (GCT) and a gate unit (GU) coupled as a single unit [20]. The GCT is a conventional GTO wafer as shown in figure 3.15. It is encapsulated in a ceramic press pack housing with very low gate-to-cathode inductance. The GU is a special gate circuit with extremely low parasitic inductance.
The main advantage of this configuration is the reduced overall parasitic inductances that appear on the device. A conventional GTO has an internal parasitic capacitance of approximately 30 nH and its drive circuit, including the coaxial connecting cable of around 300 nH. As a result the rate of rise of negative current for turning off the device is limited somewhere around 50 A/μs. This value limits $I_{TORM}$.

**Operating waveforms and parameters**

GCT and the GU together can have a total inductance as low as 5 nH which increases the rate of gate current $di_{GQ}/dt$ up until 3.5 kA/μs. This allows the thyristor to be turned off with a voltage source of only 20 V [43]. These extremely low inductances are achieved by a special construction on the thyristor internal geometry and the gate drive circuit. Which such a high $di_{GQ}/dt$ the switching time and storage times are drastically reduced. Figure 3.16 depicts IGCT’s turn-on and turn-off. As it is seen commutation times are considerably smaller than in GTOs and SCRs. Also a homogeneous and very safe turn-off is achieved due to speed and very low storage times on the wafer; it is even possible to use a snubnerless configuration.
Snubber circuits:

IGCTs can be operated without $dv/dt$ snubbers when they are assymetrical, i.e. in Voltage Source Inverters (VSI) configurations. This feature adds great advantages when compared to GTOs and SCRs since it brings savings in space and losses. However, for symmetrical IGCTS this is not relevant since there is still need for a $dv/dt$ snubber due to the reverse voltage applied to the device. The configuration recommended by manufacturers (ABB) is a RC snubber as used for the SCR. Refer to Figure 3.10. The only difference remains on the size of the component. IGCTs require smaller components providing improvements in efficiency and in cost.

Regarding the $di/dt$ capability, it is higher than in SCRs and GTOs. Usually there is no need for a current limiting inductance since the parasitic inductances of the circuit provided the value required. Nevertheless, for the STS this is also not relevant since the currents are sinusoidal; therefore, $di/dt$ is low.

Losses and Heat dissipation

The semiconductor part of the IGCT is basically an improved GTO. It has benefited of more advanced techniques in the fabrication process like the buffer layer [43] and the transparent emitter. This has lead to less conduction and switching losses when compared
to SCRs and GTOs. It even has less switching losses than IGBTs in high power applications [43].

Symmetrical IGCTs have higher on-state losses than asymmetrical ones; hence for an STS application the conduction losses remain considerable high and similar to GTOs. Therefore, so far it is not economically feasible from cooling requirements perspective to design a low voltage STS.

The cooling techniques are the same than the ones used for SCRs.

3.7 The future

Silicon is the material from which all power semiconductors are based. Silicon-based power semiconductor technology is a mature technology that has reached a point where it is not possible to develop further major improvements due to the intrinsic properties of the material. In other words, ratings as voltage blocking, current density, junction losses and thermal conductivity are limited by the inner physics of silicon.

The two major limitations of silicon are its narrow bandgap (1.1 eV) and its low thermal conductivity. The former leads to a low intrinsic breakdown electric field, i.e. a low voltage blocking capability. Blocking capacity of single devices doesn’t go above 12 kV. The latter imposes limitations on the device operating temperature due to its poor thermal conductivity. Available devices have operating temperature limits between 120°C and 150°C, requiring significant thermal management systems to keep the semiconductors operating within the temperature limits.

Research has been focused on new semiconductor materials that can provide improvements when compared to silicon. Significant technical advances are being achieved in materials like Silicon Carbide (SiC), Gallium Nitride (GaN) and diamond [15]. SiC appears as the most suitable material for the new generation of power semiconductor due its affordable price, and clear advantages when compared to Si. GaN
is also a possibility, however it provides lower ratings than SiC. Diamond is the ultimate semiconductor device. Its properties are definitely outstanding and by far more superior than SiC. Nevertheless, this is still in a very preliminary stage and it is thought that maybe in 30 years this technology could reach maturity.

SiC devices will bring dramatic improvements in the semiconductor business. Recent studies [44] comparing SiC and Silicon-based diodes have shown that the breakdown voltage can be improved by a factor of around 40 times. The operating temperatures of SiC-based devices are above 400 °C, which could bring huge savings from cooling perspective. Additionally, and what it is maybe the most important feature form STS point of view is the reduction of on-state losses, this is said to be reduced by a factor of 10.

Even when commercially SiC-based thyristors are far away, it is important to be aware of its applicability for STS. Furthermore, SiC-based IGBTs are under ongoing research and its commercial availability may be not so far away. This could open a new possibility for STSs (IGBTs are not feasible for STS at the moment, since they have no reverse blocking capabilities, high on-state losses and low current capability) considering its advantages in control means and turn-on and turn-off times.
Chapter 4
Design of a Static Transfer Switch

4.1 Introduction

STSs are devices that rely on power semiconductors for their basic operation, i.e. commutating between power sources to keep a steady flow of electric power to the load during fault events. Besides power semiconductors for the static switches, the STS has an intelligent unit which performs all the measurement and control operations for the transfer process. The last main component of the system is the bus bar assembly which provides protection and maintenance for the device.

Commercially available STSs have ranges between 50 A and 4000 A and from 120 V to 600 V. Solutions and devices used throughout these ranges may be different considering the constraints imposed by current and voltage levels. Current brings along limitations not just regarding the semiconductors but also heat dissipation issues and bus bar protection. Voltage level deals mainly with the forward and reverse voltage capability of semiconductors. However, this is not a serious problem in the STS since voltages go up above 690 V very seldom.

The following section provides a thorough analysis of the requirements and solutions available in the market for STSs focusing on their three main block components: (1) static switches, (2) control means and (3) bus bar assembly. In the static switch section the focus is on Silicon Control Rectifiers (SCRs); nevertheless other possibilities like Gate Turn Off Thyristors (GTOs) and Integrated Gate Commutated Thyristors (IGCTs) are analyzed considering that they could have some potential use in future switches. The other two remaining sections are analyzed regardless of the type of semiconductor selected since their operations are not affected by them.
4.2 Static Switches

Static or power electronic switches are integrated by a combination of power semiconductors and a driver for controlling the commutations process. The interaction between these two elements defines the characteristics of the switch. These elements can replace mechanical and electromechanical devices to perform switching operations. The use of semiconductors eliminates the traditional drawbacks of their electromechanical peers like contact sticking, bounce and tear. However, it brings along other disadvantages like high losses and lack of galvanic isolation.

As stated in Chapter 3, there are several types of semiconductors that can perform the switching. The ultimate result is the same—closing or opening an electrical circuit—no matter which semiconductor is chosen. Nevertheless, there are many features (e.g. losses, switching time, control means) that should be taken in account when selecting the proper device for the specific application, which in this case is a STS.

![Static Switch Block Diagram](image)

**Figure 4.1: Static switch block diagram [12]**

A static switch system is shown in Figure 4.1. The device is composed of a control unit which sends the signals for changing the states of the switch (depending on the semiconductor, this could be turn-on or turn-on and turn-off). The power supply block provides the energy to keep all the logic control working and also to send the signals to
the semiconductors. The driver integrates the signals from the control circuit to the power circuit by means of galvanic isolation (i.e. either by optical or transformer means). Lastly, the internal capacitances and inductances should be carefully analyzed as they affect the dynamic behavior of the switch.

Static switches can conduct current either unidirectionally or bidirectionally depending on which semiconductor they are based on and in the way these are configured. The same applies for blocking forward and reverse voltage. The requirements of these features are imposed by the applications in which they are going to be used. For example, in VSI configurations there is no need of having devices with reverse voltage capabilities. Conversely, in STSs as in Current Source Inverters (CSIs) applications, power devices must have reverse blocking capabilities since they are subjected to positive and negative voltages during every electric cycle. Figure 4.2 shows some possible combinations of semiconductor switches with their current and voltage features.
Figure 4.2: Static switch configurations [12]

The STS must be composed of two bidirectional voltage and current switches. These switches, no matter which configuration they have, must conduct during the positive and negative cycle of the voltage. They must also allow forward and reverse voltage blocking at the nominal voltage level of the electrical installation. From Figure 4.2, it is clear that there are several possibilities for the transfer switch. The following section analyses several configurations with different types of semiconductors from technical and economical perspective.

4.2.1 SCR configuration

SCRs belong to the thyristor family. They are capable of switching the current in one direction once they have been triggered (on-state) while blocking forward and reverse voltage when they are not triggered (off-state) [13]. Therefore, two pairs of SCRs connected in inverse parallel provide the solution required for a STS. It is worth to mention that most of the static transfer switches commercially available are based on SCRs. Refer to Figure 4.3 for the proper configuration.
SCR selection

There are several players in the power semiconductor manufacturing business, among the biggest stand: ABB, Mitsubishi, Westcode and Powerex [15]. All of them offer SCRs in a wide range of currents and voltages (from 250 A to 6000 A and up to 6500 V). The right election of SCRs for STSs should be based in a cost-effective solution for the whole system, i.e. good and reliable electrical performance with a competitive price.

Low voltage STSs are intended for operational voltages equal or below to 1000 V; therefore, the devices selected must withstand these ratings. If medium voltage STSs are required then higher operational voltages should be chosen according to the electrical installation for which they are applied. All these needs are covered by the wide semiconductor offer available on the market.

As with voltage ratings, manufacturers also provide a broad range for current ratings. For example ABB has a range between 730 A and 6100 A for the maximum average on-state current $I_{TAVM}$ (which is one of the key parameters for device selection), while Mitsubishi a range between 1000A and 5000A for the same parameter. Figure 4.4
summarizes the offer available in the market for discrete SCRs based on currents and voltages.

![Current and voltage ranges covered by commercially available SCRs](image)

**Figure 4.4: Current and voltage ranges covered by commercially available SCRs**

In order to choose the right thyristor for the application it is important to make some remarks regarding the ratings and electrical characteristics provided by manufacturer’s data sheets. Voltage and currents are usually the first parameters to be taken into account when choosing the SCR, current should be chosen according to the thermal ratings of the device while voltage according to its electrical breakdown capability.

Every manufacturer provides information regarding $I_{TAVM}$ and the maximum RMS on-state current $I_{TRMS}$ at a fixed temperature case (usually 70 °C, however this can vary according to different manufacturers). These currents are defined by the standard IEC60747-6 as the average and RMS values of the maximum on-state current (half sine wave) that can flow through the device without rising the $T_j$ of the semiconductor above its maximum limit (125 °C). A $T_j$ working beyond its limits severely affects the blocking
capabilities of the device since the leakage current of the junctions rises exponentially with temperature.

For calculating the voltage rating there is no fixed rule since they are related to the source. ABB in [16] recommends a factor of 2.5 above the maximum voltage level of the line. The following example illustrates how to calculate current and voltage ratings.

Figure 4.5 shows a 300 kW, 0.8 P.F. load connected to a 3-phase, 440 V system. From basic electric circuit theory line current $I_s$ is calculated:

$$I_s = \frac{300000}{\sqrt{3 \times 440 \times 0.8}} A = 492.06 A$$  \hspace{1cm} (4.1)

The maximum current that flows through the thyristor is $I_m = \sqrt{2} \times 492.06 = 695.88$ A. From here, it is possible to calculate $I_{TAV} = I_m / \pi = 221.50$ A and $I_{TRMS} = I_m / 2 = 347.93$ (see Appendix A). Once these two values are known, and together with $V_{DRM}$ and $V_{RMM}$ it is easy to choose the required thyristors from the manufacturers’ datasheet. In this case the selected semiconductor is ABB 5STP 03X6500 (see Appendix B).

![SCR calculation example](image)

Figure 4.5: SCR calculation example
Apart from just discrete units, semiconductor manufacturers also offer power modules (i.e. single devices connected in a certain topology for specific applications within a single block). These modules offer advantages of high voltage and current switching characteristics, and higher speed than that of conventional SCRs. As regards of a static switch module, this means two SCRs connected in reverse parallel within a single block; therefore two blocks would be needed instead of four discrete SCRs for a single phase STS. Yet, it is worth to mention that the range is more limited than for discrete units. Rating availability of such devices is shown in Figure 4.6.

![Figure 4.6: Ratings of SCRs in reverse parallel modules](image)

ABB has gone further than assembling a power module; they have developed the Bi-Directional Control Thyristor (BCT) [17] which integrates two anti-parallel high power SCRs in one single silicon wafer assembled into an unique housing. This feature provides the designer of a static switch with considerable improvement in size, reliability and cost for the end product, even more than with the modules explained earlier. The current and voltage ratings for the BCT are high; therefore it could be an appropriate solution for the higher end of the STS.
Gating requirements

The main purpose of a gate driver for a SCR is to provide a gate current of the right amplitude, at the right time and of the right duration [16]. Thyristors are current-controlled devices and therefore they need drivers that behave like current sources. These drivers need to be isolated from the power circuit for a reliable operation. This is accomplished either by pulse transformers or optocouplers.

IEC 60747-6 [46] defines several gate driver parameters for thyristors (SCRs, GTOs and GCTs). These should be provided by manufacturers and followed by the end-user in order to have an adequate operation of the device. Among the most important gate parameters are: (1) gate current pulse amplitude $I_{GM}$, rate of current rise $diO/dt$ and the pulse current duration $t_p(I_{GM})$.

Considering that SCRs don’t need high currents, reverse voltage from gate to cathode during off-state operation nor a steady current from gate to cathode during on-state operation, it can be said that they have simple driver requirements than GTOs and IGCTs. Usual values for $I_{GM}$ should be between 2 A and 5 A usually, $diO/dt$ may be around 2 A/μs and $t_p(I_{GM})$ around 20 μs.

Even when a SCR needs just one pulse to be triggered, drivers usually send a burst of pulses with the aim of ensuring the firing (if one pulse fails most likely the next one will turn on the device). This is because sometimes is difficult to predict the exact moment when the device can turn on, especially when current and voltage have a considerable phase shift. For an STS application this accuracy on the time of the pulse is critical since it can either avoid or allow cross current between sources. More detailed information regarding the pulse timing is given on the control issues section.
Snubber concept

Semiconductors are very powerful devices for controlling currents and voltages; however, they are susceptible of failure if operated outside their Safe Operation Area (SOA). It is very important that a thyristor keeps its voltage between anode and cathode within acceptable limits when turning off its current. The transient voltage generated during turn-off depends upon the commutation inductance, commutation voltage and \(\text{di/dt}\) during turn-off and turn-on of the semiconductor [18].

As explained in Chapter 3 (Figure 3.10), a capacitor and resistor in series (RC snubber) are connected in parallel between anode and cathode for limiting the transient voltage and damping the ringing [19]. An optimal design of this circuit branch leads to a minimum capacitance utilized representing cost, space and power savings for the overall system.

For STS applications, the worst situation from the point of view of the reverse overshoot voltage (transient generated during turn-off) is when the load is lagging around 90° from the voltage (inductive loads). That means that the thyristor current \(I_T\) reaches zero when the voltage across the thyristor is on the most negative side of the wave. Refer to Figure 4.7. Even if purely inductive loads are rare, this case will be used for example purposes.
Figure 4.7: Worst case scenario for SCR turn-off (purely inductive load)

When the current is going through zero, it continues conducting due to remaining charges in the junction until it reaches a maximum point (maximum reverse recovery current $I_{R_{RM}}$). Once at this point the voltage tends to overshoot because of the rate of current $di/dt$ ($V = L \times \frac{di}{dt}$). Afterwards the reverse recovery current $I_{RR}$ starts decreasing until it reaches a steady level which is the reverse leakage current $I_{R_{SM}}$. Refer to figure 3.5.

Manufacturers have their own recommendations regarding how to calculate optimum snubber values. ABB provides several curves according to the voltage blocking rating of the devices. These graphs give the values of the elements needed provided that the commutation inductance $L_c$ and the reverse voltage $V_R$ are known. Figure 4.8 shows these curves.
Figure 4.8: ABB recommend curves for obtaining optimum snubber values

To properly use this graph, $\frac{di}{dt}$ needs to be calculated. For this purpose the commutating voltage $V_C$ and the $L_C$ are needed. Since it is not known which will be the final configuration of a static transfer switch (configuration may vary according to end-customers), is very difficult to find $L_c$. However, for calculation purposes it is obtained assuming a short circuit current $I_{SH}$ of twenty-five times the nominal current. Using the values from Figure 4.5:

$$L_c = L_{phase} = \frac{440}{\sqrt{3 \times 2 \times \pi \times 50 \times 25 \times 492.06}} = 0.066 \text{mH} \quad (4.2)$$

$V_C$ is known from the sine wave (source) and it is 440 V. This yields a $\frac{di}{dt} = 6.69$ A/$\mu$s. Now with $\frac{di}{dt}$ value, the reverse recovery $Q_r$ of the thyristor should be obtained at maximum temperature junction, i.e. $T_{Jmax} = 125^\circ C$ from the device datasheet. The value obtained is $Q_r = 3500 \mu$As. The next step is to define the value for the voltage overshoot ratio, a reasonable value could be 1.8 which yields a maximum reverse voltage $V_{RM} = 1120$ V. Once we have all these values clear, the capacitance can be obtained from Figure 4.8.

ABB provides three curves according to the peak repetitive reverse off-state voltage $V_{RMM}$ of the semiconductors. In each of the graphs there are several curves according to the reverse voltage overshoot ratio. Once the curve is chosen, the capacitance is obtained from the vertical axis (considering the highest y-axis point) and afterwards with that same value, the resistor is obtained from the correspondent x-axis value. For this case $C_s =
0.625 μF and R = 10.27 ohms. Since there are no commercial values for those numbers, the next commercial values are chosen. Figure 4.9 shows a simulation of the commutation process with the aforementioned values using MATLAB.

![Figure 4.9: SCR voltage conducting 180° with a fully inductive load](image)

It is worth to mention that the smaller the overshoot voltage the higher the capacitance that is needed. A higher capacitance brings more losses, more space and of course more cost. Therefore, there is a trade-off for the designer between these issues and the overshoot voltage.

**Thermal issues**

Temperature management is a key issue in power semiconductor devices. On-state, turn-on and turn-off losses appear as heat which is dissipated in the device contributing to a considerable rise in the operating temperature. The heat should be transferred to a cooling medium as efficiently as possible in order to keep the device working properly (i.e. below $T_{j\text{max}}$).

As stated in Eq. (3.1) in Chapter 3, the total power losses are needed in order to define the cooling system requirements. Once the thyristor has been tentatively chosen, the next step is to define the losses in order to calculate the cooling means that the circuit needs. The following equation [20] renders them.
\[ P_{ON-STATE} = V_{TO} \times I_{TAV} + r_T \times I_{RMS} \]  

\[ = 1.2 \times 221.5 + 0.0023 \times 347.93^2 = 544W \]

\( V_{TO} \) and the \( r_T \) are provided by the device manufacturer while \( I_{TAV} \) and \( I_{RMS} \) are calculated from the example of Figure 4.5. Eq. (4.3) represents the losses while the thyristor is conducting. It is worth to mention that the turn-on and turn-off losses are not being taken into account for total power loss calculation for the STS application; hence the on-state losses represent the total losses for analysis purposes. The first reason is that the thyristor commutates with a very low rate of current \( di/dt \) (natural commutation) during normal operation; therefore, turn-off losses are negligible. The other reason is that the operation is either 50 Hz or 60 Hz.

Once the losses have been calculated, it is possible to calculate the cooling needed. Considering a maximum junction temperature \( T_{j,m} = 125 \) °C, ambient temperature \( T_a = 40 \) °C, and the values obtained from the datasheet for \( R_{JC} = 85 \) K/kW and \( R_{CS} = 15 \) K/kW, Eq. (4.4) yields the thermal resistance of the cooling system:

\[ T_{j,m} - T_a = P_T (R_{JC} + R_{CS} + R_{SA}) \]

\[ R_{SA} = 0.05625 \) °C/W\]

The cooling system is composed of a heat sink and a cooling medium which can be either gas or liquid. The heat sink is usually made out of aluminum for its low thermal resistance and ease of shaping. The gas is usually air; air cooling can be achieved by natural or forced convection, with the latter using fans for keeping the necessary airflow through the heat sink flanges. Refer to Figure 4.10 for illustration of natural and forced air convection. Water or oil cooling is another possibility considering that they have higher heat transfer coefficients [19]. However, the solutions are rather complicated and used for very high power applications.
The system needs a cooling system with a maximum $R_{SA} = 0.05625 \, ^\circ\text{C}/\text{W}$. For this particular example a natural air convection aluminum heat sink is enough for each thyristor. The model E3177 could be chosen from manufacturer Thermaflow [23]. Drawing and dimensions are shown in millimeters in Figure 4.11.

![Diagram showing natural and forced air convection](image)

Figure 4.10: Air convection [20]

![Diagram showing dimensions of heat sink](image)

Figure 4.11: Dimension in of the heat sink needed for the example of figure 4.5 [23]
4.2.2 GTO Configuration:

As the SCR, the GTO also belongs to the thyristor family. It appeared in the middle of the 70’s as an answer to the demand for power controlled inverter units [15]. It has the feature of being able to be turned off by a high current between its anode and gate. Though this feature makes it more attractive than SCRs, there are others that have thwarted its widespread use like conduction losses, elaborated snubber units and cumbersome gating circuitry capable of supplying very high currents [36].

The main applications for GTOs have been and still are VSIs where they don’t have to worry about blocking high reverse voltages [20]. Thus, most of the offer available on the market is of asymmetrical devices. Indeed, the only main player offering a symmetrical GTO is Westcode Semiconductors [37]. On the other hand, STS applications need symmetrical devices; therefore, the feasibility of using GTOs is quite low. Nevertheless, some calculations and assessment of advantages and disadvantages compared to the SCR-based solution are addressed in the following paragraphs.

The configuration of a GTO-based STS looks exactly the same as with SCRs but there are some changes on the behavior of the electrical system. Refer to Figure 4.3. First of all the GTO is able to stop the flow of current at any time; therefore, there is no need to wait until the natural zero crossing of the current to turn off the thyristor. This could drastically reduce the transfer times to levels of $\mu$s considering that there is no more dependence on the point-of-wave or on the power factor of the load. However, even when the transfer time can almost be instantaneous there is still a detection time limiting the total transfer time; therefore this advantage is somehow limited by the fault detection algorithm.

**GTO Selection**

It is almost the same as with the SCR; however, there is one more important parameter that we need to take in account: $I_{TGM}$. This is the maximum current that the GTO is able
to break at certain conditions specified by the manufacturer. For the case of an STS it should be specified as the current peak plus a safety margin. Figure 4.12 refers to the offer of symmetrical GTOs available on the market.

![Symmetrical GTOs](image)

Figure 4.12: Symmetrical GTOs available on the market

**Gating requirements**

Regarding gating signals, GTOs are more demanding than SCRs. When comparing symmetrical GTOs and ABB’s SCRs, the gate current for turning on GTOs is ten times higher than with SCRs. Moreover, GTOs need a very high gate current for turning off (typically 35% of the current to be controlled) and with a high $di_{GO}/dt$ [31], meaning that for turning-off a current of 300 A approximately a negative current of 100 A is needed between gate and anode.

Since GTOs have a much higher holding current $I_H$ than SCRs, there is a need of a continuous current (between 1A and 5A) at the GTO gate to avoid unlatching of the thyristor. Additionally, a negative voltage (usually above 1V) is needed between gate and cathode in order to provide the device with blocking capabilities. All this features require
complex, bulky and inefficient gate drives that clearly shadow the advantages that it could offer for STS applications.

**Snubber concepts**

As stated in Chapter 2, GTOs require RCD snubbers as shown in Figure 3.14. These elements must be able to withstand the full current to be turned off. When the device is turned off the current flowing through the device commutates to the diode and charges the capacitor, keeping the rate of rise voltage within safety margins [38]. During turn-on the capacitor is discharged through the resistor adding losses proportional to the energy stored in the capacitor.

The fact that snubber components have to withstand the full current adds cost, volume and complexity. Moreover, there is one additional component (diode) when compared to SCR snubber. Therefore, from snubber circuit perspective and for STS applications, the SCR outperforms by far the GTO.

**Thermal issues**

Thermal constrains are higher than withSCRs because of higher losses. Consequently, there is a need for more cooling means. For the example showed in Figure 4.5 and using the Westcode S0700KC17D symmetrical GTO instead of ABB SCRs, the system produces on-state losses in the order of 1443.88 W. From datasheet manufacturer [37] and applying Eq. (4.3) the requirements for the cooling systems are obtained. Calculations show that even assuming an ambient temperature of 20°C we will need a heatsink with a thermal resistance of 0.012°C/W or less. This is a very low value and only achievable with cooling methods with a water flow of around 6 lt/min [39].
4.2.3 IGCT Configuration

The IGCT integrates a GCT with a multilayered printed circuit board that provides the gating signals. The GCT also belongs to the thyristor family and it is an offspring of the GTO. Its main advantage relies on its very low inductance driver system—allows having extremely high $di/dt$ for gating signals—, which has been achieved by means of an optimized housing and integrate drive concept [20]. The gate provides very high and fast currents capable of turning the device off as fast as in 1 μs; achieving considerable less turn-off losses than any other device on its field.

As with GTOs, the main application for these devices is VSIs. Therefore, the majority of the market offer is for asymmetric devices. Nevertheless, Mitsubishi\textsuperscript{2} and ABB have a few symmetrical models (reverse blocking capabilities). Hitherto, symmetrical IGCTs have been applied in CSIs and, in Dynamic Voltage Restorers (DVRs) and Dynamic Uninterruptible Power Supplies (DUPS) [34]. Even when the availability of such devices at the moment are only for blocking voltages of 6500 V—which may be too much for STS requirements and impose high prices for its applications—and relatively small currents, it is worth to take them in account since more devices with different ratings are under development.

The configuration of an IGCT-based STS looks exactly the same as the SCR-based; however, there are some changes on the parameters of the electrical system that must be pointed out. The advantages in commutation times are exactly the same as with GTOs from STS perspective. Even when the IGCT has faster commutation times than GTOs this is not relevant for the STS operation since both are extremely short compared to the detection times that the system needs. Nevertheless, there are other benefits that are worth of paying attention since could simplify the lay-out of the system in a near future.

\textsuperscript{2}Mitsubishi offers the GCT unit and drive separately.
IGCT Selection

It is exactly the same as with SCRs and GTOs; therefore, no additional explication or comparison is needed. Figure 4.13 shows the market availability of symmetrical IGCTs.

![Symmetrical IGCTs available on the market](image)

**Figure 4.13:** Symmetrical IGCTs available on the market

**Gating requirements**

As explained above, IGCTs are a combination of a driver circuit and the thyristor in one package. This brings easiness from engineering point of view. The gate is capable of delivering currents as high as the full turn-off current with only 20 V between gate and cathode [31] and the end-user just have to provide and AC source for the driver unit (40 V or 28 V square wave according to ABB recommendations) [35]. Gate commands are provided by optical means, this could be a tricky situation since the optical signals must have a high signal to noise ratio, especially if the systems are functioning on hard environments from EMI (Electromagnetic Interference) perspective.
Snubber concepts

One of the IGCTs advantages is its ability to turn off snubberlessly, this is true for assymetrical devices. However, symmetrical devices are needed for STSs applications and these types of IGCTs do need snubber circuits to limit the overvoltage.

Turn-on snubbers are also needed in the form of a choke and a sampling diode to limit the $di/dt$ when used in VSI or CSI configuration. This is mainly because of the freewheeling diode which imposes limitations on the rate of current rise. Yet, for STS applications there are no diodes. Therefore, there is no limitation for $di/dt$ and the diode can be avoided.

Thermal issues

Devices available from Mitsubishi and ABB offer relative high on-state losses in comparison to GTOs and SCRs. For example ABB reverse blocking IGCTs offer $r_f$ of 11 and 6.4 mΩ. These values are high compared to SCRs and GTOs, approximately ten times more, which make very unfeasible an IGCT-based STS.

This is understandable since the main advantage of the IGCT is the reduced turn-off losses, which come in account when the operation is under high frequencies. Nonetheless, for this application the frequency is either 50 Hz or 60 Hz; consequently, no relevant improvements are done to the overall operation. Maybe in the following years with improvements in the semiconductor manufacturing, this technology could become attractive for STSs applications.

4.2.4 Pricing matters

Semiconductors are expensive devices due to their fabrication process. As its correspondent electromechanical switches their price is directly proportional to their current and voltage ratings and also to the features that they offer (e.g.: commutation
times, turn-off capability, integrated driver, etc.). Consequently it is very important to assess the most adequate solution from STS perspective. GTOs offer more features than SCRs and IGCTs even more than GTOs; therefore, it is logic that the price of such devices follow the same tendency. GTOs are usually four to five times more expensive that SCRs while IGCTs at least double than GTOs.

For a technically and commercially feasible STS design the most cost-effective solution should be taken in account. As explained in this section, even when GTOs and IGCTs offer more advantages than SCRs, these are not really relevant for the STS operation or are countered by their own disadvantages. Furthermore, in some cases these features are limited by external factors like in the case of the detection time.

Even when the SCR is relatively old (from the 60’s), it is still the most appeasable solution for the STS. It does the work properly and for the cheapest price possible. Perhaps in a near future with wide bandgap devices [15] the use of GTOs or IGCTs could become viable for a STS.

4.3 Control Issues

STSs work under the premise that transfer between sources must be as fast as possible since they are feeding critical loads. The ITIC/CBEMA curve [24], which is a power acceptability curve and is widely used through industry for benchmarking electric equipment regarding power quality issues, states that most sensitive loads tolerates a maximum loss of power of half a cycle without failure. This means that STSs must accomplish their duties within this time frame.

Discontinuity of power during STS operation is determined by the load transfer time, which can be divided in two intervals: (1) detection time and (2) transfer time [14]. Detection time comprises the interval between the fault appears and the control system detects it. Transfer time comprises the thyristor logic and operation time. It is not possible to assure a total transfer time for all conditions, since both times are heavily dependent on
the type of disturbance and on the operating condition of the electrical system (i.e. load power factor and point-on-wave of initiation of the fault) when the transfer is initiated [25].

Most of the STSs manufacturers claim that their equipment can achieve transfer times within quarter of a cycle. This is usually a myth and careful analysis shows that this is not true for all possible conditions [26]. It is not the scope of this document to make a careful analysis of the topic, nevertheless in the following section some examples will be shown for a better understanding. (A. Sanino) [25] provides a thorough analysis of time dependence on the operating condition system.

The control scheme of a STS is composed of two blocks: (1) Detection block and (2) gating block which are responsible for the interval times explained above.

a) Detection Block

A common STS detection block is shown in Figure 4.14. It consists of a mathematical algorithm (dq0 transform), a filter and a comparator. The dq0 block transforms the voltage signal to a synchronous rotating frame, the low-pass filter provides protection against voltage spikes and the comparator gives the transfer signal if the value is lower or higher than a preset threshold.

![Figure 4.14: Block Diagram of the voltage-detection circuit [27]](image)

Most of the literature reviewed [16, 25, 27, 28] states that the most convenient detection technique is based on the dq0 transform. This transform is based on Park’s
transformation [24] for electrical machines and consists in converting the system phase voltages into a synchronously rotating frame as follows:

\[
\begin{bmatrix}
V_x \\
V_y \\
V_z
\end{bmatrix} = \frac{2}{\sqrt{3}} \begin{bmatrix}
1 & 0 & 1 \\
-\frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} & -\frac{1}{\sqrt{2}} \\
1 & 1 & 1
\end{bmatrix}
\begin{bmatrix}
V_d(t) \\
V_s(t) \\
V_r(t)
\end{bmatrix}
\]

(4.5)

The three phase system is transformed into a two fixed reference system αβ in Eq. (4.5). From here, Vo is eliminated as it is the zero-sequence component and then the system is once more transformed to obtain the rotating dq coordinate system as showed in Eq. (4.6):

\[
V^{(dq)}(t) = e^{-j\theta(t)}V^{(αβ)}(t)
\]

(4.6)

From Eq. (4.7) the amplitude of the supply vector is obtained. Later this value is compared with the threshold set by the end-user for start the transfer process when necessary.

\[
V_{dq} = \sqrt{V_d^2 + V_q^2}
\]

(4.7)

This technique provides very good results for detecting three-phase balanced faults with detection times that are almost immediate since it allows the control scheme to see a balanced three-phase system as a DC-quantity. However, when the fault is unsymmetrical (fault in one or two phases) the detection times rises considerably. Figure 4.15a shows the system’s output for a 70% three phase voltage sag while Figure 4.15b for a 70% voltage sag on phase A with a 0.85 p.u. (per unit) threshold. The graphs were simulated using the
dq0 detection block in Matlab. As it is seen from the figure, the detection time for the first fault is immediate while for the second case it takes around 3 ms.

![Figure 4.15: dq0 response]

a) dq0 response to a 70% symmetrical Voltage Sag   b) dq0 response to a 70% unsymmetrical Voltage Sag

The low-pass filter is usually set with a cut-off frequency of 50Hz or 60 Hz according to the frequency system. The threshold is variable and it depends on the customer needs. It should have the possibility of being parameterized from the control panel of the STS.

b) Gating scheme:

A three phase STS is composed of twelve power switches (semiconductors), each one of them should have its own control signal for turning on and off. This means that a control circuit with twelve independent outputs should be arranged for driving the whole system. Figure 4.16 depicts the block diagram of the gating scheme.
The current polarity & zero crossing detection block is responsible for giving the gating logic accurate information about the direction of the current and which semiconductor is conducting at which moment. Furthermore, this block should be fed by clean signals coming from low-pass filters in order to avoid misdetection due to spikes or glitches. In the case of failure or abnormal situation in the preferred source, the detection system sends a signal to the gating logic, which with all the necessary information sends the appropriate sequence of signals to the semiconductors for an adequate transfer process.

During normal operation of the STS, three pairs of thyristors conduct while the other three pairs remain inactive. Figure 4.17a shows the principal leg (connects the preferred source). The gating pattern for this leg should be as the one shown in Figure 4.17b. The example shows only the gating of phase R leg for illustration purposes (the gating patterns for the other thyristors are identical, just displaced 120°). Here two signals are needed (The signal for T₂ can be the same as for T₁ but just with a half period delay). In order to behave as a bidirectional switch, the gate of one thyristor should be fired immediately after the turning off of the other. For example if I₁₂ is crossing the zero point then T₁ should be triggered.
There are two ways to handle the gating strategy for a SCR configuration when a failure is detected [29]: 1) zero-current strategy and 2) commutation strategy. The first technique consists in inhibiting the signals from the active leg (part of the switch which is carrying the current) as soon as the fault is detected and once the current has decreased to zero trigger the inactive leg of the switch (from alternate source). This is usually referred as a “break before make” switching (BBM). Figure 4.18 shows STS principal and auxiliary legs for phase R along with an arbitrary waveform for example purposes, here if a fault (voltage sag) is detected when the current and voltage load have the same polarity \( t_1 \), then the control logic inhibits gating signals for \( T_{1p} \) and \( T_{2p} \), and waits until the current extinguishes through theSCRs and then triggers \( T_{2a} \). The same procedure applies to other phases.
This strategy works well; however, it can provide long transfer times which may be not acceptable for the static switch requirements [29]. If the fault occurs in the beginning of a positive cycle, then the system will have to wait almost half cycle to commutate.

![Diagram](image)

Figure 4.18: STS commutation process

The second strategy is a bit more complicated and prone to failure; however, it achieves considerable faster commutation times. It consists on firing incoming thyristor $T_{1a}$ or $T_{2a}$ (depending on the current polarity) as soon as the fault is detected. If commutation is successful there will be an interval in which the load is being fed by the two sources; therefore, it is a make before break switching (MBB) [25]. Using the same example as shown in Figure 4.18 and assuming that a voltage sag is yielded at instant $t_1$, then the sequence of events would be the following:

- Fault is detected
- Direction of current is detected. Current is flowing from source to load->$T_{1p}$ is conducting
- $T_{1a}$ is triggered even when $T_{1p}$ is still conducting. $\rightarrow$ Successful commutation (MBB transfer)
- $T_{1p}$ stops conducting
- $T_{2a}$ is fired once $T_{1a}$ current decreases to zero (normal gating pattern)
• Control returns to normal state

Another scenario would be when the voltage and current have different polarities, e.g. during intervals when feeding an inductive load. If the load has the characteristics shown in Figure 3.18 and a voltage sag happens at instant $t_2$, the sequence of events would be as follows:

• Fault is detected
• Direction of current is detected (from source to load) $\Rightarrow T_{1p}$ conducting
• The control will trigger $T_{1a}$, however polarity across the thyristor is negative ($V_{2(t)} > V_{1(0)}$) $\Rightarrow T_{1a}$ doesn’t conduct
• The control then waits to the zero crossing of $T_{1p}$ and then fires $T_{2n}$ (BBM transfer)
• Control returns to normal state

The risk involved with this strategy is that if for some reason there is a misfiring in the gating strategy, there is the possibility of cross current flowing between the sources. Typical causes are mistakes in control/sensing system, i.e. when the current polarity is detected erroneously. In the example of Figure 4.18; if thyristor $T_{2a}$ is fired instead of $T_{1a}$ during the fault event at $t_2$, then a cross current between the sources flows. In this case, the only impedance limiting the current is the source’s internal impedance. Hence, a high current flows most likely triggering protective devices.

Even when most STS manufacturers claim that their products achieve a maximum transfer time of $\frac{1}{4}$ cycle, this is very doubtful [25]. As explained before, careful analysis of switching conditions reveal that transfer time depends on operation conditions of the electrical system and on the type of faults. Therefore, there is no way to guarantee if a successful MBB operation can be achieved for all circuit conditions.
4.4 Bus bar assembly

The last main component of a STS is the bus bar assembly. Most commercially available STS (MGE, Liebert, Piller) bus bar assemblies are composed by five Molded Case Circuit Breakers (MCCB) as shown in Figure 4.19. MCCB1 (SW1) and MCCB2 (SW2) provide isolation and protection for source one and two respectively, whereas MCCB3 (SW3) provides it for the load. Furthermore, MCCB4 (SW4) and MCCB5 (SW4) allow maintenance bypass for the installation from both sources. The circuit breakers should be provided with Normally Open (NO) and Normally Close (NC) auxiliary contacts for monitoring their status.

![Diagram of bus bar assembly](image)

Figure 4.19: Commercially available STS configuration [33]

These circuit breakers should be connected is such a way with the control logic and also between them to ensure the correct operation of the system, i.e. avoid source paralleling and cross current flowing among the sources. For example, in the case that an SCR of the conductive leg (Source 1) is short circuited then the transfer should be
inhibited and the circuit breaker of the other source SW2 shunt tripped in order to prevent spreading of the fault. Similarly when an SCR from the active leg is detected open then the system must transfer to the inactive leg, shunt the active switch SW1 and inhibit transfer until repair is made.

Additionally, mechanical interlocked devices must be provided for bypass switches (SW4 and SW5) to prevent the operator of closing both at the same time. All transfers to and from bypass shall be MBB transitions for continuity of power to the load equipment. An electrical interlock between bypass of the preferred source and the isolation SW2 from source 2 can also be provided if required by the customer if further security is required.

Regarding protection of semiconductors, most manufacturers tend to overrate the rating of semiconductors in order to achieve higher short circuit capacities as well as I’t ratings and thus achieve fuseless protection. For example, MGE overrates its semiconductor device between 200% and 600% [30]. There are exceptions like Socomec who still uses fuses for semiconductor protection.

A fused-based solution for protecting the semiconductors would be the most adequate one from technical perspective. It would require shunt trippable switch-disconnector-fuses for replacing the MCCBs and providing the required isolation. Considering that ABB Oy is already the world market leader in these kind of products, the use of such device (if developed in the near future) within the STS could give the company an advantageous position if the device is thought to be developed at some point of the future.

A fused-based protection scheme is shown in Figure 4.20. Three high speed power semiconductor fuses should be placed at the input of the static switches for short circuit protection in case of an external fault. When dimensioning fuses for power semiconductors protection some more details must be taken in account than when doing so for normal electrical installations, since the unique characteristics of the semiconductors.
First the fuse should be rated according to the operating voltage and the RMS value of the line current. According to manufacturers, line current has several correction factors according to: (1) ambient temperature, (2) thermal connection, (3) forced air cooling and (4) frequency [32]. Once the rated current of a given fuse has been selected, several characteristics like $I^2t$ ratings, peak currents and arc voltages should be coordinated between the semiconductor and the fuse.

If we refer to Figure 4.20 assuming that 493 A is flowing (as example shown in Figure 4.5) it is possible to define the rated current of the fuse after applying the correction factors. Since the data given on fuse datasheets often refers to values measured at $20^\circ$C and the ambient temperature assumed for the example was $40^\circ$C, a correction factor of 0.9 must be applied. Other correction factors will be neglected for the purpose of this example.

Once a tentative fuse with suitable current and voltage ratings is selected (for this particular case a Bussman size 3 rated at 550 A and 660 V IEC) (see Appendix C) the coordination between the semiconductor and fuse must be done.
The first step is to compare both \( I^t \) ratings of the devices. IEC 60747-6 [46] defines the limiting load integral for thyristors over a period of time of 10 ms (half cycle at 50 Hz) and a temperature junction of 125°C. IEC 60269 [47] defines that electrical characteristics (\( I^2t \)) should be given by the manufacturer (Bussmann provides its information at 20°C, 0.15PF and rated voltage). Correction factors (CF) given by manufacturer can be applied if short circuit power factor (PF) and operation voltage are different. From Busmann’s datasheet, \( I^t \) is 135000 A²s at 660V, since the operation voltage is 440V a correction factor of 0.65 should be applied according to Figure 4.21a. This yields an \( I^t \) of 87500 A²s. From thyristor ABB 5STP 03X6500 datasheet (see Appendix B) \( I^t \) of 101000 A²s is obtained.

![Graphs](image)

**Figure 4.21:** Electrical characteristics provided by fuse manufacturers [32]

Thyristor \( I^t \) is greater than the fuse \( I^t \), therefore and adequate protection is achieved. It is important to remark than even when both devices would have a similar \( I^t \), this could still lead to a safe protection margin since the electrical rating for the fuse are given in the worst conditions. This means a “cold fuse” at 20°C (the fuse temperature under operation is definite higher which leads to a faster burning) and a very low PF [32].

The last factor to take in account is the peak voltage that appears across the fuse when it melts. This voltage should be coordinated with the non-repetitive peak reverse voltage \( V_{RSM} \). For this particular case the operating voltage is 440V, thus from Figure 4.21b it is seen that the peak reverse voltage is around 950V which is easily withstood by the thyristor.
4.5 Other considerations

Besides the three main blocks that were explained in the precedent sections, there are other details that should be taken into account for designing a reliable STS.

STS stands out as an element that assures almost 100% of redundancy for electrical installations; thus, it has to provide redundancy for itself also. Otherwise, it will represent a single point of failure. Redundancy within the STS means that all its control logic and inner circuitry needs to have double or triple independent power supplies feeding different DC buses [33]. Moreover, each board should be fuse protected for avoiding bus bar short circuit.

Isolation of the STS in case of load side faults is also a major concern on the design. STSs are usually equipped with current sensing schemes for measuring the current on the load side [33]. If a fault is produced then the scheme sends a signal to the control logic for blocking the transfer with the aim of preserving the integrity of the alternate source and keeps the fault isolated.

As stated in Chapter 2, SCRs need a minimum current $I_H$ to remain in their conduction state. Therefore, in the case of very low load or no-load conditions there is a risk of malfunction of the STS. The problem is tackled in such a way that an STS internal load is automatically connected when the system detects that the output load is drawing a current below a certain threshold [30].

The STS is a very complex device and even if the modus operandi of its main component blocks have been explained with certain detail, there are still other auxiliary functions that have not been addressed due to the scope of this work. Communication and customer interface software is a wide topic that requires further analysis.

EMC is another broad area that should be carefully analyzed in order to comply with international standards (EN 50091-2). Redundant power supplies and the transients
generated by thyristor operation may interfere beyond standards limits; consequently, EMC filtering must be considered.

Lastly but not least is the enclosure factor. The enclosure should be adequate for the thyristors cooling methods (air-based or liquid-base) and also for the bus bar assembly devices (switch-disconnector-fuses and/or MCCBs). Further, it should provide modularity and easiness of manipulation in the case of need of replacing parts.
Chapter 5
Conclusions

The main conclusion of this work is that the SCR is the most cost-effective solution for a STS design. Even when this study has mainly focused on low voltage STSs, all the concepts and recommendations are also applicable for medium voltage STSs. Furthermore, the study and feasibility of single static switches for different purposes can be also derived from this document as it is one of the components analyzed within the STS design.

The electrical characteristics of SCRs outperform other semiconductors like GTOs and IGCTs. Yet, when GTOs and IGCTs are superior devices that have been derived from the SCR, they cannot provide a considerable advantage on the operation of the STS. GTOs and IGCTs yield the possibility of controlling the turn-off of the device, whereas SCRs don’t. However, this advantage is clearly ousted by their high conduction losses, limited availability and high prices.

The design of the STS was approached dividing it into its three main blocks: (1) static switch, (2) control scheme and (3) bus bar assembly. Each block was carefully depicted addressing solutions and limitations, and also giving design recommendations where applicable according to semiconductor manufacturers’ information, commercially available STSs and literature reviewed. It is clear that a STS is not a simple device and its development, if carried out, would imply several technical challenges. Moreover, the manufacturing of such a device with commercial purposes would require available trained staff for commissioning, and end-user training and support due to the its complex nature.

Finally, the STS looms as a very interesting product within the critical power segment for the next years. Still, when they are already some players established on the market, there are several factors like: upcoming energy crises, aging power infrastructure and an increase in IT and telecom equipment installation; that will drive a growth on the need of
such a device. Emerging economies also should be seen as potential markets since the trend among biggest industries is to move their manufacturing units to those regions.
REFERENCES


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[47] IEC 60269-4 ed. 4.0 (2006). Low-voltage fuses - Part 4: Supplementary requirements for fuse-links for the protection of semiconductor devices

[48] www.sandc.com

[49] www.socomec.com
APPENDIX A

Calculation of $I_{TAV}$ and $I_{RMS}$ for a half sine wave
Figure A.1: Half sine wave

\[ I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_m^2 \sin^2(\omega t) \, dt} = \frac{I_m}{\sqrt{2\pi}} \sqrt{\int_0^{2\pi} \sin^2(\omega t) \, dt} = \frac{I_m}{\sqrt{2\pi}} \sqrt{\int_0^{2\pi} \frac{1}{2} (1 - \cos(2\omega t)) \, dt} = \frac{I_m \sqrt{\pi}}{2\sqrt{\pi}} = \frac{I_m}{2} \]
APPENDIX B

5STP 03X6500 Thyristor Datasheet
$V_{DRM} = 5600 \text{ V}$
$V_{DSM} = 6500 \text{ V}$
$I_{T(\text{AVM})} = 350 \text{ A}$
$I_{T(\text{RMS})} = 550 \text{ A}$
$I_{T(\text{SM})} = 4.5 \times 10^3 \text{ A}$
$V_{(T0)} = 1.2 \text{ V}$
$R_T = 2.3 \text{ m\Omega}$

**Phase Control Thyristor**

**5STP 03X6500**

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate

### Blocking

**Maximum rated values**

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<th>Symbol</th>
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<th>5STP 03X6200</th>
<th>5STP 03X6800</th>
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<td>6200 V</td>
<td>5600 V</td>
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<tr>
<td>$V_{DRM}$, $V_{TSM}$</td>
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<td>5300 V</td>
<td>4000 V</td>
</tr>
<tr>
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<td>6700 V</td>
<td>6300 V</td>
</tr>
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### Characteristic values

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<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward leakage current</td>
<td>$I_{(F)}$</td>
<td>$V_{GEB}, T_A = 125, ^\circ \text{C}$</td>
<td>150</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse leakage current</td>
<td>$I_{(R)}$</td>
<td>$V_{GEB}, T_A = 125, ^\circ \text{C}$</td>
<td>150</td>
<td>mA</td>
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<td></td>
</tr>
</tbody>
</table>

$V_{GEB}$/$V_{RMB}$ are equal to $V_{DSM}$/$V_{TSM}$ values up to $T_A = 110\, ^\circ \text{C}$

### Mechanical data

**Maximum rated values**

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<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>min</th>
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<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mounting force</td>
<td>$F_M$</td>
<td>$\text{Device unclamped}$</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>kN</td>
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<tr>
<td>Acceleration</td>
<td>$a$</td>
<td>$\text{Device unclamped}$</td>
<td>50</td>
<td>m/s²</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Acceleration</td>
<td>$a$</td>
<td>$\text{Device clamped}$</td>
<td>100</td>
<td>m/s²</td>
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### Characteristic values

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<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weight</td>
<td>$m$</td>
<td>$F_M = 10 \text{ kN}, T_A = 25, ^\circ \text{C}$</td>
<td>34.8</td>
<td>35.4</td>
<td>mm</td>
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<tr>
<td>Housing thickness</td>
<td>$H$</td>
<td>$D_a = 10 \text{ mm}$</td>
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<td>mm</td>
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<td>Surface creepage distance</td>
<td>$D_a$</td>
<td>$D_a = 21 \text{ mm}$</td>
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<td>mm</td>
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1) Maximum rated values indicate limits beyond which damage to the device may occur.

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### On-state

**Maximum rated values**

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<tr>
<td>Average on-state current</td>
<td>I_{(AV)}</td>
<td>Half sine wave, T_i = 70 °C</td>
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<td>RMS on-state current</td>
<td>I_{(RMS)}</td>
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<td>550</td>
<td>A</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Peak non-repetitive surge current</td>
<td>I_{SWM}</td>
<td>t_p = 10 ms, T_i = 125 °C, V_o = V_R = 0 V</td>
<td>4.5x10^3</td>
<td>A</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Limiting load integral</td>
<td>I_P</td>
<td></td>
<td>101x10^3</td>
<td>A^2s</td>
<td></td>
<td>A^2s</td>
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<tr>
<td>Peak non-repetitive surge current</td>
<td>I_{(SWM)}</td>
<td>t_p = 8.3 ms, T_i = 125 °C, V_o = V_R = 0 V</td>
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<td>A</td>
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<tr>
<td>Limiting load integral</td>
<td>I_P</td>
<td></td>
<td>98x10^2</td>
<td>A^2s</td>
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### Characteristic values

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<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-state voltage</td>
<td>V_T</td>
<td>I_r = 1000 A, T_i = 125 °C</td>
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<td>V</td>
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<tr>
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<td>V(TH)</td>
<td>I_r = 300 A - 900 A, T_i = 125 °C</td>
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<td>V</td>
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<td>V</td>
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<td>Slope resistance</td>
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<td>2.3</td>
<td>mΩ</td>
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<td>mΩ</td>
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<td>Holding current</td>
<td>I_H</td>
<td>T_i = 25 °C</td>
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<td>mA</td>
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<td>mA</td>
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<tr>
<td></td>
<td></td>
<td>T_i = 125 °C</td>
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<td>mA</td>
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<td>mA</td>
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<tr>
<td>Latching current</td>
<td>I_L</td>
<td>T_i = 25 °C</td>
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<td>mA</td>
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<td>mA</td>
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<tr>
<td></td>
<td></td>
<td>T_i = 125 °C</td>
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### Switching

**Maximum rated values**

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<th>max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Critical rate of rise of on-state current</td>
<td>dv/dt_{crit}</td>
<td>T_i = 125 °C, I_RMS = 1000 A, f = 50 Hz</td>
<td>100</td>
<td>A/μs</td>
<td></td>
<td>A/μs</td>
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<tr>
<td>Critical rate of rise of on-state current</td>
<td>dv/dt_{crit}</td>
<td>V_o ≥ 3750 V, I_RMS = 2 A, μs = 0.5μs, f = 1 Hz</td>
<td>1000</td>
<td>A/μs</td>
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<td>A/μs</td>
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<tr>
<td>Circuit-commutated turn-off time</td>
<td>t_q</td>
<td>T_i = 125 °C, I_RMS = 1000 A, V_o ≥ 200 V, dv/dt = -1 A/μs, V_o = 0.67 V_RMS</td>
<td>700</td>
<td>μs</td>
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<td>μs</td>
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### Characteristic values

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<th>max</th>
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<tr>
<td>Recovery charge</td>
<td>Q_r</td>
<td>T_i = 125 °C, I_RMS = 1000 A, V_o ≥ 200 V, dv/dt = -1 A/μs, V_o = 0.67 V_RMS</td>
<td>900</td>
<td>μAs</td>
<td>2000</td>
<td>μAs</td>
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<tr>
<td>Gate turn-on delay time</td>
<td>t_F</td>
<td>V_o = 0.4 V_RMS, I_RMS = 2 A, μs = 0.5 μs, T_i = 25 °C</td>
<td>3</td>
<td>μs</td>
<td></td>
<td>μs</td>
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### Triggering

**Maximum rated values**

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<tr>
<th>Parameter</th>
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<th>max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Peak forward gate voltage</td>
<td>$V_{FGM}$</td>
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<td></td>
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<td>12</td>
<td>V</td>
</tr>
<tr>
<td>Peak forward gate current</td>
<td>$I_{FGM}$</td>
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<td>10</td>
<td>A</td>
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<tr>
<td>Peak reverse gate voltage</td>
<td>$V_{RSM}$</td>
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<td>10</td>
<td>V</td>
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<tr>
<td>Average gate power loss</td>
<td>$P_{G(AV)}$</td>
<td>see Fig. 9</td>
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**Characteristic values**

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<th>max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Gate-trigger voltage</td>
<td>$V_{GT}$</td>
<td>$T_J = 25^\circ C$</td>
<td>2.6</td>
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<td>V</td>
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<td>Gate-trigger current</td>
<td>$I_{GT}$</td>
<td>$T_J = 25^\circ C$</td>
<td>400</td>
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<td></td>
<td>mA</td>
</tr>
<tr>
<td>Gate non-trigger voltage</td>
<td>$V_{ND}$</td>
<td>$V_D = 0.4 \times V_{FDM}$, $T_J = 125^\circ C$</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Gate non-trigger current</td>
<td>$I_{SD}$</td>
<td>$V_D = 0.4 \times V_{FDM}$, $T_J = 125^\circ C$</td>
<td>10</td>
<td></td>
<td></td>
<td>mA</td>
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</table>

### Thermal

**Maximum rated values**

<table>
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<tr>
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<th>Symbol</th>
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<th>max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Operating junction temperature range</td>
<td>$T_J$</td>
<td></td>
<td></td>
<td></td>
<td>125</td>
<td>°C</td>
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<tr>
<td>Storage temperature range</td>
<td>$T_{op}$</td>
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<td>-40</td>
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<td>140</td>
<td>°C</td>
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**Characteristic values**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal resistance junction to case</td>
<td>$R_{th(j-c)}$</td>
<td>Double-side cooled $F_m = 8...12$ kN</td>
<td>45</td>
<td></td>
<td></td>
<td>K/kW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Anode-side cooled $F_m = 8...12$ kN</td>
<td>85</td>
<td></td>
<td></td>
<td>K/kW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cathode-side cooled $F_m = 8...12$ kN</td>
<td>95</td>
<td></td>
<td></td>
<td>K/kW</td>
</tr>
<tr>
<td>Thermal resistance case to heatsink</td>
<td>$R_{th(c-h)}$</td>
<td>Double-side cooled $F_m = 8...12$ kN</td>
<td>7.5</td>
<td></td>
<td></td>
<td>K/kW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single-side cooled $F_m = 8...12$ kN</td>
<td>15</td>
<td></td>
<td></td>
<td>K/kW</td>
</tr>
</tbody>
</table>

#### Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_{th i} (1 - e^{-t/\tau_i})$$

<table>
<thead>
<tr>
<th>$R_{th i} (K/kW)$</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>26.070</td>
<td>12.160</td>
<td>3.370</td>
<td>3.100</td>
</tr>
</tbody>
</table>

| $\tau_i (s)$ | 0.0430 | 0.0812 | 0.0151 | 0.0075 |

![Fig. 1 Transient thermal impedance junction-to-case.](image)
Fig. 2  Max. on-state voltage characteristics.

Fig. 3  On-state characteristics, 
$T_J = 125^\circ C$, 16ms half sine

Fig. 4  On-state power dissipation vs. mean on-state current. Turn-on losses excluded.

Fig. 5  Max. permissible case temperature vs. mean on-state current.
Fig. 12 Device Outline Drawing.

Related application notes:

<table>
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<th>Doc. Nr</th>
<th>Title</th>
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<tr>
<td>55YA2020</td>
<td>Design of RC-Smusher for Phase Control Applications</td>
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<tr>
<td>55YA2034</td>
<td>Gate-drive Recommendations for PCT’s</td>
</tr>
<tr>
<td>55YA 2036</td>
<td>Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors</td>
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</table>

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Internet [www.abb.com/semiconductors](http://www.abb.com/semiconductors)
APPENDIX C

Fuse Datasheet
<table>
<thead>
<tr>
<th>Size</th>
<th>Current Rating</th>
<th>15kA @ 500V</th>
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<tbody>
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<td>50</td>
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<td>50</td>
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Square Body Curves

Size 1*: 660V (40-630)A
Time-Current Curve

Size 1: 660V (200-900)A
Time-Current Curve

Peak Let-Through Curve

Peak Let-Through Curve

900 amp fuse is derated to 550V (IEC).

For complete specification data, visit our Web site at www.bussmann.com
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