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SIMULATION-ENHANCED QUALIFICATION OF PRINTED WIRING BOARD -LEVEL RELIABILITY IN MICROELECTRONICS

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ABSTRACT

In this thesis a new method was developed for relating PWB-level reliability test results to service environment performance, with the emphasis on solder joint reliability. The method consists of both experimental testing and virtual computer simulations. Realistic computer simulations demand the use of appropriate material models and correctly determined material parameters. For this purpose, a new materials testing method, the grooved-lap test, was developed for accurate assessment of solder deformation properties, especially in the case of small solder volumes. The benefits of the new testing method, in comparison to the conventional ones, was demonstrated with the help of finite-element simulations as well as analytically. It was shown by using the new grooved-lap test and uniaxial tests that under thermal stress conditions Sn-based solders exhibit various rate-controlling deformation mechanisms, such as dislocation climb controlled and dislocation viscous glide controlled creep. The rate-controlling deformation mechanisms were assessed for Sn2Ag0.5Cu, Sn3.4Ag0.8Cu, and Sn4Ag0.5Cu solders with the grooved-lap test. Furthermore, the measured data were implemented into a constitutive model, which can be used in finite-element simulation programs. This procedure enables the utilization of the life-prediction method for evaluating and developing new hardware components, being assembled with Pb-free alloys.

PREFACE

This work has been conducted under the guidance of Professor Jorma Kivilahti, to whom I express my gratitude for his constant support, and patience, during the several years that this project has been ongoing. I admire his broad and indepth knowledge, not only on technology, but in cultural and philosophical aspects as well. I have truly enjoyed our numerous discussions and they have been very important for my learning and motivation. I must admit that without his encouragement and persistence I would not have completed this work.

During these years I have worked with several companies; Centrum fuer Mikroverbindungstechnik and Fraunhover ISiT in Germany, Helsinki University of Technology, Nokia in Finland and in the US, and with Instituto Nokia de Tecnologia in Brazil. Each of these has provided me excellent opportunities and facilities to conduct this research. My stay in Germany was in part funded by a scholarship from the Academy of Finland, for which I express my sincere thanks. I want to thank my coauthors for sharing their knowledge and time and I am particularly thankful for Dr. Ephraim Suhir for his interest in my work and for his support.

A great inspiration for me has been, and is, my dear mother, who recently completed a Masters degree, and is currently working on her second book. Her example of the Nokia value “Continuous Learning” has been an invaluable motivator for me during this Thesis work.

The greatest thanks I owe to my loving wife and our wonderful children for their understanding, support, and encouragement.

Tuusula, November, 2008

Tommi Reinikainen

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LIST OF PUBLICATIONS

Appendix 1. V. Pennanen, M. Tammenmaa, T. Reinikainen, J. Zhu, and W. Lin, "TBGA Reliability in Telecom Environment", *Soldering & Surface Mount Technology*, **12**, 2, (2000) pp. 42-46.

Appendix 2. T. Reinikainen, F.W. Wulff, W. Kolbe and T. Ahrens, "A New Method to Determine Crack Shape and Size in Solder Joints", *ASME Journal of Electronic Packaging*, **117**, 4, (1995) pp. 266-269.

Appendix 3. T. Reinikainen, M. Poech, M. Krumm and J. K. Kivilahti, "A Finite-element and Experimental Analysis of Stress Distribution in Various Shear Tests for Solder Joints", *ASME Journal of Electronic Packaging*, **120**, 1, (1998), pp. 106-113.

Appendix 4. E. Suhir and T. Reinikainen, "On a Paradoxical Situation Related to Lap-shear Joints; Could Transverse Grooves in the Adherents Reduce the Interfacial Stresses", *Journal of Physics D: Applied Physics*, **41,** (2008), 115505.

Appendix 5. T. Reinikainen and J. K. Kivilahti, "Deformation Behaviour of Dilute SnBi(0.5…6at%) Solid Solutions", *Metallurgical and Materials Transactions A*, **30**, 1, (1999), pp. 123-132.

Appendix 6. T. Reinikainen, P. Marjamäki, and J. K. Kivilahti, "Deformation Characteristics and Microstructure Evolution of SnAgCu Solder Joints", *Proceedings of the 6th International Conference on Thermal, Mechanical, and Multiphysics Simulations and Experiments in Micro-Electronics and Micro-Systems EuroSimE*, Berlin, Germany, April 18-20, 2005, IEEE/CPMT, pp. 91-98.

AUTHOR'S CONTRIBUTION

In Publication 1 the author developed the method for assessing the acceleration factors, conducted the finite-element simulations, and co-authored the paper related to these subjects. The co-authors V. Pennanen and M. Tammenmaa initiated the study and carried out the experimental testing, and the co-authors J. Zhu and W. Lin brought in the global-local simulation method. The first three authors were responsible for writing the paper. In Publication 2 the author developed a new method of building the 3D model of the crack front, carried out all the failure analysis, and was the primary author of the paper. In Publication 3 the author conducted all the simulations and executed the experimentals, except the optical deformation measurements, which were carried out together with M. Krumm. In Publication 4 the author developed the concept for the analyses and co-authored the paper together with the E. Suhir, who did the mathematical modeling of the new shear test method. In Publication 5 the author did all the experimental and theoretical work and wrote the paper with the co-author J. K. Kivilahti. In Publication 6 the author carried out the assessment of the solder deformation mechanisms, did all the microscopic analyses, and did the assessment of the Anand's model parameters together with co-author P. Marjamaki, who conducted the mechanical tests. All the authors were responsible for writing the paper.

1. INTRODUCTION

It can be estimated that only in the mobile phone industry more than 5 billion individual solder joints are produced each day. This estimate is based on the current mobile phone market size, and on the fact that today's mobile phone has approximately from 1500 to over 3000 solder joints on it's printed wiring board (PWB). Soldering is the primary method to connect individual components such as memory chips and resistors or capacitors on the PWB in the microelectronics industry in general. In addition to mobile phones and other consumer electronic equipment, microelectronic systems are controlling and monitoring nearly ubiquitously our daily living environment, related to almost everything from transportation, communication and health care to manufacturing and energy production. The solder joints form both the electrical and mechanical connections between the components and the PWB. I.e. the electrical signals run through the solder medium, but also the solder physically attaches the components on the PWB. It is clear that a mechanical detachment or a fracture in any of the thousands, or tens of thousands (depending on the application) of solder joints on the PWB results in electrical discontinuity in the circuit and most probably leads to the failure of the entire system that the electronics is controlling or monitoring.

Based on the description above it can be proposed that in terms of units produced per day, the solder joint is the most important structural element in the world today. This is somewhat paradoxical situation because of two reasons. Firstly, due to a historical background and due to the infrastructure of the current microelectronics manufacturing industry, the solder joints are primarily formed by tin-based alloys and tin (Sn) is well known to have poor mechanical properties. For example, the tensile strength of tin is on the order of few tens of MPa, whereas that of wrought copper can be several hundreds of MPa, and that of steel can be several thousands of MPa. Secondly, the mechanical properties and deformation behaviour of tin and its alloys are not well known and the underlying physics is not well understood. Comparing to another important structural material, steel, the research done on the mechanical properties of tin and its alloys is very limited. The understanding of the microstructure of iron and understanding the positive effects that can be achieved on it's mechanical properties by adding various alloying elements and by conducting various heat

treatments, has lead to the systematic development of thousands of different steel alloys with tailored properties for specific applications. The situation with tin-based solders is quite contrary. For example, it has been noted that several orders of magnitude difference in the mechanical strength of eutectic tin-lead solder have been reported by various researchers in the literature [1]. This can be only attributed to the very limited understanding of the effect of the tin-alloy microstructure on its mechanical properties and also to not understanding the effect of test conditions on the measurement results.

Electronic packaging, i.e. integration of the active and passive components etc. with the complete electronic system, can in general be divided in three levels. The different levels of packaging are typically fabricated using different manufacturing technologies, and also often in practice done by different manufacturers. The term 1^{st}-level packaging relates to the technologies and activities of integrating the semiconductor chip into a protective housing, which can then be practically handled in further manufacturing steps. By term 2^{nd}-level packaging is meant the manufacturing technologies in which the various active and passive components are assembled on printed wiring boards. Today, soldering the components on the PWB by using surface-mount technology (SMT), is the primary method for 2^{nd}-level packaging. 3^{rd}-level packaging consists of the methods and technologies of attaching the assembled PWB(s) or other modules to the housing of the electronic system.

According to the famous Moore's law, which was first stated in 1965, the density of transistors on a semiconductor chip doubles every two years [2]. This may in part be a self-fulfilling prophecy, but nevertheless this prediction has been surprisingly accurate now for over 40 years. This trend can still be expected to continue at least 15-20 years before the laws of physics, i.e. dimensions reaching atomic measures, may become a restricting factor for further miniaturization. Because of this there is a continuous trend in microelectronics of increasing the number of solder joints of IC (integrated circuit) packages. For saving the printed wiring board real estate, and for reducing electrical losses, the distance, i.e. pitch, between adjacent solder interconnects is continuously diminishing [3]. For example, majority of the ball-grid array (BGA) packages in high-end mobile phones currently have pitch of 0.5 mm, while the state-of-the art technology is 0.4 mm, with plans already existing for implementing 0.3 mm

pitch components. This continuous reduction of physical dimensions and increasing functionality on the PWB naturally increases the concern of interconnect reliability, specifically related to 2nd-level packaging. As mentioned earlier, tin-based solders have very low mechanical strength, compared to most other metals and even to many polymers. Because of this, it can in general be expected that the solder joint is the weakest link on the PWB, in terms of mechanical reliability. As a rule-of-thumb it can be stated that the mechanical strength of all other PWB-level interconnect and packaging technologies must exceed the mechanical strength of the solder joints on PWB in the final application environment. Consequently, for example in microelectronic equipment with long service-life, over 15 – 20 years, the most common failure mechanism is solder joint fatigue due to thermal-mechanical stresses.

The reliability of solder interconnects has been under extensive research since the introduction of the surface-mount technology (SMT) in the eighties. This research effort has further been intensified since the announcement of the Restrictions on Hazardous Substances (RoHS) directive in the electronics industry, which was implemented July 1st 2006 [4]. In the RoHS directive the use of the metal lead (Pb) is banned, among other materials, due to its toxicity to humans and due to the problems it causes to the environment. Lead is a major constituent of the eutectic SnPb solder, which until RoHS was the defacto alloy used in microelectronics. Today, the most widely used Pb-free solders are based on the Tin-Silver-Copper near-eutectic system (so called SAC alloy), but extensive research is still on-going to find new solder materials with improved mechanical and chemical properties.

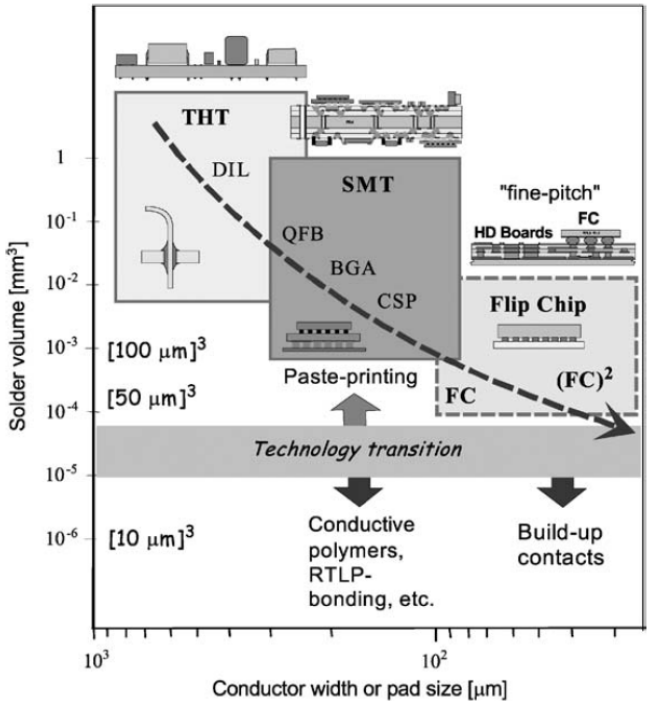


Figure 1. Impact of miniaturization on electronics production [3].

With the diminishing solder joint size in state-of-the art microelectronic systems, such as mobile communication devices, a new aspect must be taken into account when analyzing solder joint reliability. The size of the individual grains in the solidified solder starts soon be of the same size as the whole solder joint itself [5, 61]. The current solder alloys are primarily based on tin, which is a metal that has mechanically anisotropic crystal structure [6, 7]. In practice this can mean that the individual solder joints on, for example, a BGA component have significantly different mechanical properties between each other, depending on the orientation of the one or two tin grains, which form the solder joint. This can lead to significant difficulties in the design-for-reliability of 2nd level packaging interconnects, unless that variation is well understood and can be controlled. However, currently there is no reliable information of the severity of this risk, nor how to control this potentially significant variation. In part, this thesis will provide methods and tools for analyzing solder materials in small

dimensions, and hence will help in mitigating the risks related to further miniaturization of microelectronics.

In this work is demonstrated a methodology for the qualification of new HW technologies for microelectronics, with the primary focus on improving the accuracy of solder joint reliability simulation. For the purpose of optimizing both the accuracy of the results and the time spent for qualifying new technologies, and hence shortening time-to-market, the methodology takes the benefit of both numerical simulations and experimental testing. In the beginning of the thesis a work-flow is presented, which evaluates if the different reliability tests for the new components and modules are relevant, considering the service environment requirements of the final products. Then, depending on the design-life of a product, the load levels and durability requirements for the component or module level qualification tests are set so that the expected field reliability will be achieved. Some applications of this methodology are presented in Publication 1. For developing accurate reliability simulation methods, it is important to understand the associated failure mechanisms. This is the focus in Publication 2, where we study in detail the fatigue crack propagation in the solder joint of an SMT component.

As stated before, the solder joint should be the weakest link in terms of mechanical reliability on the printed wiring board. For this reason in this work special attention is paid to the solder joint reliability analysis. As also stated before, a very large scatter exists in the literature regarding the eutectic SnPb solder deformation properties. This can be attributed to limited knowledge of the effect of solder microstructure and the test conditions on the stress-strain behaviour of the solder materials. It is important that the temperature and strain-rate dependent stress-strain relations are correctly assessed, for this data to be utilized with good confidence in reliability simulations. Hence, first several common test methods for assessing solder deformation properties are analyzed in terms of their suitability for the purpose (Publication 3). Moreover, in Publications 3 and 4 a new test method is developed, which yields to significantly improved test results, compared to any of the conventional test methods. In Publication 3 the benefits of the new test method is presented by numerical simulations and by practical experiments. In Publication 4 an analytical model is developed, which explains the theory behind the new test method. For accurately

simulating solder joint deformation and fatigue, it is essential to understand the various deformation mechanisms that may be present during typical loading conditions. These are analyzed in Publication 5. Finally, in Publication 6 the deformation mechanisms occurring in a SAC solder are assessed, and the constants for a constitutive model are determined, which allows for conducting the developed qualification method for the currently mostly used solder in the microelectronics industry.

2. QUALIFICATION METHODOLOGY FOR MICROELECTRONICS

New hard-ware (HW) technologies are constantly introduced in the microelectronics industry to enable better performance, reduced size, and lower cost. To facilitate the requirements of continuously shortening product development cycles, the qualification of the new technologies must be conducted in a very time and cost effective manner [8]. The new technologies must meet the requirements set by the product service environment and the intended service life. However, these requirements should not be excessively exceeded. Should the reliability requirements not be met, the high number of field-failures would lead to high warranty costs and dissatisfaction of the customer. On the other hand, making the new technologies excessively durable might significantly increase the cost of the new devices. Both of these described situations are not acceptable in today's highly competitive markets. Hence, it is essential that qualification procedures are established, which guarantee that new HW technologies meet or exceed customer expectations, and can be offered at the right price.

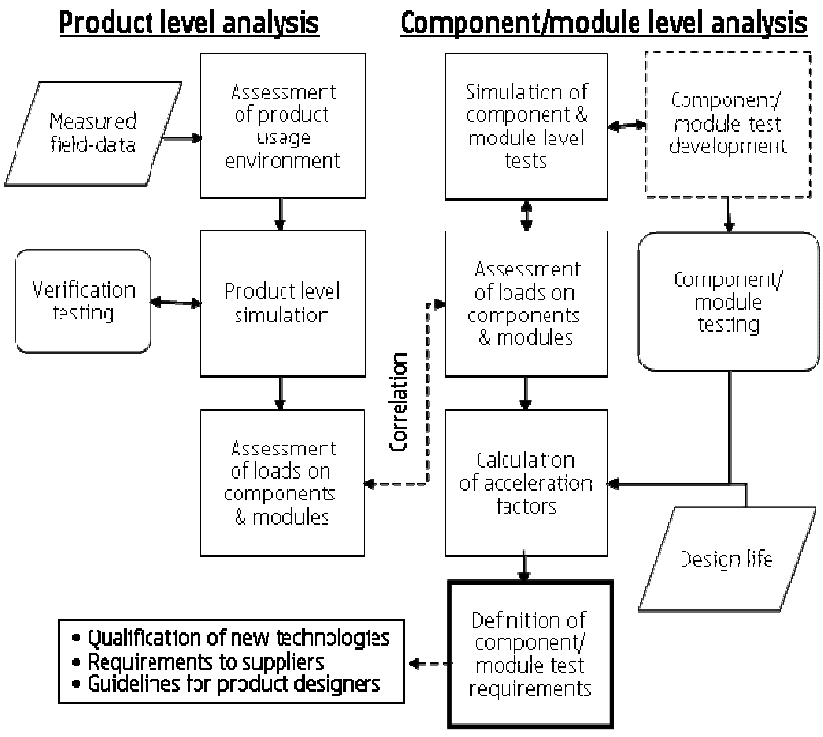


Figure 2. Flow-chart of the qualification procedure for ensuring reliability of new HW components and modules.

2.1 Work-flow of qualification of microelectronic components and modules

The qualification of new HW technologies regarding their reliability performance is today conducted most efficiently by combining physical testing and finite-element simulations [9, 10, 11, 12]. It has also been recently claimed that if the simulation results show wide enough margin to the acceptance limits (e.g. number of cycles to failure), then only the simulations might be sufficient to ensure the product field reliability [13]. While this can be considered as the ultimate target for the method development in design-for-reliability, in this work we prefer to focus on a methodology that combines testing with computer simulations.

Various load types such as thermal, humidity, static mechanical, or mechanical shock and vibration loads can stress electronics during the service life of a product. Thermal loads may originate from the ambient temperature, or can be generated due to the

operation of the equipment itself. Thermal loads will lead to thermal-mechanical stresses due to thermal gradients, or due to the difference in the coefficient of thermal expansion (CTE) of the various associated materials [14, 15, 16, 17, 18]. Cyclic thermal-mechanical loads can lead to fatigue failure at the various interconnects or material interfaces of a microelectronic assembly. Humidity can absorb particularly in the polymeric materials and that can facilitate corrosion or electromigration. Either of these phenomena would affect detrimentally the reliability of an electronic system. Static or quasi-static mechanical loading can be imposed on the printed wiring board when the whole device is bent, or for example in a situation when key pad pressing leads to direct loading on the PWB [19, 20, 21]. Mechanical vibration commonly affects electronic products particularly during transportation, or constantly during the life-time of a microelectronic product that is used for example in vehicles or aircrafts. If mechanical vibration exites some of the lower natural frequencies of the PWB, the component interconnects are at the risk of a quick wear-out due to mechanical fatigue. Particularly portable consumer electronics are often dropped during their normal service life and this creates very high shock and vibration loads on the PWB that can be of several thousands gs. Such shock and vibration loads can lead to a sudden over-stress failure, or to a fatigue failure of the electrical interconnects in the system [22, 23, 24].

Figure 2 depicts a qualification flow-chart for assessing the PWB-level requirements of components or modules in a microelectronic product. The methodology consists essentially of two parts; 1) Product level analysis, where the service loads of the final product are estimated, and 2) Component/module level analysis, where appropriate component and module reliability tests are developed and conducted, based on the service loads and the service life-time requirements. It is important that a good correlation exists between the service loads and the test loads, as depicted in Figure 2. In the product level analysis, on the left side of the chart, are estimated the load types and load levels that would be stressing the various HW components and modules during usage of the product. Such analysis can be conducted purely by simulations, or by a combination of simulations and physical testing. For example, the thermal loads that are imposed on the product can either be measured by using thermo-couples, or

can be estimated by simulations using the finite-element method or by using methods based on computing-fluid-dynamics (CFD).

Once the product level assessment has been completed, the obtained loads are transferred on the components of which's' reliability is to be estimated. This phase is typically done by using the before mentioned numerical simulation tools, since it is generally not possible to obtain the needed very localized loading conditions experimentally. In this procedure the 'global' product-level loads are transferred to a separate, more detailed, 'local' component simulation model by defining the respective boundary conditions, such as the temperature profiles [17].

The right-hand side of the flow-chart in Figure 2 consists of developing appropriate component- and module-level reliability tests, simulating and conducting the tests, and assessing the component reliability, using for example the Weibull distribution [25]. Further, the results can be used for setting reliability requirements to component suppliers, or defining design guidelines to product design engineers. When developing the component- and module-level reliability tests, it is important that loads imposed by the test are similar to the loads that are imposed by the usage of the product. This is best ensured by comparing the simulation results between the service environment and the test conditions. For expediting the testing, the test-loads are higher than the service loads to accelerate the occurrence of failures, and the field-reliability is estimated by using acceleration factors. However, it is essential that the failure mechanisms are exactly the same in the test as in the field conditions [26]. Otherwise the test results have no relation to reality and the results are only misleading.

By utilizing the simulation methodology presented in Chapter 4 it is technically possible to estimate the field-life reliability based only on finite-element simulations. However, when analyzing new HW technologies, with new technology solutions and potentially with new materials, there is a risk that not all the relevant details of new structures are adequately captured by the simulation model, for example due to lack of accurate material data. For this reason it is proposed in Figure 2 that when qualifying new technologies, the computer simulations are used primarily for assessing the acceleration factor between the test and the field load conditions. If there is some deviation between test and simulation results, for example due to inaccurate material

data, that should not significantly affect the accuracy of the estimated acceleration factor, if the solder deformation mechanisms are correctly considered in the simulation model.

As an example, in a telecom base station the temperature can be estimated to vary between +10 and +45 ºC or 0 and +60 ºC, depending on its operation and outside temperature [12]. However, thermal cycling can be conducted with temperature extremes -40 ºC and + 125 ºC and hence obtain the reliability test results faster. This is because the failure mechanism, solder joint fatigue due to creep, is the same in both loading conditions. The temperature limits for this widely used test profile are based on the temperature dependent mechanical behaviour of the solder and printed wiring board materials. The lower limit, -40 ºC, is the temperature where creep deformation starts becoming active with the eutectic SnPb solder (homologous temperature above 0.5). The upper limit, +125 ºC, is just below the glass-transition temperature of the epoxy resin in the common printed wiring board material FR4. Hence, this temperature range provides the maximum acceleration for creep based fatigue of the eutectic SnPb solder on PWB, without changing the deformation mechanisms, or introducing other discontinuities (T_g-temperature).

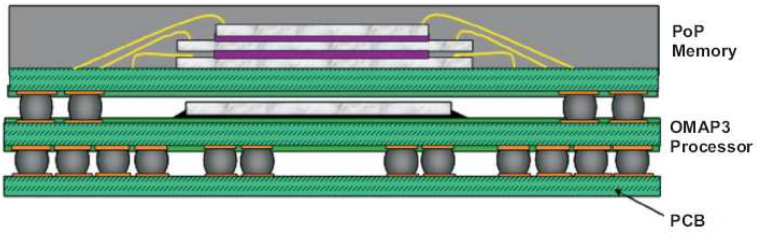


Figure 3. A stacked BGA package containing a processor chip and a stack of memory chips [29].

Today's microelectronic systems are becoming increasingly complex, from the perspective of mechanical and materials integration (Figure 3). Area-array components can have thousands of solder interconnects connecting them to the printed wiring board, the IC packages can contain multiple stacked IC-chips, chips are thinned to enable lower profile components, and the high-density circuit boards have various build-up layers and utilize μ-via technology to enable routing of the conductor traces

[27, 28]. With the 0.4 mm pitch ball-grid array (BGA) technology the adjacent solder joints have less than 150 μm distance from each other, and the higher density technology with 0.3 mm is already under development [29, 30]. To tackle the various, sometimes contradictory, design requirements, numerical optimization is emerging as an efficient tool and is increasingly used in the development of new components and modules [31, 32, 33, 34, 35].

3. CHARACTERIZATION OF SOLDER MATERIAL PROPERTIES

As is described in Chapter 4.1, several deformation mechanisms can be active in solder joints, depending on the solder composition, grain size, temperature, stress level etc. For being able to accurately predict solder joint reliability by simulations, it is important that all these factors are taken into account, when assessing the constitutive relations of the solder alloys. Otherwise the stress-strain (or creep) relations can not be accurately predicted, and the acceleration factors between the test and service conditions are not valid, and the analysis results will be greatly misleading.

In general, the uniaxial tensile test, either with constant rate of deformation, or with constant stress, is, due to its simplicity, the most accurate test method for assessing the deformation behaviour of metals. However, regarding solder alloys there are some aspects, which make the shear test more suitable for the purpose. As mentioned before, solder deformation is very dependent on the grain size and morphology. It is difficult to control these parameters accurately with the relatively large tensile test samples, but can be easily done with shear test samples by ensuring that the thermal mass of the sample is close to that of actual solder joints, and that the temperature profile of the soldering process is similar to that of the reflow profile of actual microelectronic assemblies. Secondly, while soldering components to the printed wiring board, the molten solder typically dissolves some material from the component terminations and the soldering pads on the PWB. The dissolved materials can be considered as additional alloying elements in the solder, and can significantly affect its mechanical properties after solidification. It is very difficult to introduce such additional alloying elements in the uniaxial tensile test samples by the usual sample preparation methods. However, this effect is automatically taken into account in the shear test, if the interface materials of the shear test samples are the same as in a real

microelectronics application. Thirdly, with the diminishing size of microelectronic solder joints, the grain size in the solder can be the size of the actual joint. This can have a significant effect on the solder deformation, since the rigid interfaces may constrain the plastic or creep deformation that occurs along the active slip planes of the solder material, and also because the tetragonal crystal structure of β-tin may have very anisotropic deformation characteristics. Although the significance and detailed physics behind these phenomenona are yet unknown, they can be indirectly taken into account with the shear test, by ensuring that the sample dimensions are similar to real microelectronic solder joints.

3.1 The new grooved-lap shear test

Several various types of test geometries have been proposed for shear testing of adhesives, solders, and welding structures, such as the single-lap joint, the double-lap joint, and the ring-and-plug test [36, 37]. However, when analyzing these in more detail, for example by the finite-element method, it is evident that state of stress can be very non-uniform, and such tests have also very high normal stress components near the joint edges. For assessing the stress-strain relation of any material, it is essential to know the state of stress, whether shear or uniaxial, and the conventional shear tests are not suitable for this. For welding structures, the Iosipescu test yields to a significantly more uniform shear stress distribution in the weld area, and the new grooved-lap joint has been developed for solder joints, with similar benefits [38, 36].

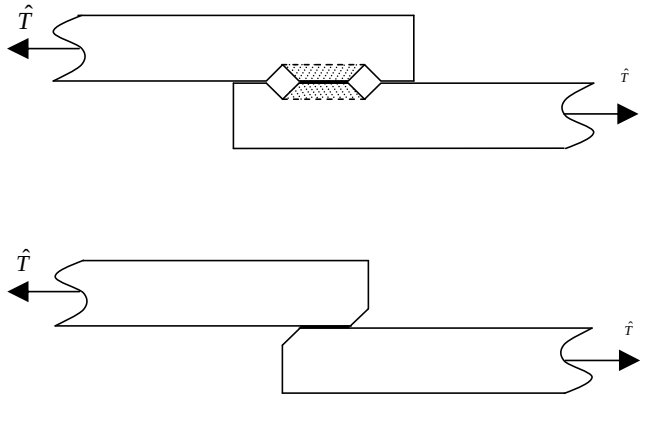


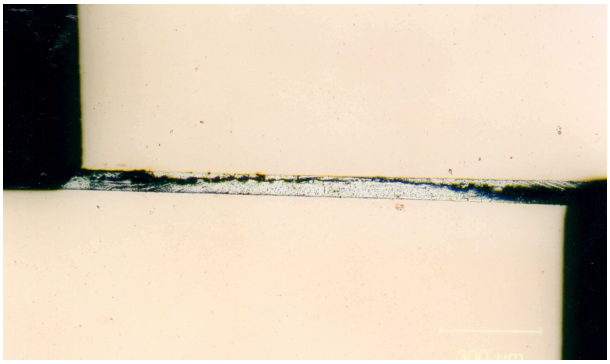
Figure 4. Schematic of the a) Grooved-lap test and b) Single-lap test [42].

Figure 4 shows a schematic of the single-lap joint and the new grooved-lap joint. The grooved-lap joint is essentially a single-lap joint, with transverse grooves machined in the pins, which separate the solder joint area from the rest of the pins. The finite-element analyses prove the practical benefits of the grooved-lap test over the other shear tests, but they do not explain why the test has such improved properties [36, 37]. The significantly more uniform stress distribution of the grooved-lap test than the single-lap test can also been demonstrated experimentally, as depicted in Figure 5. The figure shows optical images of the cross section of the two shear tests after few percent of deformation. The single-lap joint in Figure 5a exhibits extensive deformation at the edges of the joint, due to the non-uniform shear stress distribution and the high normal stress components. The grooved-lap test in the Figure 5b shows the boundaries of the individual solder grains with uniform appearance through the joint. The grain boundaries become visible optically due to surface relief, which is accommodating part of the mechanical deformation.

3.2 Analytical model of the grooved-lap test

An analytical model has been developed for comparing the grooved-lap test to the single-lap test [39, 40, 42]. Although the benefits of the grooved lap test are much more significant regarding the normal stress components, for the sake of simplicity here is presented the analysis of the shear stress distribution. Details of the analysis of the normal stress components are presented in reference [39].

a)



b)

Figure 5. Optical image of (a) a single-lap joint and (b) a grooved-lap joint shear tests after few percentage of deformation. In the single-lap joint deformation concentrates at the edges, whereas in the grooved-lap joint deformation is uniform through the joint.

A lap shear joint with transverse grooves in the pins is schematically shown in Figure 4a. The main difference between this joint and the conventional joint in Figure 4b is that the shaded areas in the pins of the grooved joint are not subjected to the direct action of the external tensile forces, $\hat{T}$. This circumstance 'excludes' these portions of the pins from being parts of the bonded components that experience direct action of the external forces and includes these portions into the bonding structure instead. Although the Young's modulus of the pin materials might be high, the increase in the thicknesses of the bonding structure, if the grooves are sufficiently deep, might be significant. The resulting increase in the interfacial compliance of the joint might be appreciable, and could exceed the interfacial compliance of the thin solder layer,

despite the low modulus of the bonding material. Thus, the grooves can add more compliance to the bonding structure. In the numerical example in Chapter 3.2.3 is demonstrated that this positive effect can overwhelm appreciably the negative effect of 'thinning down', also because of the grooves, the pins: thinner pins are more compliant with respect to tension. As is known, the lowest interfacial stresses take place in assemblies with stiff pins and compliant adhesives [41]. In this analysis the structure in Figure 4a is idealized by an equivalent model shown in Figure 6. It is assumed that the grooves are introduced at the very ends of the solder layer, so that the bonding structure has a predetermined length defined by the distance between the grooves.

3.2.1 Analysis of the shear stress

In the problem in question, the interfacial shear stress $\tau_0(x)$, must be symmetric with respect to the mid-cross-section of the joint. The stress should therefore be of the form:

$$\tau_0(x) = C\cosh kx, \tag{1}$$

where k is the parameter of the interfacial shearing stress, and C is the shearing stress at the mid-cross-section. In Figure 6, the forces in the cross-sections of the upper component #1, and the lower component #2, can be found by integration as elaborated in [42], and it can be shown that,

$$\tau_0(x) = \frac{k\hat{T}}{2}\frac{\cosh kx}{\sinh ka}. \tag{2}$$

For very long joints this formula yields:

$$\tau_0(x) = \frac{k\hat{T}}{2}e^{-k(a-x)}, \tag{3}$$

i.e., the interfacial shearing stress concentrates at the joint's ends, and for very short joints the formula yields

$$\tau_0(x) = \tau_0 = \frac{\hat{T}}{2a}, \tag{4}$$

so that the interfacial shearing stress is uniformly distributed over the joint length. The formula (2) results in the following stress at the joint ends:

$$\tau_0(\pm a) = \frac{k\hat{T}}{2}\coth ka \quad \text{, and} \quad \tau_0(0) = \frac{k\hat{T}}{2}\frac{1}{\sinh ka}. \tag{5}$$

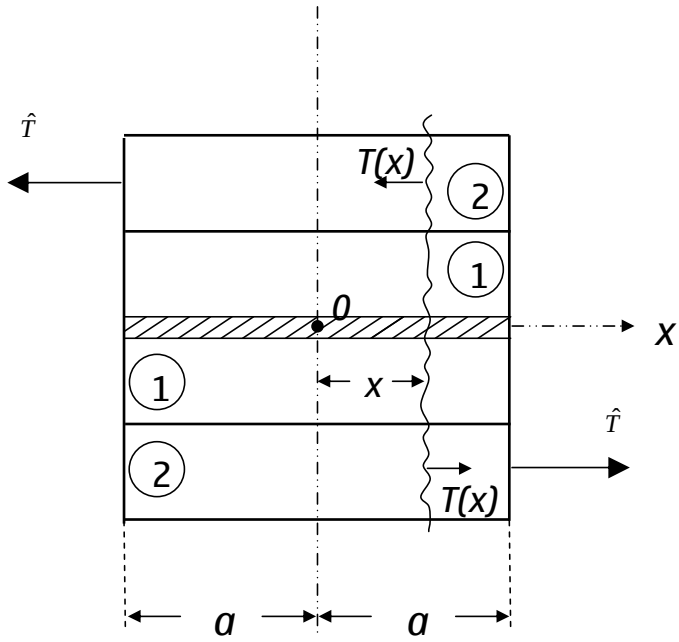


Figure 6. Idealized lap shear joint structure. Portions of the pins experience direct actions of the tensile forces $\hat{T}$. The shaded area is solder [42].

3.2.2 Interfacial compliance and parameter of the interfacial shear stress

In [42] it is shown that the interfacial compliance of the pins is

$$\kappa = \frac{3-\nu}{\pi}\frac{2a}{G}. \tag{6}$$

Further, in [42] it is shown that the interfacial compliance of the materials of the bonding structure (solder and the portions of the pins between the grooves in the grooved joints), with thickness of h, can be derived as

$$\kappa = \frac{u}{\tau_0} = \frac{h}{G} \tag{7}$$

One should use this formula, when evaluating the interfacial compliance of thin-and-long bonding materials. If thick and short bonding materials are used, the interfacial compliance can be expressed as

$$\kappa = 3\frac{3-\nu}{\pi}\frac{2a}{G}. \tag{8}$$

The parameter k of the interfacial sharing stress was introduced in the formula (10) to characterize the effect of the interface length and the interfacial compliance on the magnitude and the distribution of the interfacial shearing stress. It is shown in [42], that k can be expressed as

$$k = \sqrt{\frac{2\lambda}{\kappa}}, \text{ where} \tag{9}$$

$$\lambda = \frac{1-\nu}{Eh} \tag{10}$$

is the axial compliance of one of the pins and 2λ is the total axial compliance of the joint and

$$\kappa = \kappa_0 + 2\kappa_1 \tag{11}$$

is the total interfacial compliance of the joint.

3.2.3 Numerical example of the grooved-lap test

Using the formulae above, a numerical example is presented here to show in practice the difference in shear stress distribution between the single-lap test and the grooved-lap test [42]. The following values are used in the calculations:

- Length of the solder joint, 2a=2mm
- Width of the solder joint, b=1.5mm
- Thickness of the solder solder joint, h =0.1mm
- External force =100N
- Thickness (height) of the pins, h=3mm
- Elastic constants of the pins material, E=210GPa and ν=0.3
- Elastic constants of the solder material, E=44.3GPa and ν=0.35

Note that considering uniform shear stress along the solder joint, the above data yields the shear stress τ = 33.33 MPa. For the regular single-lap joint, this data yields at the center of the joint

$$\tau_0(0) = \frac{k\hat{T}}{2}\frac{1}{\sinh ka} = 32.83MPa\,,$$

and at the edges of the joint

$$\tau_0(\pm a) = \frac{k\hat{T}}{2}\coth ka = 34.34MPa\,.$$

For the grooved-lap joint, this data yields at the center of the joint, $\tau_0(0)$= 33.20 MPa, and at the joint edges $\tau_0(\pm a)$= 33.61 MPa. This data is presented graphically, along the solder joint in Figure 7.

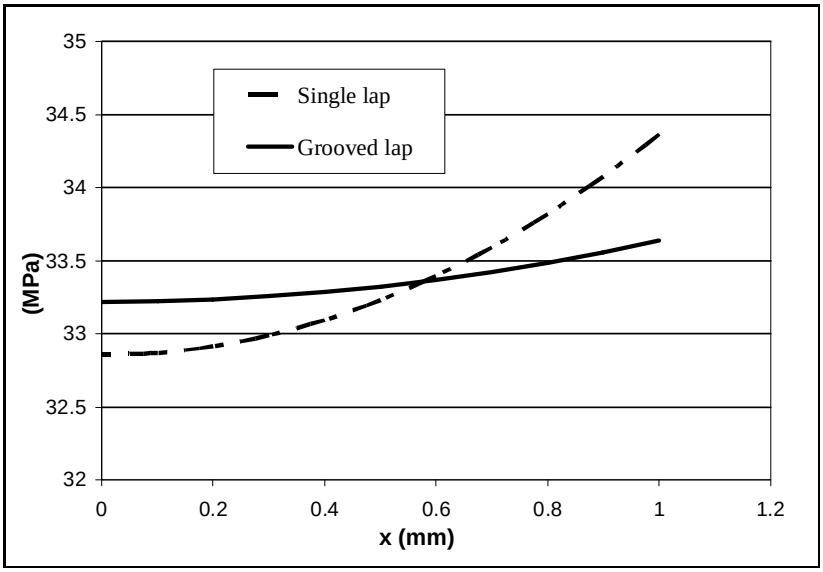


Figure 7. Shear stress distribution in the single-lap joint and in the grooved-lap joint [42].

It was mentioned earlier that the positive effect of the grooves is much stronger when considering the normal stress components than the shear stress distribution. The mathematical analysis of the normal stress is somewhat more elaborate and is presented in detail in reference [39]. In the reference [39] is shown that based on an analytical model the maximum normal stress at the edge of the joint in the grooved-lap test is only 17% of the respective stress in the single-lap joint. This fact explains the observations in the shear test experiments shown earlier in Figure 5a and Figure 5b.

4. DEVELOPMENT OF SOLDER CONSTITUTIVE MODELS

With the rapid advances in computational power and in numerical algorithms, the finite-element method (FEM) has been established as and integral part of state-of-the-art design-for-reliability methods and practices. The FEM allows to take into account for all geometric details of the structures of component boards, which may be relevant for the reliability of the product. Moreover, today's FEM softwares have a wide variety of material models to describe the physical and mechanical responses of the dissimilar materials that are present in the structure. The earlier main bottlenecks of

efficiently utilizing FEM in solving practical analysis problems were primarily the complex construction of the finite-element model, and long calculation times. For example, in electronics reliability analysis it has until recently been more practical to use simpler semi-empirical methods, such as the Engelmaier model, which has been used in the two IPC standards related solder interconnect quality and reliability [43, 44]. The main drawback in such models is that their applicability is limited to rather well-known component board structures. If there are major changes in the geometry of the structures, or in their material properties, then such semi-empirical models need be re-calibrated. The increasing popularity of the FEM is largely due to advances in the pre- and post-processing capabilities, i.e. in the ease of usage and interpretation of the results, and in significantly reduced solution times, which is due to improved numerical algorithms and higher computing power and cheaper data storage capacity.

Although the simulation times have reduced to a fraction to what they were about ten years ago, it is still good practice to build FE models that only consider the relevant details of the component board structures, to reduce the model size and consequently increase the speed of reaching the solution. Hence, in solder reliability analysis the global-local method has been established as the most efficient methodology and is today preferred by the majority of reliability and simulation engineers [9, 45]. In this method a coarse global model is run first, which is only designed to capture the macroscopic displacements. The displacements are then used as the input boundary conditions for the local model, which has all the geometric and material details of the solder joints. Figure 8 illustrates this methodology used in the case of a bumped area array component. A coarse quarter-symmetry global model of the component-PWB assembly is depicted on the left-hand side of Figure 4. On the right-hand side is the local structural model of a single solder joint, with all the geometric and material details of the component and the printed wiring board that directly affect the stresses on the solder joint. In the subsection 4.2 and in Chapter 5 will be described the reliability prediction methodology used in this global-local approach.

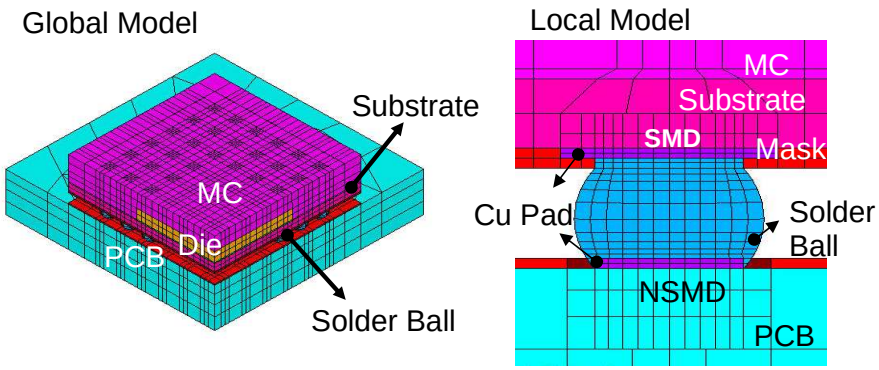


Figure 8. Finite-element mesh exhibiting the global-local modeling approach [9, 45].

4.1 Deformation mechanisms in solder joints

When assessing the reliability of solder joints, it is important to understand the underlying mechanisms of deformation that may be active in the service environment and during the tests [46]. If, for example, acceleration factors are used to estimate the field-life based on accelerated tests, then the same deformation mechanisms must be active in both conditions, otherwise the acceleration factors are not valid. Several deformation mechanisms may be active simultaneously, but generally only one of them is controlling the rate of deformation. However, the governing deformation mechanism can change in different loading conditions, and is typically strongly dependent on temperature, strain-rate, and microstructure.

In thermal cycling loading conditions the solder is accommodating the stresses primarily by creep mechanisms, i.e. plastic deformation mechanisms, in which various diffusion mechanisms control the rate of deformation. The main such rate-controlling deformation mechanisms reported for Sn-based solders are grain-boundary sliding and dislocation climb or viscous glide controlled creep [46, 47, 48]. The rate-controlling deformation mechanisms can be estimated by determining the activation energies and stress exponents during the steady-state creep using, for example, Equation 1.

$$\dot{\varepsilon} = CE/T \left(\sigma/E\right)^n \exp\left(-Q/RT\right), \tag{12}$$

where n is stress exponent, Q is the activation energy of the rate-controlling deformation mechanism, E is temperature dependent Young's modulus, T is temperature, and C is a constant. The stress exponent is typically between 1...2 for grain-boundary sliding controlled deformation mechanism, 5…7 for dislocation climb-controlled deformation mechanism, and 3 for dislocation viscous glide controlled deformation [47, 49]. The activation energies for the deformation mechanisms should be those of grain-boundary diffusion, dislocation core diffusion, and interdiffusion of solute atoms, respectively. However, using the activation energy value as an indicator of the governing deformation mechanism is difficult because of the lack of accurate data on the respective diffusion mechanisms. For example, the measured apparent activation energies for the creep of Sn range between 46 kJ/mol and 109 kJ/mol [50]. In the power-law creep deformation regime, most of the effective deformation is due to dislocation glide, but the rate of deformation is controlled either by dislocation climb or dislocation viscous glide mechanism [51]. Whether dislocation climb or glide is controlling the rate of deformation, depends on the amount of alloying, and the type of hardening effects caused by the alloying elements. The transition from dislocation-climb controlled deformation (Metal-type) to glide-controlled deformation (Alloy-type) with increasing solute concentration has been demonstrated by the Sn-Bi system [52, 53].

At high stresses, the power-law dependency between stress and strain-rate breaks down since the diffusion-based mechanisms are no longer rate-controlling. This break-down occurs typically at stress-levels $\tau=10^{-3}G$ (τ=shear stress, G= temperature compensated shear modulus) and in general it is proposed that above this stress level the stress – strain-rate relation becomes exponential [49, 51]. With Sn-based solders there can be seen a clear change in the deformation at the stress level of $\tau =10^{-3}G$, but both exponential and power-law stress – strain-rate dependencies have been observed above this stress level [47, 53, 54].

Other potential deformation mechanisms at the intermediate and high stress levels are cross slip and twinning. Cross slip has not been reported to occur in Sn, and this can be assumed to be valid also for Sn based alloys [55]. The probability of twinning in Sn increases with decreasing temperature and increasing strain rate. At room temperature

twinning has been observed to occur when strain-rate is approximately $5 \cdot 10^{-1}$ 1/s or higher [55].

4.2 Constitutive model for solder deformation

As mentioned in the previous chapter, the power law of Equation 1 breaks down at certain stress level and the rate dependency becomes exponential. This phenomenon of the steady-state creep rate can be captured by utilizing the hyperbolic sine function, as first proposed by Garofalo [56];

$$\frac{d\varepsilon}{dt} = C_{ss}\left[\sinh(\alpha\sigma)\right]^n \exp\left(\frac{-Q_a}{kT}\right). \tag{13}$$

The Ansys and Abaqus finite-element simulation softwares have implemented the Anand's model in their material model library [57]. It was originally developed for simulating hot-working of aluminium alloys, but has been later shown to apply well also for solder creep deformation simulation [58, 59, 60, 9]. The model consists of the flow equation (3), which is essentially of the same form as Equation 2 of Garofalo for secondary creep, and of the evolution equations (4, 5, and 6). Due to the introduction of the evolution equations, the model is capable of modeling strain hardening in constant strain-rate testing and the primary creep phase in constant stress testing.

$$\frac{d\varepsilon_p}{dt} = A\left[\sinh(\xi\sigma / s)\right]^{1/m} \exp\left(\frac{-Q}{kT}\right) \tag{14}$$

$$\frac{ds}{dt} = \left(h_o\left(|B|\right)^a \frac{B}{|B|} \right) \frac{d\varepsilon_p}{dt} \tag{15}$$

$$B = 1 - \frac{s}{s^*} \tag{16}$$

$$s^* = s^{\wedge}\left[\frac{d\varepsilon_p / dt}{A}\right] \exp\left(\frac{Q}{kT}\right)^n \tag{17}$$

The constants for the Anand's model for two lead-free solders and the near-eutectic SnPbAg solder are presented in Table 1. The parameters C_i in the table refer to the respective labelling used in the Ansys software.

Table 1. Constants of the Anand's model for Pb-free and the SnPbAg solder [9, 61].

	Parameter	Sn2Ag0.5Cu	Sn4Ag0.5Cu Sn3.4Ag0.8Cu	62Sn36Pb2Ag	Definitions
C1	S_o (MPa)	6.6	1.3	12.41	Initial value of deformation resistance
C2	Q/k (1/K)	8500	9000	9400	Activation energy / Boltzmann's constant
C3	A (1/s)	500	500	4e06	Pre-exponential factor
C4	ξ	4.3	7.1	1.5	Multiplier of stress
C5	m	0.16	0.3	0.303	Strain rate sensitivity of stress
C6	h_o (MPa)	6100	5900	1379	Hardening constant
C7	s^ (MPa)	28.7	39.4	13.79	Coefficient for deformation resistance saturation value
C8	n	0.04	0.03	0.07	Strain rate sensitivity of saturation (deformation resistance) value
C9	a	1.3	1.4	1.3	Strain rate sensitivity of hardening

5. SOLDER DAMAGE MODELLING AND VERIFICATION

The currently most popular solder joint fatigue life estimation method is that developed by Robert Darveaux, see for example Reference [62]. The method is based on relating the visco-plastic deformation strain energy, obtained from FE analysis, to the number of cycles-to-failure of the solder joint. The correlation is established by comparing the simulation results to a sufficient number of experimental thermal cycling test results. Thermal cycling fatigue failure results are expressed in the form of the two-parameter Weibull distribution, where α is the 'characteristic life', 63.2% failure rate of the population. In general, thermal stress fatigue consists of the period

of crack initiation (eq. 7), and crack growth (eq. 8). The fatigue life α is the sum of these two equations. In eqs. 7 and 8 a is the diameter of the solder mask opening and Δw is the visco-plastic deformation strain energy consumed during one thermal cycle, and is obtained from the simulations. Constants K_1-K_4 are assessed experimentally. The dye-and-pry technique is used to assess the number of cycles to crack initiation. It has been noted that the number of cycles to crack initiation is typically only 10% of the total life, hence some analysts prefer to omit the crack initiation phase from the fatigue life estimation [59]. This is particularly the case if the simulations are not used to estimate the absolute fatigue life of the solder joint in the filed conditions, but if they are only used to assess the acceleration factor, as proposed earlier in Figure 2.

$$N_o = K_1 \Delta w^{K_2}, \tag{18}$$

$$N_p = \frac{a}{K_3 \Delta w^{K_4}}, \tag{19}$$

$$\alpha = N_o + N_p, \tag{20}$$

It is important that the constants K_1-K_4 are used only together with the material model, which has been used in their assessment. If the solder material, and consequently the material model, change, the constants K_1-K_4 need be reassessed. This methodology has shown to provide good results, as shown in Figure 9 for the case of the eutectic SnPb solder. Only 15% difference was observed between the simulations and the thermal cycling test results when analyzing several various area-array components.

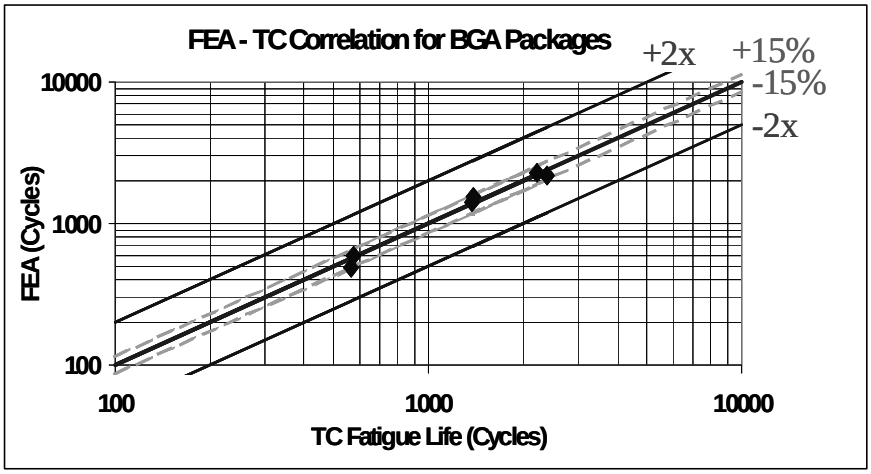


Figure 9. Comparison of predicted (FEA) and experimental cycles-to-failure in thermal cycling test [63].

6. SUMMARY OF THE THESIS

In this work a new method has been developed for assessing acceleration factors between reliability tests and service performance. The procedure combines the benefits of experimental testing and virtual computer simulations. For efficient utilization of numerical simulation tools, such as the finite-element methods, it is essential that the input data used in the analyses/simulations are accurate. It was noted earlier that despite a substantial amount of previous research conducted on solder joint reliability, some fundamental aspects of solder deformation mechanics still remain unknown to the research community, and that this can lead to uncertainties in design-for-reliability of microelectronics products, particularly with further miniaturization of the dimensional features of component boards.

In this thesis a new solder joint test method, the grooved-lap shear test, has been developed and presented in detail, which overcomes the previous problems of accurate assessment of solder deformation properties in small dimensions. The new shear test enables the most accurate definition of appropriate material models, and the model constants to be used in conjunction with reliability simulation tools. It has also been emphasized in this work, that for utilizing accelerated stress tests, such as the thermal cycling test, the failure mechanisms must be the same in the test conditions and in the

service conditions, and the governing deformation mechanisms in both situations must be understood in detail for developing the appropriate material models. It has been shown that tin-based alloys in thermal stress conditions have various active rate-controlling deformation mechanisms. With the relatively large-grained solidification structure, as is the case with as-soldered SMT assemblies, the observed deformation mechanisms in thermal stress conditions are dislocation climb controlled creep (metal-type) and dislocation viscous glide controlled creep (alloy-type), and their occurrence depends on alloying, temperature, and rate of loading. Finally, the developed shear-test method has been utilized for assessing the deformation mechanisms of selected SAC alloys. It was observed that the rate controlling deformation mechanism with these SAC alloys is dislocation climb controlled creep with low stress levels, until the power-law brakes down and on higher stress levels the deformation becomes more controlled by the intrinsic lattice resistance. Furthermore, the measured data has been fitted in the Anand's model, which is the solder material model mostly used in microelectronics industry for finite-element based solder joint reliability predictions.

The thesis consists of six publications, of which the main results and conclusions are summarized in the following.

Publication 1, entitled **"TBGA Reliability in Telecom Environment"** describes a methodology to effectively utilize finite-element simulations to ensure reliability of solder joints in telecommunications equipment. The methodology is based on a combination of simulations and experimental testing with the aim to determine an acceleration factor between the test and field load conditions. Experimental thermal cycling testing with temperature range -40 – 125 ºC is conducted with two different BGA-type components, which are soldered on an FR4 board, and checked periodically for electrical continuity, and finally followed by failure analysis to analyze the failure mechanisms. A global-local finite-element method is utilized for the simulations, and the associated failure model and respective constants had been previously determined with other test data. It is first confirmed that the FEA-based prediction method correlates well with the experimental failure data with of the tested TBGA components. Then two different field-condition thermal cycles are simulated; +10 – 45 ºC and 0 – 60 ºC. The simulations lead to the respective acceleration factors of 7

and 3.9, and consequently it is possible to estimate the life (in years) of equipment under the thermal cycling conditions that are proposed to occur in the field.

Publication 2, entitled **"A New Method to Determine Crack Shape and Size in Solder Joints"**, describes the development and application of a method to accurately measure the fatigue crack size in thermally cycled solder joints. The shape and path of the crack that develops in a solder joint as a result of thermal cycling stresses is usually characteristic to the specific component-PWB assembly. In this paper the method is demonstrated with a 1206 SMT ceramic capacitor soldered on an FR4 printed circuit board. A component assembly is thermally cycled, but removed from the test chamber before electrical failure. Then 15-20 metallurgical cross-sections are made and photographed of the sample. A simple method is proposed to manually assess the distance between the crossections and for developing the 3D image with the aid of a CAD software. It is shown that the crack front can be highly curved and the crack length in general can not be estimated from a 2D image, i.e. from a single cross-section. Knowing the characteristic fatigue crack path is required for utilizing any of the main methodologies developed for finite-element –based reliability prediction for solder joints. Additionally, this method may be used for estimating the crack growth rate, and hence used for further improving the accuracy of solder fatigue failure models.

Publication 3, entitled **"A Finite-Element and Experimental Analysis of Stress Distribution in Various Shear Tests for Solder Joints"**, evaluates the feasibility of various commonly used shear tests for assessing solder deformation properties. The shear test methods analyzed in this study are the double-lap test, the ring-and-plug test, and various common modifications of the single-lap test. Moreover, a new shear test is introduced, the grooved-lap test, which leads to a nearly uniform stress distribution along the solder joint length, as well strongly reduces the peeling stresses at the joint ends, in comparison to the conventional shear tests. The various shear tests are analyzed by the linear and non-linear finite-element method, and also by using an optical deformation measurement method of actual physical samples. The linear finite-element simulations show qualitatively the high variation of the shear stress along the solder joint between the different test methods. It also shows a very high variation of

the peeling stresses among the different tests. In the qualitative analyses the grooved-lap test demonstrates significantly more uniform shear stress along the solder joint and lower peeling stresses than the conventional shear tests. The non-linear simulations of the single-lap test and the grooved-lap test take into account the deformation due to creep in the solder joint. These simulations are compared to optical measurements of the creep deformation during the respective tests. Both the simulations and measurements show that the solder joint of the single-lap test is rotating during creep, due to the highly inhomogeneous stress distribution at the beginning of the test. Moreover, the simulations and tests conducted with the grooved-lap test show the opposite result; the initially uniform stress distribution does not change during the test, and only shear deformation can be detected at the solder joint. It is concluded that the new grooved-lap test is the most appropriate one for assessing solder deformation properties, since the test sample is easy to prepare, the microstructure of solder can be made similar to real solder joint, and due to it's nearly pure shear-stress distribution, which enables for accurate assessment of the stress-strain relation.

Publication 4, entitled **"On a Paradoxical Situation Related to Lap-shear Joints; Could Transverse Grooves in the Adherents Reduce the Interfacial Stresses"**, the new grooved-lap shear test method is further analyzed by utilizing analytical (mathematical) modeling. While the finite-element simulations and experimental test results shown in Publication 3 demonstrate the benefits of the new grooved-lap shear test in practice, they don't explain the physics behind the test. Here analytical modeling is used to explain, why the new grooved-lap shear test performs as well as it does, compared to the conventional single-lap shear test. Introducing the transverse grooves in the conventional single-lap test has two different contradicting effects, in terms of the shear stress distribution in the solder joint. By reducing the thickness of the pins, they contribute to the increase of axial compliance of the pins, which has a negative effect in terms of the shear stress distribution (shear stress becomes less uniform). However, due to the presence of the grooves, the parts of the pins that are attached to the solder joint can be thought to become part of the bonding structure. This increases the interfacial compliance of the bonding structure, and hence reduces stress concentrations and has a positive effect on the shear-stress distribution. It is shown that this positive effect significantly overwhelms the negative effect of

increased axial compliance and the presence of the grooves has an overall beneficial effect on the shear-stress distribution in the solder joint. Moreover, other previous observations from Publication 3, such as the effect of the pin thickness and the effect of the Young's modulus on the stress distribution are explained by the developed analytical model.

Publication 5, entitled **"Deformation Behaviour of Dilute SnBi(0.5…6at%) Solid Solutions"** depicts a detailed study on the governing deformation mechanisms in various dilute SnBi solder alloys under steady-state tensile loading. It appears that the SnBi system is ideal for studying the various deformation mechanisms in Sn, due to the strong effect of Bi on the Sn-lattice. The tests are conducted with dog-bone samples with the grain-size of the order of 100 μm, which resembles that of practical solder joint applications. Hence, grain-boundary sliding is not demonstrated in these tests since it only becomes a dominating deformation mechanism with samples that have very small grain size (< 10 μm). It is shown, that depending on the amount of dissolved Bi in the Sn-matrix, and on the temperature, the governing deformation mechanisms vary, and consequently the stress-strain relation of the alloys is significantly affected. With low Bi content (0.5 at%), Sn depicts "Metal-type" creep behaviour, where deformation is controlled by dislocation pipe diffusion. Such deformation is characterized by a long steady-state range in the creep test (secondary creep) and a clear strain-hardening behaviour in the tensile test. When Bi-content of Sn is increased to 3 at%, the mechanical behaviour changes completely. In this "Alloy-type" deformation the secondary creep phase is practically non-existent, and the tensile test curve shows strain-softening, instead of strain hardening. Such creep and stress-strain curves can be explained by a deformation mechanism that is governed by dislocation viscous glide, where the diffusion of the solute (Bi) atoms is slower than dislocation climb. Due to the various deformation mechanisms, which depend on the content of Bi in the Sn-matrix, for example the ultimate tensile strength at room temperature can vary from from 30 MPa (0.5 at% Bi) to over 60 MPa (6 at% Bi) ($d\varepsilon/dT \sim 10^{-5}$ 1/s). In addition, phenomena such as serrated flow (Portevin-Le Chatelier effect) and discontinuous precipitation of Bi from the Sn-matrix are observed with these alloys. Finally, when comparing the results of this study to other studies on the eutectic SnBi alloy, it is proposed that the deformation of the eutectic

alloy is dominated by the Sn-matrix, which is alloyed with equilibrium amount of Bi (depending on temperature). This observation is very important, considering the mechanical testing of solder alloys in general, and in part can be used to explain the huge scatter in the literature data on various solder alloys.

Publication 6, entitled **"Deformation Characteristics and Microstructural Evolution of SnAgCu Solder Joints"**, analyzes the microstructure and mechanical properties of three SnAgCu solder alloys. It is shown that the initial microstructure of the grooved-lap shear stress test joint resembles closely that of actual solder joints on printed wiring board. The initially very large grains on the joints of CSP components may recrystallize due to thermal or mechanical stresses and deformations. Also twinning is observed to occur due to a fast drop shock deformation. The constants of the Anand visco-plastic constitutive model are assessed. As a result of the creep tests and the constant deformation rate stress-strain tests it can be concluded that the deformation mechanism is controlled by dislocation climb, until the power-law break-down, when it becomes less controlled by diffusion mechanisms but more by the intrinsic lattice resistance. It is noted that the assessed constitutive model parameters are only valid for the large grain-size microstructure. If recrystallization occurs, for example due to thermal – mechanical cyclic loading, then grain-boundary sliding may become a dominating deformation mechanism on the affected area. This observation should be considered when developing simulation-based reliability prediction methods, either by including the effect of recrystallization in the damage model, or by developing a material model that can accommodate the changes due to recrystallization.

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