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STAMP FABRICATION FOR ULTRAVIOLET NANOIMPRINT LITHOGRAPHY

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This thesis investigates the fabrication of stamps for ultraviolet nanoimprint lithography (UV-NIL). UV-NIL is an attractive method for replacing optical lithography as a fabrication method as minimal size of the structures nears 20 nm.

Stamp fabrication methods were analysed, compared, and tried. Finally, a fabrication process integrating a transparent conductive atomic layer deposition (ALD) layer to dissipate charges during the electron beam lithography (EBL) patterning process was chosen. The ALD layer was sandwiched between the glass substrate and a pattern layer of silicon dioxide. Various test patterns, such as dots and lines, were fabricated. After defining the patterns via EBL, they were transferred to the pattern layer via a plasma etching step.

After pattern fabrication, the patterns were positioned on a mesa via a wet-etching step, producing a pedestal of about 15 μm height. Following the etching, the stamp was covered with a release layer, and the imprinting process on the NIL-addon of the mask aligner was investigated. The results were analysed and will be used for further improvement of the process.

Imprinting was successfully demonstrated on several different substrates with different surface roughnesses.

Preface

This thesis was carried out in the Optoelectronics Group of the Department of Micro- and Nanosciences in the Aalto University School of Science of Technology, formerly known as Helsinki University of Technology.

Otaniemi, March 31, 2010

Maria Klonner

Contents

Abbreviations

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
ALE	Atomic Layer Epitaxy
BOE	Buffered Oxide Etch
BSE	BackScattered Electrons
CVD	Chemical Vapor Deposition
DIW	DeIonized Water
DOF	Depth Of Focus
EBL	Electron Beam Lithography
EUV	Extreme UltraViolet
FIB	Focused Ion Beam
HEL	Hot Embossing Lithography
HF	HydroFluoric Acid
HMDS	HexaMethylDiSilazane
HSQ	Hydrogen SilseQuioxane
ICP	Inductively-Coupled Plasma
IPA	Isopropyl Alcohol
ITO	Indium Tin Oxide
ITRS	International Technology Roadmap for Semiconductors
LED	Light Emitting Diode
NIL	NanoImprint Lithography
NMP	N-Methyl-2-pyrrolidon
PDMS	Poly(dimethylsiloxane)
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PEDOT	(3,4-Etylenedioxythiophene)
PMMA	PolyMethyl MethAcrylate
PSD	Position Sensitive Device
PVD	Physical Vapor Deposition
PSS	poly(styrenesulfonate)
RF	Radio Frequency
RIE	Reactive Ion Etching
SCIL	Substrate Conformal Imprint Lithography
SE	Secondary Electrons
SEM	Scanning Electron Microscopy
SFIL	Step-and-Flash Imprint Lithography
SSIL	Step-and-Stamp Imprint Lithography
STM	Scanning Tunneling Microscopy
TCO	Transparent Conductive Oxide
TEM	Transmission Electron Microscopy
T-NIL	Thermal NIL
UV	Ultraviolet
WD	Working Distance
WEC	Wedge Error Compensation

1 Introduction

Nanotechnology is bound to have an ever increasing influence on our daily life in the future. This development is propelled forward by an intricately linked network of factors, such as new technologies, new theoretical understanding, new applications, and again new technologies. Nanostructures are present in several fields of science, so the field of nanotechnology is a very interdisciplinary one, uniting so diverse disciplines as biology, chemistry, materials science, optics, physics, or electronics.

In order to enable cheap and mass-produced products using nanotechnology, new fabrication methods are needed as the current ones are associated with high capital costs. Several technologies are heralded to be potential replacements of current methods - nanoimprint lithography (NIL) is one of them. Nanoimprint lithography is a parallel technology and thus has a high throughput.

NIL offers several advantages over conventional lithography. First, NIL does not have any fundamental limit for resolution; the resolution is only dependent on how small structures can be fabricated in the stamp. Second, NIL is a low-cost fabrication method [17, 5, 48] which makes it especially attractive. Furthermore, NIL offers parallel and fast fabrication of micro- and nanostructures [65]. Especially when compared to conventional fabrication methods with a similar resolution, such as electron beam lithography, this advantage gets even more pronounced. A fourth reason is the ability of NIL to produce three-dimensional features [50], unlike any other contemporary method. This can be exploited to drastically reduce the number of process steps used in a dual damascene process which is used in microprocessor fabrication for fabricating contacts and wiring levels. NIL could imprint both the wiring and the contacts to the lower layer in the same step. With a suitable resist, one might even avoid the need for further processing.

However, the requirements posed on nanoimprint lithography (or any other replacement of current optical lithography) are very high: Requirements concerning parameters such as throughput, defect density, inspectability, alignment, resolution, or reproducability have to be fulfilled. Currently, work is done to ensure that all those requirements might be met in the near future. Therefore, it is especially important to find cheap methods for patterning the stamps, which for the special case of ultraviolet light nanoimprint lithography are still rather expensive due to the needed transparency.

This thesis explores stamp fabrication for nanoimprint lithography. Chapter 2 outlines the history of nanoimprint lithography and presents the different types of nanoimprint lithography found in literature. Moreover, a motivation for the usage of NIL is given. Chapter 3 discusses the demands posed to the imprint resins and how the imprinting process can be modelled. Chapter 4 describes the fabrication processes and their requirements. Treated are both pattern fabrication techniques as well as the etch of the pedestal holding the structures. Furthermore, it explores alternative fabrication processes and the release layer. This is followed by Chapter 5, which introduces the fabrication equipment used for the experimental part of the thesis. The thesis ends with the presentation and discussion of the research results in Chapter 6, followed by a summary of the thesis in Chapter 7.

2 Nanoimprint Lithography

This chapter starts with the description of the motivation for developing nanoimprint lithography, followed by Section 2.2 dealing with the principles of nanoimprint lithography. Section 2.3 and its subsections introduce different variants of nanoimprint lithography as well as their advantages and disadvantages. In the end, Section 2.4 presents a few applications of nanoimprint lithography.

2.1 Motivation

Since the beginning of microtechnology with the invention of the transistor in 1948 [36][1], miniaturisation has been progressing rapidly, roughly following a law of progression first stated by G.E. Moore in 1965 [44]. Due to the demands that Moore's law imposes on micro and nanofabrication, companies have started to work together and bundle their research by developing the International Technology Roadmap for Semiconductors (ITRS). The aim of ITRS is to give some guidelines towards which goals research and development efforts should be concentrated.

Currently, progress in microelectronics is mainly driven by optical lithography, which is at the heart of miniaturization. For getting smaller and smaller structures by optical lithography, two factors are important: the mask and the light source. The mask provides the structures to be transferred onto the substrate. Making masks is an extremely expensive process as they have to be highly defect free, of the size of the substrate wafer for maximum throughput and their dimensions are about the same as they are on the substrate afterwards[2]. The wavelength of the light source determines the maximum resolution possible with the system. The most common lightsource in state-of-the-art systems nowadays is an ArF laser source with a wavelength of 193 nm. At 193 nm, a resolution of about 45 nm is possible without any special measures [32]. With water immersion lithography, it allows the fabrication of 32 nm features [33].

The resolution of an optical system can be described by an equation originally employed by Lord Rayleigh in astronomy. It states, that the resolution R

$$R = k_1 \frac{\lambda}{NA} \tag{1}$$

depends on the wavelength of light λ, the numerical aperture NA of the lens, and a technology factor k_1 [20]. Lowering the resolution is achieved by either decreasing the wavelength or the k-factor, or by increasing the numerical aperture. A change to a lower wavelength is difficult and demands a major change in process parameters, in addition to requiring new mask, resist, and lens materials. For extreme-UV (EUV) lithography using 13.5 nm [39], for example, reflective optics are needed as no traditional lens material would be transparent enough to give the required power densities. However, many steps can be taken to reduce k_1. First, all resolution enhancement techniques, such as phase-shift masks or optical proximity correction strive to lower k_1. Furthermore, information by the tool producer about the specifics of each tool can be used already in the design stage to compensate for their flaws [61].

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[1]The first integrated circuit (then called *solid circuit*) was developed by Kilby in 1958 [36, 60], the first modern diffused circuit was presented in August 1959.

[2]If projection lithography is used, the mask may be up to four times larger than the final structures.

An additional challenge is the flatness of the substrates required by the limited depth of focus (DOF), defined as

$$DOF = \pm k_2 \frac{\lambda}{NA^2}, \tag{2}$$

which depends on another process-related constant k_2. Typically, DOF poses not only stringent requirements on the flatness of the wafer; in addition, it also limits the thickness of photoresist that can be used.

For every new generation of production facilities, the cost for tool replacement and materials development increase. This economic stress resulted on one hand in trying to extend the lifetime of current technology tools by using processes such as immersion lithography or double exposure and on the other hand in exploring disruptive lithographic techniques that would provide high resolutions at significantly lower cost [39]. Several lithography tools (see Table 1 for an overview) compete for the 22 nm node in the ITRS. Electron beam lithography can reach resolutions of down to 10 nm, but due to its low throughput it is not very feasible to use it for mass production. X-ray lithography has demonstrated a resolution of 50 nm; however, the tool is rather expensive and it remains to be seen, if a resolution of 25 nm can be reached [13]. Another tool would be nanoimprint lithography, which was introduced in 1995 [13] and soon after mentioned in the ITRS as one possible replacement technology for optical lithography.

Table 1: A comparison of different lithographic patterning techniques showing their practical and actual resolution limits. Adapted from Ref. [65].

	Resolution limit	
Lithography type	**Practical**	**Ultimate**
UV/ contact/ proximity	2500 nm	125 nm
UV projection	150 nm	50 nm
EUV projection (soft X-rays)	90 nm	30 nm
X-rays/ proximity/ 1:1 mask	70 nm	10 nm
Ion beam	30-50 nm	resist: 10-20 nm
Electron beam	40-50 nm	resist: 7-20 nm
Electron beam projection	90 nm	35 nm
Imprinting (embossing)	20-40 nm	5-10 nm
Printing (contact)	30-50 nm	10 nm
Scanning probe microscopy methods	15 nm	0.5 nm

2.2 Principles of Nanoimprint Lithography

Nanoimprint lithography (NIL) is a reproduction technique based on permanent deformation of a polymer and was introduced by Chou *et al.* [13] in 1995. The process consists of three steps: first, a stamp with nanopatterns on its surface is pressed into a soft polymer. In the second step, the polymer is hardened and the stamp is removed, leaving an exact image of its structures behind. Third, the patterns are transferred into the underlying substrate. This is usually achieved by anisotropic etching, such as reactive ion etching (RIE) and includes removal of the undesired residual layer that forms during imprint. NIL is capable of doing a full-wafer imprint [42, 65, 58], thus offering a simple way to mass-produce devices.

2.3   Types of Nanoimprint Lithography

The term NIL under a close definition comprises the processes thermal nanoimprint lithography (T-NIL, also called hot embossing), ultraviolet nanoimprint lithography (UV-NIL), step-and-flash imprint lithography (SFIL), and step-and-stamp imprint lithography (SSIL).

2.3.1   Thermal Nanoimprint Lithography

T-NIL is based on the very old idea of forming a material softened by heat which resolidifies when it gets cold. This was, for example, used in combination with a seal ring and the wax of a candle to seal letters. More recently, vinyl records, compact disks, and DVDs are fabricated using the same principle [65].
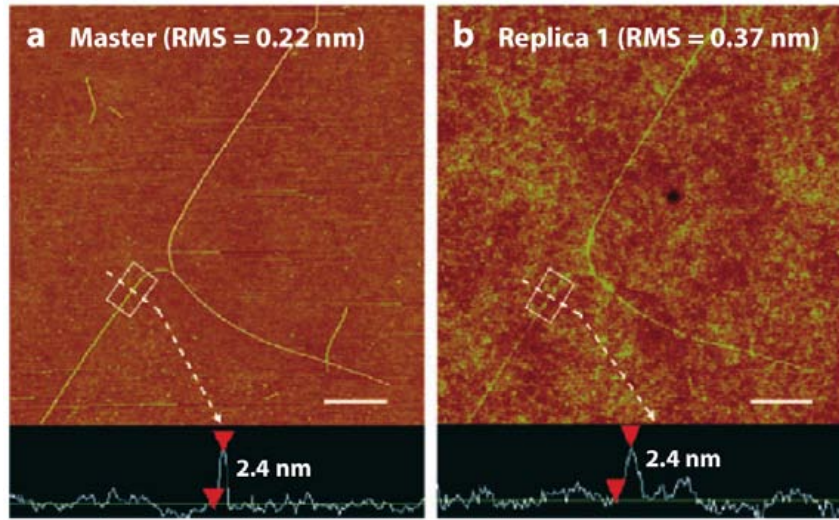

Figure 1: Atomic force microscopy images of (a) a master template and (b) the faithfully imprinted replica of a 2.4-nm-diameter single-wall nanotube strucure on the template. The white scale bar is 1 µm. [17]

T-NIL is the technology introduced in 1995 by Chou *et al.* [13] to reproduce features with a resolution of 25 nm. Two years later, a resolution of 6 nm was reached [15], and recently, NIL has demonstrated resolutions of down to 2.4 nm, as shown in Figure 1. T-NIL employs a patterned stamp[3] that under high pressure is pressed into a thermoplastic polymer to imprint the structures. Thermoplastic polymers are polymers that are glassy at room temperature. When they are heated, the molecule chains can move easier. Above its glass transition temperature T_g, the polymer turns rubbery and can be deformed as indicated in Figure 2. However, the vincinity of T_g is not really suitable for imprinting, as the mobility of the chains is still too low and the imprint would not be permanent [17]. If the temperature is increased to the melting point T_m, the viscosity of the polymer decreases even more as it becomes liquid. For imprinting, a temperature of about 50 °C above T_g is usually used, because at those temperatures the polymer has a low enough

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[3]The stamp is called mold[13]/ mould[28], master[23] or template [39], depending on the background of the author and whether further replication is performed.

viscosity to keep the time needed for imprinting small, while keeping the time needed for cooling down reasonable.
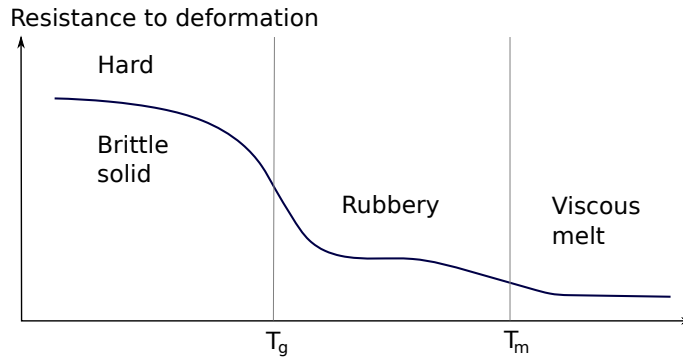

Figure 2: Mechanical resistance to deformation as a function of the temperature for an amorphous polymer. The glass transition is marked by a large change around T_g . Adapted from Ref. [65]

A T-NIL stamp is usually fabricated from silicon. Silicon is the material of choice, as it is cheap and the fabrication steps are well known. However, any material hard enough could be used as long as it can accomodate some kind of anti-stiction layer and has a heat expansion coefficient similar to the one of the substrate and the resist so that no misalignment or distortion due to heat occurs. In addition, the stamp should be easy to clean and have as low of a surface energy as possible (if necessary by including a release layer). Low defect density and inspectability for defects are also important, as well as high Young's modulus to provide the necessary hardness for the stamp. As the stamp-resin-substrate combination is going to be heated, the heat capacity should be low so that the amount of energy needed for heating is as low as possible.

The repeated heating and cooling cycles make T-NIL unsuitable for multi-layer device fabrication, and if the materials are poorly chosen, T-NIL can suffer from decreased throughput and improper overlay due to differences in thermal expansion coefficients [39].

2.3.2 Ultraviolet Nanoimprint Lithography

UV-NIL describes the idea of using a UV-curable resist instead of the thermoplastic polymers used in hot embossing; thus, it is a low pressure room temperature process. Using a UV-curable resist circumvents the problems connected with T-NIL due to high temperatures and pressures [29]. UV-NIL was originally developed as step-and-flash imprint lithography (SFIL) in the late 1990s [16]. The basic process steps are shown in Figure 3 for a two-layer imprint resist sytem, but there is no real difference to using a single layer of imprint resist.

A liquid, photosensitive resist of low viscosity is dispensed on the substrate, usually by spinning. The resist is cured by photopolymerization due to UV radiation through the transparent stamp under a low pressure[4]. Producing this stamp is slightly more complex than producing a stamp for T-NIL as will be explained later in Chapter 4. After curing,

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[4]Alternatively, the substrate may be transparent and the stamp made out of a non-transparent material; in this case the UV light would have to come through the substrate.
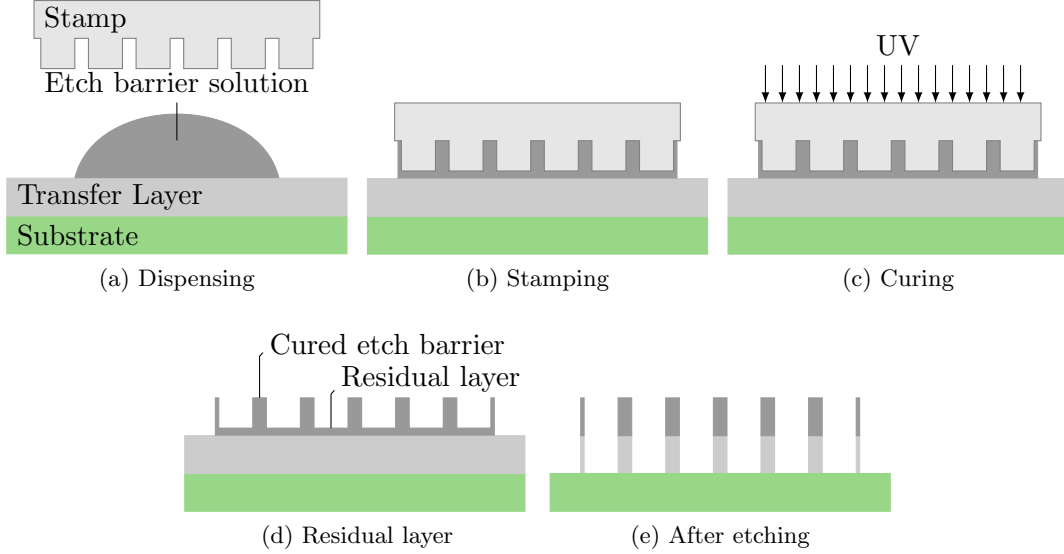
Figure 3: Process scheme of UV-imprint and pattern transfer, using a double layer system. The molded top layer, called etch barrier, is coated on the planarizing transfer layer. (a) A resist droplet is dispensed onto the transfer layer, and (b) after stamping, the resist is (c) cured. After demolding, (d) the imprinted patterns and the residual layer stay and the substrate can be etched to produce (e) the final structure. Adapted from Ref. [65].

the template is separated from the substrate and a perfect image stays behind. The time needed for curing depends mainly on the power of the UV light source and the sensitivity of the resist and is usually in the range of a few seconds, compared to minutes for T-NIL [48], as the viscosity of the resist does not hinder the filling of the stamp cavities.

An added benefit in UV-NIL stems from the use of optically transparent templates that can facilitate alignment as the substrate can be seen through the stamp.

2.3.3 Combinations With Optical Lithography

Both nanoimprinting methods leave a thin residual layer of resist over the substrate between the imprinted patterns. This layer has to be removed before pattern transfer to the substrate. A way to avoid this step and, at the same time, achieve easier imprinting of both small and large features is mixing optical lithography and nanoimprinting. This is sometimes called the mix-and-match approach [65]. In this approach, small patterns are structured as usual, while large features are defined by a metal layer on the stamp blocking the UV-light and thus shielding it from curing, this is shown in Figure 4. The unexposed resist can be developed away. If a thin metal layer is deposited on the protrusions as well, the formation of the residual layer is similarly prevented [18].

Additionally, the metal allows for more precise alignment, as the contrast is higher than when just glass is used [18]. An added benefit of the process is the ability to use shorter imprinting times and lower pressures, because only small, fast-sinking structures are present on the stamp.

(a) Before stamping.

(b) UV-exposure.

(c) After exposure.
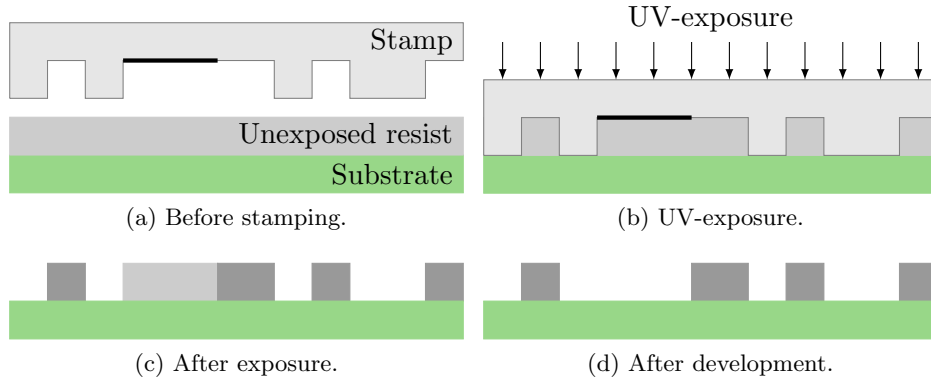
(d) After development.

Figure 4: Mix-and-match process: (a) a stamp with nanoscale protrusions and an opaque area (b) is imprinted into the resist and UV light is applied, curing the resist under the structures. (c) After demolding, the nano-patterns are transferred and the resist under the opaque area is rendered soluble in developer. (d) The stamp after developing away the soluble resist, the residual layer has been neglected.

2.3.4 Other Nanoimprint Processes

Out of the above mentioned processes many variations of NIL have been developed. SFIL is a type of UV-NIL in which the stamp is used for imprinting a substrate bigger than the patterned area by moving the stamp over the area to be imprinted, dispensing a droplet of imprint resist, and subsequently imprinting and curing the pattern. Afterwards, the stamp is moved to the next position on the substrate. This process was introduced in 1999 by Colburn *et al.* [16].

(a) Stamp
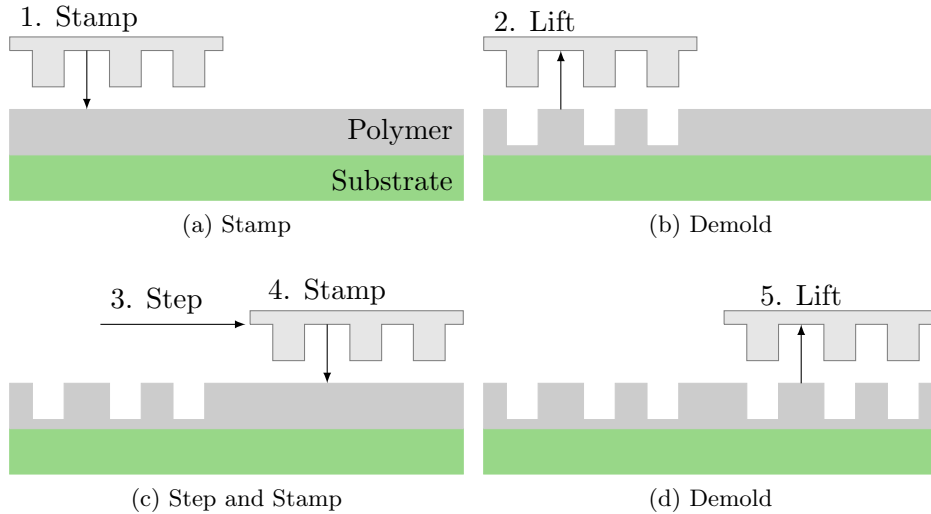
(b) Demold

(c) Step and Stamp

(d) Demold

Figure 5: Working principle of step-and-stamp and step-and-flash imprinting processes.

SSIL is a process similar to SFIL for hot embossing. The stamp is moved over a thermocurable polymer which is locally heated over its T_g, imprinted, and cured by cooling down. The idea is that local heating of the substrate reduces the thermal cycling time.

The working principle of both SFIL and SSIL is illustrated in Figure 5.

Microcontact printing is not really a nanoimprint lithography method and is listed here only for the sake of completeness. A patterned substrate is dipped in a liquid, thereby forming a self-assembled monolayer (SAM) on the protrusions. This SAM is then transferred to the substrate by contact printing. Both microcontact printing and UV-NIL can employ a soft stamp made of, *e.g.*, poly(dimethylsiloxane) (PDMS).

2.4 Applications

Applications of nanoimprint lithography can be divided into two categories: pattern-transfer applications and polymer devices. The first category uses the imprinted resist as a mask to transfer the structures into the underlying material. This process is the one that is meant to replace optical lithography in transferring patterns fast and reliably; placing special emphasis on technological challenges such as overlay accuracy, error detection, fast imprint cycles and critical dimension control [65]. Potentially, three-dimensional structures might also be involved. The second category uses the imprinted resist as it is, which has many applications in optics, electronics and nano-biotechnology. A wide range of polymers with specific properties is available. Examples for devices include patterned magnetic media for hard-disk drives, sub-wavelength metal-strip gratings, polymer optics, and bio applications [65].

The ability to produce three-dimensional (3D) structures is one of the big advantages of UV-NIL [16]. This advantage has as a direct consequence in the dual damascene process for fabricating wiring and via level in a semiconductor chip in the same processing step [50]. Doing so reduces the total number of processing steps by removing the need for doing the two optical lithography definition steps with subsequent etching to define the wiring level and the via level separately. Even though the template fabrication process is not trivial due to the low-contrast resist needed to produce three-dimensional patterns, 3D structures can be reliably replicated with one imprinting step and a subsequent dry etching step in CHF_3 plasma. The exposed resist depth defining the 3D pattern depends on the exposure dose used for exposing the resist in electron beam lithography.

Nanoscale metal wiring has also been produced by a combination of nanoimprint lithography and a lift-off process [13]. This technique was shown to produce 25 nm diameter Ti/Au dots with a 120 nm period.

3 Imprint Resin

This chapter first introduces some general concepts concerning imprint polymers. Section 3.1 discusses properties specific to thermoplastic resists, while Section 3.2 deals with the basics of UV-NIL resists and Section 3.3 introduces functional imprint formulations.

One very important ingredient of the imprint process is the imprinting resin. It has to have perfect adhesion to the substrate and should not stick to the stamp. This ensures that the resist will adhere to the substrate despite the high forces during demolding, even in densely patterned areas [29]. Although the imprinted resist can be used directly, for example for microfluidic channels or nano-optic devices, its patterns are usually transferred to the underlying layers. This happens by a descumming step removing the residual layer followed by a plasma etch step transferring the features. Without completely changing the imprinting process, a residual layer of about 50-100 Å [37] is unavoidable. However, it does protect the stamp from direct contact with the substrate, thus increasing the lifetime of the stamp because wear is reduced [18]. However, for residual layer thicknesses of around 100 Å, Lee *et al.* [37] reported a glass-like structure of the residual layer which would not cushion the stamp anymore.

From the above paragraph one can deduct the specifications of an imprinting resist: it needs a silicon containing part providing the plasma etch resistance, a surfactant reducing the surface energy towards the stamp so that it adheres poorly, a component allowing for fast curing and one for fast filling. Obviously, imprint formulations for thermal embossing and UV-NIL differ from each other, as does the imprinting process and the curing. Figure 6 shows an example for a UV-NIL imprint resist formulation.
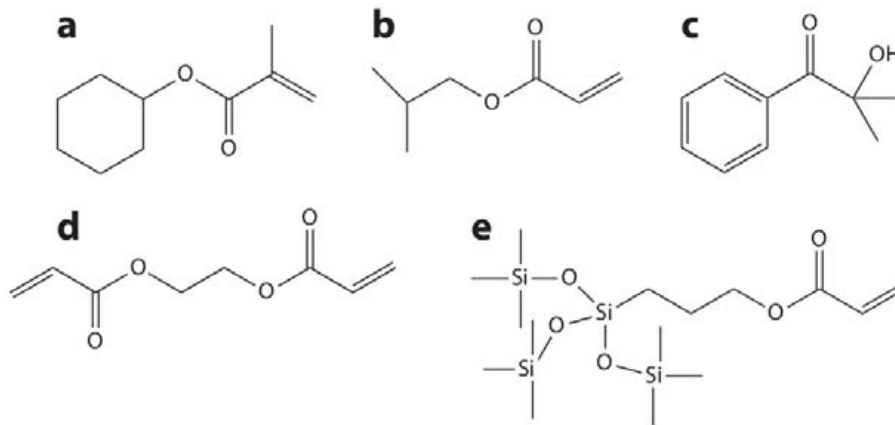
Figure 6: Typical resist formulation [17] contains (a) cyclohexyl methacrylate (28 wt%; a low-viscosity linear monomer), (b) isobutyl acrylate (20 wt%; a low-viscosity and low-vapor-pressure monomer), (c) 2-hydroxy-2-methyl-1-phenyl-1-propanone (Darocur 1173 Ciba) (2 wt%; a photoinitiator and free-radical generator),(d) ethyleneglycol diacrylate (20 wt%; a cross-linker), and (e) acryloxypropyl-tris(trimethylsiloxy)silane(30 wt%; a silicon-containing monomer). A fluorinated surfactant (not shown) is present in 15 wt%.

To understand how the imprinting process works, basic polymer flow theory will be presented. The effects of polymer flow are more visible in hot embossing where the viscosity of the resin is usually higher than in UV-NIL, thus filling of cavities is not as trivial.

Polymers are long chains of monomers, with a molecular weight M_w. This molecular weight determines many properties of a polymer, including transition temperatures, stiffness, strength, viscoelasticity, toughness, and viscosity [65]. M_w is defined by the weight of a molecule expressed in atomic mass units and can be calculated from the molecular formula. Poly(methyl methacrylate) (PMMA), a high-molecular-weight solution such as 500 kg/mol (also: 500 k) is usually used for electron beam lithography due to its high contrast, whereas for hot embossing a lower weight PMMA of around 35 kg/mol might be used. PMMA has a strong increase in temperature-dependent viscosity with M_w. The molecular weight is not affected by hot embossing where the polymer chains just move to fill the cavities, whereas in UV-NIL or electron beam lithography the chemical composition is changed by chain scission due to the radiation.

The imprinting time and uniformity are determined by the squeeze flow of the thin polymer film, and as a consequence also on the fill factor. The fill factor describes the distribution of protrusions and space on the stamp, both microscopically and macroscopically. To avoid bending of the stamp and a non-uniform thickness of the residual layer, the fill factor should be constant over the surface of the stamp, which is demonstrated in Figure 7.
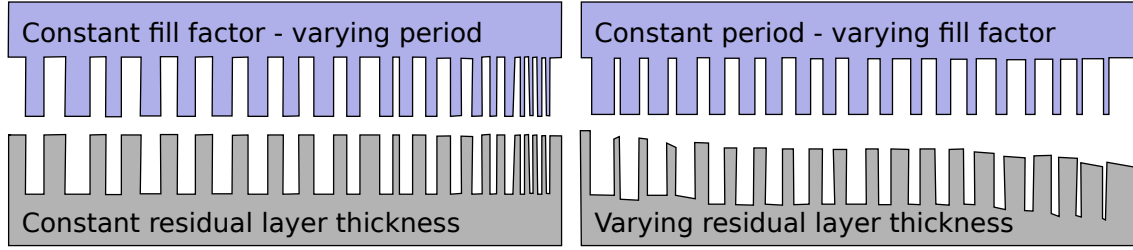

Figure 7: Variations in fill factor and its effect on the residual layer thickness: fill factor variation leads to a large variation of the residual layer thickness. Adapted from Ref. [65].

The Stefan equation [31, 10] comes from a two-dimensional model of polymer flow. Figure 8 illustrates the geometrical quantities of the equation

$$t_f = \frac{\eta_0 s^2}{2p} \left(\frac{1}{h_f^2} - \frac{1}{h_0^2} \right),$$

where t_f is the sinking time, s is the area of the protrusions, η_0 is the viscosity of the polymer, h_0 is the resist thickness before and h_f after imprinting[5], and p the imprinting pressure. According to this equation, nano-sized structures sink into the resist faster than microsized structures. This in turn leads to the fact, that combining micro and nano structures on one stamp can lead into problems if the resist flow is not taken into account, for example by providing dummy structures that ensure a constant flow of resist, because large structures need more time to imprint than small ones. This is a direct consequence of Equation 3. Dummy structures are especially important near big structures, to keep the fill factor constant and provide space for the resist to go to. Equation 3 also shows, that the time needed for imprinting can be decreased by raising the imprinting pressure or decreasing the viscosity, for example by heating the system to higher temperatures. Providing more resist results in lower imprinting times as the resist is not as limited in its mobility. Nevertheless, it should be thin enough to enable subsequent patterning.

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[5]This resist height can be described by $h_f = h_0 - \frac{WD}{s}$, with W and D the width and depth of the cavity, respectively.
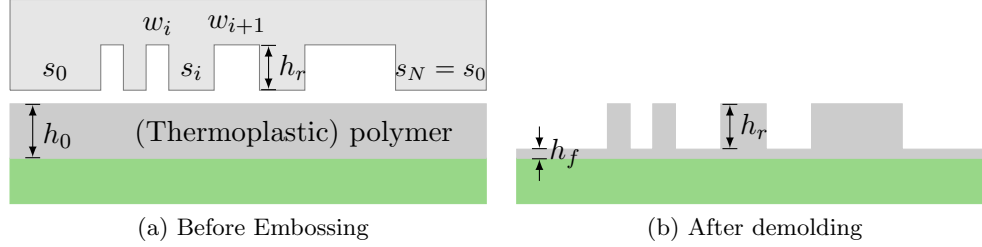
(a) Before Embossing   (b) After demolding

Figure 8: Geometrical definitions used to describe polymer flow for a stamp with line-shaped features of length L.

3.1 Thermal Resist

T-NIL resists are thermoplastic materials for which the requirement of having a low Young's modulus[6] and a low viscosity can be met simultaneously by raising the temperature above the glass transition temperature T_g of the polymer. This lowers both values by several orders of magnitude in comparison to their room temperature values [29].

Above their glass transition temperature T_g, polymers are highly-viscous liquids which react to forces in one of three ways [63]: (i) they respond instantaneously with an elastic deformation; (ii) they undergo elastic deformation within their typical relaxation times (this is called creep behaviour), and (iii) they flow within a time scale dependent on their viscosity. The latter is a non-recoverable plastic deformation and thus is utilized in T-NIL. Both relaxation time and viscosity depend on the temperature of the polymer and decrease with increasing temperature. A further reduction of viscosity occurs due to high shear forces when the polymer behaves like a non-Newtonian liquid [63].

The fact that elastic and plastic deformation happen at the same time, and their time scales depend on temperature, complicates the modelling of polymer flow. However, this can be described by the time-temperature relationship of the Williams-Landel-Ferry (WLF) equation [31, 63]

$$\log\left(\frac{\tau}{\tau_0}\right) = \log\left(\frac{\eta}{\eta_0}\right) = \frac{-C_1(T - T_0)}{C_2 + (T - T_0)}, \tag{4}$$

where τ is the time constant of the polymer response, η is the viscosity and T the absolute temperature, with the index 0 denoting the respective values (τ and η) at a reference temperature. For $T_0 = T_g$ the constants take the values $C_1 = 17.44$ and $C_2 = 51.6K$. This equation states that the ratio of variables such as viscosities or relaxation times vary exponentially with temperature.

As a consequence, this leads to guidelines concerning imprinting parameters for T-NIL. If the temperature is limited, the imprint time increases; for short imprint times the temperature has to be increased. A change in temperature leads to a larger change in time due to the exponential dependence. A fast, low-pressure, low-temperature imprinting process for T-NIL cannot exist if the polymer is stable at reasonable temperatures. It would lead to an elastic, reversible deformation that would relax once the pressure is removed [63]. Insufficient time will lead to incomplete filling of cavities [31].

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[6]Materials with a high Young's modulus are usually used as stamp materials due to their hardness. Diamond has a Young's modulus of 1050 GPa and silicon one of 131 GPa [65].
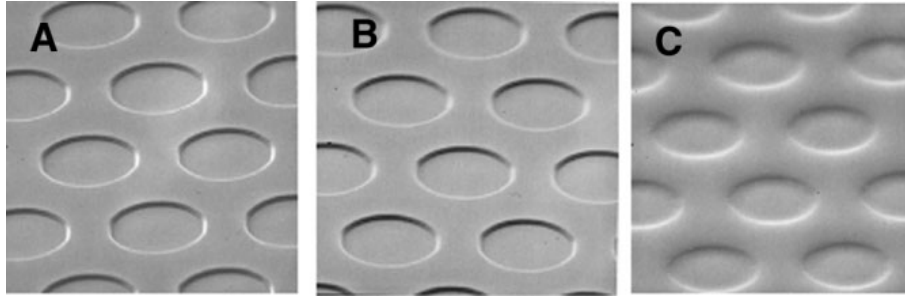
Figure 9: Scanning electron microscope images of patterns imprinted in (a) poly(benzyl methacrylate) and (b) poly(cyclohexyl acrylate). Poly(cyclohexyl acrylate) is a polymer with a T_g near room temperature, that is why (c) it shows visible relaxation of the imprinted patterns after demolding [29].

In practice, an imprinting temperature of about 70 to 90 °C above T_g is chosen to bring the polymer to its viscous state. T_g is dependent on all factors that limit or enhance molecular motion, such as intermolecular forces, chain branching or crosslinking, bulky and stiff sidegroups, or flexible bonds and sidegroups. Depending on the desired glass transition temperature, the polymer has to be chosen and the imprinting pressure and temperature adjusted accordingly [29]. If this is not the case, the polymer can relax too early as demonstrated in Figure 9.

The polymer flow is characterized by the viscosity parameter, which is a proportionality factor between the applied forces and the resulting velocity gradient. Therefore, at a given force or pressure a lower viscosity results in a higher flow gradient. The worst case to consider is a Newtonian behaviour where no shear thinning takes place, resulting in a case called *zero shear limit* [63].

Both Scheer *et al.* [63, 64] and Heyderman *et al.* [31] report that completely filling large patterns is harder than filling small cavities. This seems to be due to the necessary transfer of polymer over large lateral distances for micrometer sized structures. Filling of cavities starts from the edges with two different filling mechanisms at work. The first one is a viscous flow of polymer from the borders; the second one is due to mounds of polymer being forced up from the surface. The latter mechanism is favoured by a higher embossing pressure. Capillary action also plays an important part [31]. After corners have been filled, the polymer tries to minimize its surface energy by filling in circular shapes when flowing into large cavities. Figure 10 illustrates the results of incomplete filling.

Imprinting time, temperature, and resist thickness are closely connected. For a given combination of temperature and imprinting time, lowering the temperature means an increase in the time required for imprinting. Decreasing the initial thickness of the polymer requires raising the temperature. This seems to be due to adhesion of the polymer to the substrate and stamp surface, hindering the mobility of the polymer chains [31].

3.2   UV Curable Resists

UV-NIL needs imprint resins possessing several important material characteristics to support quick and faultless imprinting [39, 17]. First, the viscosity of the material has to be low at room temperature so that the liquid resist fills the protrusions fast and it can be
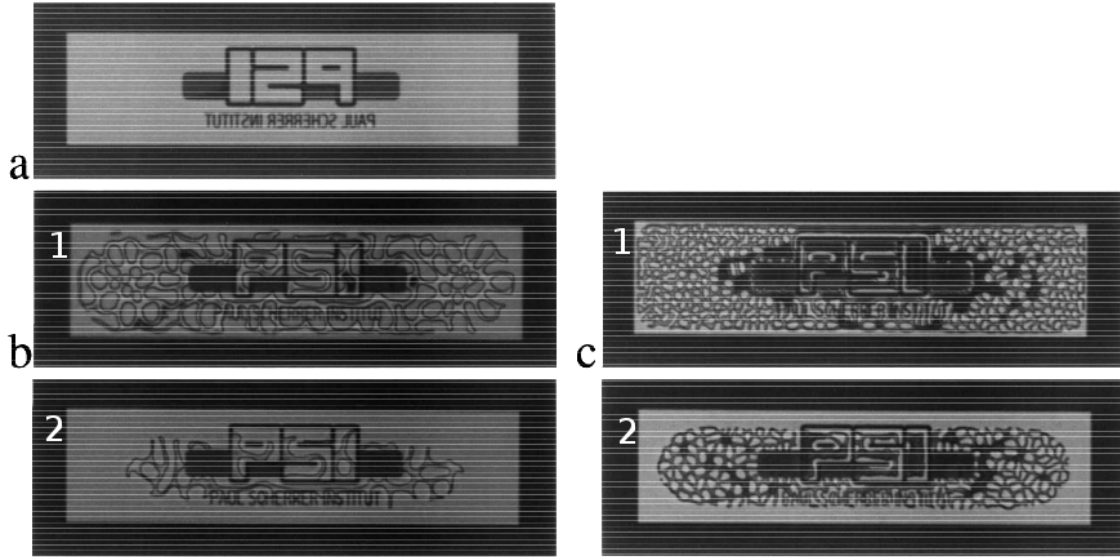
Figure 10: Optical images of (a) stamp and corresponding embossed polymer showing complex patterns due to incomplete filling: (b) 100 nm thick 25 kg/mol PMMA, $T =$ 170 ℃, F=150 kN, t=10 min, and (c) 100 nm thick 75 kg/mol PMMA, T = 200 ℃, F=150 kN, t=2 min. The first and second picture differ in the time that has passed since imprinting started. The involvement of mounds in the filling of the cavities can be clearly seen. Adapted from Ref. [31]

easily dispensed. Second, it must be photosensitive and must photocure quickly to achieve high throughput. Additionally, the separation force between the template and the resist should be as low as possible to prevent defects and stamp fouling. Moreover, the material needs sufficient stability in order to prevent pattern collapse and to provide resistance to plasma etching. Finally, sufficient thermal resistance is also required to withstand the etching temperature or the temperatures of any further processing steps.

A typical liquid resist, as shown in Figure 6, consists of a photoinitiator, a monomer with high Si content for plasma-etch resistance, a cross-linking agent to provide mechanical strength, a bulk polymerizable organic monomer, a fluorinated surfactant reducing adhesion to the template, and a low-molecular-weight monomer to reduce the viscosity of the solution [16, 29, 17]. Depending on the bulk monomer used, an imprint resin can have different properties. As a bulk monomer, polymers such as acrylate formulations, vinyl ethers, aldehydes, and epoxides have been used.

Most commonly used and available are acrylate formulations, which are known to have a low viscosity and a fast curing rate. However, their shrinkage during curing is rather large, about 10 %, and furthermore, their radical-based photopolymerization is inhibited by the presence of oxygen [29, 39]. Oxygen can increase the time needed for curing and lead to the formation of an uncured band of resist. This can be prevented by increading the exposure time or imprinting in an oxygen-free environment.

Other bulk monomers can completely circumvent the problem of shrinkage and oxygen-inhibition by using oxygen-inhibition free cationic polymerization. The most promising of these are vinyl ethers due to their low viscosity and high tensile strength. A UV curable imprint resist based on vinyl ethers showed significantly faster curing rates and higher

tensile strengths than the acrylate materials [17]. Additionally, a higher dry etch resistance due to its high silicon content and lower shrinkage after curing have been experimentally determined [29]. With a suitable underlayer, it could even easily be spun onto a substrate, making its dispense less time-consuming than the droplet dispensing technique used in SFIL. However, the separation force was measured to be much higher, which could induce cohesive failure leading to higher defect rates. Despite those hopeful experiments, acrylate based materials dominate the market as the are (a) commercially available and (b) can be improved by adding various surfactants into the resist formulation.

A list of resists, together with their manufacurers and, if available, components is given for reference in the appendix in Table B.1. The amount of experimental data in literature, however, is still lacking.

3.3   Functional Imprint Formulations

Functional imprint formulations change the behaviour of an imprint resin by changing its chemical composition in addition to the components necessary for simple imprinting.

There are two reasons, why functional imprint formulations are of interest. First, by functionalizing the resist, adhesion to the template can be avoided, for example by adding a component that forms a low surface energy layer on top of the resist. Second, if the resist is not used as a mask to transfer the patterns to a layer on the substrate, but stays and forms a part of the final component, a functional imprint can for instance provide the desired properties.

Template fouling occurs when resist adheres to the imprint template, and can be prevented with a functional imprint formulation [39, 17]. Imprint resists have to have a high crosslink density providing mechanical strength and a high concentration of silicon for the etch resistance. The combination of those two factors makes stripping the imprint resin from the stamp difficult with common solvents, oxygen plasma, pirhana, or similar solutions, especially as the high silicon content makes it nearly quartz like. Several approaches to solve this problem have been tried, one being application of release layers as described in Section 4.4, the other one being inclusion of reversible or degradable cross linkers. The former has been shown to not completely be able to prevent fouling [39]. The latter uses stripable imprint resists to prevent template fouling [17]. By replacing the cross-linker of the resist formulation with one that can be easily degraded by heat or acid, the resist can be stripped rather easily. In addition, the material has to be compatible with imprinting, so it needs to be soluble in the imprint material, and its viscosity has to be low. A promising candidate has been found in tertiary diester diacrylate, which allows faithful imprinting. Costner *et al.* [17] state, that these materials are not yet ready for production usage, as their mechanical properties need more tuning and they are not yet suitable for imprinting small structures.

Another application for functional imprint formulation is the dual damascene process explained in Section 2.4. Using a functional imprint material might save additional process steps. For achieving this, the material should be a functional dielectric fulfilling five key requirements: it should (1) be thermally stable at 400 ℃ which is needed to allow further processing steps, (2) be liquid at room temperature so that imprinting is possible, (3) be photocurable, (4) have a low dielectric constant, and (5) provide sufficient mechanical stability after curing so that the features are kept from collapsing [39].

4 Stamp Fabrication for UV-Nanoimprint Lithography

Stamp fabrication for hot embossing and UV-NIL are performed rather similarily: the desired patterns are written into the resist via electron beam lithography (EBL). The resist is then developed and further processed. One option for further processing is doing a lift-off after exposing positive resist; the other option is using the (negative) resist directly as a mask for etching the underlying material. Positive resist develops away in the areas where it was exposed, whereas negative resist gets crosslinked during exposure and is removed from unexposed areas.

The stamp can be made of various materials including metals, dielectrics, semiconductors, and polymers. One of the first stamps used for T-NIL was made of silicon dioxide on silicon [13]. The first UV-NIL stamp used chromium as an etch mask for fused silica.

Section 4.1 discusses different pattern fabrication methods. Following that, Sections 4.2 and Section 4.3 describe etching of the mesa in the center of the stamp and alternative fabrication methods, respectively. The chapter ends with Section 4.4 introducing and comparing release layer formulations.

4.1 Pattern Fabrication Methods

In general, stamp fabrication using EBL is easier for T-NIL, because the stamp material can be conducting. Therefore charging effects related to the lack of charge dissipation in insulating substrates can be avoided . As transparent substrates are needed for UV-NIL, stamps are almost exclusively made out of quartz or fused silica, although sapphire and diamond are additional options. Most materials transparent to UV light are non-conducting. Because of this, the use of charge dissipation layers is widespread.

When insulating substrates are patterned with a beam consisting of charged particles, those particles build up charge near the surface if no charge dissipation layer is present. This surface charge causes an unbalanced surface potential, resulting in drifting of the beam. For instance, when using an electron beam, this drift leads to severe pattern distortion in EBL writing, and makes it difficult to take micrographs [35, 43]. Figure 11 illustrates the charging effect as seen in the scanning electron microscope (SEM).

4.1.1 Metal Layer Under Resist

One option to provide conductivity is to use a metal layer underneath the negative resist. The metal layer (about 10 nm thickness is enough for charge dissipation purposes) is then etched using the resist as an etch mask and after resist stripping, the metal is used as an etch mask for the underlying substrate material which is typically some kind of glass. This was the first method used to fabricate UV-NIL templates as chromium coated glass wafers were readily available and had processes well known from the production of optical lithography masks. Additionally, chromium has a high etch selectivity with respect to silicon dioxide [70]. Chromium is etched in chloride based etches, and not attacked by the fluorine based etch chemistries used for etching SiO_2. The first stamps thus were quarter photomask plates, with dimensions of 65 mm × 65 mm ×6.35 mm. Their thickness prevents bending of the stamp which can be an advantage.

During the silicon etch, it is necessary to find a balance between producing sufficient but

not too high amounts of fluorocarbons which protect the surface from etching, giving a better sidewall quality.

4.1.2 Integrated Transparent Conductive Layer

An alternative for dissipating the charges is integrating a transparent, conductive material into the stamp, as illustrated in Figure 13. This can, for instance, be an atomic layer deposition (ALD) of a ZnO/Al_2O_3 nanolaminate or a layer of indium tin oxide (ITO). The conductive material is then covered with a layer of transparent oxide such as SiO_2 or Si_3N_4 about 80 to 100 nm thick [48], out of which the features are patterned. The features
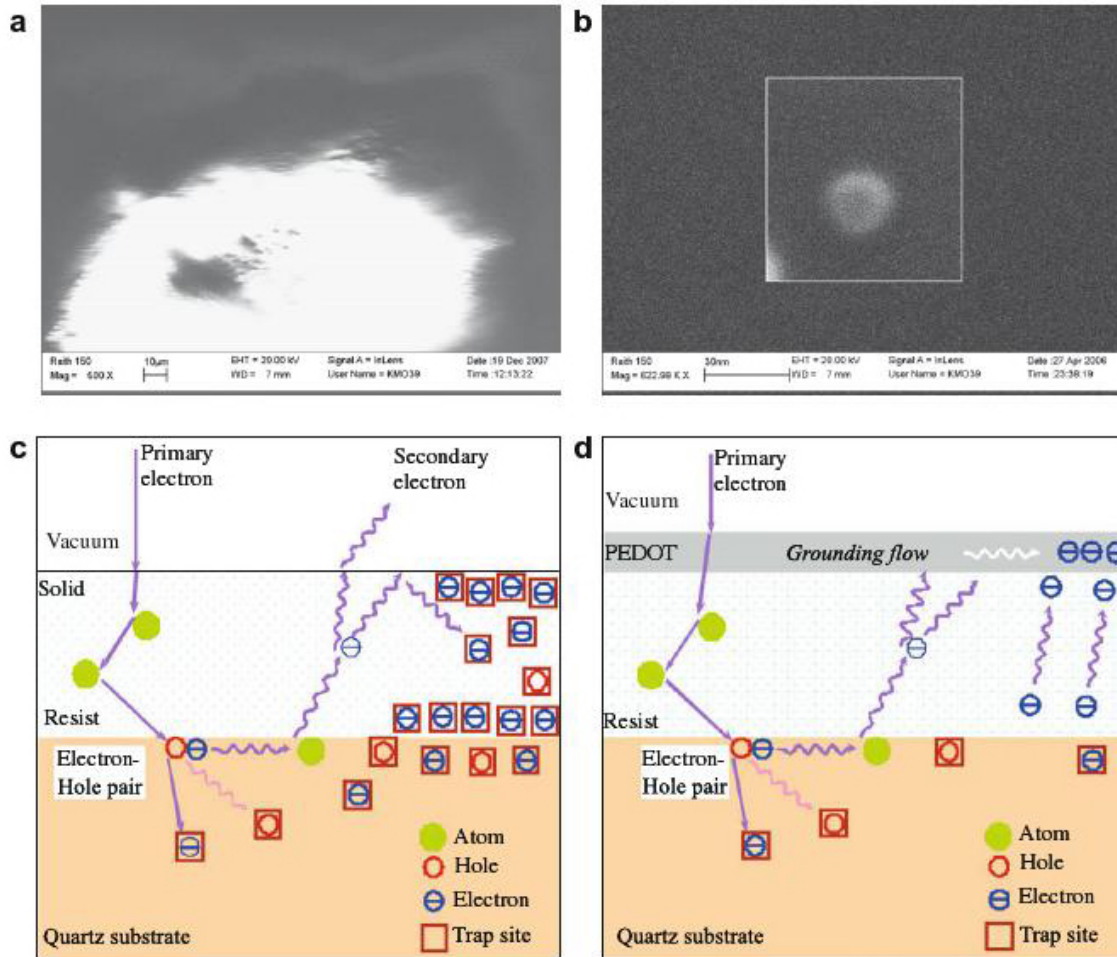

Figure 11: (a) SEM image of a quartz substrate coated with negative resist being exposed to the e-beam. A bright surface area caused by the built up surface charge is seen. (b) SEM image of a quartz sample coated with negative resist and (3,4-Etylenedioxythio-phene)/poly(styrenesulfonate) (PEDOT/PSS). Zoomed window shows the contamination dot produced by an e-beam on the top surface with no surface charging effects. (c) A schematic diagram of electron trajectories showing charges built up and (d) the schematic diagram of electron trajectories with PEDOT/PSS top coating showing significantly less charge build-up [43].

are defined by EBL and transferred via plasma etching to the oxide layer. The advantage of this method over the one presented above is, that the conductive layer is integrated into the finished stamp, thus allowing for easy inspection with a scanning electron microscope (SEM). Additionally, microloading during dry etching is avoided as the selectivity of oxide to ITO is very high [6, 19].
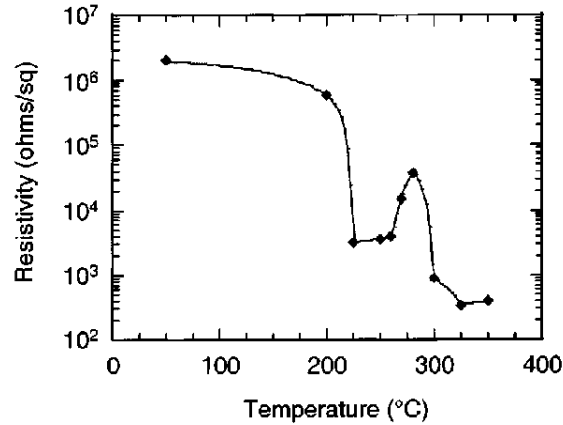

Figure 12: Plot of resistivity vs bake temperature for a 500 Å thick ITO film. Sn oxidation and a film phase transformation account for the changes in resistivity [19].

ITO is usually sputtered or evaporated on the substrate after which it is of milky appearance. By annealing at around 350 to 400 °C, ITO becomes transparent and the resistivity decreases. The dependency of the resistivity on the annealing temperature is illustrated in Figure 12. For a 60 nm thick annealed ITO film on a 6025 fused silica blank a sheet resistivity of about 270 Ω was reported [48]. Optical transmission at the wavelength of 365 nm was measured to be 85 %. A value of $2 \times 10^6 \, \Omega$ is given for the sheet resistivity of ITO before annealing [19], with a mention that the roughness of ITO increases slightly after annealing.

Additionally, it is important, that the ITO layer adheres well to the underlying (glass) substrate, and that its stress, resistivity, and surface roughness are sufficiently low. Moreover, composition, crystal structure, optical transmission and reflection as well as etch characteristics have to be taken into account [19]. Especially the compatibility with the release layer is important. It has been reported, that the commonly used release layer of fluorosilanes adheres less to ITO than to quartz, leading to large amounts of resist sticking to the stamp [41]. This happens, because ITO is part of the final stamp surface, as illustrated in Figure 14. By carefully choosing the release layer, the problem of detachment can be overcome.

Another factor to take into consideration is the oxide layer. The oxide layer on top of the conductive layer is, with about 100 nm thickness, much thicker in comparison to the 15 nm of chromium. Consequently, Nordquist *et al.* investigated the influence of intrinsic stress in those layers on the image placement [48].It turned out, that a 100 nm thick low-temperature plasma-enhanced chemical vapor deposition (PECVD) (T <250 °C) SiO_2 layer showed a compressive stress of 300 MPa and Si_3N_4 exhibited a tensile stress of 300 MPa, while the one of SiON was below the accuracy of 30 MPa of the measuring device used. Therefore, if high alignment precision is needed, it is imperative to avoid stress because
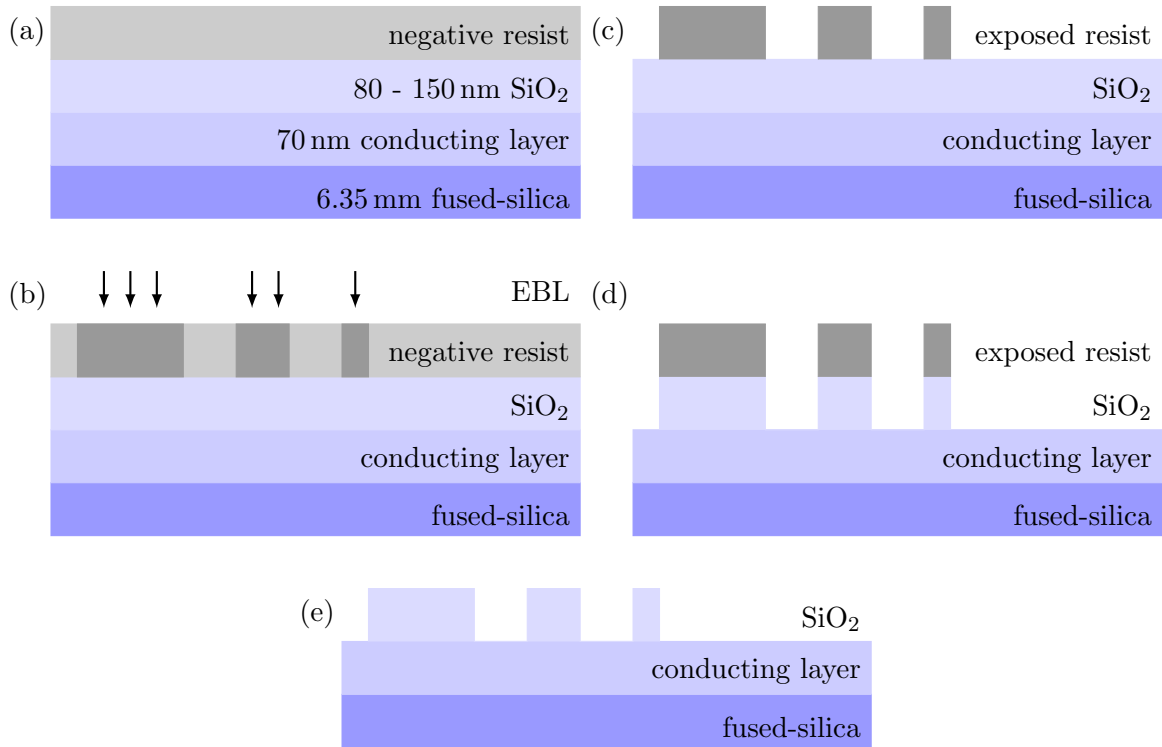
Figure 13: Processing steps for UV-NIL stamp. (a) First resist is spun on the stack of SiO$_2$, conducting layer and glass substrate. (b) Then the resist is exposed via EBL and (c) developed. (d) The resist is used as a mask to etch the underlying SiO$_2$, and (e) after stripping of the resist, the stamp is finished.

Figure 14: Surface morphology of the finished stamp containing SiO$_2$ structures and a transparent conductive ITO layer. The release layer is shown in red.

of possible misplacement and image distortion.

4.1.3   Addition of Sacrificial Conductive Layer

One further possibility to avoid charging of an insulating sample is to add a very thin (maybe 5 nm to 10 nm) conducting layer on top of the EBL resist to ensure charge dissipation during exposure. After exposure the layer is removed, the resist developed and the substrate etched.

Mohamed *et al.* used a water-soluble conductive polymer, PEDOT/PSS, as the top conductive coating on the photoresist layer [43]. PEDOT/PSS can be removed by rinsing with deionized water (DIW) after the e-beam exposure prior to the development process.

Alternatively, a metal layer of about 7 nm thickness can be deposited, either by sputtering or evaporation. Prior to development the metal is removed by a short dip in a suitable etchant.

4.1.4   Critical Energy Electron Beam Lithography

An approach managing completely without charge-dissipation layer is presented by Joo *et al.* [35]. It proposes to execute EBL at the critical energy. The critical energy is defined as the energy "where the charge balance between incoming and outgoing electrons leaves the surface neutral". This prevents pattern distortion usually present due to charging effects. A 60 nm thick layer of hydrogen silsesquioxane (HSQ) is spin coated directly on the glass wafer, and the critical energy is determined with the scan square experiment. The idea is, that an electron beam negatively charges insulators, so the total electron yield σ is smaller than one. The total electron yield is the sum of the secondary electron yield δ and the backscattered electron yield η: $\sigma = \delta + \eta$. For very low beam energies, the surface can become positively charged ($\sigma > 1$) when more electrons leave the material than are originally implanted. At the critical beam energy, outgoing and ingoing electrons are in balance [34].

The critical energy is determined from SEM images with the scan square method. If increasing and decreasing the magnification gives no change in color in the area of increased magnification, the critical beam energy has been found. For lower voltages the rectangle formed by incidenting electrons in Figure 15 after zooming in and out would be darker than the background and positively charged, for higher energies brighter and negatively charged as then the electron collection efficiency at the detector is higher.

Using this method to determine the acceleration voltage for EBL, gratings of 55 nm linewidth have been fabricated. It is assumed, that much smaller patterns will not be possible due to inherent limitations of the method [35].
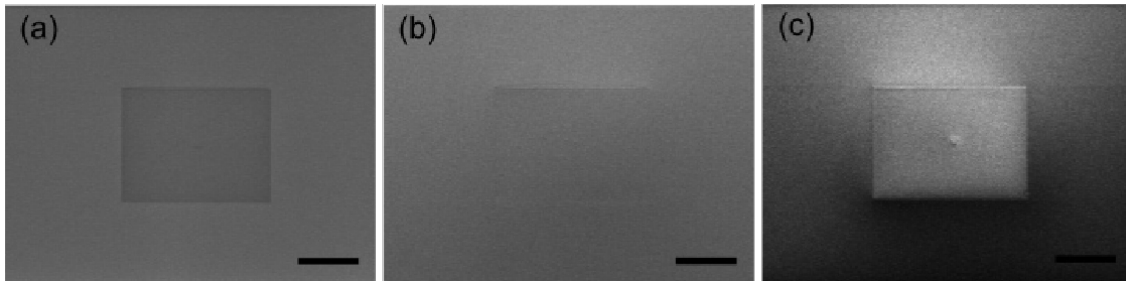

Figure 15: Scan square method for determining the critical energy. The images are taken with an acceleration voltage of (a) 0.5 kV, (b) 1.3 kV, and (c) 2 kV. The scale bar indicates 200 μm [34]. In this case, the critical energy would be 1.3 kV.

4.1.5   Stamp With Structures of Oxide-Covered Resist

A setup similar to the one in Section 4.1.2 was used by Mancini *et al.* with the main difference, that they left out the dielectric layer out of which the structures were patterned [41]. Instead, they spin coated HSQ on ITO, which after exposure and development was

coated with 5 nm of SiO_2 to provide an interface for the release layer. HSQ is a spin-coatable organic silicon oxide which mostly is used as a low-k dielectric. However, it can also be used as a high-resolution e-beam resist. When cured, HSQ becomes a durable oxide, making it suitable for directly patterning the imprint structures.

4.2   Etching of the Pedestal

A pedestal or mesa of about 15 µm to 25 µm height is etched around the patterns to prevent the circumference of the stamp from interfering with the act of imprinting [17, 68]. The process is illustrated in Figure 16. If no mesa were present, all of the resist on the stamp area would have to be moved into cavities or out of the stamp area completely. As the resist only flows distances of around 1 mm, as discussed in Chapter 3, this would lead to an uneven residual layer and generally a bad imprint.
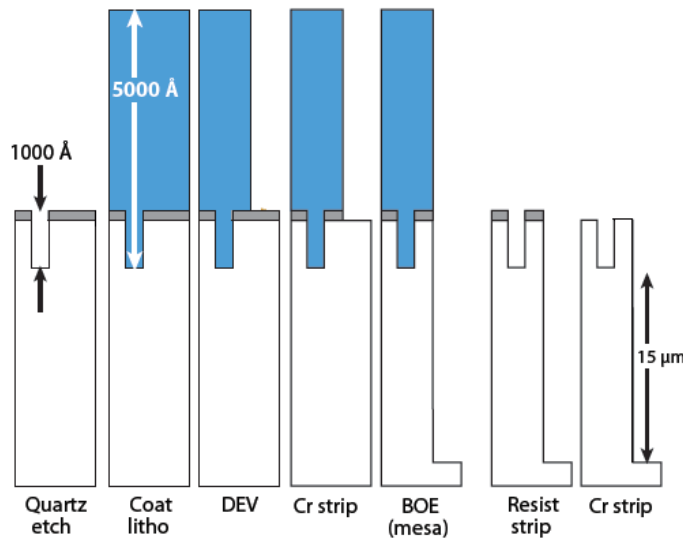

Figure 16: Template fabrication process flow for mesa generation. The process flow is drawn from left to right. Adapted from Ref. [17].

Etching the step requires protecting the patterned area from the quartz etch. Therefore, the stamp is coated with optical lithography resist. The adhesion of the resist to the underlying chromium and/or quartz layer plays an essential role in the success of this step. As wet etching with hydrofluoric acid (HF) or buffered oxide etch (BOE) is not a safe process, replacing it with an ICP-RIE etch has also been investigated [68].

Grosse *et al.* [27] give detailed instructions on how the wafer has to be prepared for wet etching of up to 33 µm of fused silica with one layer of resist mask only. They start with thoroughly cleaning the wafer at temperatures of 150 °C in concentrated chromofluoric acid for 5 - 15 h, followed by a rinse in deionized water and nitrogen blow-drying. Afterwards, the samples are annealed for 8 hours in a vacuum oven at 300 °C before spinning hexamethyldisilazane (HMDS). Both steps help to increase the adhesion of the resist to the sample by removing the adsorbed water surface. In the next step, the photoresist (AZ5214e) is spun on the surface, prebaked and exposed. After development, the weakened resist is hardened again by a 20 min flood exposure as well as an extended hardbake cycle of several hours at temperatures between 120 and 180 °C in a vacuum oven. The

extended baking procedures ensure that the photoresist is fully polymerized and resists the hydrofluoric acid.

The etch rate has a definite dependence on temperature and concentration of the hydrofluoric acid (which is solved in ammonium fluoride etchant). They report that temperatures between 30 and 40 °C give the best results.

The use of BOE has also been reported by others [57, 45, 66, 46], although details of the process were not given in the papers.

4.3 Alternative Fabrication Processes

Apart from fabricating the stamp patterns via EBL, it has been proposed to pattern the stamps with a focused ion beam (FIB) [1]. The group suggested two different fabrication processes, direct milling and milling of a mask with a consecutive inductively coupled plasma reactive ion etching (ICP-RIE) step. The first process uses a Cr/Au layer to dissipate charges during milling. An aspect ratio of about 4:1 can be reached. Higher ratios are rather difficult due to the geometrical limitations of milling with an ion beam. Although the process produces smooth sidewall profiles and surfaces, the gaussian beam distribution profile limits the minimum size that is directly millable. Moreover, the material removal rate is very low, times up to 40 min are needed for an area of 100 μm^2. Also, charging and beam drift limit the yield of successful wall formation to about 20 %. As a modification, they propose patterning a thin Cr/Au layer which is used as a mask for the ICP-RIE etch.

Another fabrication method proposes employing existing laser pattern generators used for phase shift masks [68]. Those pattern generators have the advantage that they are faster than the e-beam systems usually used and can fabricate sharply defined features.

Although stamps are usually made from hard materials, soft materials can also be used. Especially for large area imprints, it is believed that they are beneficial as they can bend to uniformly conform to the substrate. Potential materials for that are polymers such as PDMS [8]. Although those stamps can not reach the resolution of hard masks, they are cheap to fabricate and can be easily copied several times from a silicon master by hot embossing. Moreover, by using fluoropolymers, the need for a release layer disappears as the polymer itself has low surface energy [30]. For reasons of stability and easy handling, those stamps are attached to a quartz plate.

4.4 Release Layer

When the stamp is drawn away from the substrate after imprinting, the imprint resist should adhere to the substrate and smoothly detach from the stamp. However, two factors make this difficult. First, the surface energy of quartz is higher than that of the substrate or transfer layer, increasing the probability of the resist sticking to it. Second, the high density of nanoscale protrusions increases the surface available on the stamp and thus its surface energy. Both of these factors have led to the introduction of a layer that lowers the surface energy of the stamp in relation to that of the substrate, in order to reduce the adhesive forces. Three methods to achieve this goal have so far been explored: (1) adding a release agent to the imprint resist, (2) coating the stamp with a release layer, and (3) fabricating the stamp out of a material with low surface energy.

Adding a release agent to the imprint resist is a way to decrease the separation forces [17, 14]. The release agent moves to the top during spinning of the resist, where it forms the (liquid) surface layer [7]. This leads to a situation, where the adhesion of the imprint resin to the substrate is strong but the adhesion to the stamp surface is weak.

However, coating the stamp with a release layer is the most widespread solution. Some groups have demonstrated the application of plasmadeposited fluoropolymers or fluoro-doped carbon-like diamond layers [21]. Nevertheless, the most common release layer consists of a self-assembled monolayer (SAM) of (per)fluoropolymers [29]. The advantage of fluoropolymer SAMs (FSAM) over plasma-deposited fluoropolymers is, that the latter partly incorporates into the imprinted material, which limits the lifetime of the release layer [4]. FSAMs, such as 1H,1H,2H,2H-perfluorodecyl-trichlorosilane (FDTS), can be applied either in a liquid-phase or a vapor-phase deposition via a silanization process [28]. Vapor phase deposition is better suited to nanostructures, as the density of structures can lead to insufficient liquid wetting, especially in trenches. The FSAM molecule consists of a polar headgroup and a long, inert tailgroup. Figure 17 shows an example of such a molecule. The active headgroup trichlorosilane binds covalently to the silicon dioxide surface of the stamp [16] and forms siloxane bonds, Si-O-Si, while releasing Cl [28]. The reaction is self-limiting and stops, when the complete surface area is covered with the monolayer. The resultant surfactant coating is chemically and thermally stable; this is especially true if followed by an annealing step to increase the strength and density of bonds and networks [4].

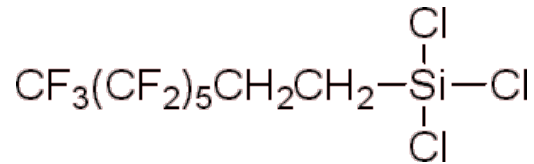$$CF_3(CF_2)_5CH_2CH_2-\overset{\displaystyle Cl}{\underset{\displaystyle Cl}{Si}}-Cl$$

Figure 17: Example of a FSAM molecule: 1H,1H,2H,2H-Perfluorooctyl-trichlorosilane, also known as Trichloro(3,3,4,4,5,5,6,6,7,7,8,8,8-tridecafluorooctyl)silane or Trichloro-(1H,1H,2H,2H-perfluorooctyl)silane, with the linear formula $CF_3(CF_2)_5CH_2CH_2SiCl_3$ or $C_8H_4Cl_3F_{13}Si$.

The surface treatment should keep the anti-adhesive properties, even after thousands of imprints have been executed. Up to a thousand successful imprints with a fluorosilane-treated stamp have been reported [29]. With a good release layer, stamps have been reported to be self-cleaning [7, 5]. This is advantageous, as particles on the stamp or on the substrate are one of the main problems reducing the yield in nanoimprint lithography. Especially if particles on the stamp stay there, all following imprints will bear the defect. A self-cleaning stamp eliminates the need for expensive cleaning steps between imprints.

A rather interesting concept for a release layer has been presented by Profactor GmbH with a spin-on release layer material called BGL-GZ-83 [52]. In contrast to the conventional anti-stiction layer which mostly needs a vapor phase deposition in a nitrogen atmosphere, BGL-GZ-83 offers a simple approach at atmospheric conditions. The coating is less than 100 nm thick and reaches its full anti-stiction abilities eight hours after application. Depending on the resist and the cleaning process used for the stamp, one application of BGL-GZ-83 lasts more than 50 imprints.

Finally, low surface-energy material stamps have been reported [29, 28, 30], using (amor-

phous) fluorinated polymers, such as Tyflon. Some of them offer an additional advantage by being flexible, a feature that makes imprinting large areas easier. Various release layer approaches are listed in Appendix B.2.

5 Fabrication Equipment

This chapter describes the equipment used for fabrication, characterization, and testing of UV-NIL stamps. It is divided into three sections, dealing with imaging methods, as well as additive and subtractive processes, respectively.

5.1 Microscopes and Exposure Equipment

5.1.1 Scanning Electron Microscopy and Electron Beam Lithography

A scanning electron microscope (SEM) is a type of microscope in which highly focused electrons are used to image the sample. A schematic diagram of a SEM is shown in Figure 18. The electrons are emitted by a source, either by field emission or by a Schottky field emitting cathode. The electrons are accelerated by the acceleration voltage V_{acc} which is applied between the cathode and the anode and can be as low as $100\,\mathrm{V}$ and as high as $50\,\mathrm{kV}$.
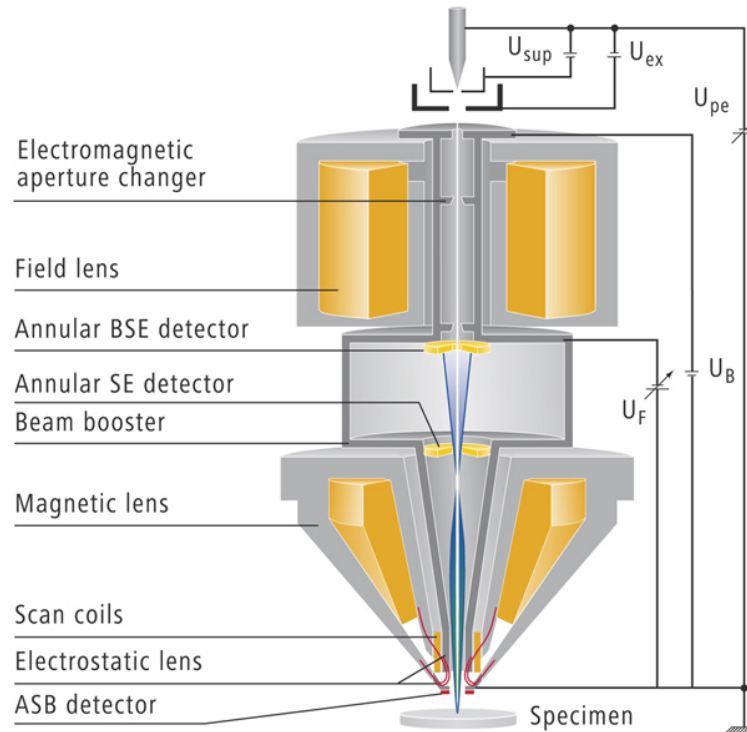

Figure 18: Schematics of an EBL system showing the operating principle of the GEMINI® field emission column used by the Zeiss Supra 40 SEM [12].

Focusing and demagnification of the electron beam can be achieved by using electron lenses, as depicted in Figure 18. Electron lenses can be implemented as electromagnetic or electrostatic lenses. Electrostatic lenses are faster, whereas electromagnetic lenses are more simple. The principle of operation is based on the Lorentz force due to the electric and magnetic fields acting on the electrons. Electron lenses have poorer performance than lenses used for light due to spherical and chromatic aberration. This means that the

electrons must be kept close to the optical axis, which limits the maximum write field size for which aberrations are still low [55].
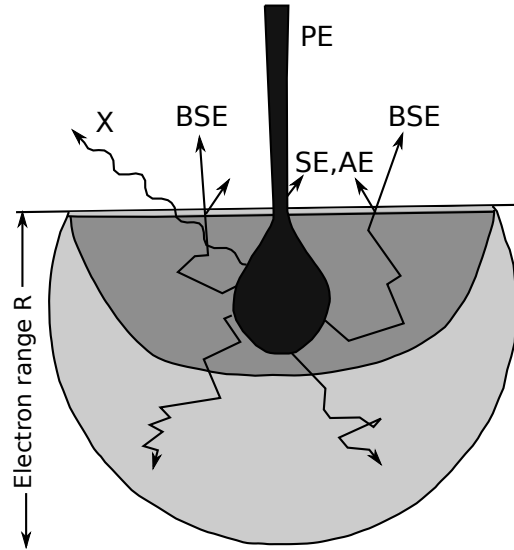

Figure 19: Origin and information depth of secondary electrons (SEs), backscattered electrons (BSEs), Auger electrons (AEs), and x-ray quanta (X) in the diffusion cloud of electron range R for normal incidence of the primary electrons (PEs). Adapted from Ref. [56].
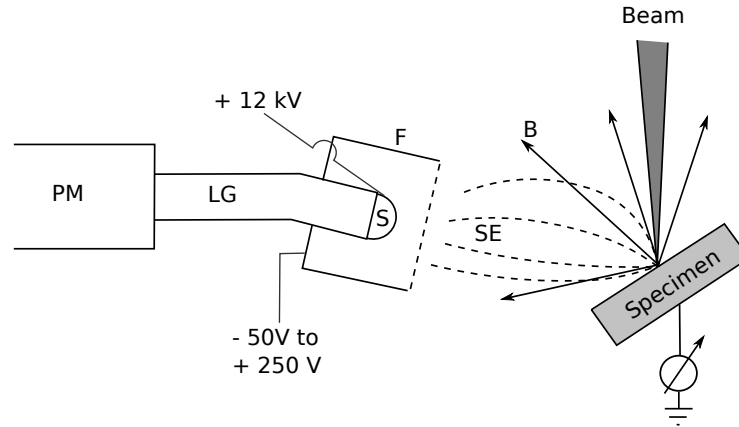

Figure 20: Schematic diagram of the Everhart-Thornley detector: BSE trajectories (B), SE trajectories (SE), Faraday cage (F), scintillator (S), light guide (LG) and photomultiplier (PM). Adapted from Ref. [26].

The primary electrons (PEs) hitting the sample create particles, mainly secondary electrons (SEs) and backscattered electrons (BSEs), as shown in Figure 19. From deeper areas of the sample x-rays are created. All of these scattered particles can be used for imaging [56]. Since SEs only image a thin layer on the sample surface, they mostly give information about the topography of the sample. In contrast, BSEs are created deeper in the material, and their scattering rate depends on the materials present , leading to higher contrast for materials of different atomic number [56]. SEs are collected using an

Everhart-Thornley detector, shown in Figure 20. (Secondary) electrons are collected by the (positively) biased grid and strike the scintillator (protected by a faraday cage from stray electrons), whereby light is emitted. The light is guided to a photomultiplier. The electrons are then used for producing an image of the sample [26, 56]. Depending on the bias of the grid, both SEs and BSEs can be collected.

An electron-beam lithography (EBL) system consists of a relatively high energy electron beam which is scanned over the surface of a resist coated sample which it exposes. Quite often, a SEM is upgraded to an EBL system by adding a beam blanker and some pattern generator software. Due to the shape of the electron beam, this type of system is often called a gaussian-beam direct write system. The beam exposes one pixel of the pattern at a time. This serial behaviour makes EBL a rather slow system on one hand, but on the other hand, it is possible to reach very high resolutions. The Zeiss Supra 40 SEM with the Raith Quantum pattern generator, which has been used as EBL equipment for this thesis, has a Schottky field emission tip with a beam spot capable of producing 2.1 nm resolution at an acceleration voltage of 1 kV and 0.8 nm at 30 kV. However, even though the nominal beam spot might be very small, scattering of the beam in the resist, chromatic and geometric aberration, as well as space charge effects lead to a higher effective beam diameter [20]. The resist is mostly exposed by the secondary electrons that are produced during forward scattering [22]. The scattered electrons cause proximity effects, leading to variations in linewidth depending on the local feature size [40]. Especially with dense features proximity correction measures become important, and the necessary calculation time additionally slows down the exposure process.

The simplest implementation of an EBL system consists of two deflectors, one of which blanks the beam and one of which scans the beam across the sample in a raster pattern. The beam is blanked in all areas that should not be exposed. As the beam can only be shifted over a limited area in this way, the sample stage has to be moved to access bigger areas. The area that can be exposed without moving the stage is called write field. Write fields are available in different sizes, depending on the magnification used. Generally, a smaller writefield gives a smaller step size which in turn leads to a higher resolution.

Another factor influencing EBL is the time required to expose the resist, which depends on the sensitivity of the resist and the total beam current on the sample. The beam current increases with the square of the aperture [55, 20].

The acceleration voltage that is applied to the column in order to accelerate the electrons defines the energy of the electron beam. Lower energy corresponds to lower penetration depth of the electrons, as well as clear surface structures, and less damage, charging, and edge effect. On the negative side, the resolution is decreased for lower acceleration voltages. Another tradeoff is necessary for the working distance (WD), which is the distance between the sample surface and the electron column. A small WD leads to high resolution and DOF and vice versa [55]. Regularily shaped dots over a writefield of 500 µm × 500 µm have been demonstrated with a high WD [49].

The number of electrons that hit the sample within a given area for fully exposing the resist is called the dose. The exposure dose depends on the beam current I (in nA), the dwell time t (in ms), and the step size Δx (in µm) according to the following formulas

$$\text{line dose} = \frac{It}{\Delta x} \tag{5}$$

and

$$\text{area dose} = \frac{It}{(\Delta x)^2},\tag{6}$$

where the area dose is given in $\mu C/cm^2$ and the line dose in pC/cm. The dwell time t influences the beam speed v via the relation $v = \Delta x/t$. For exposing gratings or other polygon-shaped patterns, the area dose is used. The line dose is needed for exposing text or single-pixel lines. For good pattern placement accuracy, line edge smoothness, and small feature sizes, it is recommended to (1) use a small write field size, (2) use a small step size, (3) use settling times of at least 2 ms, (4) use beam speeds of around 4 mm/s, (5) find a good focus point, and (6) use line mode instead of meander mode for exposing areas. For small features, it is additionally advantageous to employ a high beam energy and a small beam current, corresponding, as seen above, to a small aperture [55].

5.1.2 Nanoimprint Lithography Option for the Mask Aligner

The mask aligner MA6 from Karl Süss was used to test the imprinting process. It is equipped with a UV-NIL module, shown in Figure 21, which allows mounting of quarter-photomask plates and performing the imprint process. The mask aligner can deal with both transparent substrates that are imprinted with a silicon stamp, or non-transparent substrates that are imprinted with a transparent stamp, *i.e.*, a stamp made of glass or PDMS.

A quarter photomask plate is a piece of fused silica with dimensions of 6.5 cm × 6.5 cm × 6 mm. When used as a NIL stamp, it contains the patterns in the center area, which is elevated from the stamp surface by a 13 to 25 µm high pedestal. The stamp is fixed to the UV-NIL module and the stamp is positioned over the substrate, which is covered with a suitable imprint resist. After aligning the stamp with the substrate, a process with a specified accuracy of 0.5 µm, the imprint is performed. The stamp, held in place with a vacuum, is lowered onto the substrate, and the resist is given time to fill the structures. Once this process is completed, the resist is crosslinked by flooding it with UV-light having a wavelength of 365 nm, after which the stamp and the substrate are separated and the imprint is completed.

5.1.3 Atomic Force Microscopy

Atomic force microscopy (AFM) is a type of scanning probe microscopy that evolved from the scanning tunneling microscope (STM) and differs from it in the fact, that forces are measured [9] instead of the tunneling current. This allows examination of conductive as well as insulating samples. An AFM (schematically depicted in Figure 22) consists of a deflection sensor, a microfabricated tip on a cantilever and a movable stage. The sample on the stage is scanned by the tip attached to the cantilever. During scanning, the force between the tip and the sample is measured by monitoring the deflection of the cantilever [20, 11]. This is most often done with a position sensitive device (PSD) [20] that measures the deflection of a laser beam reflected from the probe. With a four quadrant PSD not only the vertical displacement, but also the twisting of the probe due to friction can be measured.

The operating principle of an AFM is based on the forces between the atoms of the tip and the sample (Figure 23). Those forces can, for example, be described by the Lennard-
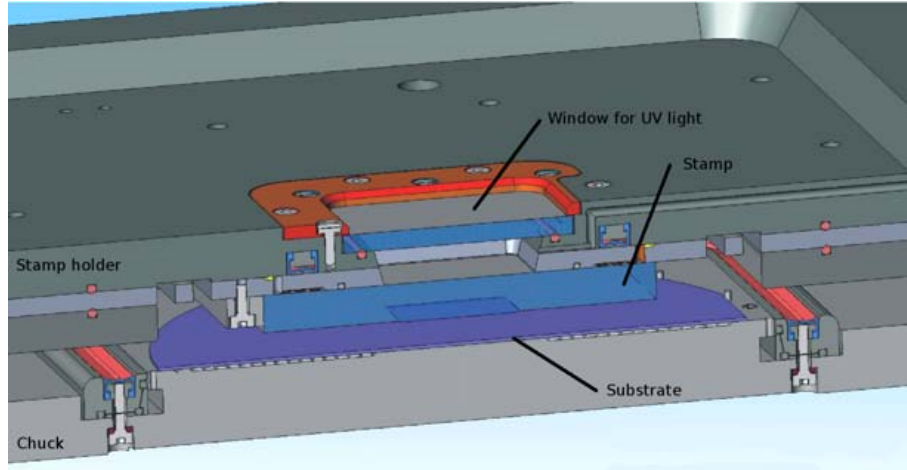
Figure 21: Cross-sectional view of the UV-NIL module of the mask aligner. Adapted from Ref. [67].
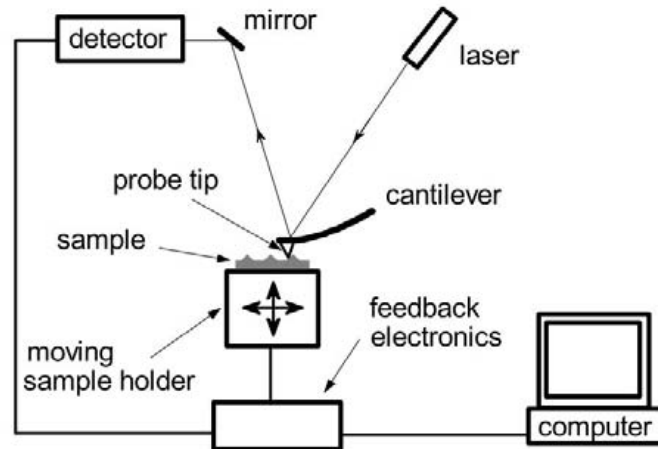

Figure 22: Schematics of an AFM system showing the main parts [2].

Jones potential [24, 20], which includes an attractive force term due to Van der Waals forces proportional to $-Ar^{-6}$ and a repulsive force term $+Br^{-12}$ due to Pauli's exclusion principle. The potential energy between the tip of the probe and the sample causes a deflection of F/k in z direction. The force F can be calculated, if the spring constant k of the (usually rectangular) cantilever is known. The spring constant for a cantilever with dimensions w, t and L is given by

$$k = \frac{Ywt^3}{4L^3},\tag{7}$$

where Y is the Young's modulus. A low spring constant leads to higher sensitivity which is usually preferred. For high resonance frequencies $f_0 = \frac{\omega_0}{2\pi} \approx \frac{1}{2\pi}\sqrt{k/m}$, the mass m of the cantilever should be low.

An AFM can be operated in several modes, the most important ones being contact, tapping and non-contact mode [20, 9, 10]. In *contact mode* the deflection of the cantilever versus its
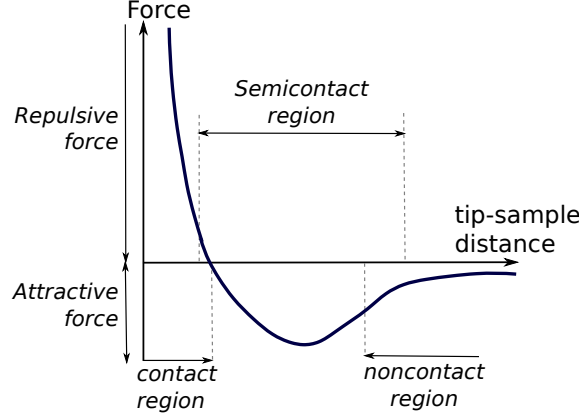
Figure 23: Forces modeled by a Lennard-Jones potential and their use in different AFM modes. Adapted from Ref. [38].

position on the sample gives a topographic image of the sample. The height is controlled by a feedback loop, which maintains a constant force between the tip and the sample. This leads to more controlled imaging conditions. This mode can achieve up to atomic resolution in the vertical dimension. However, the tip easily scratches the surface due to lateral forces.

In *non-contact mode* the tip is not in direct contact with the sample (good for soft samples). The resolution is not very high due to small variations present in the far-reaching forces.

For higher resolution the resonance frequency is often measured instead of deflection. As the cantilever is brought closer to the surface, the spring constant will change $k_{\text{eff}} = k - dF/dz = k - F'$ and with it the resonance frequency

$$\omega = \sqrt{\frac{k_{\text{eff}}}{m}} = \sqrt{\frac{k - F'}{m}} \approx \omega_0 \left[1 - 2\frac{F'}{k} \right]. \tag{8}$$

The force gradient F' contains the sample-tip distance. Constant oscillation frequency is maintained by adjusting the average tip-to-sample distance.

In *tapping mode* the tip is set to vibrate at an amplitude of about $10\,\text{nm}$ [20]. The tip oscillates near its resonance frequency with a constant amplitude. Interaction with the surface changes the vibration amplitude; thus, the force can be measured. The tip taps the surface gently, and scratching is considerably reduced compared to the contact mode. This mode is suitable for soft samples and still penetrates the thin water layer that may assemble on the sample surface [9].

A semi-contact mode Ntegra Probe NanoLaboratory was used to characterize the surface morphologies in this work. Surface roughnesses as well as the dimensions of the structures on several materials were measured. For small samples the universal measurement head was used, whereas a scanning head was used for characterizing the whole wafer after, for example, ITO deposition. The difference is, that the former uses a moving sample stage whereas the latter moves the measurement head while scanning.

5.2 Material Deposition

Methods to deposit dielectric and metallic thin films play a central role in numerous microfabrication processes. Deposition of thin films from the gas phase can be divided into two major categories, physical vapor deposition (PVD) and chemical vapor deposition (CVD). PVD techniques need a direct line-of-sight [22], so that the materials can move from the source to the sample without being obstructed. CVD, in contrast, uses a diffusive-convective transport of gaseous precursors that form layers on the substrate at temperatures between 100 °C and 900 °C [22].

PVD processes used for fabricating samples in this thesis include thermal evaporation and sputtering. The CVD processes used include plasma enhanced chemical vapor deposition (PECVD) and atomic layer deposition (ALD).

5.2.1 Thermal and Electron Beam Evaporation

Thermal evaporation, one of the oldest film deposition methods [40], is based on the heating of a source material at very low pressures ($<10^{-5}$ Torr [7]). The source material is heated up to the point at which it starts to evaporate. The low pressure conditions inside the evaporation chamber ensure that the evaporated-molecule plume can travel unobstructedly through the chamber and is deposited on the sample surface. Furthermore, low pressures prevent deposition of contaminants which could otherwise be included into the plume via foreign molecules present in the chamber [40].
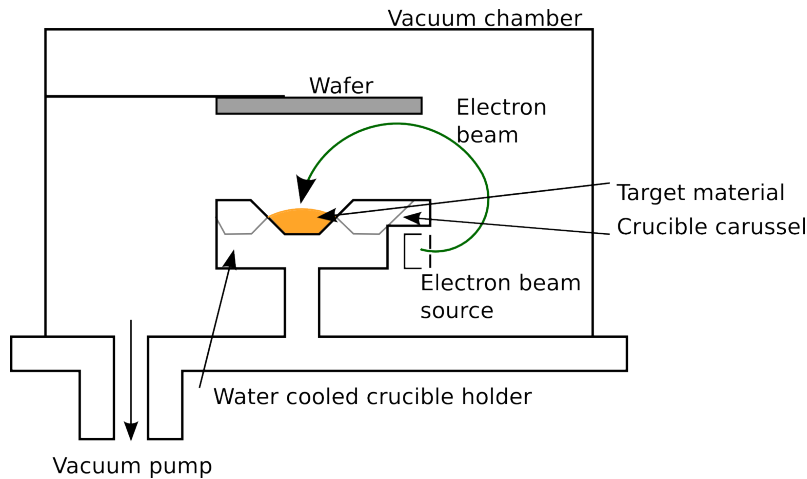

Figure 24: Schematics of an e-beam evaporation reactor.

Evaporation of the source material is usually done via resistive heating or by an electron beam. In resistive heating the current through a filament heats the substance to be evaporated. This easily deposits contaminations from the filament material together with the target material.

A less contaminating method is electron-beam evaporation [40], which is depicted in Fig-

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[7]At a pressure of 10^{-5} Torr, the mean free path in air is about 5 m. This is higher than the average distance between the source and the wafer (usually less than a meter) and ensures that the material will deposit onto the sample without colliding with other gas molecules.

ure 24. An electron beam is directed onto the crucible, in which the material is locally heated and evaporates onto the sample positioned above it. Due to the local heating, the vessel is not hot enough to emit material, leading to a much cleaner deposition. However, the e-beam can induce substrate damage by x-ray radiation if the intensity of the e-beam gun is too high [40].

Thermal evaporation is a highly directional process, so uniform coverage of three-dimensional structures is very difficult [40]. This lack in conformal covering makes thermal evaporation perfectly suited for lift-off processes.

5.2.2   Sputter Deposition

Sputtering is a material deposition technique in which the material deposited on the substrate (situated on the anode as shown in Figure 25) is sputtered from a negatively biased target (at the cathode) bombarded with positive gas ions [40]. Sputtering can be used for a wider range of materials than thermal evaporation. Moreover, it has a better step coverage and usually the adhesion of the films to the substrate is better. The superior adhesion is due to the high energies of between 10 and 100 keV with which the ions are ejected from the sputter target. The ions can penetrate into the surface of the sample, thus increasing adhesion [40].
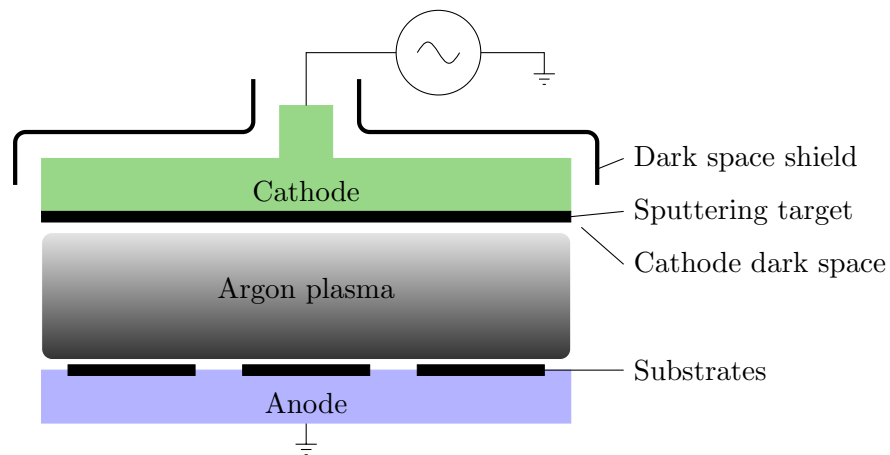

Figure 25: Schematic illustration of a RF-sputtering system.

The film properties can be controlled via the applied bias voltage, the pressure and the substrate heating. Sputtering is a rather slow process, and needs a high vacuum to keep the mean free path for the ions as long as possible. The following equation describes the amount of material sputtered, W,

$$W = \frac{kVi}{P_T d},$$
(9)

where P_T is the gas pressure, d is the anode-cathode distance, V is the working voltage, i the discharge current and k a proportionality constant.

An Oxford 400 DC magnetron sputtering system with four targets was used for depositing chromium. In this system only metals are allowed, although it could also process indium tin oxide.

5.2.3   Plasma Enhanced Chemical Vapor Deposition

An Oxford Plasmalab 80+ system has been used for plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 , and this system is schematically depicted in Figure 26. The setup is similar to the one employed in RIE reactors. A radio-frequency (RF) electric field ionizes the reactant gases which enter the chamber via the showerhead top electrode. The bottom plate is usually grounded to avoid high-energy ion bombardment from the plasma [40], and the bottom electrode includes a heater for substrate temperature control. Temperature control is necessary because the temperature of the substrate influences the uniformity of the deposited films. The deposited films are non-stoichiometric, as the deposition reactions vary widely. Film deposition involves almost exclusively neutral species, although the plasma also contains ions and electrons. Bombardment by ions may change the deposition of the film and generally increases its quality [40].
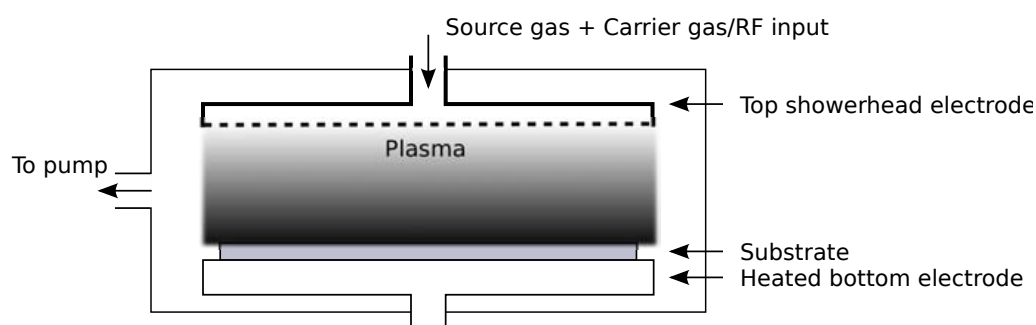

Figure 26: Schematic illustration of a plasma CVD system.

Achieving films with low stress and high quality demands controlling the properties of the plasma, which depend on the reactor pressure, RF frequency, RF power, and growth temperature in order to increase the ion bombardment. A low reactor pressure means a longer mean free path. Consequently, ions can gain more energy while being accelerated towards the sample, increasing film quality. However, if the pressure is too low the defect rate will increase as well because the process changes to physical vapor deposition. At frequencies higher than the ion-transition frequency, ions can not follow the changing field anymore and experience only the time average of the RF amplitude. Thus lower frequencies increase the ion energy. Increasing RF power leads to more intense ion bombardment due to the increase in ion current which also increases the deposition rate. There is no easy rule to determine the required RF power; it has to be chosen by evaluating the ratio of power density to deposition rate. The last important factor is the growth temperature. High temperatures with low growth rates lead to fast surface diffusion in relation to the incoming flux. The adsorbed species have time to diffuse to step growth sites and can form single crystalline materials. [40]

5.2.4   Atomic Layer Deposition

Atomic layer deposition (ALD) is a cyclical CVD process, in which the precursors are strictly separated from each other and thus self-limit the reaction to one monolayer. The precursors are pulsed alternately and the reactor is purged with an inert gas in between [59, 53, 2]. The growth process consists of four steps [53] as depicted in Figure 27: (1)

a self-terminating reaction of the first reactant (A), (2) a purge or evacuation to remove the non-reacted reactants and the gaseous reaction by-products, (3) a self-terminating reaction of the second reactant (B), or another treatment to activate the surface again for the reaction of the first reactant, and (4) a purge or evacuation. These four steps constitute a reaction cycle. Each reaction cycle adds a given amount of material to the surface, known as the growth per cycle. To grow a material layer, reaction cycles are repeated until the desired amount of material has been deposited.
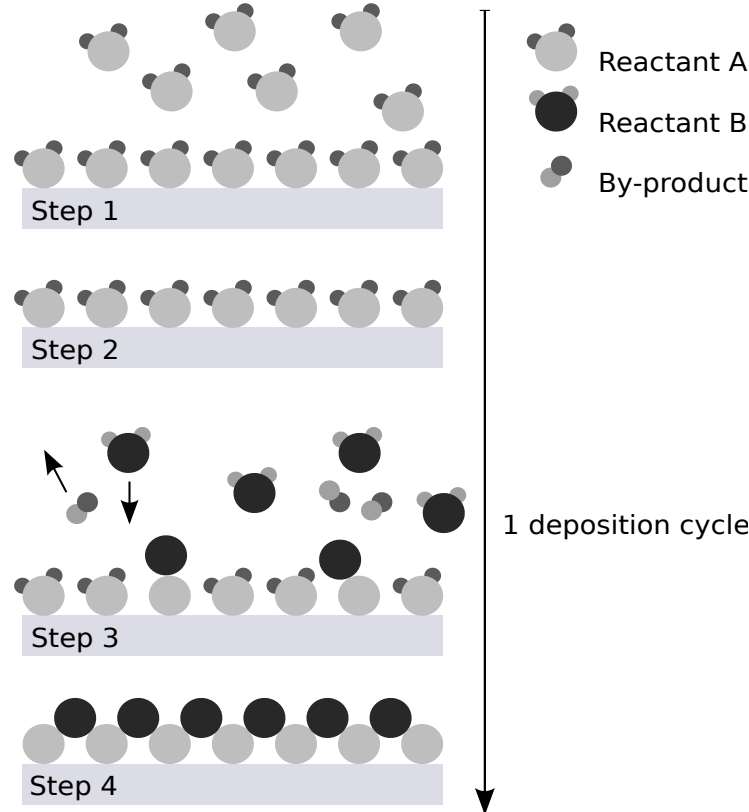

Figure 27: A schematic representation of the basic principle of the ALD process.

ALD has several advantages [47, 59]. First, it has an accurate and simple thickness control which is not related to the reactant flux homogeneity. Second, the material composition can be controlled on an atomic level. Third, due to the separation of the precursors, there are no gas-phase reactions. This allows using highly reactive gases for effective material utilization. Additionally, the processing temperature windows are often wide, making the process easy to control. Furthermore, the films produced by ALD are often very dense and perfectly conformal to the structures already present which is of great advantage to many applications.

5.3   Etching

5.3.1   Reactive Ion Etching

Reactive ion etching (RIE) is a plasma etching method in which plasma is created between two parallel plates by an RF power supply working at $13.56\,\text{MHz}$ and applied to the

bottom electrode while the top electrode is grounded [54] as is shown exemplarily in Figure 28. Accumulating electrons on the DC-isolated bottom plate create a negative self bias. The self bias exerts an acceleration voltage towards the bottom plate which is directly proportional to the ion density and thus cannot be controlled separately.
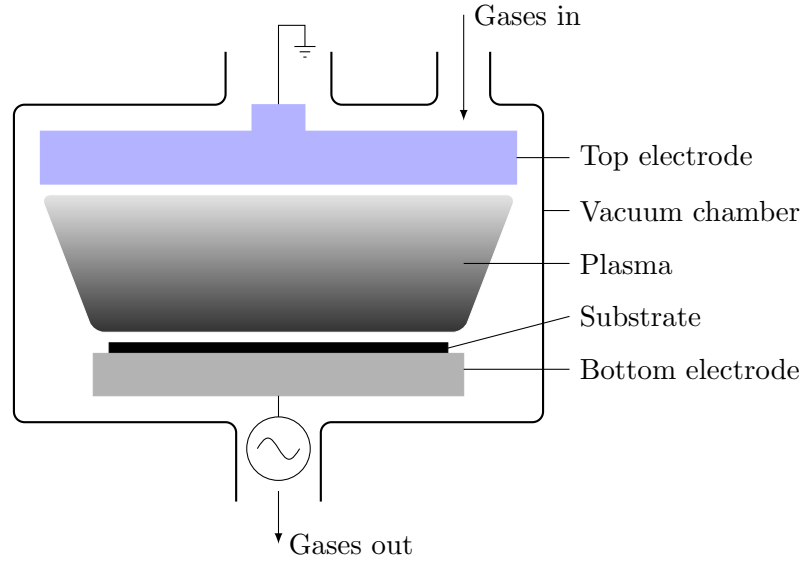

Figure 28: Schematics of an RIE system.

Figure 29 shows the most important steps in RIE: electrons in the plasma create ions which are accelerated towards the sample surface due to the self-bias of the bottom electrode. The ions are adsorbed on the surface, react with it and the reaction product desorbs and diffuses away.

In conventional reactive ion etching, high RF powers are usually used to maintain a reasonable etch rate and vertical profiles. This leads to bombardment of the samples with high energy ions which could result in device damage. Additionally, high pressure, typically above 10 mTorr, is needed to maintain a stable plasma. This could result in additional surface roughness and an undercut profile [54]. The problem of not being able to control ion energy and plasma density independently has been addressed by the invention of the ICP-RIE.

An Oxford 80+ RIE was used for etching. Mainly it was used for etching the SiO_2 layer after EBL in the ALD stamps, but also for transferring the imprinted patterns into the underlying substrate.

5.3.2 Inductively Coupled Plasma-Reactive Ion Etching

Inductively coupled plasma reactive ion etching (ICP-RIE) was invented out of the need to etch high-aspect ratios with dry etching. Dry etching using RIE had three problems [40]: (1) low etch rates, (2) the inability to maintain high aspect ratios over the etch depth of a few tens of microns, and (3) poor performance of masking layers. To overcome those problems, high plasma densities ($>10^{11} cm^{-3}$) to achieve high etch rates are needed while operating at low pressures (1 to 20 mTorr) to increase the directionality and discourage
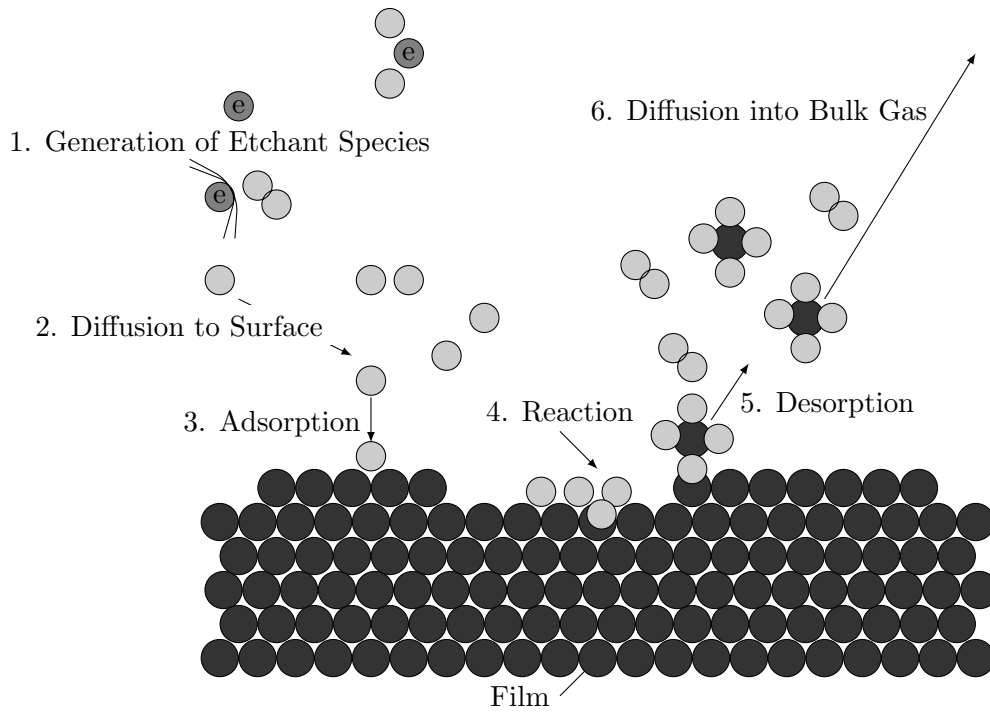
Figure 29: Main processes occuring in a plasma etch process. Adapted from Ref. [40].
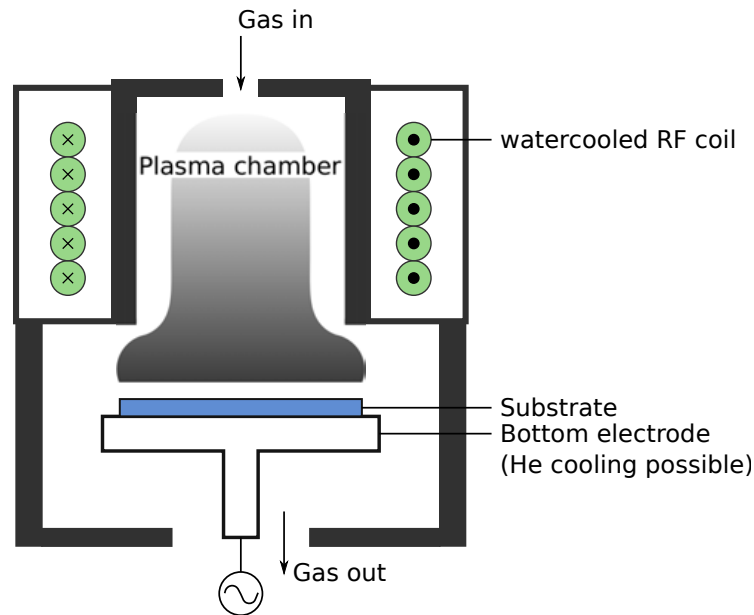
microloading [40, 70].

Figure 30: Schematic drawing of an ICP-RIE system.

An ICP-RIE consists of two chambers, the plasma chamber, and the sample chamber as seen in Figure 30. In the plasma chamber plasma is produced inductively with a power source operating at 13.56 MHz. The varying magnetic field induces a varying electring field

in the chamber, leading to ionization of the etch gases and formation of a high-density, low-pressure, and low-energy plasma.

The plasma is shielded from the electric field of the RF to avoid capacitive coupling, which tends to create higher energy ions. The electron density in such plasma sources reaches values $>10^{12}\,cm^{-3}$ [40].

A second RF source is used to accelerate ions towards the sample and to bias the bottom electrode on which the sample is located. This biasing directs the ions towards the sample for etching. The wafer chuck can be cooled with liquid nitrogen to temperatures of about $77\,K$ and this temperature can be maintained to achieve cryogenic etching [40, 62].

An additional benefit of ICP-RIE, as mentioned above, is that it avoids microloading or microtrenching [70]. Microloading is the vertical overetch that occurs at the foot of the sidewalls of the patterns during oxide etching. It is the result of the local accumulation of ions reflected on the sloped sidewalls that increases the etch rate locally. The effect of microloading is decreased in ICP-RIE in comparison to RIE due to the possibility of reducing the bias power while keeping the plasma densities constant.

6 Results and Discussion

This chapter begins with Section 6.1 introducing the UV-NIL stamp fabrication process used in the scope of this thesis. This includes remarks on the charge dissipation layer (Section 6.1.1), oxide pattern layer (Section 6.1.2), pattern fabrication (Section 6.1.3), and mesa etch (Section 6.1.4). Subsequently, Section 6.2 describes the imprinting process. Section 6.3 gives some useful advice on fabrication, and Section 6.4 presents results of the thesis. The chapter ends with Section 6.5 discussing the results.

6.1 Stamp Fabrication

Fabricating a stamp for UV-NIL is not as trivial as the fabrication of a T-NIL stamp that can use silicon. The difficulty is based on the fact, that the transparent substrates used for stamp fabrication are usually insulating as already mentioned in Section 2.3.2. For providing a conductive layer, several processes were explored during the course of the present thesis, although only one was tested for finally producing a stamp. This final process integrates a transparent conductive layer into the template, similar to the one described in Section 4.1.2.

A model of the final stamp used for imprinting is shown in Figure 31, and the fabrication process is given in full detail in Appendix A.
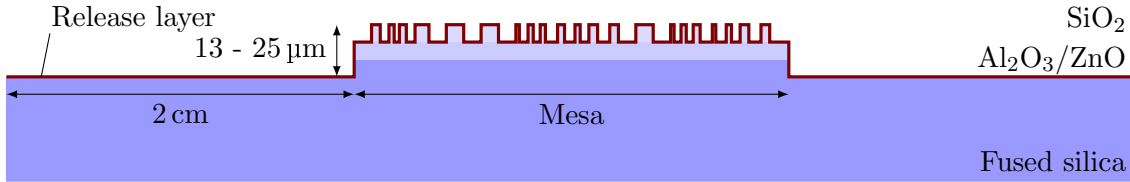

Figure 31: Final stamp structure. The nanostructures fabricated out of SiO_2 are located on top of the conductive layer of Al_2O_3/ZnO nanolaminate. The mesa is composed of the SiO_2, the nanolaminate, and the fused silica. The complete stamp surface is covered with the release layer.

6.1.1 Charge Dissipation Layer

Indium tin oxide (ITO) was first used as the transparent conductive oxide (TCO) layer as described in Section 4.1.2. About 70 nm of ITO was evaporated onto a blank wafer and then annealed in an oxygen-rich atmosphere at 350 °C for 30 minutes to provide the necessary transparency and conductivity. After annealing, the surface morphology of the sample was observed with an AFM. The AFM scans of the annealed ITO layers in Figure 32 show a surface roughness varying between 20 and 100 nm. Such a variation of surface roughness is considered to be high in the nanoimprinting process where the features to be imprinted can be of dimensions in the same range.

Pokaipisit *et al.* investigated the properties of ITO evaporated at 150 °C and annealed in air or vacuum. Their findings show that the resistivity of ITO films annealed in air decreases as the annealing temperature increases from 200 to 300 °C, and that the resistivity increases with a further increase of temperature up to 350 °C. For annealing in vacuum,
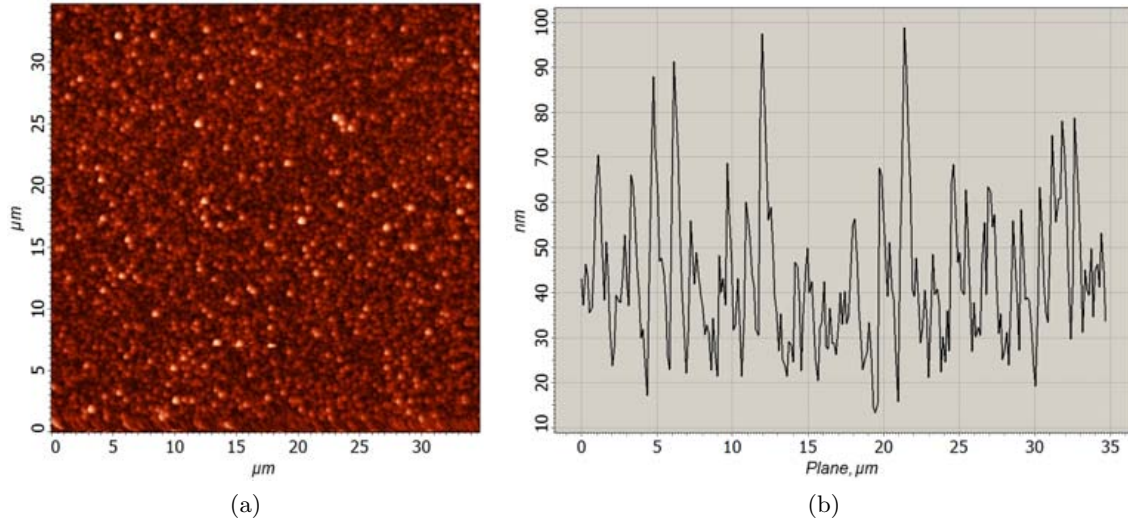
Figure 32: ITO surface morphology measured by an AFM: (a) 35 µm × 35 µm AFM scan of an ITO layer on sapphire and (b) the surface roughness profile along a line on the ITO surface.

the resistivity is decreasing over the whole range of annealing temperatures. The optical transmittance, however, increases for both cases with an increase in annealing temperature. The transmittance is highest with 83 % for annealing in air at 300 ℃. The sudden increase in resistivity above 300 ℃ is attributed to the introduction of oxygen, resulting in disturbed grains and defects in the ITO film. Oxygen deficiency, on the other hand, is the reason for the high conductivity of ITO [51].

Annealing also increases the grain size, although the increase is a bit less for films annealed in vacuum than in air. The ITO film appears to be nano-structured with an average grain size of about 40 nm. That size depends on the annealing temperature and is higher for higher temperatures [51]. Those values are similar to the ones obtained from Figure 32. As the annealing process was originally designed with conductivity and transparency in mind (and due to the lack of a vacuum oven), annealing took place in air.

In order to circumvent the large grain sizes, the fabrication process was switched to an Al_2O_3-ZnO sandwich structure fabricated by ALD. This ALD nanolaminate consists of 16 periods of 4-nm-thick ZnO and 3-Å-thick Al_2O_3 amounting to about 70 nm in total thickness. The thin layer of Al_2O_3 prevents ZnO from crystallising, thus keeping the nanolaminate smooth. The higher smoothness is visible in both the SEM image of Figure 34 as well as the AFM scan of Figure 33. The material has sufficient conductivity because ZnO is a II-VI semiconductor with good conductivity and transparency.

On one of the two stamps that were fabricated, pure ZnO was deposited instead of the nanolaminate due to an error in the ALD operation. This did not seem to have any influence on the conductivity or granularity of the surface. The other stamp used 70 nm of the nanolaminate as intended.
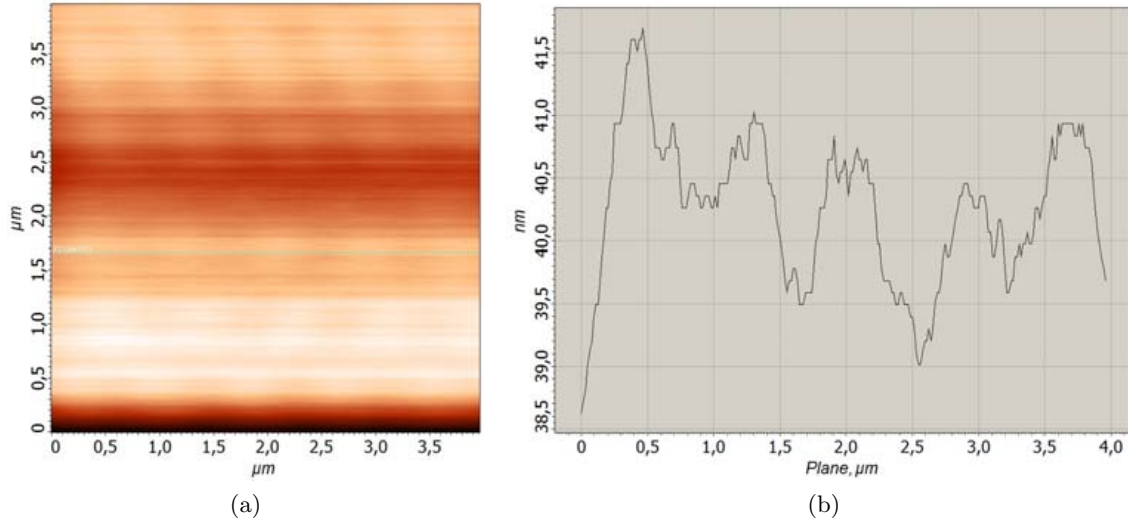
(a) (b)

Figure 33: (a) 4 µm × 4 µm AFM scan and (b) the corresponding line profile of the ALD nanolaminate showing a negligible surface roughness.
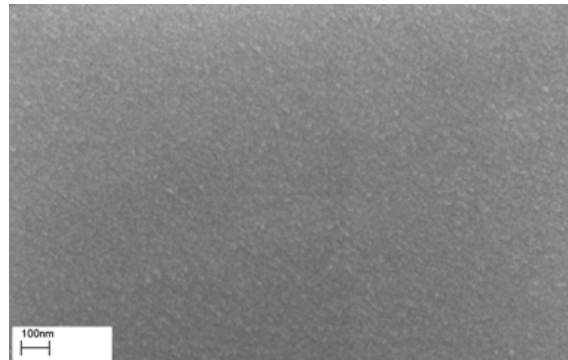

Figure 34: SEM image of the ALD nanolaminate layer. The surface is visibly smoother than that of the ITO or SiO_2 layers in Figure 38.

6.1.2 Oxide Pattern Layer

The next step involved in the fabrication of the stamp was the deposition of about 200 nm of SiO_2 using PECVD. The compatibility to the TCO and the surface roughness of SiO_2 layers were investigated because the final nanostructures of the stamp are patterned out of them. Initial tests were executed with SiO_2 deposited on annealed ITO layers.

Several different recipes were tested on the ITO layers, including "SiO_2 base" at a deposition temperature of 300 °C, "SiO_2 stress controlled" and "SiO_2 22 nm/ min". The details of all these recipes are given in Appendix A.1.

Figure 35 shows a PECVD SiO_2 layer on annealed ITO. It was observed that SiO_2 nucleates around the ITO grains. This results in a much larger grain size and, thus, an increased surface roughness. As illustrated by Figure 36, this leads to SiO_2 grains with similar dimensions to the nanostructures. Those grains are clearly visible after transferring the resist structures into the SiO_2.
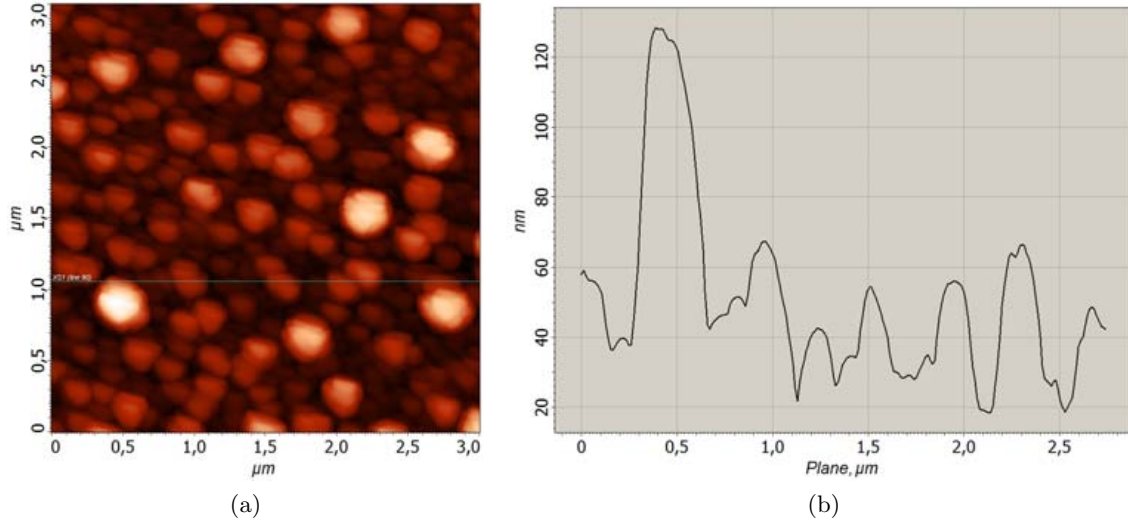
Figure 35: (a) $3\,\mu m \times 3\,\mu m$ AFM scan and (a) a surface line profile of a $200\,nm$ thick PECVD SiO_2 "SiO_2 $22\,nm/\min$" recipe on annealed ITO.
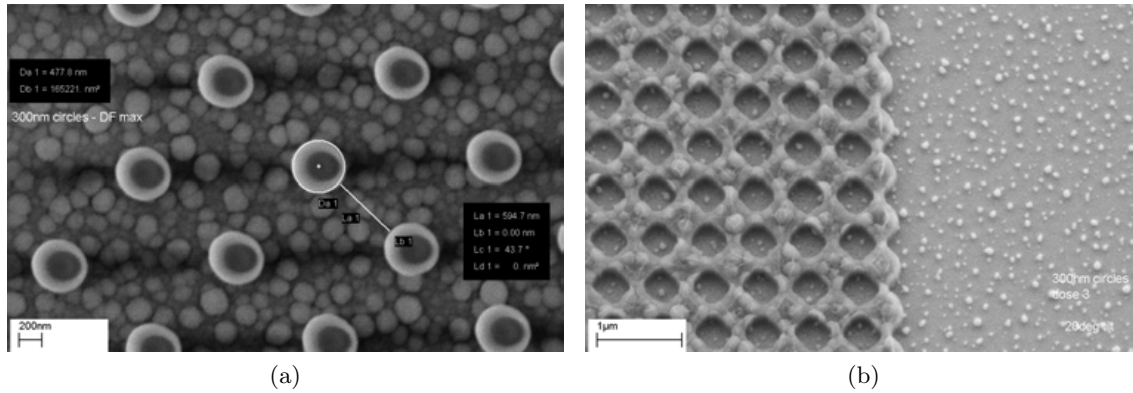

Figure 36: (a) Top-view SEM image of EBL-patterned resist dots of about $480\,nm$ in diameter displaced about $600\,nm$ apart showing the grain size of SiO_2-on-ITO in comparison to the size of the structures. ITO was evaporated for $130\,s$ and the "SiO_2 $22\,nm/\min$" recipe was used for SiO_2 deposition. (b) Top-view SEM image of structures after pattern transfer into the SiO_2 on the same substrate shows that the SiO_2 grains are clearly visible in the etched structures.

This high surface roughness led to the preparation of separate tests to investigate the properties of silicon dioxide. SiO_2 was deposited with three different recipes on blank sapphire wafers. The recipes were "SiO_2 base $170\,°C$", "SiO_2 stress controlled", and "SiO_2 Tapio $200\,nm$". Figure 37 shows the AFM scans from these samples, and Figure 38 presents SEM micrographs of two of those layers. All three of them promise better properties than the "SiO_2 $22\,nm/\min$" recipe used earlier. In contrast to the initial tests, the new ones were also executed at lower temperatures. Although temperatures below $300\,°C$ usually give low quality films, in this case they helped to increase the smoothness of the deposited SiO_2.
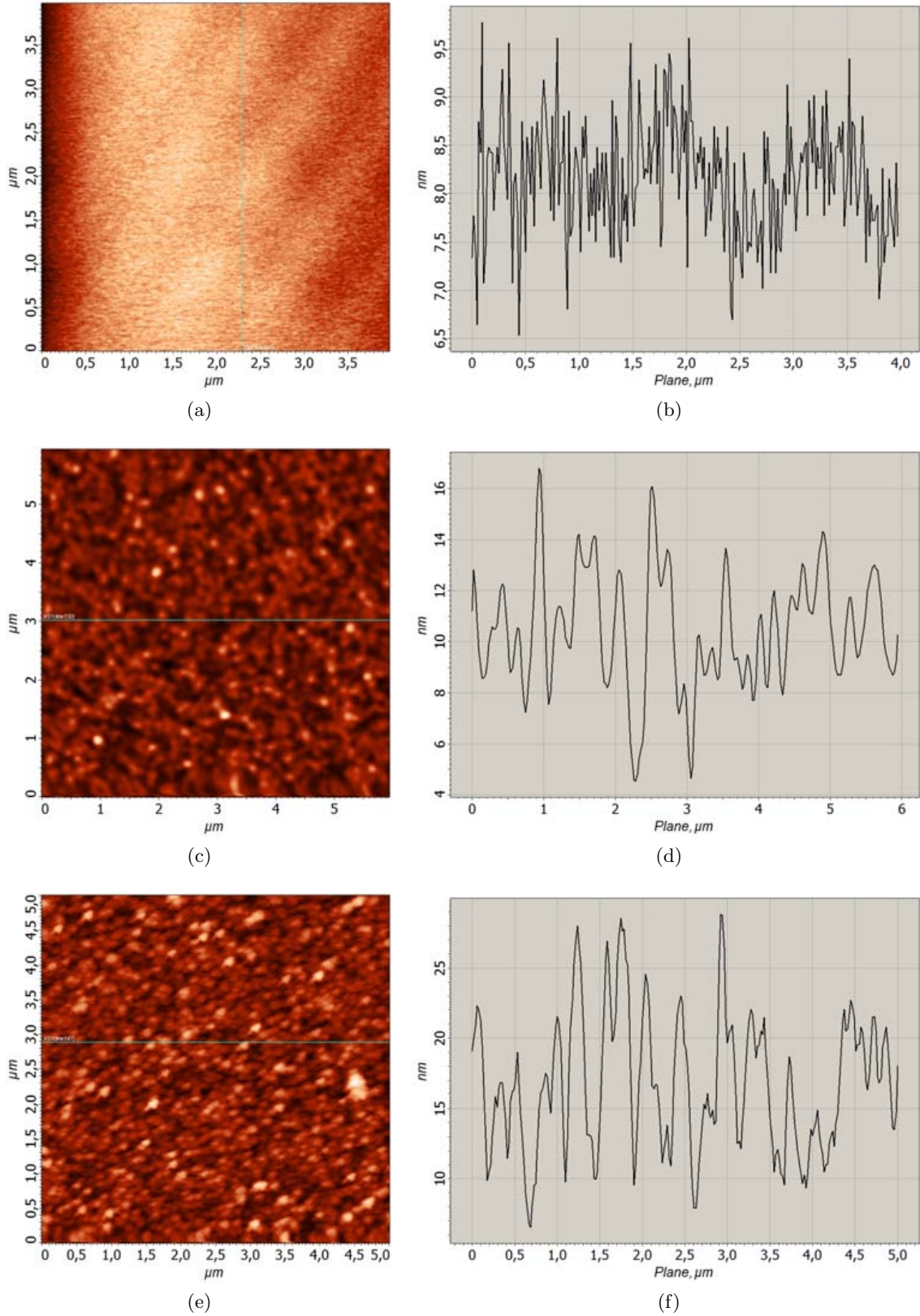
Figure 37: AFM scans (left) and the corresponding line profiles (right) from the SiO_2 test samples fabricated by PECVD recipes: (a,b) "SiO_2 base 170 ℃", (c,d) "SiO_2 stress controlled", and (e,f) "SiO_2 Tapio 200 nm".
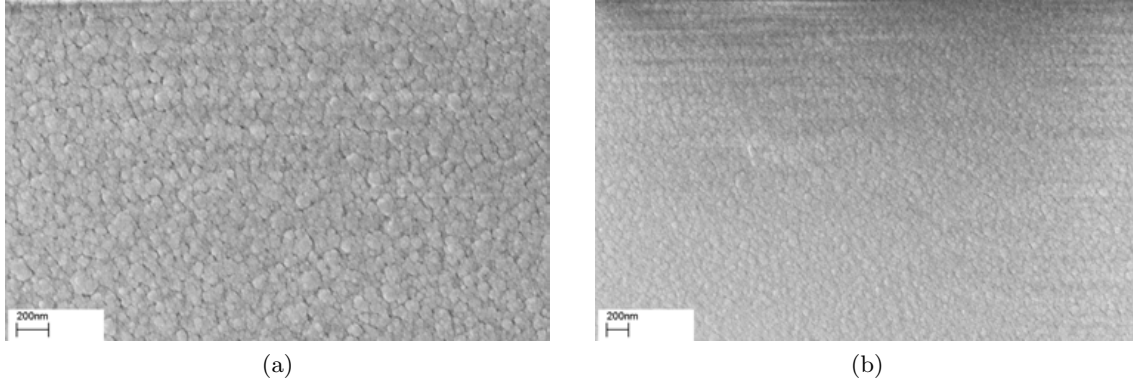
(a)   (b)

Figure 38: SEM images of (a) SiO$_2$ layer deposited with the recipe "SiO$_2$ base" at 190 °C and (b) SiO$_2$ deposited with the recipe "SiO$_2$ stress-controlled" at 200 °C.

Our experimental results demonstrate that the adhesion of SiO$_2$ to the annealed ITO is very good. This is illustrated in Figure 39. Good adhesion is obviously advantageous when working with multilayer structures.
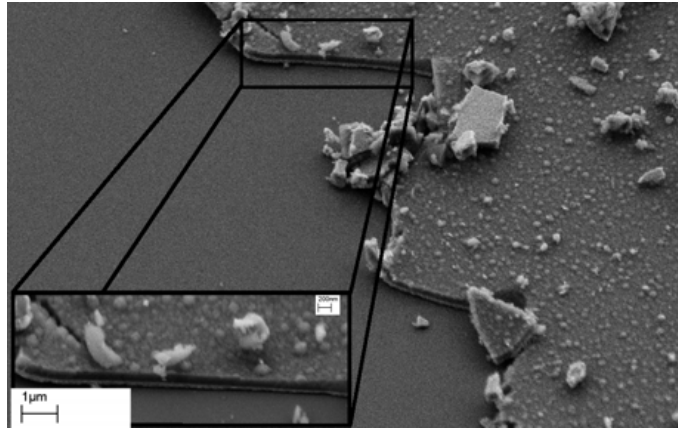

Figure 39: Adhesion of SiO$_2$ to ITO. The sandwich structure of 70 nm ITO and 200 nm SiO$_2$ is clearly visible, and it is a bit detached from the sapphire substrate due to an intentional scratch made. The micrograph is taken with a tilted stage to better see the layers. The recipe "SiO$_2$ base at 300 °C" was used in PECVD.

Finally, for the stamp fabrication the recipe "SiO$_2$ Tapio 200 nm" was chosen to deposit SiO$_2$ on the Al$_2$O$_3$-ZnO nanolaminate at the temperature of 200 °C.

6.1.3   Pattern Fabrication

On top of the SiO$_2$ layer a chemically enhanced negative EBL resist (see Appendix A.4 for more details) is spun. Spinning lasted 45 s at 6000 rpm and a cover was used to allow spinning to a lower thickness as the cover prevents the quick evaporation of the solvent. This resist was chosen because it is a negative resist that is not sensitive to UV light, meaning that no special precautions are necessary when handling it. The resist is then pre-baked for 30 min in a convection oven at the temperature of 85 °C. The pre-bake step

evaporates the solvent of the resist and prepares it for EBL.

The resist was exposed in the Raith EBL-system described in Section 5.1.1. The exposure was done at an acceleration voltage of 4 kV with an aperture of 20 μm and a beam current of about 0.030 to 0.045 μA. The exposure of the used resist usually demanded doses of 5 to 12 μC/cm²[8], depending on the density of the structures patterned and their dimensions. Lines, text, grids, and circles formed the different structures exposed.

After exposure the samples were post-baked in a convection oven at 95 °C for 30 min to cross-link the polymers in the resist. Afterwards the sample was developed in pure AR 300-46 (Allresist, Germany) for 60 s, rinsed with de-ionized water (DIW) and blow dried with N_2. The patterns were inspected under an optical microscope and by SEM. Some images of the patterns directly after development are given in Figure 40.

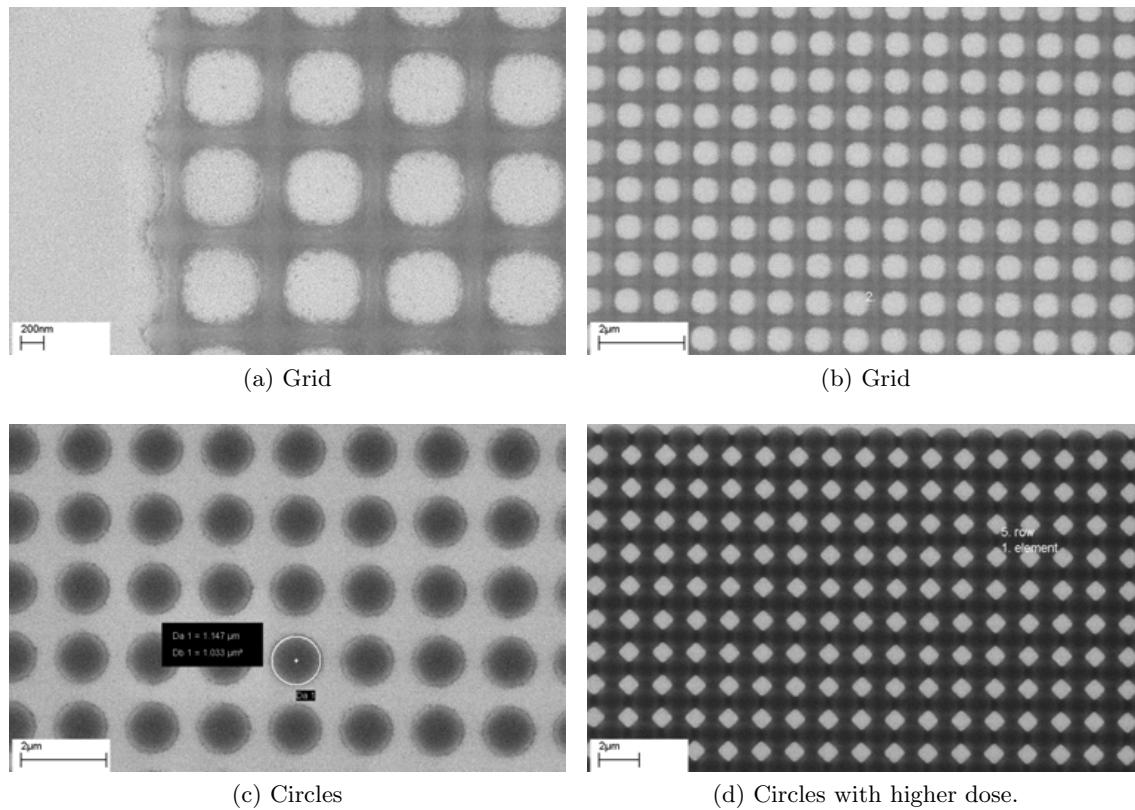(a) Grid

(b) Grid

(c) Circles

(d) Circles with higher dose.

Figure 40: SEM images of the resist patterns on the stamp directly after development but before the plasma etch step. Inspection in a SEM is easy due to the TCO layer.

Subsequently, the SiO_2 layer was dry-etched in a reactive ion etching (RIE) system. In this process, the resist acts as a mask to etch the SiO_2 layer. To enhance the etch-resistivity of the resist, a hard-bake at 130 °C can be executed. In the case that some resist has to be removed after etching, the remover AR 300-70 containing N-Methyl-2-pyrrolidon (NMP) is used. Figure 41 shows some SEM images of the structures after plasma etching.

The conducting layer stays part of the sample, thus allowing easy inspection of the stamp features without the need of evaporating metal to avoid charging.

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[8]For PMMA, for example, the correct dose would be much higher, around 70 μC/cm².

(a) Circles

(b) Lines
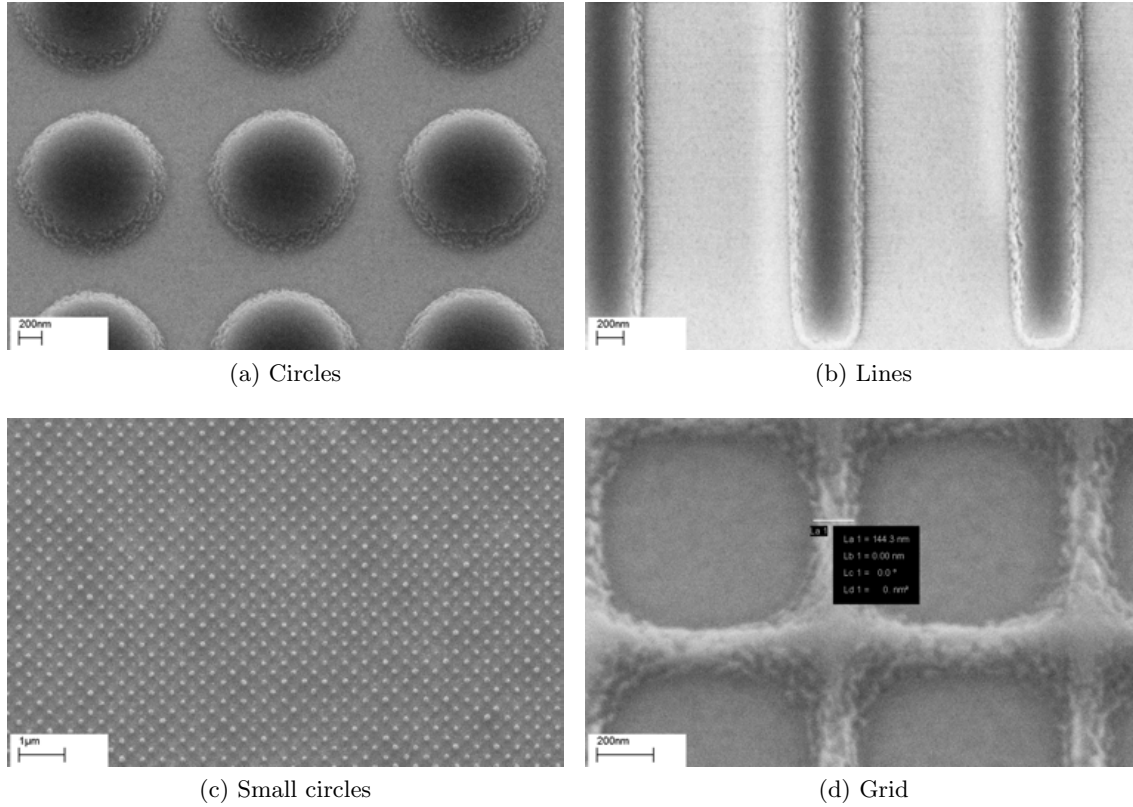

(c) Small circles

(d) Grid

Figure 41: SEM images of the SiO_2 structures on the stamp after plasma etching.

6.1.4 Mesa Etch and Release Layer Application

The stamp fabrication is finished once the mesa etch step is executed. This is a rather complex etch step, involving etching about 15 μm to 25 μm of fused silica. The wafer preparation was similar to the one described in Section 4.2. Slight adjustments were made to the process concerning baking times and temperatures because a vacuum oven was not available. The stamp was cleaned, dehydrated, and coated with conventional AZ5214e photoresist. The optical lithography to define the mesa was executed using a self-made plastic mask.

After development and more dehydration bakes (the complete process details are given in Appendix A.2), the stamp was immersed into a buffered HF (BOE) solution, which was magnetically stirred, for 10 min. BOE ensures a more controlled etching than pure HF, because the etch solution does not exhaust itself over the time of a long etch step. With a profilometer, the step height was measured after 10 min to determine the etch rate. Assuming that the resist does not get removed by HF, the etch rate is calculated by comparing it to the profilometer curve from before etching. For a desired step height of 15 μm, an etch time of about 3.5 h was determined. This is about half of the currently demonstrated practical limit of 33 μm with a single photoresist mask.

The etch resulted in a pedestal of about 13 μm in height on the first stamp, which proved sufficient for imprinting. The borders were not sharply defined. This could be due to the self-made plastic mask or due to underetching on the resist-glass interface. Furthermore,
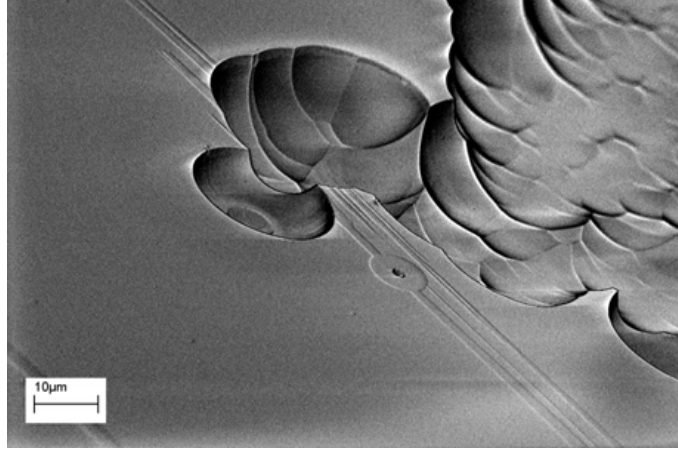
Figure 42: SEM micrograph of craters due to BOE etching on the fused silica surface. In the foreground is the mesa, which has one circular hole and is connected to the lower area. The surface roughness in the top right corner is also due to etching. The image has inverted colours, to clearly show the holes.

the stamp exhibits several pinholes in the mesa area, especially near the borders. In those places the HF solution managed to penetrate through the depleted resist and attack the glass. Luckily, none of the holes affected any of the structures. The slow breakdown of the resist was already visible after 3 h of etching, as craters were formed inside the mesa area and on its border. An example of the emerging pinholes is illustrated in Figure 42.

As a last step in the stamp fabrication the release layer BGL-GZ-83 (Profactor, Austria) was applied. The process steps for this phase are specified in Appendix A.3.

6.2   Imprinting Process

AMONIL MMS 4 (AMO GmbH, Germany) was used as an imprinting resist. This resist is specified to give a 200 nm layer when spun at 3000 rpm. The process details are given in Appendix A.5.

For the imprinting process, first the stamp is mounted in the appropriate holder. It is held in place both mechanically and by vacuum. The resist-covered substrate is put on a special wafer chuck, which is free of vacuum grooves in the imprint area and has some freedom to move, thus allowing better parallelization of the substrate and the stamp. The stamp in the stamp holder is then moved down for wedge error compensation (WEC), which is performed outside the mesa area between the stamp and the substrate. The height of the mesa is entered in the software, so that the distance between mesa and substrate is known.

After WEC, the stamp can be aligned to the substrate, if some structures are already present. Subsequently, the process chamber is evacuated, and the pressure chamber provides a controllable imprint pressure once the stamp has moved down. This pressure is exerted by N_2 flowing in the pressure chamber above the mask. After the specified imprinting time has passed, the resist is cured by UV radiation and the chuck moves slowly down to separate the substrate and the stamp.

6.3   Experimental Observations

The dimensions (65 mm × 65 mm × 6.35 mm) of the fused silica blank make many clean-room processes which are optimized for thin wafers unsuitable or more complex for stamp fabrication. Applying the ALD nanolaminate, for example, requires using a different process chamber to accomodate the stamp, and changing it takes about half a day. The evaporator, where the stamp would be held above the particle beam, is not usually equipped with holders supporting the weight and thickness. The same is true for the SEM, EBL, and spin coating. For those three processes specialized holders are needed to support the dimensions and the weight of the stamp. In EBL/SEM, the holder has to provide the desired flatness and charge dissipation from the sample. The spin coating chuck, on the other hand, has to provide support against the forces during spinning. Additionally, it needs a very flat surface in order to reach the necessary vacuum pressure.

RIE and PECVD are free from these problems, as the sample can just be put on the bottom electrode directly. In ICP-RIE, however, the blank would have to be balanced on an extended beam which fixes the blank with vacuum and then moves it in the actual process chamber. Apart from the square shape of the stamp, its height is also problematic here; especially as the plasma is designed to act on the surface of wafers about 5.5 mm thinner.

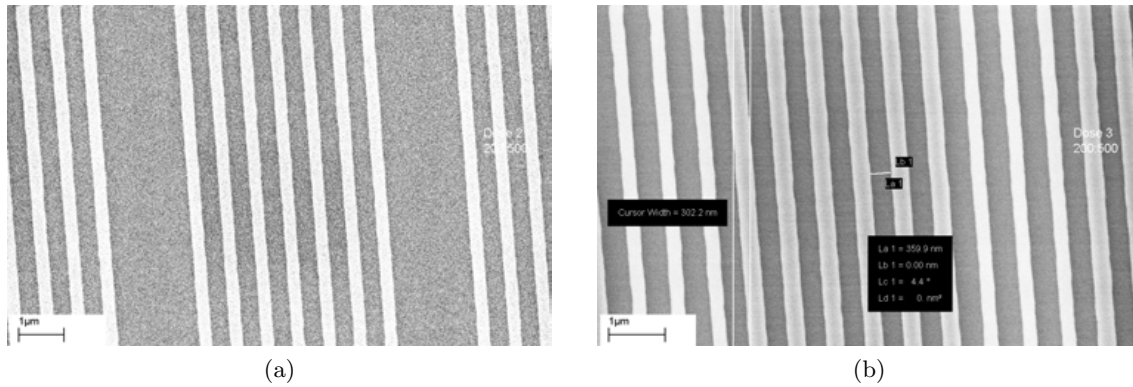(a)   (b)

Figure 43: Influence of the stepsize on the pattern. When the lateral pattern dimension is not an integer-multiple of the stepsize, an uneven dose distribution considering several lines. For too low of a dose, this leads to (a) missing lines, for sufficiently high doses it is seen as (b) a thinning of lines.

For EBL, there are many other things to take into consideration as well. For example the practical limitations of the writing process dictate that for a given writefield size w the minimal basic stepsize is given by $\frac{w}{2^n}$, where n is the number of bits. If the minimal stepsize for a 200 nm line is 0.044 μm, it would fit in 4.54 exposure runs. This implies, that some lines in the grating actually consist of 4 and some of 5 runs, thus giving way to a periodicity in the exposure than can be clearly observed in Figure 43 and is explained in Figure 44. Due to the lower dose, the sample in Figure 43a is missing some lines, where the accumulated dose was not high enough, to completely expose the resist. When defining the patterns to be exposed, one should always take care to adjust the pattern size to the step size used. An arbitrarily small step size is usually not possible, due to limitations imposed by the beam speed, which for clearly defined borders should be around 5 mm/s.
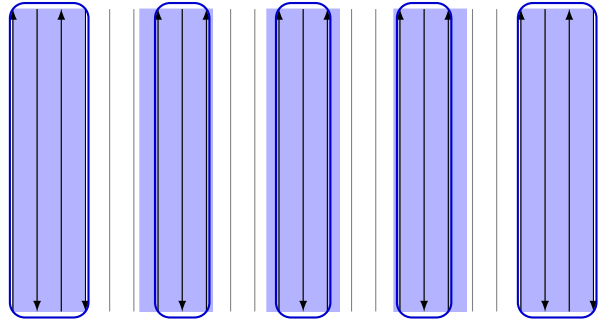
Figure 44: If the period of the pattern is not an integer multiple of the step size, the dose per area will vary over the exposed pattern, thus leading to a thickness variation over the pattern. This variation is indicated by the blue outline. The intended shape is indicated by the area shaded in light blue.

6.4 Imprinting Results

In the unpatterned areas of the stamp the filling of large cavities can be observed. Figure 45 demonstrates, that the resist first assembles in mounds on the substrate surface. Then the resist fills in along the mounds and via capillary forces around the borders. Given enough time, the area will close up until it is completely filled. This agrees with the findings from Section 3.

Imprinting has been tried on epi-ready sapphire wafers as well as processed wafers. The latter consist of a GaN on sapphire wafer, GaN with 50 nm of SiN, and a wafer having a rough p-GaN surface. Figures 46 and 47 show close-up views of different imprinted patterns. Figure 48 depicts an imprint from a stamp on which most of the structures were eroded due to overetching, rendering them hard to make out. The remaining low-height SiO$_2$ structures where nevertheless faithfully reproduced in the imprinting resist.

Figure 49 shows some SEM images of imprinted nanopatterns on sapphire taken under an about 80° from the top. In these micrographs, the 3D imprinting profile of the structures is visible.

Figures 50 and 51 show AFM scans of the imprinted patterns, comparing them to the corresponding SEM image of the structures. Finally, Figure 52 depicts imprinted structures that originate from a stamp area in which the structures were (due to etching) not as clearly defined as in those areas shown above.

6.5 Discussion

The acceleration voltage influences the minimum possible resolution. A higher beam voltage results in a better resolution. For the patterns in the stamp, both 4 kV and 10 kV were used, in comparison to 20 kV that is usually used for EBL. Using a voltage higher than 10 kV was not possible due to charging effects, even though a TCO layer was present.

One set of problem arises from the dimensions of the stamp. An area of 2.5×2.5 cm takes about 10 days to write if most of the area is covered. High coverage of the stamp surface with structures has two advantages. First, it is easier to find the structures again after imprinting and second, it makes filling of the cavities easier because there are no large
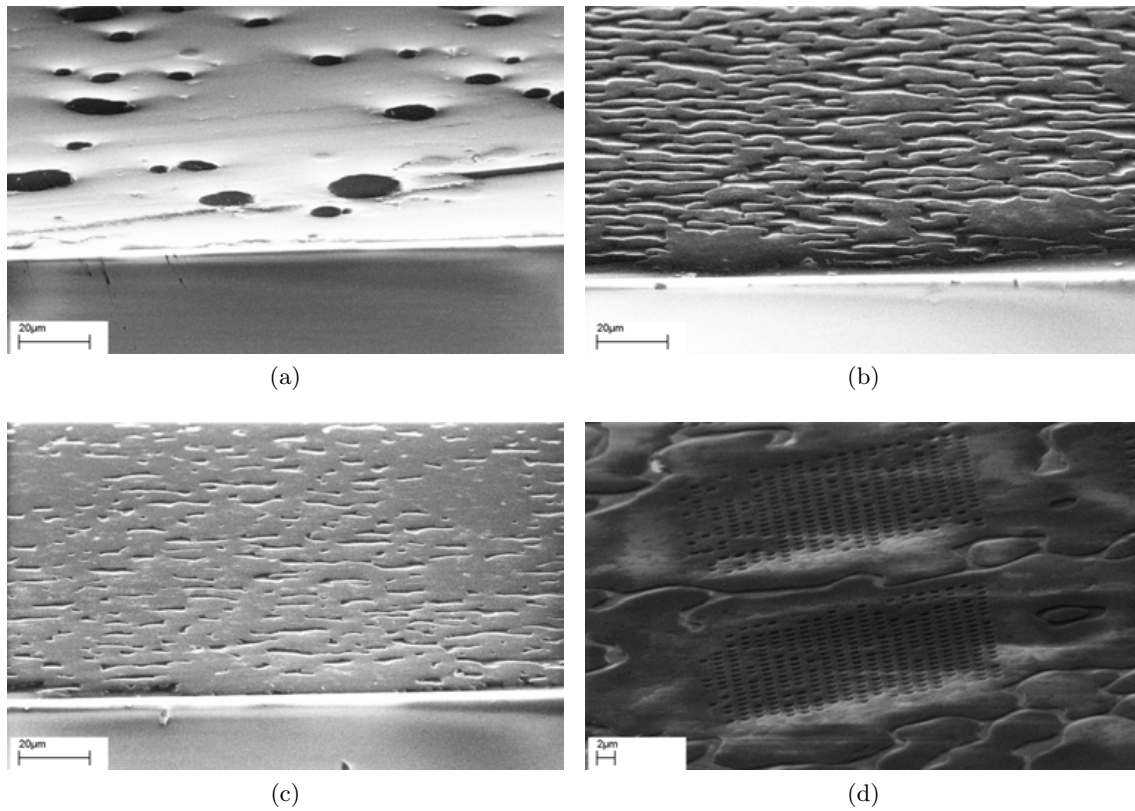
Figure 45: (a)-(c) Resist fills large cavities during imprint. Such large cavities exist, for instance, between nanopatterns in the unpatterned areas. The imprinting time is increased from the left to the right. (d) The filling of the cavities between two areas of patterns. The filling in the patterns is complete, and the polymer has almost completed the filling of the space in between. The images are taken from different imprinted samples.
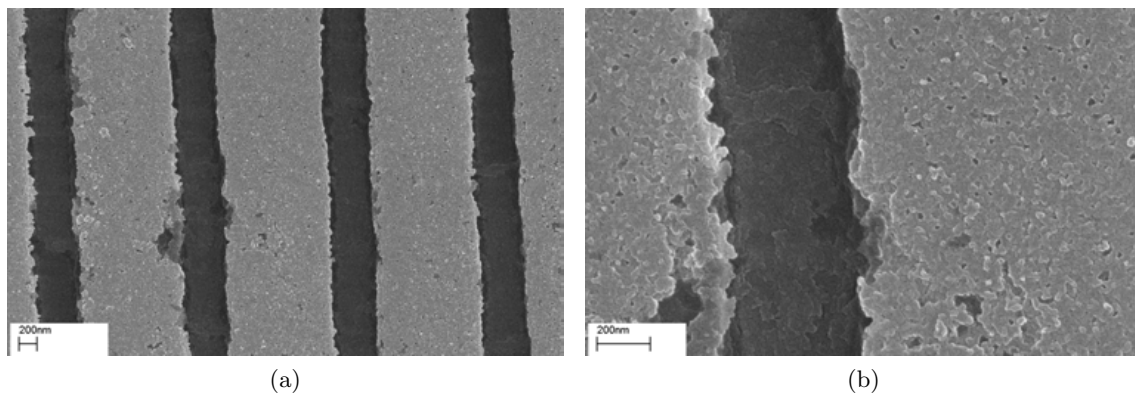
Figure 46: SEM image (a) of lines imprinted on SiN on a GaN substrate. (b) A close-up image of a single line.
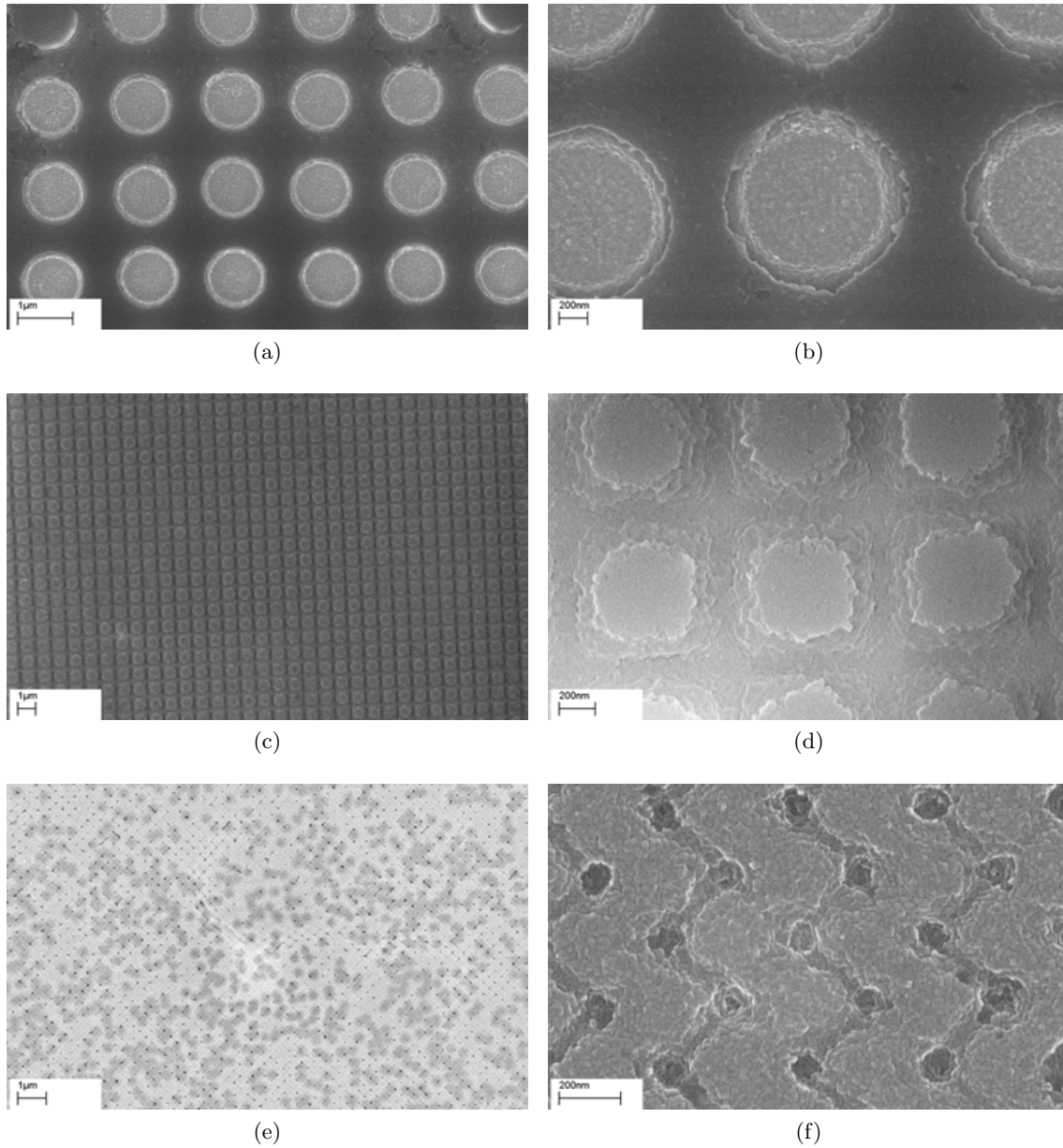
Figure 47: SEM micrographs showing (a) holes with a diameter of about 890 nm, (b) a close-up view of the previous structure, (c) cylinders imprinted via a grid of lines, and (d) a close-up view of few cylinders. The holes have been imprinted on a sapphire wafer, while the cylinders were imprinted on a GaN surface covered with 50 nm of SiN. (e) SEM image of an array of very small holes imprinted on a p-GaN wafer. The large gray spots in the background are due to the rough surface and are completely covered with resist. (f) A close-up view of the same structure on a plain sapphire wafer.
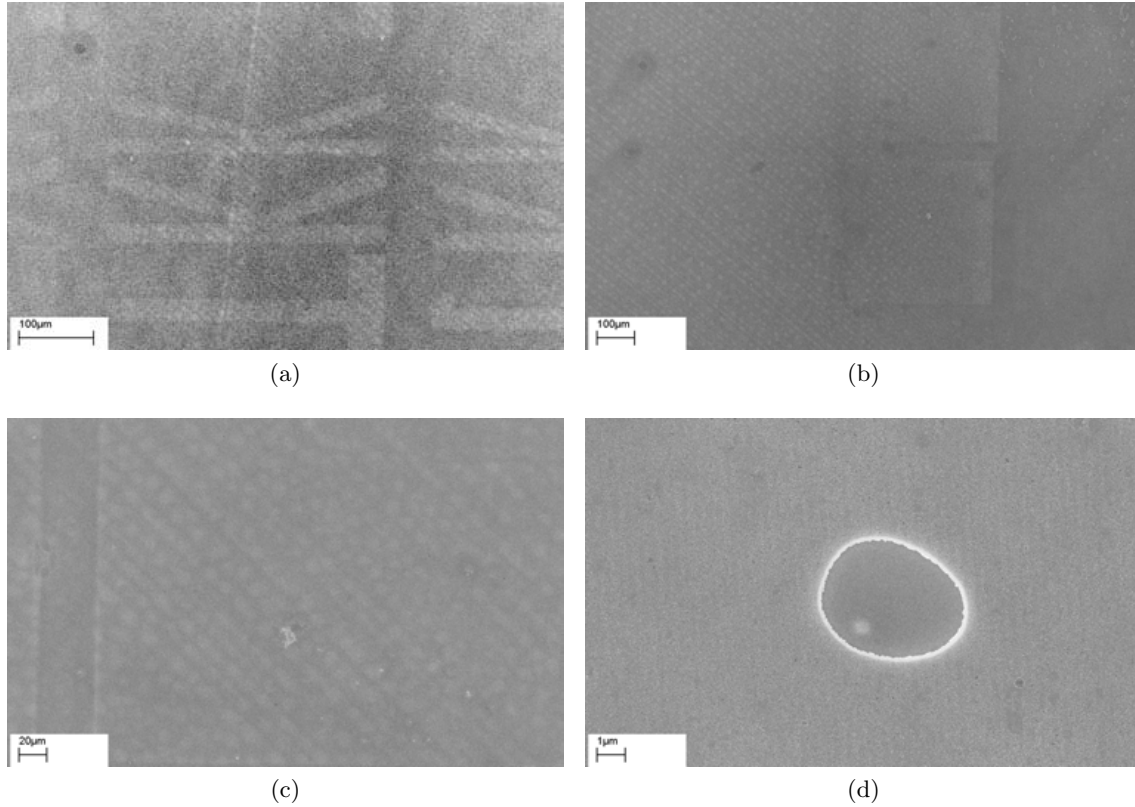
Figure 48: These SEM micrographs illustrate imprinting of structures that are almost invisible in the stamp. In (a) the letters TKK have been imprinted and can be seen, in (b)-(d) squares of lines are shown. Although the lines seem very washed out and faint, they are still reproduced. The imprint was done on a GaN on sapphire substrate.
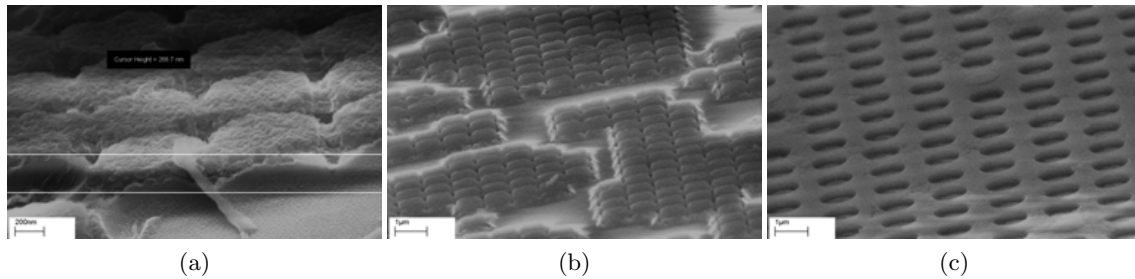
Figure 49: SEM image showing a side-top view of imprinted structures on a sapphire wafer. (a) and (b) show an array of dots, while (c) shows an array of holes.

cavities. Large cavities, as mentioned above, take long to fill. A writing time of ten days is rather long, especially, as it blocks the EBL for all the other users. Additionally, there are no alignment marks on the stamp. Usually, those would be written by a FIB, but the dimensions of the stamp make that impossible. The lack of alignment marks easily leads to large misalignment between exposures written at different times. The reason can either be unintentional rotation (after all, the stamp is rotationally symmetrical) or just not defining the u-v coordinate system on the stamp exactly as before. The u-v coordinate

(a)

(b)

(c)
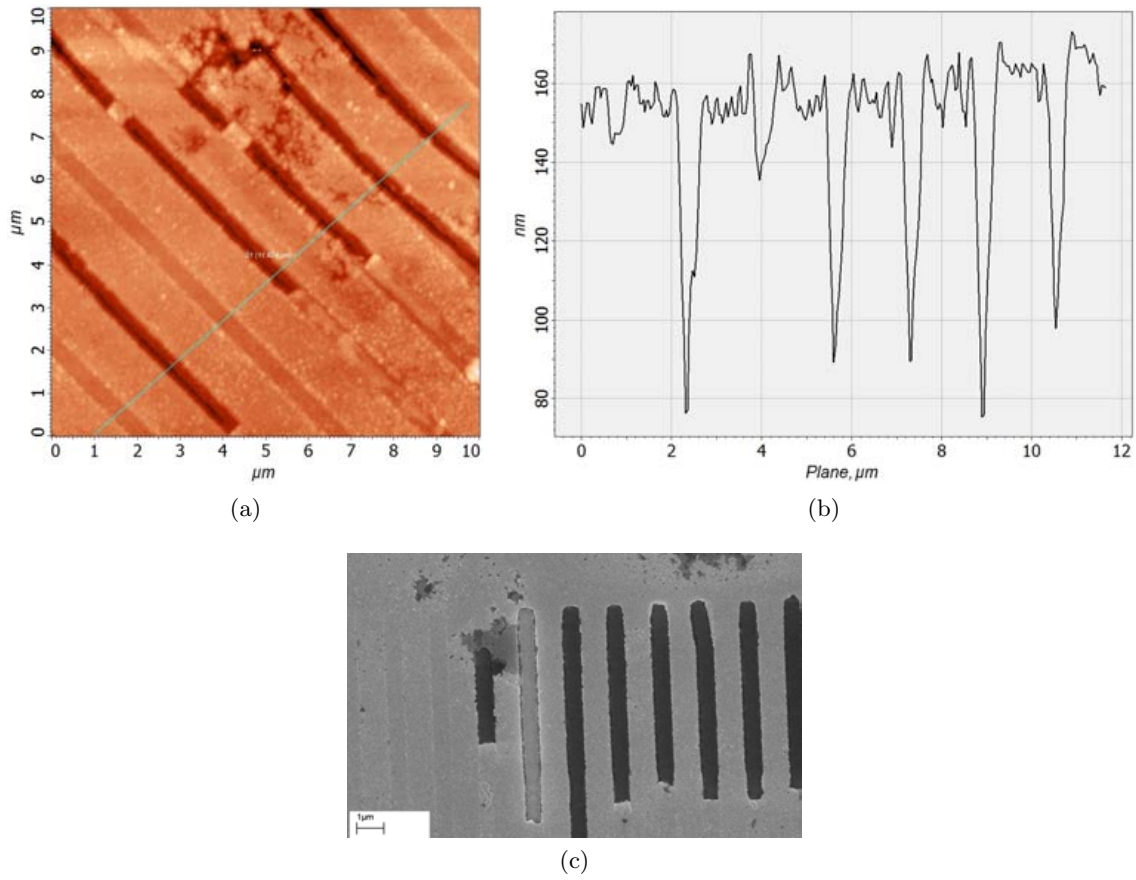
Figure 50: (a) 10 µm × 10 µm AFM scan of imprinted lines. The deeper (darker) grooves are due to imprinting with resist structures, while the not so deep ones are due to imprinting with the etched SiO$_2$. (b) The corresponding profile of a crosssection of the lines. (c) A SEM micrograph of a similar area of an imprint on SiN on GaN.

(a)

(b)
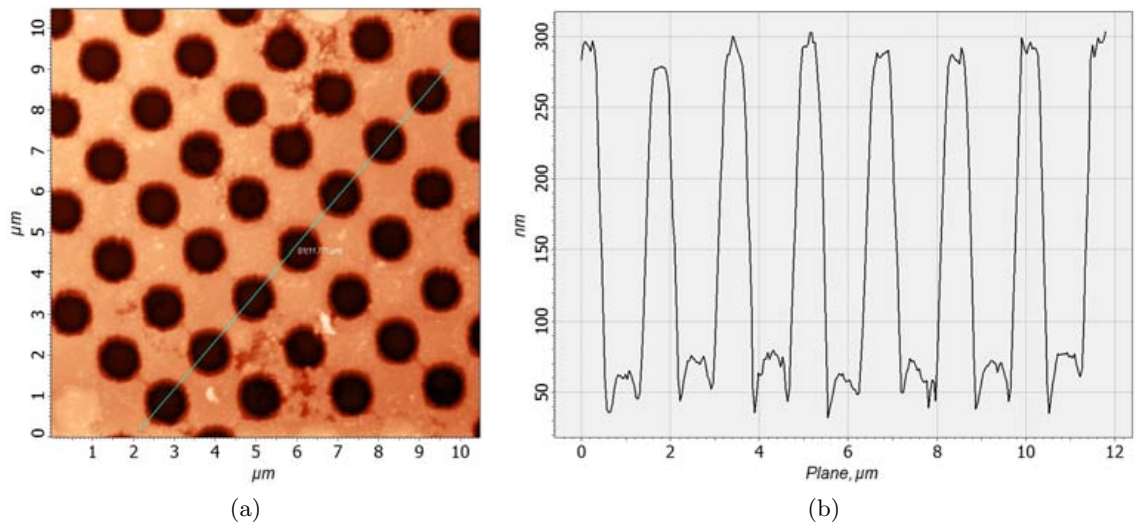
Figure 51: (a) 10.5 µm × 10.5 µm AFM scan of imprinted holes and (b) the corresponding line profile.
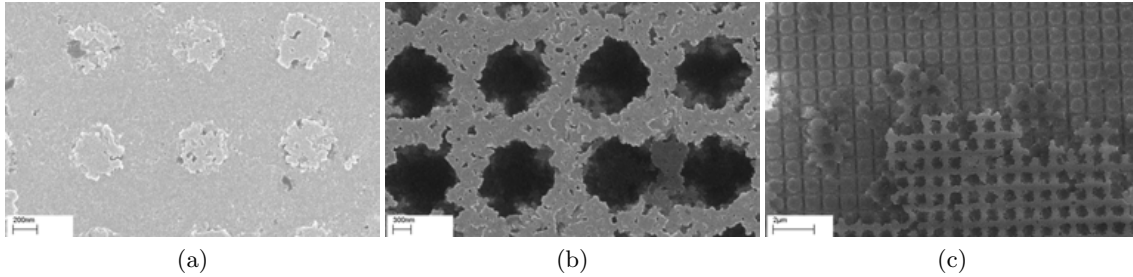
Figure 52: SEM images of imprints on SiN on GaN. All of them show artefacts of removing the resist that remained on the stamp after dry etching. The acetone and remover could not completely remove the resist, and some of it just came loose and moved to a new, slightly offset position.

system aligns the structures to be written to the sample.

One complication has been noticed, namely scumming occuring in dense lines. Scumming describes the fact, that the resist lines are not completely separated, but connected by a thinner layer of partially exposed resist. This happens, when the negative resist in the exposed areas is overexposed, and the electrons scatter into the areas where the resist should not be exposed. Scumming is also discernible in the imprinted features, where it manifests as a lowering in imprint height. Figure 53 illustrates scumming.

The fabrication process is still not completely controlled. Plasma etching of the silicon dioxide layer poses its own difficulties. The resist thickness of the patterns is not uniform over the whole sample area. Especially for dense or small structures scumming can be observed, leading to an uneven resist distribution. Because of this, the resist is exhausted faster in thinner areas, easily leading to overetching during the plasma etch step. When the resist is then removed, parts of it can continue to stick to the stamp, even after extended periods of cleaning in acetone and resist remover. Example of structures imprinted with a low-quality stamp are shown in Figure 52. Also the height difference in Figure 50 is due to that effect, as parts were imprinted with resist still present and parts only with the etched silicon dioxide. Here, a closer investigation into the etching effects executed on top of a glass substrate could surely improve the imprinting results.
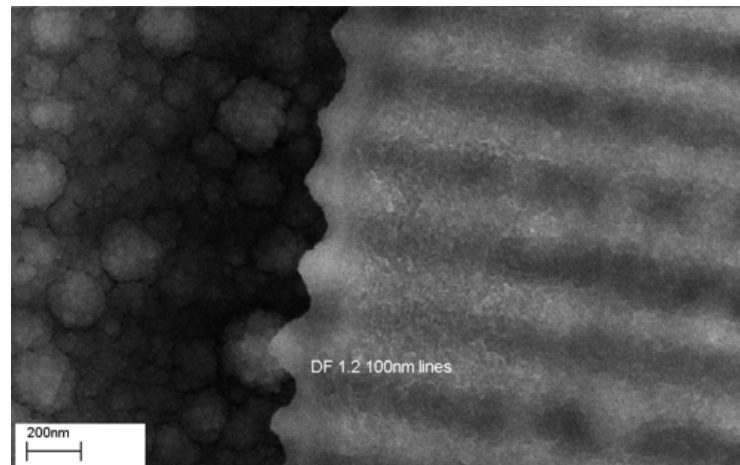
Figure 53: Scumming can be clearly seen as a remaining thin resist layer between the lines (darker than the grating) in the right half of the image. The silicon dioxide in the background (left half of the image) was deposited using the recipe "SiO$_2$ base" at 300 ℃.

7 Summary

This thesis investigated the fabrication of stamps for UV-NIL. UV-NIL is a new lithography method for smaller feature sizes than possible with optical lithography. In order to reach the goal, literature was examined and potential fabrication processes determined. A suitable resist for EBL was chosen and the processes were investigated experimentally in more detail. After the initial tests, the process which integrates a transparent conductive layer in the stamp was chosen for implementation.

It turned out, that the process using ITO as a transparent conductive oxide as proposed widely in the literature was not suitable for fabrication on Micronova's equipment, as the surface roughness of the ITO was prohibitively high. Instead, an ALD-nanolaminate of Al_2O_3-ZnO was employed as a conductive layer. This nanolaminate provides both conductivity and a flat surface, thus preventing nucleation of the subsequently deposited SiO_2 on its grains.

The structures were defined by EBL from a negative EBL resist and transferred into the SiO_2 layer by plasma etching in a RIE system. After pattern fabrication, the stamp underwent a wet etch in buffered HF to define a pedestal on which the patterns are in better contact with the imprint resist. As a final step, a release layer preventing template fouling was spin-coated onto the stamp. Several stamps have been successfully fabricated and tested.

Imprints were then performed on several different substrates with widely varying surface morphology. All features on the stamp were faithfully imprinted, even features of almost negligible height. Although the imprinting worked sucessfully, the fabrication process is still open for further improvements as not all process steps are completely mastered.

Higher acceleration voltages could be investigated to prevent the common problem of scumming in small, dense structures defined by EBL. It is thought, that a high voltage could reduce the amount of (back)scattered electrons into the non-exposed resist. Furthermore, the EBL system quite often gave non-predictable results. A systematic study of those problems should include stage problems, the influence of the current on the dose, and why sometimes patterns or parts thereof are left unexposed. This would definitely improve the results in the future.

A further line of investigation is an improvement of the wet-etching process. The current process produces many craters on top of the stamp surface which can potentially damage the fabricated patterns. Better process control could be achieved by increasing the adhesion, using a higher-quality mask, and depositing a thin chromium layer under the photoresist.

As the current thesis only studied the basic imprinting process, further work could be done to develop more advanced imprinting processes. First, the imprint process can be parametrized to work successfully with the automatic settings of the NIL module of the mask aligner. Second, imprinting using an alignment to already existing structures can be investigated. Third, the influence of the time that passes between spinning the imprint resist and the actual imprint on the viscosity of the resist and the quality of the imprints can be investigated. And finally, further processing, *e.g.*, a lift-off or etching the patterns into the underlying layer via (ICP-)RIE, should be investigated.

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A   Process Flow and Parameters

A.1   Complete List of Plasma Enhanced Chemical Vapor Deposition Recipes

All recipes used for the deposition of SiO_2 layers by plasma enhanced chemical vapor deposition (PECVD) are given in Table A.1. If not otherwise specified, the given temperature was used.

Table A.1: Process parameters for all the SiO_2-PECVD recipes used in this work..

Recipe Name	SiO_2 Tapio 200 nm	SiO_2 base 170 ℃	SiO_2 22 nm/ min	SiO_2 stress controlled
Comments	200 nm in 3:20 min	41 nm/ min, ca. 328 nm		ca. 67 nm/ min
duration [min]	4:20	8:00	10:00	4:00
temperature [℃]	200	170	300	300
SiH_4 flow [sccm]	8.5	4.0	5.0	22.5
N_2O flow [sccm]	710	320	710	750
N_2 flow [sccm]	161.5	120	161.5	420
Power [W]	20	20	7	15
Pressure [mTorr]	1000	2000	1000	1000

A.2   Stamp Preparation for the Wet-Etching Step

To prepare the stamp, it was first submerged in remover for an hour, followed by a bath in acetone with ultrasound for half an hour, and then for another 2 hours in acetone, until the surface looked clean and all resist was removed. This was followed by a 15 min rinse in isopropanol (IPA) and then the stamp was blow dried with N_2. To dehydrate the stamp, it was consequently put into a convection oven at 120 ℃ for 16 h. Afterwards, the wafer was submitted to hexamethyldisilazane (HMDS) priming for 2 min directly after taking it out of the oven. After the priming step, AZ 5214 photoresist was spun at 1000 rpm for 60 s and subsequently baked at 95 ℃ for 20 min in a convection oven. After this soft-bake the resist was exposed in the mask aligner using the flood exposure setting for 60 s. A plastic mask on which the center 2 cm × 2 cm were opaque was used for exposure. After exposure, the stamp was developed for 53 s in developer solution, rinsed with water and blow dried. Following an optical check of the developed resist, the stamp underwent another flood exposure, this time for 270 s to completely crosslink the resist. As a last step before etching in hydrofluoric acid (HF), the stamp was hard baked in a convection oven at 120 ℃ for several hours.

A.3   Release Layer Application

The spin-coatable release layer BGL-GZ-83 (Profactor GmbH, Austria) was used. Prior to spinning, the stamp was baked in a convection oven at 120 ℃ for half an hour to remove

excess water. The release layer was applied by spin coating for at 1000 rpm 30 s, followed by an acceleration step of 1600 rpm/s up to 2000 rpm where it is spun for another 30 s. After 8 h, the full anti sticking ability should be in effect. The durability of the release layer is specified up to 50 imprints by the manufacturer.

A.4   Resist Data

The negative EBL resist AR-N 7700 from Allresist (Germany) is based on 2-methoxy-1-methylethylacetate with 1-methoxy-2-propyl-acetate (PGMEA) as a safer-solvent; it is a chemically enhanced resist with high sensitivity, high resolution and high plasma resistivity. Structures with a resolution of 40 to 100 nm can be produced with a layer thickness of 80 and 400 nm. The contrast of the resist is more than 5, which makes it suitable for small structures.

Some of the changes in sensitivity experienced during EBL exposure could be explained by the fact, that according to a sidenote in the datasheet e-beam resists based on novolak like AR-N 7700 have a higher sensitivity directly after spin-coating than after waiting for a few hours or days. The sensitivity is recuced by about 3% after 3 h, about 6% after 24 h and 8% after 72 h.

A.5   Imprint Resist

The preparation of the imprinting substrate for the imprint resist AMONIL MMS 4 begins with heating the substrate[9] for 30 min at 120 ℃ to remove residual water. The primer AMO-PRIME is spin-coated for 30 s at 3000 rpm, followed by a 1 min baking step at 115 ℃. After cooling down a bit, AMONIL is spincoated at the recommended speed of 3000 rpm for 30 s.

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[9]Specified is a minimum of 10 min at 160 ℃, but the convection oven in Micronova does not offer such high temperatures.

B   Additional Tables

Table B.1: Imprint resists

Ref.	Name, Contents and Comments
[29]	mr-L 6000 (Micro Resist Technology, Germany)
	A multifunctional epoxidized novolak resin and a photoacid generator. UV-curable, essentially a chemically amplified negative photoresist sensitive to near-UV exposure.
[19]	Darocur 1173 (2-hydroxy-2-methyl-1-phenyl-propan-1-one, Ciba Inc.) dissolved in SIB 1402.0 (1,3-bis(3-methacryloxypropyl)tetramethyldisiloxane, Gelest).
	Agitated in a VWR MV-1 vortexer, filtered to 100 nm, and degassed in an ultrasonic bath.
[69]	AMONIL-MMS4 (AMO GmbH, Germany)
[69]	PAK-01 (Toyo Gosei, Japan)
[69]	NILTM105 (home-developed)
	Contains pre-polymers, a photoinitiator, and a solvent. $\eta = 740\,\mathrm{mPa}$
[3]	NXR-2000 (Nanonex Corporation, USA)
	Contains a reactive silicon containing oligomer, a photoinitiator, and an acrylate monomer

Table B.2: Release Layer Formulations

Ref.	Name and Comments
[70]	Optool DSX (Daikin Industries, Ltd.)
	Applied in liquid phase. Deposits a thin layer of fluorocarbon film a the surface.
[52]	BGL-GZ-83 (Profactor GmbH)
	Applied by spinning.
[16]	0.2 wt. % solution of tridecafluoro-1,1,2,2tetrahydrooctyltrichlorosilane in HFE7100 (3M CO)
	Has to be carried out in a drybox containing nitrogen. Quartz stamp is immersed in the solution for 15 min and then rinsed in HFE7100 for 15 min.
[41]	Tridecafluoro-1,1,2,2-tetrahydrooctyltrichlorosilane (Gelest Inc.)
	Used for HSQ on ITO.
[21]	Fluoropolymer
	Plasma deposited in an RIE system
[4]	Tridecafluoro-1,1,2,2,tetrahydrooctyltrichloro-silane (CF_3-$(CF_2)_5$-CH_2-CH_2-$SiCl_3$) (Gelest Inc.)
	Cleaned in Piranha etch for 30 min to remove surface organic contaminants. The chemical is applied at a temperature of 90 ℃ for 1 h.
[19]	Tridecafluoro-1,1,2,2-tetrahydrooctyl trichlorosilane (Gelest Inc.)
	Vapor exposure to to the chemial at 760 Torr (precursor plus N_2) for 2 h followed by a 15 min anneal at 100 ℃. Used for ITO/SiO_2 stamp.
[25]	0.5 % (v/v) (Tridecafluoro-1,1,2,2-TetraHydrooctyl)Dimethylchloro-silane in toluene (Gelest Inc.)
	Self-assembled monolayer used for biomolecules.
[28]	1H,1H,2H,2H-perfluorodecyl-trichlorosilane
	Vapor phase deposition avoids the problem of wetting on the nanoscale.
[7]	[1H,1H,2H,2H]perfluorooctyl-triethoxylsilane
	Added to the imprint resin where it forms the surface layer of the resin
	tridecafluoro[1,1,2,2]tetrahydrooctyl-trichlorosilane
	Is additionally used to treat the stamp in a liquid phase deposition.