Publication [P1]

2.4-GHz Receiver for Sensor Applications

Jere A. M. Järvinen, Jouni Kaukovuori, Jussi Ryynänen, *Member, IEEE*, Jarkko Jussila, *Member, IEEE*, Kalle Kivekäs, *Member, IEEE*, Mauri Honkanen, and Kari A. I. Halonen, *Member, IEEE*

***Abstract*—This paper describes a receiver designed to meet the stringent power consumption requirements for sensor radio, which operates at 2.4-GHz ISM band with Bluetooth. To enable the reusability of the Bluetooth system, only slight changes are made in the radio parameters. The symbol rate is decreased and the increased modulation index removes the energy maximum from the channel center, which enables a low-complexity direct-conversion receiver solution. To meet the speed and power requirements, this receiver is fabricated in a 0.13-μm CMOS process. The 3.4-mW direct-conversion demonstrator receiver includes a low-noise amplifier, which is merged with quadrature mixers, local oscillator buffers, and one analog baseband channel with a 1-bit limiter for analog-to-digital conversion. The receiver consumes 2.75 mA from a 1.2-V supply. The receiver achieves 47-dB voltage gain, 28-dB NF, −21-dBm IIP3, and +18-dBm IIP2.**

***Index Terms*—Analog integrated circuits, CMOS, filter, mixer-baseband interface, radio frequency (RF), receiver, sensor networks.**

I. Introduction

AMBIENT intelligence visions and wireless sensor networks require suitable radio communication technologies to come true. Therefore, radio design principles and solutions appropriate for wireless sensor networks have raised a lot of interest recently [1]–[4]. Admittedly, a number of small devices could benefit from being connected wirelessly together, forming wireless mesh networks and enabling connectivity to devices like mobile phones or personal digital assistants (PDAs), acting as a user gateway between the Internet and sensors. However, the major technical bottlenecks of these prospects have been the lack of appropriate radio access methods from the power consumption point of view and the necessity of handling networking topologies of a large number of nodes power efficiently. A new radio system is required to support the connectivity to sensors. However, to avoid the need to add yet another radio to the mobile phone, Bluetooth with slight changes in the radio parameters was utilized to overcome the shortcomings that Bluetooth has from the sensor networks viewpoint [5].

The extremely low power consumption and material costs are the key requirements for sensor radio modules. To achieve over-1-year stand-alone operation, extremely small active and stand-by currents are required. In addition, because the sensors are powered by the button cell batteries, the supply voltage is limited to 1.0–1.5 V. One-dollar bill material costs in a few years time scale require a small device with minimum number of external components. A high integration level can be achieved by using, for example, the direct-conversion receiver (DCR) architecture. The demand for low cost requires the use of CMOS technology without additional process options, like high-quality resistors or capacitors. Currently, the speed of the transistors in modern deep sub-micrometer CMOS processes is not the limiting factor. However, the challenges for receiver (RX) design emerge from the poor "analog" performance of the transistor. For example, the available gain from a single transistor is only moderate. In addition, in a CMOS DCR, the flicker noise increases the noise figure (NF) significantly and must be considered already in the downconversion mixers. Moreover, the flicker noise seems to be ever increasing problem as the gate insulator thickness is made thinner. However, a higher NF than, for example, in cellular systems can be tolerated because the sensors are typically short-range devices [6].

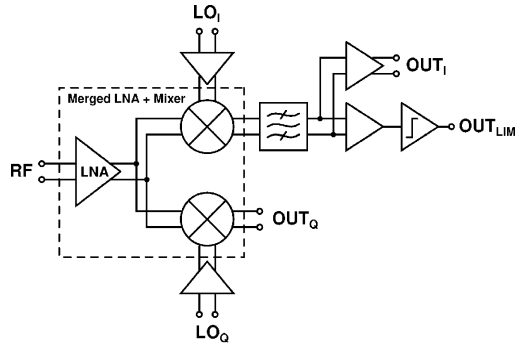


Fig. 1. Block diagram of the receiver.

The block diagram of the fabricated DCR is presented in Fig. 1. The measured active current consumption of the whole RX with a single baseband channel is 2.75 mA from a 1.2-V supply. With two baseband channels, the current consumption would be 2.83 mA. Section II gives an introduction to wireless sensor networks and describes the radio system where the designed RX IC is planned to operate. Sections III and IV cover issues related to the circuit design of the RF front-end and analog baseband, respectively. Experimental results are given in Section V, and the paper is summarized in Section VI.

II. System Introduction

The system used in wireless sensor networks needs to support scalability and be dynamically reconfigurable. The mobile terminals would roam in the "sea of sensors," and thus

Manuscript received November 16, 2004; revised January 27, 2005. This work was supported in part by the Nokia Research Center, the Nokia Foundation, and the National Technology Agency of Finland.

J. A. M. Järvinen, J. Kaukovuori, J. Ryynänen, and K. A. I. Halonen are with the Electronic Circuit Design Laboratory, Helsinki University of Technology, FIN-02150 Espoo, Finland (e-mail: jere.jarvinen@ecdl.hut.fi).

J. Jussila, K. Kivekäs, and M. Honkanen are with the Nokia Research Center, 00045 Nokia Group, Helsinki, Finland.

Digital Object Identifier 10.1109/JSSC.2005.847273

TABLE I
BASIC LEE RADIO PARAMETERS

Physical bit rate	333 kbps
Frequency band	2.4 GHz (ISM band)
Modulation	2GFSK (h = 2.4, BT = 0.5)
Duplex	TDD
Co-existence of multiple devices Connection setup channel Data delivery	 CSMA FDMA
Jamming avoidance	FDMA

the static network configurations cannot be considered. On the other hand, the traditional master–slave type topologies with the master acting as a network coordinator are impractical because the coordination typically demands much more activity from the master node that any small-size mobile device or even sensor node could tolerate. None of the current standardized radio access for peripherals fulfills these requirements in a satisfactory manner. Standard Bluetooth is too power-hungry and suffers from relatively long device discovery and connection setup times. ZigBee, based on IEEE 803.15.4, is another standard that claims to overcome some of the limitations that Bluetooth encounters. However, it does not support very well the dynamic topologies that are an essential requirement for a mobile sensor solutions and has only slight improvements in power consumption compared to Bluetooth.

The basis of the system development was to circumvent the situation where a new radio would be needed in a mobile terminal. The amount of supported radio accesses in the mobile terminal is already large keeping the integration and cost challenges immense. To avoid the need to add yet another radio to the mobile phone, Bluetooth was identified to be capable of providing the connectivity from mobile terminal to the sensors with slight changes in the radio parameters to overcome the shortcomings that Bluetooth has from the sensor networks viewpoint [5]. A low end extension (LEE) for Bluetooth was designed allowing the reusability of Bluetooth radio in the mobile terminal. The overall concept includes two device categories, "dual-mode" Bluetooth device in the mobile terminal, capable of connecting to the sensors in addition to the standard Bluetooth devices and the "stand-alone" sensor device, which can support only the short-range energy-optimized connectivity. Table I shows the air interface parameters for LEE [5].

In LEE, the design is limited by the reusability requirement of the Bluetooth RF at the mobile terminal end, which means that the 2.4-GHz ISM band must be used and the channel bandwidth must comply with Bluetooth. LEE circumvents the shortcomings of the normal Bluetooth by avoiding frequency hopping and enhancing the modulation index. The DCR uses 1-bit limiters for the analog-to-digital conversion. The 1-bit resolution together with the large modulation index makes the receiver insensitive to strong reception signals. The LEE baseband features two major modifications to Bluetooth. First, the symbol rate 333.3 kb/s is one third of Bluetooth symbol rate and the 2GFSK modulation index is increased in such a way that the channel bandwidth remains the same as in Bluetooth. The larger modulation index removes the energy maximum from the channel center. Thus, a low-complexity DCR approach can be applied for the stand-alone RF without any modifications on the filters

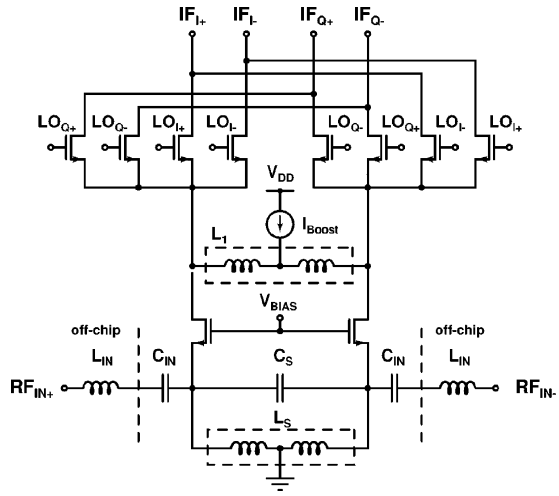


Fig. 2. LNA and I/Q-mixers.

on the Bluetooth RF chip. The increased modulation index also gives more freedom to design power-efficient synthesizer solutions for the stand-alone modules. Furthermore, the chosen modulation scheme is very robust against Bluetooth interference. The air interface parameters are important factors since practically they determine the optimum radio architecture and its performance. Tradeoffs between hardware implementation issues and performance, such as spectral efficiency and data rate, can be done by adjusting those parameters. The details of the radio system concept can be found in [5].

III. RF FRONT-END

The RF front-end consists of a low-noise amplifier (LNA), which is merged with quadrature mixers and local oscillator (LO) buffers. The I-mixer is followed by a baseband channel, and the Q-channel mixer is loaded with resistors, which enables the separate characterization of the RF front-end in a dc operation point equal to the I-channel mixer.

A. LNA and Quadrature Mixers

The LNA, which is merged with I/Q-mixers, is shown in Fig. 2. Compared to the solution where separate LNA and mixers are used, the current consumption of a merged structure with the same performance can be decreased by the amount of the dc current, which flows through the mixer switch transistors. In this receiver, the simulated current consumption of the combined LNA and mixer including the biases is 1.4 mA. If separate LNA and mixers were used, the current consumption would be at least 30% higher.

The LNA is a balanced common-gate (CG) amplifier with a moderate-Q inductor load (L_1). The CG configuration is used instead of the common-source topology because of the improved reverse isolation. In addition, in the CG configuration the Miller effect is avoided. Therefore, no cascode stage is needed, which is crucial in low-voltage applications. The differential input matching to 100 Ω is implemented with two

LC-resonators. With shunt capacitance C_S, the value of the source inductor L_S is decreased to the level, which is suitable for on-chip integration. Furthermore, to save the silicon area, an inductor with a very small area was chosen. In this design, when the area of the inductor L_S was decreased, the series resistance R_{LS} of the inductor was increased, which lowered the quality value of the inductor. The thermal noise of the inductor has an insignificant effect on the total output noise. However, if the Q-value of the source inductor is decreased significantly, the resonator impedance will be lowered. As a result, part of the input signal leaks into the resonator, which decreases the signal-to-noise ratio (SNR). In addition, the finite Q-value of the inductor L_S affects the input matching. Because the drain–source resistor $r_{\rm ds}$ of the input transistor is much larger than the impedance of the load of the LNA, the load has an insignificant effect on the input matching. Thus, the input matching is

$$Z_{\rm IN} = \left(sL_{\rm IN} + \frac{1}{sC_{IN}}\right) + \left(\frac{sL_S + R_{LS}}{sL_S(sC_{\rm tot} + g_m) + R_{LS}(sC_{\rm tot} + g_m) + 1}\right) \quad (1)$$

where

$$C_{\rm tot} = 2C_S + C_{\rm gs} + C_{\rm par}. \quad (2)$$

$C_{\rm gs}$ is the gate–source capacitance of the input transistor, g_m is the effective transconductance of the input transistor, and $C_{\rm par}$ is the capacitance at the source of the input transistor including all parasitic capacitances. At the resonance frequency, the input resistance $R_{\rm in}$ becomes

$$R_{\rm in} = \frac{L_S}{L_S g_m + C_{\rm tot} R_{LS}}. \quad (3)$$

As can be seen from (3), the inductor series resistance R_{LS} has an effect on the input impedance and should be taken into account.

The width of the LNA transistor is chosen to optimize the transconductance by using as small a dc current as possible. The simulated effective transconductance g_m of a single input transistor as a function of the transistor width and drain current (I_D) is shown in Fig. 3. The transistor length is selected as the minimum to maximize the transistor f_T and transconductance. The drain–source voltage ($V_{\rm DS}$) of the input transistor was set to 300 mV. As can be seen in Fig. 3, to reach a transconductance of 20 mS, which corresponds to 50 Ω, a current of at least 0.75 mA is needed even with a wide input device. Because of a stringent current budget and a nonzero resistance R_{LS}, the effective transconductance of less than 20 mS was chosen, which is shown with a dot in Fig. 3. When optimizing for a small current consumption, the subthreshold region in Fig. 3, where the g_m/I_D ratio is at the maximum, can be exploited. The input referred third-order intercept point (IIP3) of the input transistor improves with a higher overdrive voltage. However, in this design, the input transistor linearity is not critical because the out-of-channel IIP3 is limited by the baseband.

The disadvantage of CMOS switching transistors is the high intrinsic flicker noise, which is the largest noise contributor in this design. According to simulations, the flicker noise of the switching transistors increases the NF of the whole receiver by 6 dB. To minimize the $1/f$ noise, the drain current of the switch transistor should be minimized, the active gate area of the mixer switch should be maximized, and the LO amplitude should be maximized [7], [8]. However, all of these methods are not suitable for a low-power low-voltage realization. For example, achieving a large LO swing with a sharp slope is current consuming in a DCR due to the high frequency of the LO signal. In addition, increasing the switch transistor gate area is impractical due to the higher parasitic capacitances, which increases the current consumption of the LO buffer [9]. Thus, the minimum gate length was chosen to keep the mixer gate capacitance small. In addition, the capacitance at the source of the switch transistor degrades the SNR [8]. The tail capacitance can be tuned out with the moderate-Q inductor L_1 between the LNA and the mixer. As a result, the resonator lowers the effect of the mixer flicker noise [10]. According to simulations, the inductor improves the NF and the voltage gain of the receiver by approximately 7–8 dB.

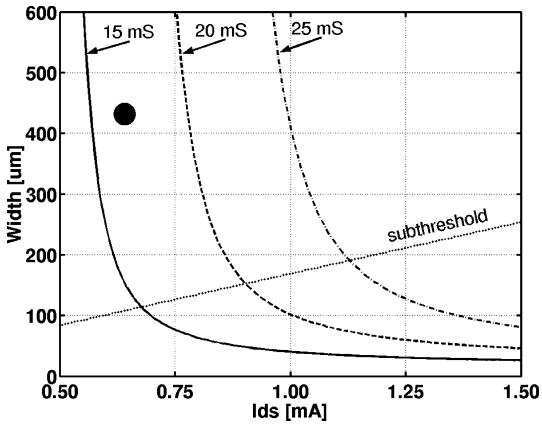


Fig. 3. Effective transconductance (15, 20, and 25 mS) of the input transistor as a function of transistor width and drain current. The selected width and I_D of the input transistor are shown with a dot.

The mixer noise performance can be additionally improved by minimizing the drain current of the switch transistors, because the mixer output noise is directly related to the amount of the dc current of the switches [8]. Typically, the voltage gain and linearity improve with a larger switch current but, in this design, the noise of the switches is the most critical parameter because of the low gain of the LNA. As a result, very different currents are required in the switch transistors and in the LNA transistors to optimize the performance of the front-end and the whole receiver. In this design, the dc current that flows through the switch transistors is reduced with an additional current source I_{Boost}, which is approximately 70% of the total drain current of the LNA input transistors. Compared to existing solutions [11] and [12], where separate current boosts are used, this design has a single boost current at the center tap of the load inductor L_1, which is a virtual ground. As a result, the thermal noise generated by the boost current source $I_{\rm Boost}$ will cause only common-mode noise at the output of the mixer. If separate

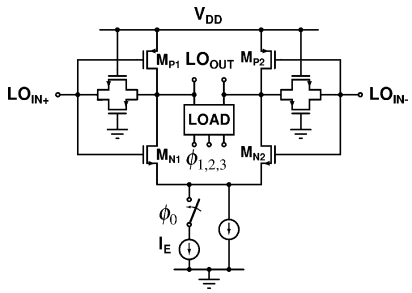


Fig. 4. LO buffer.

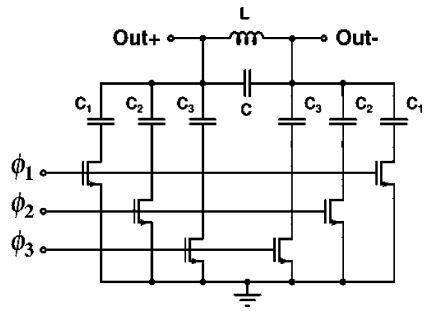


Fig. 5. Load of the LO buffer.

boost current sources were used at the output nodes of the LNA, the parasitic capacitance would increase in that node. As a result, the Q-value of the *LC* resonator would be lower. It follows that the voltage gain would degrade and the following stages would have more effect to the output noise. In addition, separate current sources would cause an output noise voltage, which is comparable to the noise generated by the input transistors. Because the NF in this design is dominated by the flicker noise of the switches, the current boost to the center tap of L_1 has a relatively small effect on the total performance. However, the significance of the presented current boost method to the total output noise depends heavily on the selected process technology and the topology of the receiver.

B. LO Buffer

The LO signals are amplified and buffered using balanced LO buffers shown in Fig. 4. The input stage of the LO buffer is a combination of nMOS and pMOS transistors. With typical LO input signal levels (i.e., > -10 dBm), the buffer operates in the large signal region. When the large LO signal has the maximum or minimum amplitude, it latches the input transistors such that the cascoded input transistors are not on simultaneously. The output signal is a sum of $V_{\rm DS}$ voltages of the complementary transistors (M_{N1} and M_{P2}, or M_{N2} and M_{P1}). When compared to a conventional nMOS differential pair, the presented structure offers approximately a 4–5 dB larger voltage signal to the mixer gates with the same dc current. The nMOS–pMOS transistor pairs between the input and output are used for biasing.

The load of the LO buffer, which consists of an inductor L, a capacitor C, and capacitors C_1–C_3, is shown in Fig. 5. The resonator having a high Q-value was designed to achieve a sufficient LO signal swing with a small current consumption. As a result, the bandwidth of the LO buffer is narrow and the center frequency is sensitive to process variations. With a tunable capacitor load, the LO signal can be adjusted. Three-bit tuning with a range of $\pm 13\%$ covers all process corners. The tuning was realized by adding capacitors C_1–C_3 to the *LC*-resonator. When the maximum capacitance setup is used, the Q-value of the resonator is lowered, which degrades the available signal swing. Thus, an extra current source I_E was added to increase the output signal swing of the LO buffer when the maximum capacitance setup is used. As a result, the LO signal amplitude variation can be kept within three decibels. The simulated total current consumption of one LO buffer including biases is 0.4 mA. With the additional current source I_E, the current consumption increases to 0.6 mA.

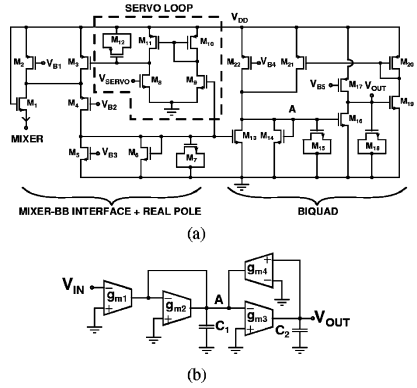


Fig. 6. (a) Third-order all-CMOS channel-select filter. (b) Prototype g_m-C biquad.

IV. Analog Baseband Circuit

A. Channel-Select Filter

The realized channel-select filter is a third-order all-CMOS filter. Fig. 6(a) shows one half of the filter. The filter is realized with two single-ended circuits, which is also called a pseudodifferential structure. This structure does not need a common-mode feedback circuit, which helps the design when using low supply voltages [13]. When low power consumption and low power supply is targeted, a simple realization of the filter is preferred [14]. The third-order filter can be separated into real and imaginary parts [15]. First, there is a mixer–baseband interface with a real pole and servo loop. The real pole is followed by a biquad stage. The filter was designed for a -3-dB frequency of 550 kHz. The total current consumption of the filter including biases is 65 μA.

B. Mixer–Baseband Interface

The mixer–baseband interface shown in Fig. 6(a) is the most critical part at baseband since it limits the dynamic range and dominates power dissipation of the baseband. The effective transconductance of the RF front-end is low. Thus, the noise contributed by the interface becomes significant. In addition,

the output impedance of the mixer is small whereas a higher impedance level is preferred in the filter to minimize power dissipation. Because of the low transconductance of the RF front-end, small load impedance at the mixer output would require a high supply current in the following baseband stage to keep the input-referred noise of that stage sufficiently small. Another possibility is to increase the mixer output impedance by using cascode devices. Hence, compared to the commonly used resistive mixer load, an interface based on cascode transistors was used. An nMOS cascode device M_1 stacked with the mixer increases the mixer output impedance without additional current. Another cascode stage implemented as a folded pMOS transistor M_4 is needed to achieve sufficiently high output impedance to the nMOS load M_6. The bias current of the pMOS cascode must be larger than the peak signal current caused by any out-of-channel interfering signal to avoid clipping. Steering some of the bias current through the nMOS current source M_5 increases the gain. The load transistor M_6 and the nMOS capacitor M_7 form the real pole of the filter.

DC offset compensation is needed since the current drawn by the mixer varies due to mismatches, temperature, and process variations. Thus, using a servo loop M_8-M_{12}, ensures a correct dc voltage at the gate of transistor M_{13}. In this design, the resulting -3-dB frequency of the highpass filter is 86 kHz. The corner frequency is a tradeoff between signal quality, start-up time of the receiver, and silicon area. A lower corner frequency would require a larger capacitance, which increases the start-up time and silicon area. The implemented pMOS capacitor has a value of 290 pF, which dominates the area of the filter.

Since the RF front-end dominates the power consumption of the receiver, the filter design concentrated on optimizing the dynamic range and keeping the required die area small. The baseband noise is dominated by the thermal noise of the pMOS current sources at the mixer output. The flicker noise is not a significant problem at baseband since all transistors are designed for a long channel length for better matching. The cascode transistors M_1 and M_4 limit the linearity of the baseband channel and the whole receiver. Linearity could be increased at the cost of increasing power consumption and silicon area.

C. Biquad

The biquad stage of the channel-select filter shown in Fig. 6(a) is derived from a g_m-C biquad prototype shown in Fig. 6(b). To enable the use of low supply voltages, the transconductors are replaced with common-source nMOS transistors instead of using, for example, differential pairs. This filter structure is suitable for applications requiring moderate linearity. MOS capacitors are used because they provide a high capacitance per unit area and sufficient linearity [16].

The first lossy integrator formed by transconductors g_{m1} and g_{m2} and capacitor C_1 is replaced with nMOS transistors M_{13}, M_{14}, and M_{15}, respectively. The pMOS transistor M_{22} is used to bias transistors M_{13} and M_{14}. The lossless integrator formed by transconductance g_{m3} and capacitor C_2 is replaced with nMOS transistors M_{16} and M_{18}, respectively. Transistor M_{17} is used for biasing. Finally, noninverting transconductance g_{m4} is replaced with transistor M_{19} and a current mirror formed by transistors M_{20} and M_{21}.

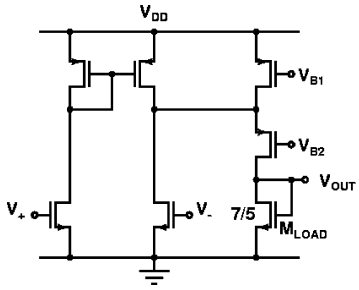


Fig. 7. Differential-to-single-ended converter.

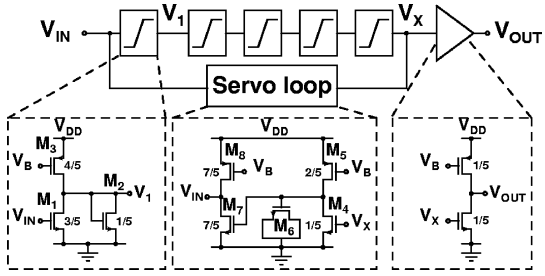


Fig. 8. Limiter.

The voltage gain can be implemented in the different stages of the biquad shown in Fig. 6(b). The voltage gain is needed to reduce the noise contribution of the following stages. In this design, a gain of 9.5 dB is implemented by increasing the transconductance of g_{m1}. Implementing gain by increasing g_{m2} would require reducing the value of C_2. However, the reduction of the value of C_2, which is small, would increase the sensitivity to parasitic capacitances.

D. Limiter

The differential signal at the channel-select filter output is transformed to a single-ended signal with a differential-to-single-ended converter using a diode connected nMOS load, as shown in Fig. 7. The single-ended limiter follows the differential-to-single-ended converter. The limiter consists of cascaded similar amplifier stages. By selecting a proper number of amplifiers, the power dissipation of the limiter can be minimized [17]. The limiter shown in Fig. 8 consists of five stages, which give a total voltage gain of 47.5 dB. A saturation-region nMOS transistor M_1 with a diode-connected nMOS load M_2 form the limiting amplifier stage. The structure gives immunity to the negative power supply interference.

One or more servo loops are needed to reduce the input-referred dc offset of the limiter to a level, which is below the wanted signal in the sensitivity level to preserve good signal quality. Each servo loop forms a highpass filter that degrades the signal quality in the receiver chain. Therefore, only one servo loop is used in the limiter. Since the limiter chain is inverting, a noninverting servo loop is required to conform a negative feedback. The width of the current-source M_5 at the input stage of the servo loop is half of the current source M_3. This way the currents used to charge and discharge the nMOS capacitor M_6

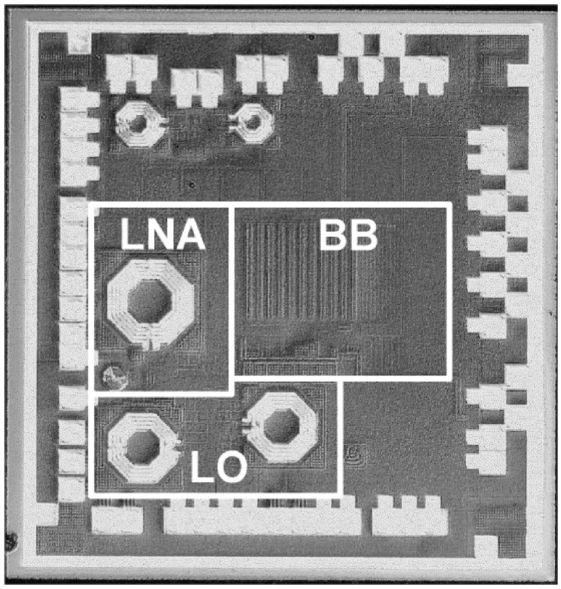


Fig. 9. Chip microphotograph.

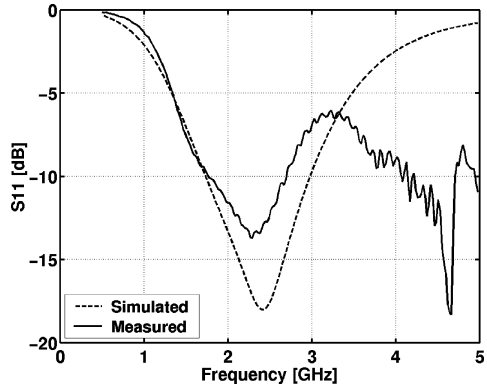


Fig. 10. Measured and simulated input matching.

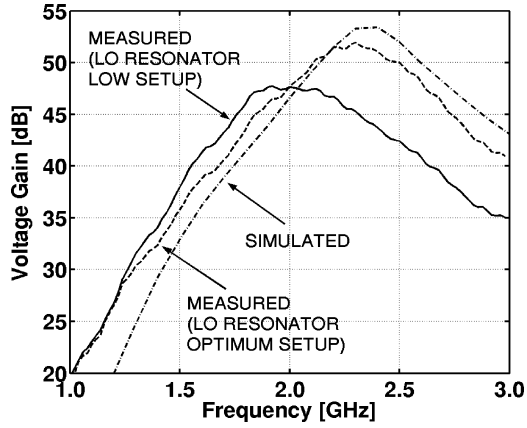


Fig. 11. Measured and simulated RF responses.

are equal when the input signal at node V_X goes rail to rail. The transistor M_7 at the output stage of the servo loop is sized equal to the nMOS load M_{LOAD} at the limiter input shown in Fig. 7 to implement unity gain.

The designed servo loop uses an integrated 280-pF nMOS capacitor, which uses most of the silicon area needed for the limiter. Since all time constants have to be implemented using MOSFETs, grounded capacitors are used. A single-ended structure was chosen, because a differential structure would double the needed silicon area. The last limiter stage is a common-source amplifier with a current-source load. Using a common-source output stage ensures a rail-to-rail output signal. The limiter current consumption including biases is 15 μA.

V. Experimental Results

The chip was fabricated in a 0.13-μm CMOS technology. The active chip area is 1.0 mm^2. In addition to the actual receiver, the chip includes test structures and additional test pads that increase the total chip area to 3.3 mm^2. The chips were bonded directly on a printed circuit board (PCB). The chip microphotograph is shown in Fig. 9.

The measured active current consumption of the whole receiver with one baseband channel is 2.75 mA from a 1.2-V supply. The measured and the simulated input matchings are shown in Fig. 10. The measured S11 is better than -10 dB within the wanted frequency band. The simulated S11 agrees well with the measured one. The voltage gain, NF, linearity (IIP3, IIP2), and receiver start-up time were measured from the analog test output of the baseband channel. During the measurements, it was found out that the LO tuning was sensitive to noise and glitches generated on the chip and PCB. Thus, to confirm the validity of the results, the receiver measurements were primarily performed with the setup where the LO resonator is at the lowest frequency of operation (LO buffer in reset mode). As a result, the maximum performance could not be obtained. The measured RF response is shown in Fig. 11. The maximum voltage gain of 47 dB is achieved at 2.0 GHz. The corresponding frequency response of the channel-select filter is shown in Fig. 12 where the measured and simulated maximum voltage gains are scaled to 0 dB for the purpose of comparison.The NF measured from the analog test output is 28 dB. In addition, the receiver gain and NF were measured at 2.0 GHz as a function of supply voltage and the result is shown in Fig. 13. The measurement shows that the receiver operates down to a 1.0-V supply. The minimum supply voltage is limited by the mixer–baseband interface, where four transistors are stacked.

The receiver IIP3 was measured by using test signals at 3.0-MHz and 5.8-MHz offsets from a 2-GHz LO. The measured IIP3 is -21 dBm at the 100-Ω input impedance. The IIP2 was measured with test tones having 2.8-MHz and 3.0-MHz frequency offsets from the LO, and the results varied between $+18$ and $+26$ dBm. For the purpose of comparison, the measured voltage gain with the optimum LO buffer setup and the simulated result are also shown in Fig. 11. With the optimum LO buffer setup, the maximum voltage gain is achieved at

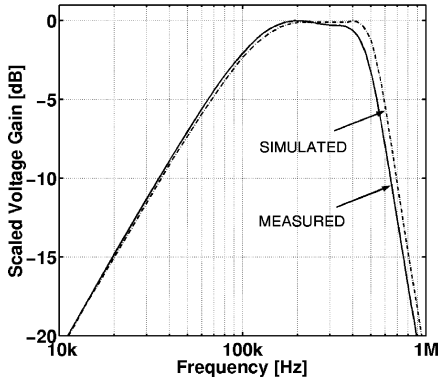


Fig. 12. Measured and simulated frequency responses of the channel-select filter.

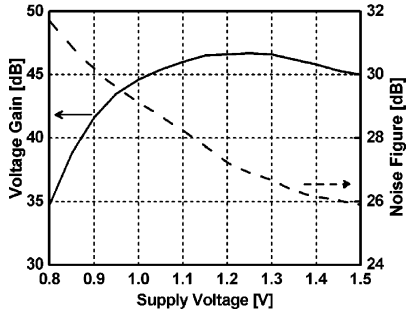


Fig. 13. Measured receiver voltage gain and NF versus supply voltage.

2.35 GHz. The measured voltage gain is 52 dB and the NF is 24.5 dB.

The start-up time plays an important role in sensor systems when the target is to minimize power consumption. The channel select filter output has settled after 50 μs. The start-up time is limited by the charging of the large capacitance at servo loop of the mixer-baseband interface. The limiter was characterized measuring the duty cycle as a function of input signal frequency and by measuring the difference between the group delays by changing the input signal level at the receiver input from -70 to -40 dBm. The measured group delay with a 200-kHz input signal is 105 ns. The measured duty cycle is shown in Table II. In the measurement, the input signal level at the receiver input was set to -60 dBm. The duty cycle was also measured as a function of the supply voltage and the measurement shows that the duty cycle does not degrade until the supply voltage goes below 1.0 V. This is due to the gain degradation in the preceding stages.

The merged LNA and mixer with the LO buffers consume approximately 94% of the receiver supply current. In the stand-by mode, the measured current consumption is 18 μA, and, according to simulations, it is mainly due to the leakage current of the bonding pad ring. Table II summarizes the measured performance of the demonstrator. The measured performance with the optimized LO signal is given in parenthesis.

TABLE II
SUMMARIZED PERFORMANCE OF THE RECEIVER

Supply voltage	1.2	V
Supply current (active)	2.75	mA
Supply current (stand-by)	18	µA
Voltage gain, RF + BB	47 (52)	dB
Voltage gain, LNA + Mixer	12.5 (14.5)	dB
Maximum gain frequency	2.0 (2.35)	GHz
NF	28 (24.5)	dB
Out-of-channel IIP3	-21	dBm
Out-of-channel IIP2	+18	dBm
S11	-10	dB
Filter –3-dB corner frequencies	86, 493	kHz
Start-up time	~50	µs
Limiter group delay @ 200 kHz	105	ns
Duty cycle (Up/Period) @ 100 kHz	49.0	
300 kHz	47.5	%
500 kHz	46.5	

VI. CONCLUSION

A 1.2-V 3.4-mW direct-conversion receiver for wireless sensor applications operating at 2.4-GHz ISM band is presented in this paper. The receiver uses a modified Bluetooth system that has optimized radio parameters for low power applications. The demonstrator receiver is fabricated in a 0.13-μm CMOS process and consists of a merged LNA and mixers, LO buffers, and one baseband channel. Special attention is paid to the simultaneous design of the mixer–baseband interface and the current boost method of the mixer. This work demonstrates that it is feasible to design a receiver for sensor applications with extremely small active and stand-by current consumption when the system allows high noise figure.

ACKNOWLEDGMENT

The authors would like to thank Dr. A. Pärssinen and A. Lappeteläinen for technical assistance.

REFERENCES

[1] C. C. Enz, A. El-Hoiydi, J.-D. Decotignie, and V. Peiris, "WiseNET: An ultralow-power wireless sensor network solution," *IEEE Comput.*, vol. 37, no. 8, pp. 62–70, Aug. 2004.

[2] R. Min, M. Bhardwaj, S.-H. Cho, N. Ickes, E. Shih, A. Sinha, A. Wang, and A. Chandrakasan, "Energy-centric enabling technologies for wireless sensor networks," *IEEE Wireless Commun.*, vol. 9, no. 8, pp. 28–39, Aug. 2002.

[3] J. M. Rabaey, J. Ammer, T. Karalar, S. Li, B. Otis, M. Sheets, and T. Tuan, "Picoradios for wireless sensor networks: The next challenge in ultra low power design," in *Proc. IEEE Int. Solid-State Circuits Conf.*, vol. 1, San Francisco, CA, Feb. 2002, pp. 200–201.

[4] P. Choi *et al.*, "An experimental coin-sized radio for extremely low-power WPAN (IEEE 802.15.4) application at 2.4 GHz," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2258–2268, Dec. 2003.

[5] M. Honkanen, A. Lappeteläinen, and K. Kivekäs, "Low end extension for Bluetooth," in *Proc. IEEE Radio and Wireless Conf.*, Atlanta, GA, Sep. 2004, pp. 199–202.

[6] G. Asada, M. Dong, T. S. Lin, F. Newberg, G. Pottie, and W. J. Kaiser, "Wireless integrated network sensors: Low power systems on a chip," in *Proc. 24th Eur. Solid-State Circuits Conf.*, The Hague, The Netherlands, Sep. 1998, pp. 9–16.

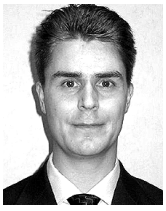
[7] T. Melly, A.-S. Porret, C. C. Enz, and E. A. Vittoz, "An analysis of flicker noise rejection in low-power and low-voltage CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 102–109, Jan. 2001.

[8] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: A simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 15–25, Jan. 2000.

[9] S. Mahdavi and A. A. Abidi, "Fully integrated 2.2-mW CMOS front end for a 900-MHz wireless receiver," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 662–669, May 2002.
[10] H. Sjöland, A. Karimi-Sanjaani, and A. A. Abidi, "A merged CMOS LNA and mixer for a WCDMA receiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1045–1050, Jun. 2003.
[11] W. Sansen and R. Meyer, "An integrated wide-band variable-gain amplifier with maximum dynamic range," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 8, pp. 159–166, Aug. 1974.
[12] J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, and K. A. I. Halonen, "A dual-band RF front-end for WCDMA and GSM applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1198–1204, Aug. 2001.
[13] D. Python, A.–S. Porret, and C. Enz, "A 1 V 5th-order Bessel filter dedicated to digital standard process," in *Proc. Custom Integrated Circuits Conf.*, San Diego, CA, May 1999, pp. 505–508.
[14] A. Baschirotto, U. Baschirotto, and R. Castello, "High-frequency CMOS low-power single-branch continuous-time filters," in *Proc. Int. Symp. Circuits and Systems Conf.*, Geneva, Switzerland, May 2000, pp. II-577–580.
[15] T. Hollman, S. Lindfors, T. Salo, M. Länsirinne, and K. Halonen, "A 2.7 V CMOS dual-mode baseband filter for GSM and WCDMA," in *Proc. Int. Symp. Circuits and Systems Conf.*, Sydney, Australia, May 2001, pp. I-316–319.
[16] A. Behr, M. Schneider, S. Fihlo, and C. Montoro, "Harmonic distortion caused by capacitors implemented with MOSFET gates," *IEEE J. Solid-State Circuits*, vol. 27, no. 10, pp. 1470–1475, Oct. 1992.
[17] R. P. Jindal, "Gigahertz-band high-gain low-noise ACG amplifiers in fine-line NMOS," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 8, pp. 512–521, Aug. 1987.

Jere A. M. Järvinen was born in Espoo, Finland, in 1977. He received the M.Sc. degree in electrical engineering from Helsinki University of Technology, Helsinki, Finland, in 2002, where he is currently working toward the Ph.D. degree.

His research interests are in development of low-voltage, low-power analog circuit techniques for sensor and wireless applications.



Jouni Kaukovuori was born in 1977. He received the M.Sc. degree in electrical engineering from the Helsinki University of Technology (HUT), Helsinki, Finland, in 2002, where he is currently working toward the D.Sc. degree.

Since 2001, he has been a Research Engineer with the Electronic Circuit Design Laboratory, HUT. His main research interests are CMOS RF circuits for wireless applications.

Jussi Ryynänen (S'99–M'04) was born in Ilmajoki, Finland, in 1973. He received the Master of Science, Licentiate of Science, and Doctor of Science degrees in electrical engineering from the Helsinki University of Technology (HUT), Helsinki, Finland, in 1998, 2001, and 2004, respectively.

He is currently a Senior Research Engineer with the Electronic Circuit Design Laboratory, HUT. His main research interests are RF circuits, low-noise amplifiers, and mixers in direct-conversion receivers.

Jarkko Jussila (S'99–M'04) was born in Jyväskylä, Finland, in 1972. He received the Master of Science, Licentiate of Science, and Doctor of Science degrees in electrical engineering from the Helsinki University of Technology (HUT), Helsinki, Finland, in 1996, 2001, and 2003, respectively.

From 1995 to 2004, he was a Research Engineer with the Electronic Circuit Design Laboratory, HUT, working on active baseband filters and direct-conversion receivers. Since April 2004, he has been a Senior Research Engineer with Nokia Research Center, Helsinki, Finland. His research interests are in the area of RF and analog integrated circuit design for wireless receivers.

Kalle Kivekäs (S'01–M'03) was born in Helsinki, Finland, in 1974. He received the Master of Science, Licentiate of Science (Tech.), and Doctor of Science (Tech.) degrees in electrical engineering from the Helsinki University of Technology (HUT), Helsinki, Finland, in 1999, 2001, and 2002, respectively.

From 1998 to 2002, he was a Research Engineer with the Electronic Circuit Design Laboratory, HUT. Since 2002, he has been with Nokia Research Center, Helsinki, where he is currently a Senior Program Manager.

Mauri Honkanen received the M.Sc degree (with honors) in electrical engineering from the Helsinki University of Technology (HUT), Helsinki, Finland, in 1995.

From 1994 to 1997, he was with the Communications Laboratory, HUT, performing research on radio propagation modeling and system modeling of RF components. Since 1998, he has been with Nokia Research Center, Tampere, Finland, where he is currently a Research Manager. His research interests include wireless transceiver architectures and short-range wireless communication systems.

Kari A. I. Halonen (M'02) was born in Helsinki, Finland, on May 23, 1958. He received the M.Sc. degree in electrical engineering from the Helsinki University of Technology (HUT), Helsinki, Finland, in 1982, and the Ph.D. degree in electrical engineering from the Katholieke Universiteit Leuven, Heverlee, Belgium, in 1987.

From 1982 to 1984, he was an Assistant with HUT and as a Research Assistant with the Technical Research Center of Finland. From 1984 to 1987, he was a Research Assistant with the E.S.A.T. Laboratory, Katholieke Universiteit Leuven, enjoying also a temporary grant of the Academy of Finland. Since 1988, he has been with the Electronic Circuit Design Laboratory, HUT, as a Senior Assistant (1988–1990) and the Director of the Integrated Circuit Design Unit of the Microelectronics Center (1990–1993). He took a leave of absence during the academic year 1992–1993, acting as the R&D Manager with Fincitec Inc., Helsinki, Finland. From 1993 to 1996, he was an Associate Professor and, since 1997, a full Professor with the Faculty of Electrical Engineering and Telecommunications, HUT, where he became the Head of the Electronic Circuit Design Laboratory in 1998. He specializes in CMOS and BiCMOS analog integrated circuits, particularly for telecommunication applications. He is the author or coauthor over 150 international and national conference and journal publications on analog integrated circuits. He holds several patents on analog integrated circuits.

Prof. Halonen served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 1997 to 1999. He was a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the Technical Program Committee Chairman for the European Solid-State Circuits Conference 2000. He was the recipient of the Beatrice Winner Award of the 2002 International Solid-State Circuits Conference.