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Life Cycle Assessment of Power Semiconductor Module Manufacturing

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Abstract

Power modules with Insulated Gate Bipolar Transistors (IGBTs) are utilized in a wide range of applications. While power semiconductor components are used to control power and enhance energy efficiency, producing such devices requires resource-demanding and energy-intensive steps, in addition to using hazardous chemicals. The need to consider sustainability as a primary aspect of the device's life cycle has become inevitable. In this thesis, the latest IGBT and Free-Wheeling Diode (FWD) design and production trends have been studied to construct a Life Cycle Assessment (LCA) model for mimicking a commercial silicon IGBT power module manufacturing phase. Recent power semiconductor developments are assessed from a sustainability aspect and the model is designed to show the most dominant environmental impacts in the device's production phase. Moreover, the literature provides background on related LCA studies in the field of electronics with a closer look at power devices. A cradle-to-gate model was built using LCA for experts (GaBi) software after a teardown process of the module. The construction of the model is shown in detail. The environmental impacts were obtained, and two categories were chosen to be quantitatively assessed; it was found that semiconductor front-end production dominates both Global Warming Potential (GWP) and ecotoxicity categories, followed by baseplate and nickel production. Furthermore, it was found that transparent presentation of the methodology for conducting the inventory and calculating the environmental impacts are mandatory steps.

Keywords Sustainability, Environmental Impacts, Life Cycle Assessment, LCA for experts (GaBi), LCIA, IGBT, FWD, Power Module

Preface

This master thesis is done under the KDT JU PowerizeD project and conducted at Aalto University, under the supervision of Professor Mervi Paulasto-Kröckel. I would like to express my deepest gratitude to my supervisor and teacher, Professor Mervi, for her exceptional support, guidance, and understanding throughout the thesis work. I am truly thankful for the opportunities granted to me by Professor Mervi. Immense gratitude is also extended to my advisor, D.Sc. (Tech.) Leena Tähkämö, for the invaluable support provided. I feel extremely fortunate to have the chance to learn from such respected experts.

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Otaniemi, 21 July 2023
Mostafa Radwan

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Abbreviations

ACD	Anode-Controlled Diode
BGA	Ball Grid Array
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical-Mechanical Polishing
CSTBT	Carrier Stored Trench-gate Bipolar Transistor
CTU	Comparative Toxic Unit
DCB	Direct Copper Bonded
DMOS	Double-Diffusion Metal-Oxide-Semiconductor
EC	European Commission
ECD	Emitter-Controlled Diode
EDS	Energy Dispersive X-ray Spectroscopy
EPA	Environmental Protection Agency
FWD	Free-Wheeling Diode
FS	Field Stop
GSD	Geometric Standard Deviation
GWP	Global Warming Potential
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
ILCD	International Reference Life Cycle Data System
IMC	Intermetallic Compound
IPCC	Intergovernmental Panel on Climate Change
ISO	International Organization for Standardization
LCA	Life Cycle Assessment
LCI	Life Cycle Inventory
LCIA	Life Cycle Impact Assessment
MELF	Metal Electrode Leadless Face
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPT	Micro Pattern Trench
MRD	Mineral Resource Depletion
MTBF	Mean Time Between Failure
NPT	Non-Punch Through
NTC	Negative Temperature Coefficient
OD	Ozone Depletion
PACE	Plasma Assisted Chemical Etching
PBT	Polybutylene Terephthalate
PCB	Printed Circuit Board
PEC	Power Electronic Converters
PFC	Perfluorocarbons
PT	Punch Through
RC-IGBT	Reverse Conducting Insulated Gate Bipolar Transistor
SEM	Scanning Electron Microscopy
SETAC	Society of Environmental Toxicology and Chemistry
UNEP	United Nations Environmental Program
VOC	Volatile Organic Compound

1 Introduction

In the last years, sustainability has become increasingly important across different fields [1],[2],[3]. Power Electronic Converters (PECs) including Insulated Gate Bipolar Transistor (IGBT) power modules are used in many different applications, e.g., industrial motors and high-speed rail [4] to realize energy-efficient use of power. Still, the life cycle of power electronics - meaning their manufacturing, use and end of life, consumes lots of resources and produces environmentally harmful emissions. One way to assess the environmental impacts of such devices is by assessing the emissions and resource exploitation throughout the device life cycle. Consequently, a technique standardized by the International Organization for Standardization (ISO) called Life Cycle Assessment (LCA) has been developed. The standardized technique is used to collect an inventory for an LCA study and assess the environmental impacts caused by the elements of the inventory. An LCA study can target a particular phase of a life cycle or the entire life cycle of a device, product, or facility.

The technique is widely known and is used in various electronics fields and applications [5],[6],[7]. Nevertheless, LCA studies published in the field of power electronics are qualitative and are not supportive of decision-making due to a lack of quantitative data [8]. Moreover, the results of quantitative LCA studies within the same scope can vary [9].

This thesis aims to investigate the implementation of a life cycle assessment technique to quantitatively assess the cradle-to-gate environmental impacts of a commercial silicon IGBT power module by building an LCA model with the available literature and software. Moreover, one of the study's goals is to investigate the idea of implementing different databases, namely ecoinvent and GaBi databases to solve one source of data limitation. Furthermore, the thesis aims to address the sources of variations and uncertainties within LCA studies and ways to reduce them. Finally, the thesis aims to show, in detail, the methodology of conducting the Life Cycle Inventory (LCI) and the results of the study including the main environmental impacts resulting from cradle-to-gate manufacturing processes of the module.

The thesis begins with a review of the latest developments in the design of IGBT and diode chips as a background of the route towards reliability and performance improvements. These improvements by default have environmental impacts that can be positive or negative. The thesis briefly investigates the production of semiconductors with a closer look at IGBT production. Thirdly, the environmental impacts of using LCA in the field of electronics, in general, are presented as background concepts of the study. The last

part of the background presents published literature in LCA of Si IGBT power modules.

The method chapter introduces the first elements of an LCA study and shows how the LCI was conducted, including a teardown section. The chapter also introduces the Life Cycle Inventory Assessment (LCIA) and the different methodologies, databases and software used. The results and discussion section shows the results of the teardown, scaling, and limitations of the model, which is an essential element in an LCA study. Finally, the most important findings are summarized in the conclusions chapter which includes LCIA interpretation. The word sustainability within the thesis is used for the environmental impacts' aspects only.

2 Silicon Power Devices

In this chapter, history, and recent developments in IGBT and diode chip technologies are presented.

2.1 Silicon IGBTs

IGBT was invented in the 1980s by Wheatley and Becke in the United States. It was first developed to compensate for the drawbacks of Bipolar Junction Transistors (BJTs) in terms of low current gain and poor safe operating area. Later in the 1990s, the advantages of IGBT over bipolar transistors and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) were described. An IGBT combines the physics of a MOSFET and a BJT by integrating the insulated gate input of a power MOSFET with the low on-state resistance of a power BJT [10]. Moreover, IGBTs integrate the high input impedance of a MOSFET with the high current density of a bipolar device, which makes IGBTs ideal for medium-frequency high-power applications [11].

The wideband gap material, SiC, for high voltage applications arise questions about further utilization of Si IGBT. SiC have better electrical and thermal properties in comparison with Si, making it a better substitute for high-voltage DC applications. The superiority of SiC in terms of electrical properties is due to wider bandgap in comparison with Si which enables SiC to oversee higher electric fields. Moreover, SiC can manage higher power densities due to excellent thermal conductivity. However, there are multiple limitations concerning wide bandgap materials, one of which is short circuit robustness [12]. Nevertheless, developments in short-circuit robustness are reported [13]. Even though SiC is used (e.g., in some automotive applications) the technology as a whole is still under development. Furthermore, the development of the device faces challenges in packaging, driver electromagnetic interference and protection [14]. Si IGBT is expected to be used and developed further alongside other SiC power semiconductors in the upcoming years [12]. On the other hand, SiC MOSFET is currently utilized in power applications and its performance has been compared with Si IGBT in many studies [15]. The combination of Si IGBT and SiC MOSFET in inverting applications is reported [16], [17].

2.1.1 Different Technologies

Since the early development of the first commercial IGBT, different technologies have been reported [18], [19], [20]. Figure 1 shows advancements in the die size for 1200V-50A IGBT. The different technologies targeted the improvement of IGBT cell design to improve the characteristics and

downsize the design. Early IGBT development utilized Punch Through (PT) technology, the technology showed poor short circuit capabilities, followed by Non-Punch Through (NPT) technology, NPT IGBTs offer low carrier concentration, lower switching losses and higher switching robustness. The downside of NPT IGBT technology is the size of the n- layer, which results in high dynamic and static losses. NPT IGBT was further developed by adding a Field Stop (FS) layer. The layer has the capability of stopping the electrical field in blocking conditions without affecting the p collector's low dose of NPT IGBT. FS IGBT has a thinner base region, offering fewer switching losses than NPT technology. Moreover, it was possible by the FS IGBT to reduce the NPT thickness by one-third. Figure 2 shows PT, NPT, and FS IGBT chip structures [12].

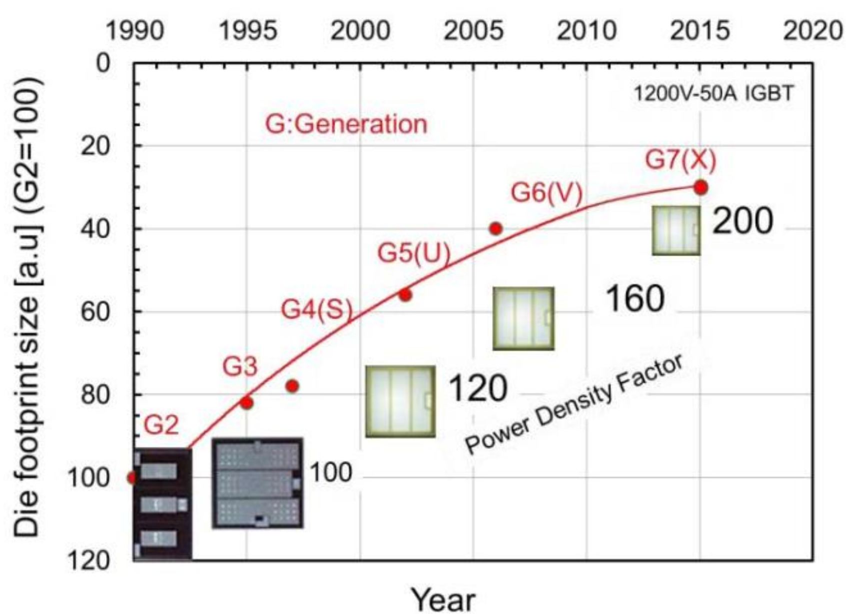


Figure 1: Advances in chip size of 1200 V IGBT since 1990 [12].

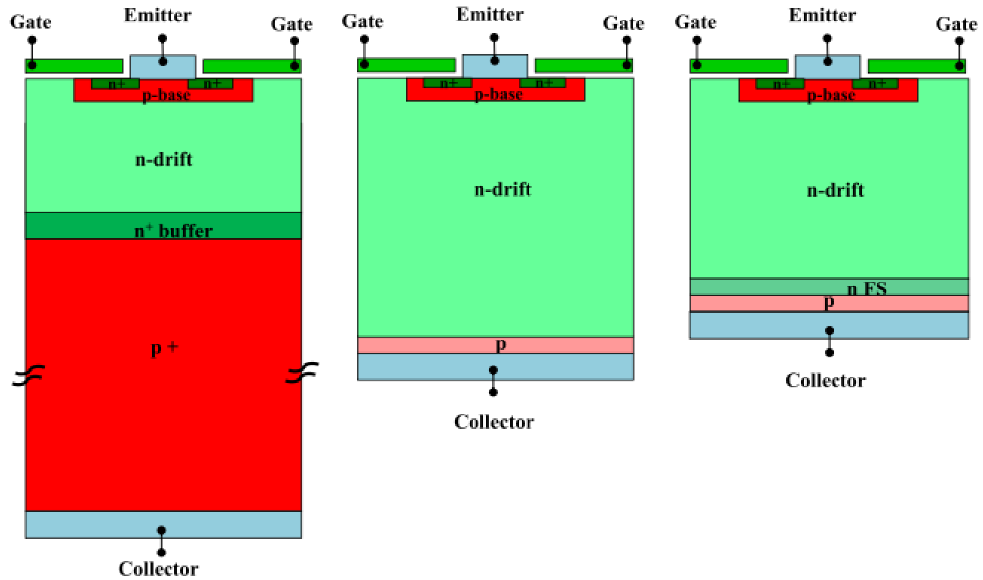


Figure 2: Punch-through, non-punch-through, and field stop structures respectively from left to right [12].

Recently, the developments are targeting better power density and aiming to further develop the chip characteristics for different applications, in addition to increasing high power junction temperature reliability by improving the packaging. Moreover, the sustainability improvements can be reflected in recent publications concerning new designs [21]. The mentioned improvements can be reflected by the different technologies of the 7th generation of IGBT.

2.1.2 Seventh Generation

One technology based on Micro-Pattern Trenches (MPTs) was reported as a 7th-generation IGBT technology [19]. Jaeger et al. [20] presented an advancement in the technology as a new sub-micron trench cell concept. The concept uses MPT cell structure with sub-micron mesas. Figure 3 shows the MPT-IGBT chip frontside. The technology increases the channel width of the IGBT by narrow parallel trenches which are separated by sub-micron mesas. The concept offers lower conduction losses compared to conventional square cell structure which is achieved by the MPT chip structure presented in the figure. That is made possible by increasing the carrier confinement during the on-state, particularly at the front side of the chip [20].

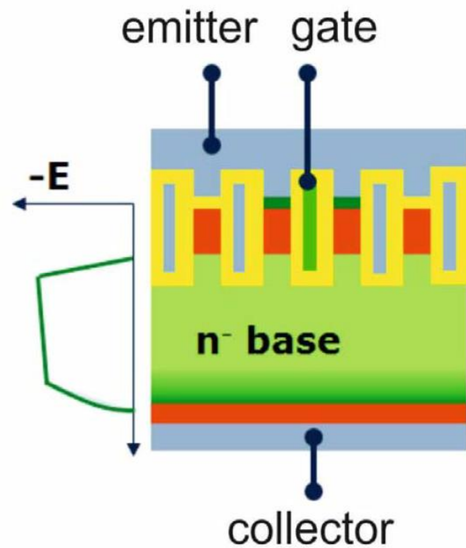


Figure 3: Front side view of MPT IGBT structure [20].

Takahashi et al. [18] presented another technology as a 3rd generation technology at the time and is still used by Mitsubishi in their latest generation "gen 7" after development [22]. The technology is Carrier Stored Trench-gate Bipolar Transistor (CSTBT). The advancements in CSTBT technology from generation 5 to 7 in terms of chip thickness are presented in Figure 4 [23].

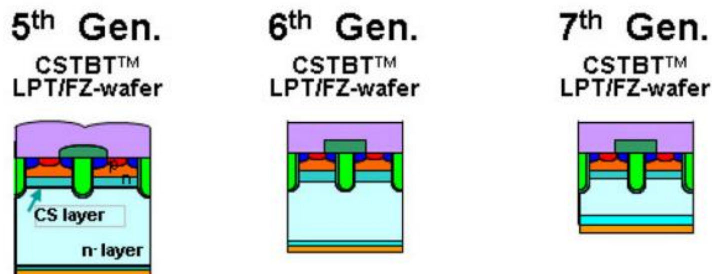


Figure 4: 5th,6th, and 7th generations of CSTBT structure developed by Mitsubishi [23].

2.1.3 IGBT Production

The production of Si IGBT chips among other Si semiconductors starts with silicon ingot growth. Large wafer diameters are desired for power devices [24], Magnetic Czochralski (m: CZ) is used to fabricate a silicon wafer with a diameter of 300 mm. The process can produce defect-free, single-crystal silicon that is used for fabricating IGBT among other power semiconductors [24]. The process takes place under a dynamic gas flow, in which only noble gasses such as argon are required due to the high temperature of the silicon

melt [25]. The growth process starts with loading the silicon into the crucible (container used to hold and melt silicon). The second step is the melting process of silicon which takes a few hours. The hot zone's first temperature is 1500C, the temperature is then regulated further within the same temperature margin to melt the silicon, and a molten silicon pool is formed. Typical growing steps then follow [25], [26]. The graphite hot zone and gas flow dynamics play important roles in the energy consumption for ingot production, Figure 5 shows the energy demand for the Czochralski growth process per kg of silicon produced with a typical hot zone and an improved recharge hot zone. Recharge refers to continuous silicon feedstock. The paper discusses silicon growth for Photovoltaics. Higher-purity silicon is used in power electronics; hence, the growth process requires higher electricity demand. One estimation of the energy requirement for polished silicon wafers used in power electronics is 2127 kWh/kg [28].

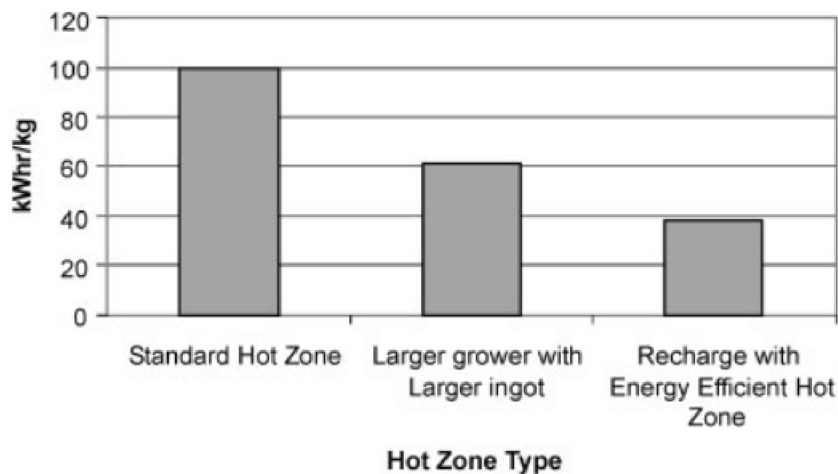


Figure 5: Energy demand for wafer production in kWh/kg considering a typical hot zone and recharge hot zone [27].

After producing the ingot, grinding, notching or orientation flattening is performed, followed by wafer slicing. Traditionally, an ID saw was used. Recently, the ID saw has been replaced by a multiple wire saw, refer to Figure 6, which results in improved yields, see Figure 7.

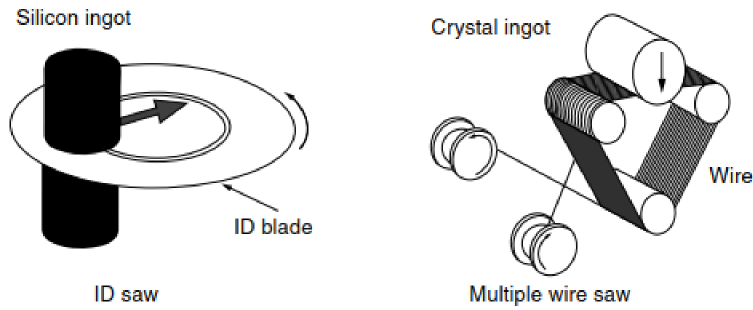


Figure 6: Schematics of ID saw, and multiple wire saw [26].

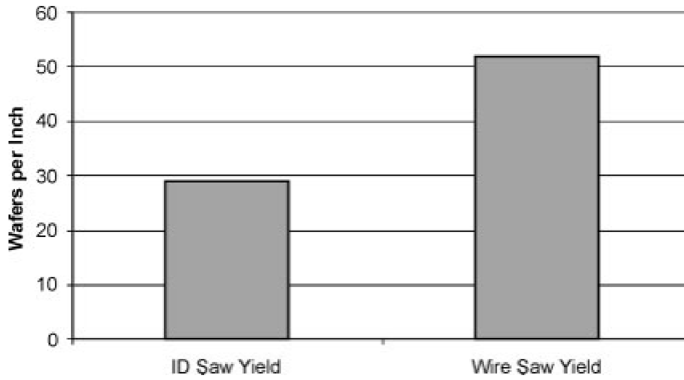


Figure 7: Yield in wafers per inch for the case of ID wire saw and multiple wire saw [27].

By the time the ingot is diced and ground, mechanical damage is induced. Chemical etchants of acidic nature, such as HNO3-HF or alkaline solution, KOH for example, are used to remove the damage. The process might be repeated until the desired outcome is achieved. Followed by edge rounding and another step of grinding or lapping. The lapping process is performed to eliminate the non-uniform damage caused by slicing. Edge polishing takes place by both mechanical and chemical, alkaline-based, processes known as Chemical-Mechanical Polishing (CMP). The process is standardized for wafers with a diameter equal to or more than 300 mm. Plasma Assisted Chemical Etching (PACE) is also used to ensure the local flatness desired. The end product from the mentioned processes is a mirror-finished surface. To remove contaminations on the wafer, a cleaning process is finally performed. The cleaning process is usually repeated multiple times during the fabrication. As per the literature, the most widely used cleaning method is called RCA clean. Which utilizes the use of two different solutions: solution one is H2O-H2O-NH4OH and solution two is H2O-H2O2-HCL.

Different technologies are implemented for manufacturing IGBT chips. A field-stop IGBT manufacturing process through epitaxy technology is

briefly taken here as an example. In their patent, May and Spanos [29] presented a method for manufacturing a field stop IGBT with an epitaxial layer, in which, a P-type substrate is prepared, where the sum of the substrate and the epitaxy equals a common silicon wafer. The final thickness in one embodiment of the patent is around 700 µm. However, in the industry, much smaller end chip thicknesses are utilized. The field stop layer is formed by the implantation of N-type ions. The ions can be of sulphur or phosphorus among other materials. In the same embodiment, an annealing temperature of 1150-1250 degrees Celsius for 5-20 hours is used for a 15–30 µm FS layer. Thermal oxidizing is then performed with temperatures ranging from 900 to 1200 degrees Celsius using pure water vapour or pure dry oxygen. The gas flow rate is around 1 L/min. Thermal oxidization, being the most widely used for silicon wafers, is one of several methods to grow an oxide layer on top of the wafer [29]. To remove the oxide layer, wet etching is used with etchants such as hydrofluoric acid. The N-type buffer and drift layers are prepared by epitaxy technology. Normal fabrication methods for IGBT then follow. The thicknesses from the embodiment are 2-40 and 10-150 µm respectively [30].

2.2 Silicon Power Diodes

Diodes are the simplest devices built based on a pn-junction. Where the p-terminal is referred to as the anode and the n-terminal is referred to as the cathode. A typical structure of a power diode with a drift zone (PiN diode) is shown in Figure 8. The drift zone which is a lightly doped n-region, done in an epitaxial process, serves to absorb the blocking voltage. The terms PT and NPT diodes refer to the ability of the applied blocking voltage's electrical field to penetrate the intrinsic zone (n-region). NPT diodes are fabricated with an appropriate doping profile. There is a direct proportion between the n-region size and the blocking voltage required for the diode [31].

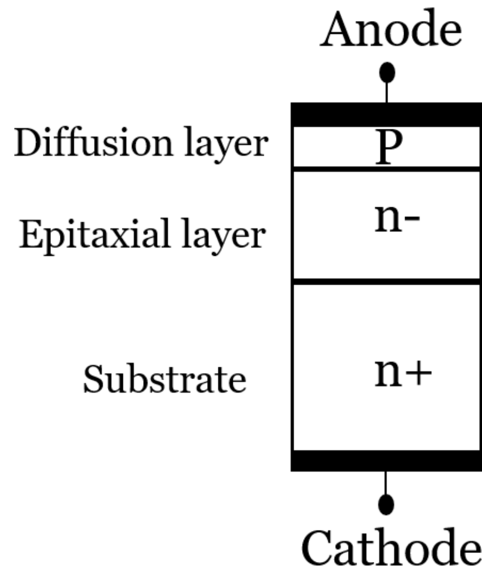


Figure 8: PiN diode structure. Adapted from [31].

In most IGBT applications, an antiparallel connection between the IGBT and the diode is implemented. The diode in that case is called a Free-Wheeling Diode (FWD). The name comes from the functionality of the diode, as it provides a freewheeling circuit for the current after the IGBT is turned off. Moreover, the time required for the diode to move into its blocking state from its conducting state (reverse recovery time) needs to be considered for high-frequency applications. That is why fast recovery diodes that have a small reverse recovery time are widely used in power modules [31].

2.2.1 IGBT and Diode Integration

In this section, some of the different structures of power diodes are presented for realizing the possible differences between the diode chips inside the module under discussion and other integration and chip technologies that exist.

2.2.1.1 RC-IGBT

The improvement of diode chips in IGBT power modules is inevitable with the improvement of IGBT chips. Maintaining low conduction losses is essential for high power gain [32], for that reason, different controllable power diodes have been implemented to achieve the desired outcome. Those implementations include MOS-Controlled Diode (MCD), Anode-Controlled Diode (ACD) Gate-Controlled Diode (GCD) and Emitter-Controlled Diode (ECD). Additionally, the integration of IGBT with a power diode on the same chip, Reverse Conducting IGBT (RC-IGBT) with Diode Control (RCDC) is commercially available [33].

The different diode technologies with IGBT are reported here considering a silicon substrate for all different technologies. Nevertheless, SiC diodes are also commercially available and are widely used in the power semiconductor industry [34]. RC-IGBT is a type of IGBTs that has the functionality of both IGBT and FWD. The implementation of RC-IGBT makes it possible to eliminate FWD chips in the module, which contributes positively to size optimization. An RC-IGBT design optimized for hard-switching applications was reported in 2014 [33]. The structure of the design is shown in Figure 9. The 6th generation of Fuji IGBTs implements trench gate and field stop bulk [35]. The RC-IGBT fabrication process is similar. Nonetheless, a backside photo-etch ion-implantation process to form the backside pn-structure is added, in addition to a lifetime control process [33].

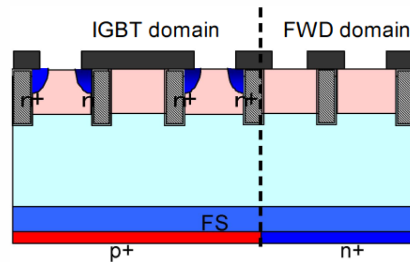


Figure 9: RCDC structure, integration of IGBT and FWD on the same chip, reported by Fuji. Adapted from [33].

2.2.2 Gate-Controlled Diode

Another concept was proposed for a higher voltage class [36], in which the use of MPT cell design is utilized for high carrier confinement to achieve a low on-state voltage drop. The diode is gate-controlled in that case. The structure of the diode is shown in Figure 10. As illustrated in the figure, the MPT structure is on the anode side with a PiN overall configuration. The anode region in that case is 2.5 µm thick. One mesa width is 0.4 µm over a 6-µm wide structure. It was argued that the GCD showed improvements in terms of switching and conduction losses compared to the same voltage class substitutes [36].

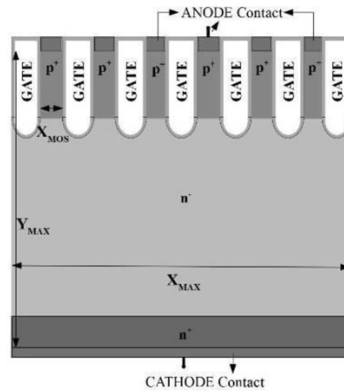


Figure 10: Cross-section of MPT structure with a gate-controlled diode [36].

2.2.3 Emitter-Controlled Diode

Rodriguez et al. [37] have published a novel structure of ECD. The design of the older generation and the newer structure is presented in Figure 11. The module under discussion is expected to have the novel structure presented in the figure. The structure utilizes a copper metallization on the anode side. This results in increasing the cosmic radiation hardness, and around 30% current density increase. The latest generation of emitter-controlled diodes is EC7, in which the diode is optimized to maintain low losses. It was reported that EC7 shows the same recovery losses compared to another generation reported as emitter-controlled-HE [37]. Umbach et al. [38] reported the technology utilization for a high-voltage class.

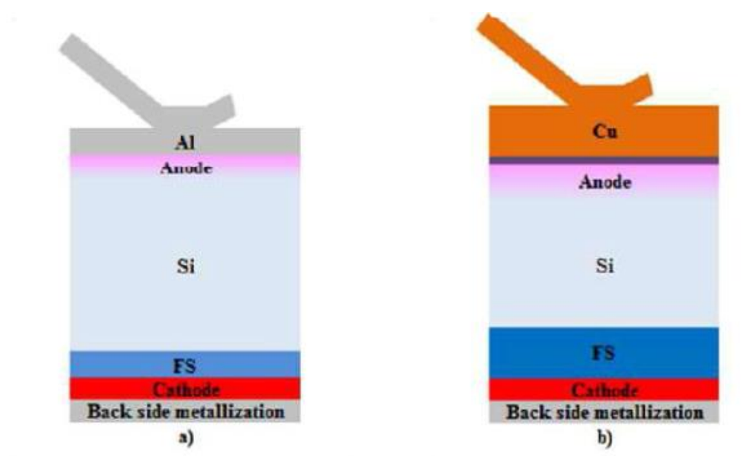


Figure 11: a) Conventional design, b) novel design of Infineon's ECD [37].

2.3 Module Structure and Packaging

A typical structure of a standard IGBT power module with a baseplate is shown in Figure 12. It is worth noting that such a structure is the most widely used by all manufacturers [39]. The structure comprises a plastic frame/lid, silicone gel for moulding, substrate, semiconductor chips, chip/system solders, terminals, wires for different connections and a baseplate.

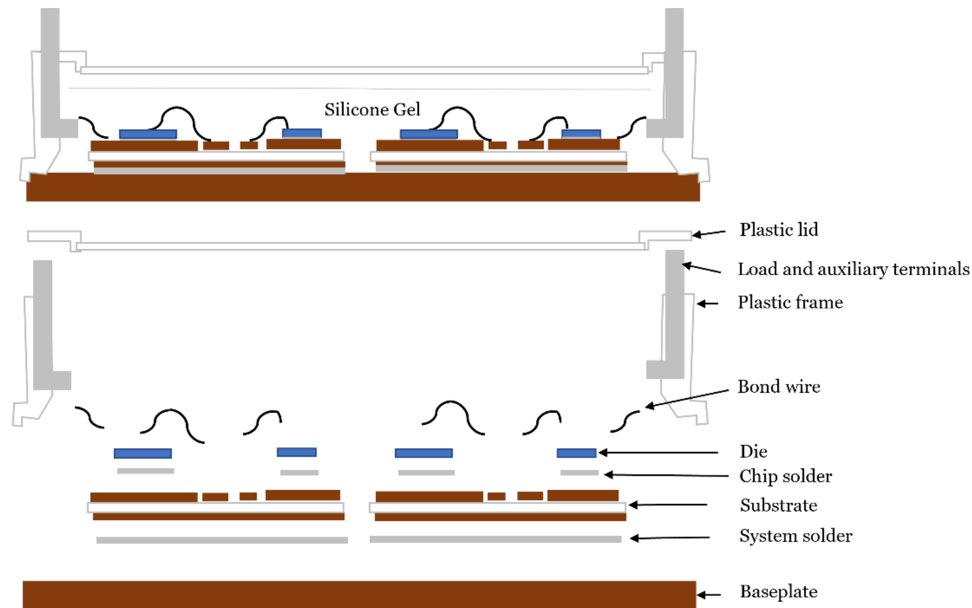


Figure 12: Typical IGBT power module structure. Adapted from [39].

2.3.1 Substrate

The most widely used substrates in power semiconductors are Direct Copper Bonded (DCB) substrates. Initially, a substrate was always combined with a baseplate. Nevertheless, in current power semiconductors, a DCB substrate may be used alone or with a baseplate. The DCB substrate is used to supply electrical connection and thermal path to the baseplate [40]. A ceramic insulation layer is bonded with two copper foils from the top and the bottom of the insulation layer. The ceramic layer can be of aluminium oxide (Al2O3) or aluminium nitride (AIN) among other materials. The top copper is then patterned and, in some cases, plated with another metal like nickel.

Producing a DCB substrate includes multiple processes with the use of a variety of chemicals. The processes, materials, and chemicals used can differ from one manufacturer to another. Figure 13 shows an example of a DCB structure, the example is for a substrate in which AIN is used as the ceramic substrate with AI2O3 as an intermediate layer [41].

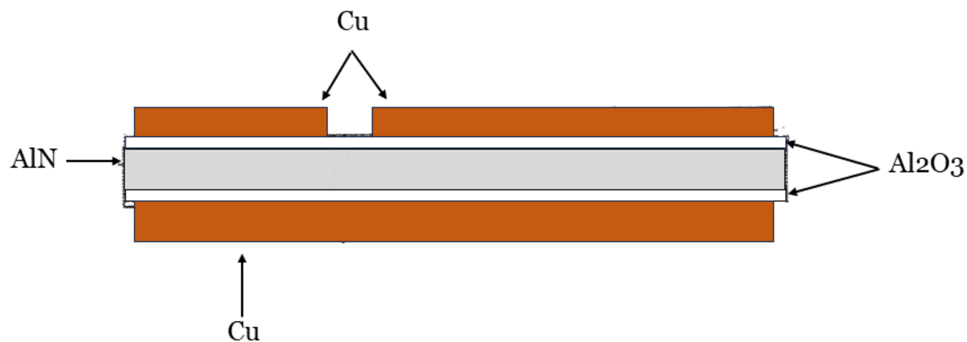


Figure 13: An example of a DCB substrate. Adapted from [41].

2.3.2 Baseplate

Baseplates are usually made of copper with a thickness of 3-8 mm. Coated with nickel 3-10 µm thick, other materials like aluminium silicon carbide [42] and copper-molybdenum are also used but less frequently. The baseplate function is to provide contact with the cooling medium (heatsink) [39]. Based on that, baseplates are mainly used in medium and high-power applications while low-power application modules are manufactured without a baseplate. The baseplate plays an important role in the module's lifetime; the lifetime of modules without a baseplate is limited by the substrate metallization due to its influence on heat dissipation and electrical conductivity, whereas the failure of modules utilizing a baseplate is mainly due to degradation within the system solder layer (solder between the DCB substrate and the baseplate) [43]. Figure 14 shows the structure of a module packaged with and without a baseplate. The design of the baseplate including the thickness and warpage plays an important role in the module's performance and reliability [44],[45],[46].

A vacuum soldering process in a soldering furnace is used to connect the semiconductor chips to the DCB substrate. The soldering process includes both electrical and thermal connections. The soldering process should be complying with the RoHS directive in the sense of having lead-free solder. The DCB is further attached to the baseplate by a soldering process that is dependent on the ceramic substrate material.

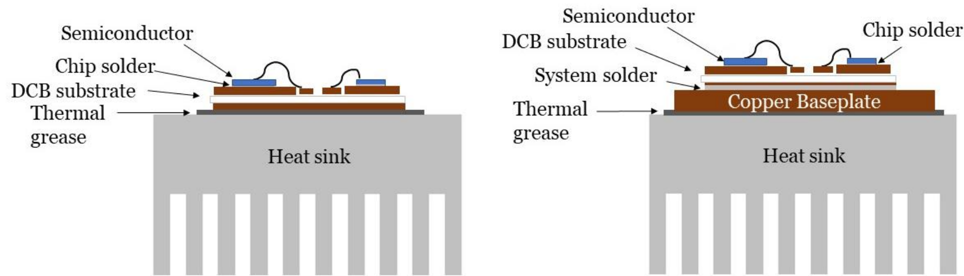


Figure 14: Power module structure without a baseplate, left and with a baseplate, right. Adapted from [39].

2.3.3 Encapsulation

The undertaken endeavours in reducing the size of the IGBT chip are reflected in the development of the packages. Figure 15 shows an example of a 1200V/35A standard power module and the shrinking in size through four different generations of IGBT chips [12].

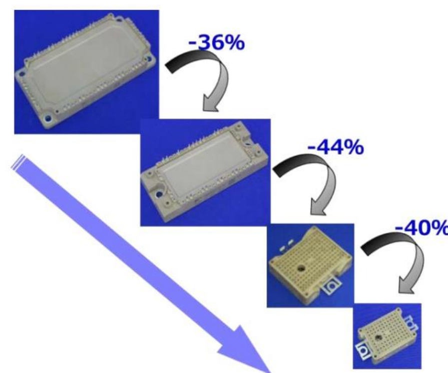


Figure 15:1200V/35A standard power module package reduction over four different generations of IGBT chips [12].

The seventh generation of IGBT is not only concerned about the chip structure and downsizing but it also addresses package reliability. The reason for that is the trade-off between increasing power density, hence rising temperature, and degrading reliability. Heinzel et al. [47] have presented an example of the difference between two recently developed technologies for Si IGBT modules in terms of package development for a 1200V/75A rating. The

package developed for the newer generation of IGBT (generation 7) utilizes a footprint reduction of 2728 mm^2 and a 25% decrease in the total weight [47].

On the contrary, not all developments in IGBT chip size reduction reflect a package size reduction. As an example, Vogel [48] reported a package that has been in use since 2005 despite chip evolutions since that time. The housing is still used with the same footprint when implemented with different generations like a 4th and a 7th generation of IGBT and diodes [49],[50]. In the same paper, the author introduced a new concept for housing that reported a 20% reduction in losses when implemented with IGBT7 and EC7. Additionally, less copper is achieved by removing the baseplate. The baseplate is compensated for by a new substrate and housing concepts.

3 Environmental Impacts

Environmental impacts as defined by the United States Environmental Protection Agency (EPA) are any change to the environment, positive or negative resulting from a facility, product, or service [51]. An example of a positive impact can be realized by preserving hectares of tropical forest [52]. The hectares of land absorb carbon dioxide from the atmosphere. Hence, resulting in a positive environmental impact. Within this thesis, the term sustainability refers only to the environmental impacts and does not consider social or cost aspects. On the other hand, a negative impact can be realized by the emission of a Volatile Organic Compound (VOC) during the manufacturing of a device, which results in photochemical smog. Smog is a smoke-fog mix that happens due to a reaction of sunlight with nitrogen oxide when at least one VOC is present in the atmosphere [53]. In this case, the emission of volatile organic compounds is an environmental aspect and air pollution, smog is an environmental impact [51].

Many countries and organizations have set goals for carbon neutrality within a specified time. The term carbon neutrality means balancing carbon emissions to the atmosphere with carbon absorptions from the atmosphere. The European Union as an example is aiming to make the continent the first to neutralize carbon dioxide emissions by 2050 [54]. Some countries aim to have the same goal by earlier dates like Uruguay and Finland. Other countries already achieved the goal and rather considered carbon negative like Bhutan [55]. The idea of greenwashing has been discussed in many studies [56],[57]. On the other hand, employing environmental aspects in a product's lifecycle is referred to as ecological design (eco-design) as defined by ISO/TR 14062 [58].

It is rather difficult to assess the environmental impacts of manufacturing, use and treatment after the lifetime. The overall geographic representation, raw materials, and the type of energy among other aspects are variables that need to be considered. Consequently, a technique standardized by ISO (LCA) is used for assessing the environmental impacts [59]. The technique is described further in this chapter. This study focuses only on the mentioned method, knowing that other methods exist for assessing environmental impacts [60][61].

3.1 Life Cycle Assessment

LCA is one of many techniques used to evaluate environmental impacts. The technique makes it possible to assess the impacts during the lifecycle of

products, services, and facilities from raw material acquisition to the final disposal. ISO 14040 has set the principles and framework for conducting an LCA study, whereas ISO 14044 has set the requirements and guidelines to implement the study [59],[62].

As illustrated in ISO 14044, an LCA study should pass through four iterative phases; goal and scope definition, in which the system boundaries and the level of details of the study are defined, where the scope corresponds to the goal of the study. The second phase of an LCA study is the life cycle inventory phase, in which the inputs and outputs of the system are collected to serve the goal of the study. The third phase is Life Cycle Impact Assessment (LCIA), in which the LCI results are assessed to evaluate the significance of the LCI items with pre-defined categories. The categories and the significance of the results can differ from one procedure/methodology to another [63], [64]. To ensure consistency, one specific methodology with one specific database should be used for assessing all different components of the study. Examples of available methodologies are CML and ReCipe. The fourth and final phase is life cycle interpretation, in which the inventory or LCIA results are interpreted and summarized to conclude the most significant points of impact to assist with decision-making and/or recommendations for making the product/facility under study more sustainable. In other words, LCA can be utilized for Eco-design mentioned in the introduction of this section. The four phases are iterative, meaning that the phases can cause changes to each other. For example, the scope of the study may change while constructing the LCI when new information arises or after releasing a misconception.

Many tools and software are utilized to conduct an LCA study, Table 1 summarizes some of the LCA tools, their developers, and the description of the software. Other software excluded from the table are CMLCA, GEMIS, and Mobius [65]. The study was conducted in 2021 when the name of LCA for experts was GaBi, and the name of the developer was Pe-international, currently, it’s Sphera.

Table 1: Popular LCA software and their description. Adapted from [65].

Tools	Developer	Description
LCA for experts (GaBi)	Sphera	The software offers the richest databases
SimaPro	PRé Sustainability	Avoids black box design for processes; the processes can be modified in contrast with GaBi
Umberto	Ipoint-systems gmbh	A flexible and powerful tool

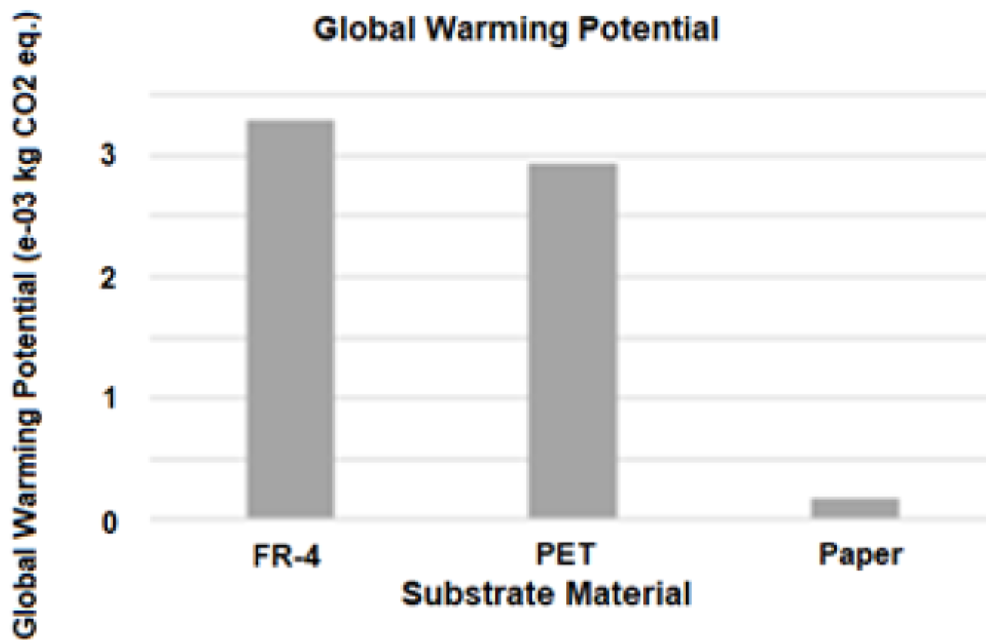
Open LCA	GreenDelta Berlin	The open-source software also does not utilize black box design for processes

Kalverkamp et al. [66] investigated the impact of using two different databases on the LCA results. The authors compared the ecoinvent database with GaBi professional database by a comparative LCA study of an internal combustion engine vs a battery electric vehicle using GaBi professional database. The results were recorded against an earlier similar study that used the ecoinvent database. The paper points to the main difference between the two mentioned databases; GaBi databases consider secondary materials in their processed material modules, whereas the ecoinvent v2.2 does not. Such differences may have a noticeable impact on the results. It was suggested that one way to reduce the uncertainty of a study is to perform the study parallelly with two different databases. Nevertheless, since this is not feasible, the authors suggested that one study using a database may motivate another to perform the same study with another database, being cognizant that the repetition would still face a structural difference between the software utilization and the database.

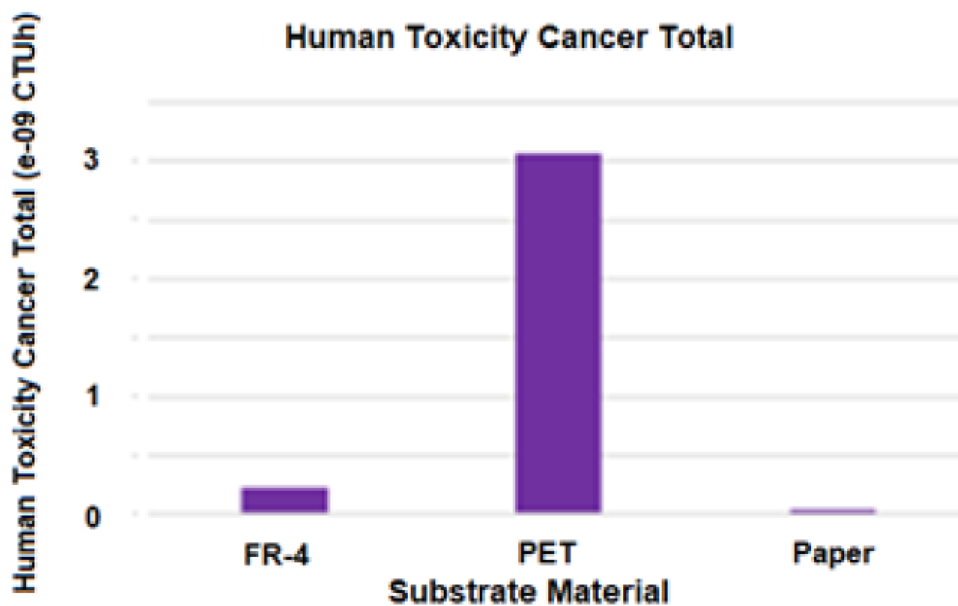
3.1.1 LCA for Electronics

Many publications in the field of LCA of electronics were reported. Some of these publications are presented here to show the state of the art of LCA in the field of electronics including semiconductors, with a closer look at power electronics and IGBTs since it is the focus of the thesis. Moreover, eco-design concepts in the field of power electronics are presented briefly in this section.

Grant. K. et al. [67] published a recent paper in which ReCiPe end point methodology was used to evaluate cradle-to-grave impacts of flame retardant four (FR-4)-based Printed Circuit Board (PCB) as the conventional substrate. The authors chose GaBi databases with Great Britain (GB) as the main route for the PCB life cycle to represent the grid mix and European standards for landfill. It was found that epoxy resin is the largest Global Warming Potential (GWP) contributor. Moreover, the authors have conducted a comparative study to show the impacts of substituting FR-4 with Polyethylene Terephthalate (PET) and paper as conceptual materials for PCB design. The result of the comparative study is shown in Figure 16. The figure shows the GWP and human toxicity cancer categories' results with the stated LCIA methodology.



(a)



(b)

Figure 16: a) GWP and b) human toxicity cancer of FR-4, PET and paper fabrications, adapted from [67].

Semiconductor chip manufacturing includes some of the most resource-intensive processes. The complexity and fast changes in designs and technologies of different semiconductor fields, make it hard to conduct a LCA

study. Moreover, semiconductor manufacturers keep almost all their process recipes confidential, which introduces a challenge in finding data for constructing an LCI. During the fabrication phase of a semiconductor chip, different classes of pollutants are emitted, in addition to the high amount of water and energy consumption. These pollutants include, but are not limited to, hazardous pollutants like fluorine, global warming gasses including CF_4, and ozone-creating VOCs such as isopropyl alcohol. Moreover, human health impact is another aspect to consider since acidic, basic, highly reactive, and toxic chemicals are used for different process steps such as fluorine (highly reactive chemical) used in etching. Also, the facility infrastructure, equipment used, raw material extraction and processing among other components contribute to the environmental impacts during the manufacturing phase of a semiconductor chip. Furthermore, the fabrication phase is not the only phase that has major environmental impacts. The impacts of the use phase and end of life can sometimes dominate those of the fabrication phase. Like in the case of a desktop main processor, in which the use phase energy-related emissions are the major emissions in the device life cycle [68].

In her book, Boyd [68] has studied GWP impact among other impacts of different Complementary Metal-Oxide-Semiconductor (CMOS) technology nodes starting from 350 nm to 45 nm nodes. The functional unit is one die over a lifetime of six thousand hours, the node reflects the device type. Personal computers purchased in 2012 contain 65 nm logic whereas 350 nm logic reflects embedded logic for the same year. The author has illustrated that for CMOS logic global warming emissions due to electricity consumption in the use phase are the highest emissions. Moreover, the author showed that GWP increases relative to the technology node complexity. Figure 17 shows the GWP represented in $kgCO_2eq$/die for seven different technology nodes in different stages of the life cycle. The author considered two fabrication scenarios in which Perfluorocarbons (PFC) abatement is applied and another where it is not. The first is a representation of a fabrication facility in the United States and the latter is a representation of a facility in China.

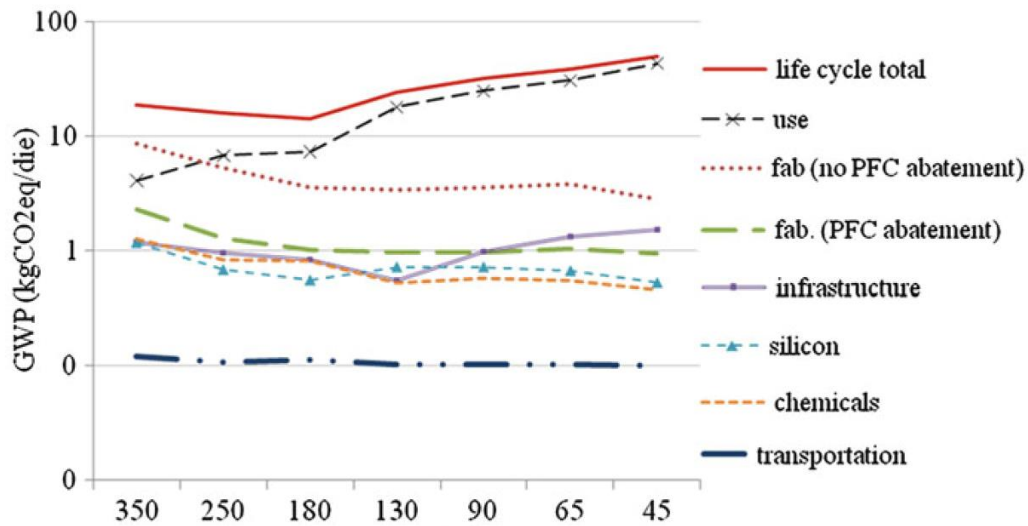


Figure 17: GWP impact represented in kgCO2eq/die for seven different technology nodes in different stages of the life cycle including fabrication with and without abatement [68].

In their paper Andrae et al. [64] used the ecoinvent database to analyse a typical Ball Grid Array (BGA)-560 package with a silicon die inside, the authors did not mention the type of the die. The results showed that silicon dies processing integrated into the package, referred to as front-end processing, accounts for around 88% of the total GWP. The paper focuses on packaging solutions to reduce environmental impacts. Andersen et al. [69] presented a similar figure for BGA-560 with front-end processing accounting for 77% of the total GWP. Both studies claim that front-end processing is dominating the overall GWP impacts.

Clement et al. [9] presented the work of five different LCA researchers in assessing the GWP of integrated circuits with die area as a unit process. Table 2 summarizes the different impacts [9]. The authors claimed that there is a big uncertainty that is induced by the lack of information from manufacturers. This does not only apply to Integrated Circuit (IC) production but rather to all semiconductor industries.

Table 2: GWP impacts represented in $kgCO2eq$ per die area in cm^2. The table shows the work of five researchers [9].

	Impact/die area	Impact/package mass
	[$kgCO_2e/cm^2$]	[$kgCO_2e/g$]
Hischier et al. (2007)	/	1
Boyd (2012)	5.5	/
Andrae et al. (2014)	2.2	/
Ercan (2016)	2.7–4.3	/
Proske et al. (2016)	5.4	/

3.1.2 LCA for Power Semiconductors

The gap between the commercially available power devices to the published sustainability data in that field is big. As is the case for other semiconductor fields, there is limited data to conduct an accurate LCA analysis. An example of that is a paper presented by Schellscheidt et al. [70], in which the ProBas database is used. Apart from mentioning the database, the paper did not provide an inventory nor methodology for the study, but rather only environmental impact percentages (qualitative data) that correspond to changes in the design. In such cases, it is hard to know whether the presented results are accurate.

Fang. L et al. [71] have published a literature review to map the research related to eco-design in PECs from 2007 until 2022, the authors suggest that there have been only limited published data in the mentioned field within the mentioned period. Moreover, the paper's findings suggest that there are four eco-design approaches used: eco-sizing, eco-reliability, energy efficiency, and multi-usage innovation. Most of the literature focus on energy efficiency which was considered a limitation [71]. Eco-reliability refers to finding a balance between sustainability and reliability [72]. Rahmani et al. [73] presented an example of multi-usage innovation towards a design for reuse and repair which rely on the components' functional value. The paper suggests that high-power application converters are mostly modular and reparable whereas, for low and medium-power modules' "reparability and reuse are still not part of the specifications during the design period" [73]. The authors proposed a design method for reparability and reuse based on an index with four indicators; price, Mean Time Between Failure (MTBF), reuse rate (based on repairing experiments), and ease of disassembly.

Recently, some publications have shown promising advances in the field. Diaz et al. [28] have presented a comparison in terms of energy demand, comparing Si and SiC power semiconductors. It was argued that SiC

devices demand more energy to produce, the paper discussed the compensation of the energy consumed during manufacturing with the energy saved during the use phase.

Nordelöf et al. [74],[75] have published a scalable LCI for automotive power electronic inverter units. The subparts of the inverter including the power module were also considered individually. The authors have used the ecoinvent database for complete processes when available. The authors have transparently shown their methods and bases of assumptions on a supplementary technical and methodological description, making it possible to use, assess, modify, or build on the LCI model [76]. Another very important finding is that the publications also showed how limited the data is in the field of power electronics.

Chalmers model (named by Baudais et al. [77]) has been utilized in other related LCA studies [77],[78],[79]. Baudais et al. [77] have shown different categories of environmental impacts of a 150-kW power inverter, in which they used the Chalmers model for constructing the LCI for the manufacturing phase. Part of the inverter unit is a Si IGBT power module. The module used in the study is Infineon's FS820R08A6P2B HybridPack Drive. The method of utilizing the Chalmers model is shown in Figure 18. The input parameter for the model is power. By using the ecoinvent database, and LCIA midpoint methodologies that comply with Product Environmental Footprint (PEF), the gate-to-gate results for manufacturing the power module are presented in Figure 19. As shown in the figure, the authors claim that more than 50% of the total global warming potential during module manufacturing is due to dies manufacturing and processing. The paper suggests that manufacturing of the power module compared to the whole inverter manufacturing counts for 31% of the total Ozone Depletion (OD), 36% of the Mineral Resource Depletion (MRD) and only 14% of GWP. Aluminium case manufacturing counts for 57% of the total global warming potential. Additionally, the paper suggests that, for the studied case, 75% of the GWP impact of the inverter unit is due to the use-phase, knowing that the study's functional unit is "Generate a three-phase AC electrical operating point for a 150-kW load (electric machine) from a 450 V DC power source, based on a lifespan of 15 years, i.e., equivalent to 10,000 h of operation" with efficiency consideration of 97%. Among 12 categories the use-phase impacts are dominant. Nevertheless, the use phase impacts are a consequence of the energy in that phase. Therefore, it is dependent on the grid mix chosen for the study, in this case, it is a global grid mix. The load conditions and conversion efficiency are also parameters that can change the results. Manufacturing counts for only 24% of the GWP. Nonetheless, manufacturing is dominant in other categories including human toxicity, non-cancerous toxicity, and freshwater ecotoxicity

with an impact exceeding 60% for the three. Lastly, transport and end-of-life phases altogether count for less than 4% of all impacts.

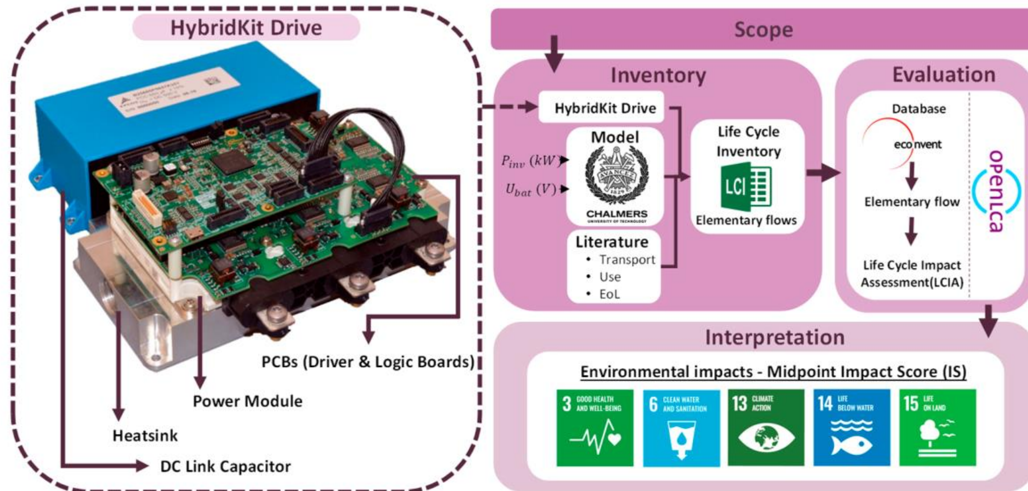


Figure 18: A method used for conducting an LCA for a Hybridpack Drive [77].

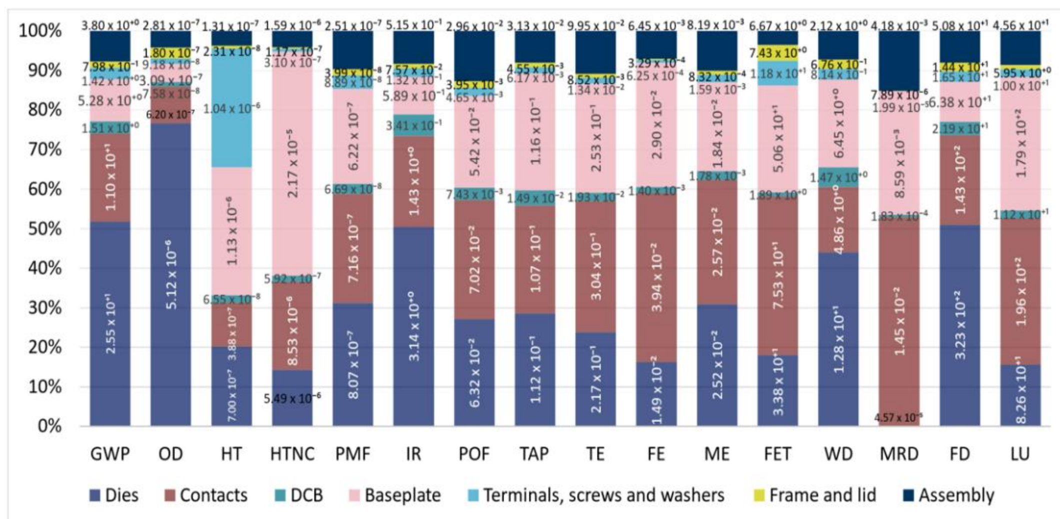


Figure 19: gate-to-gate results for manufacturing Infineon's HybridPack-Drive. [77].

On the other hand, Kockel et al. [79] argued that the utilization of Chalmers's model based on power alone (referred to as discrete scaling) does not reflect the actual environmental impact deviation. The authors have suggested a continuous scaling method, wherein the material compositions of converters' components are proportional to the power level of the converter. Figure 20 shows the comparison between using discrete scaling and continuous scaling for a Phase-Controlled Converter (PCC) within the scope of their

study. The comparison is in tons CO2 equivalent, as shown in Figure 20, the environmental impacts increase faster with the cases of discrete scaling with 20 kW and 50 kW which does not reflect a real increase in the sizes of the module, heatsink, housing and the dual active bridge (DAB). Consequently, for their study on microgrids, the scaling is based on the mass of the power module and the power of the converter. The authors utilized their scaling method as part of a comparative cradle-to-grave study between Alternating Current (AC) and Direct Current (DC) micrograds, to build a scalable LCA for AC/DC grid comparison. The LCIA methodology within the study is ReCiPe 2016 (H) midpoint and the functional unit is “the energy supply for the office building during observed lifetime”, the assumption of the lifetime was built on the transformer’s lifetime of 23-30 years with assumed 95% efficiency of a voltage source inverter composing of six IGBTs with FWDs. The potential climate change savings using a DC system instead of an AC system for a microgrid with 250 workstations were calculated. Figure 21 and Figure 22 show the system boundary for the study and the results for the mentioned scenario, respectively.

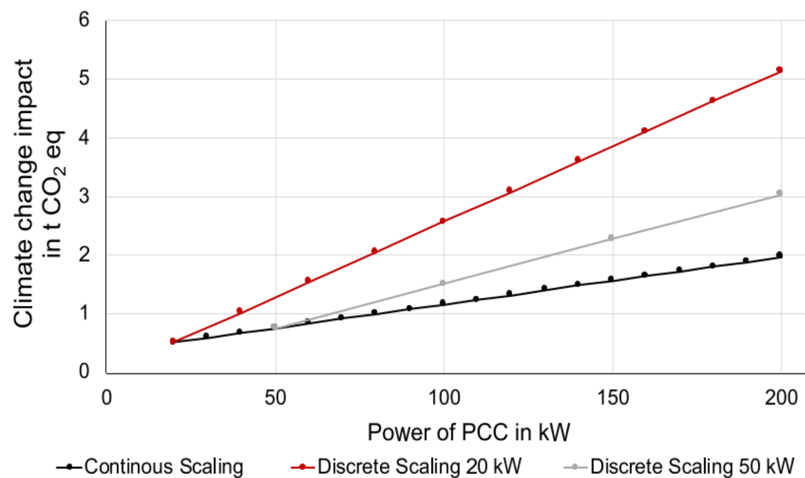


Figure 20: Comparison between using discrete scaling and continuous scaling for a phase-controlled converter [79].

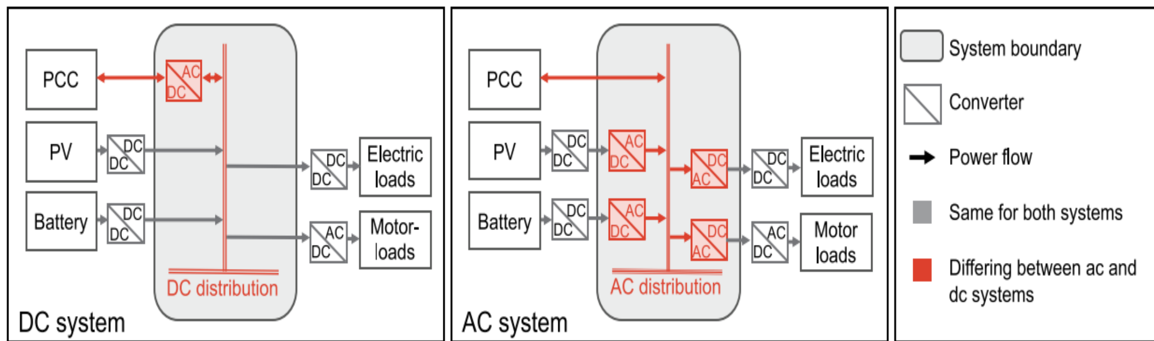


Figure 21: System boundary for a comparative study of AC and DC microgrids [79].

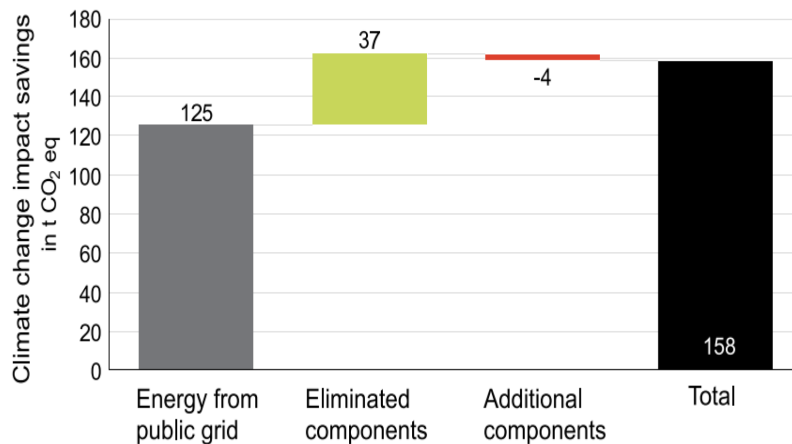


Figure 22: Climate change impact in tons CO2 eq. from replacing AC microgrid system with a DC one [79].

Another paper published in 2015, being the only paper solely focusing on the LCA of a Si IGBT power module, reported that the front-end processing accounts for 51% of the total emissions, 33% for the back end and 16% for the transportation. The authors further claimed that 79% of the front-end carbon emissions result from electricity, and around 40% of the back-end emissions are due to Polybutylene Terephthalate (PBT) production [80]. The software used in the study is GaBi with the integrated databases at that time including ecoinvent, the exact database and the LCIA methodology were not mentioned. The IGBT modelling is shown in Figure 23. Such a study is hard to assess because of the limited details presented.

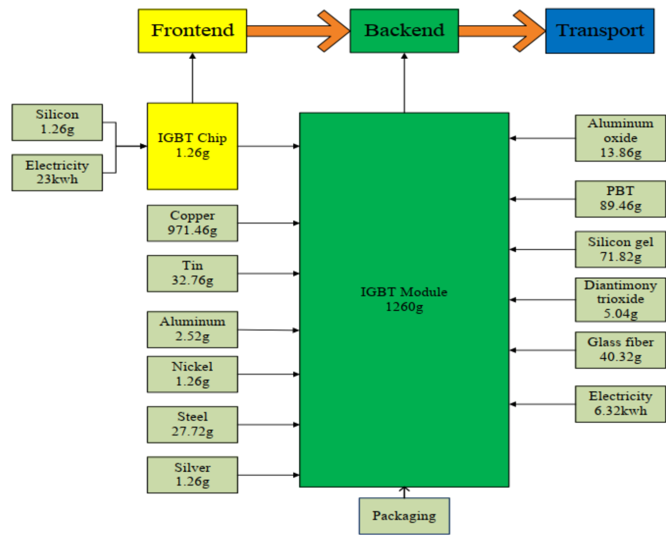


Figure 23: IGBT modelling principle in GaBi software [80].

4 Materials and Methods

4.1 Goal and Scope

The goal of the study is to build a cradle-to-gate LCA model of a Si IGBT power module to draw a baseline for further studies, especially for comparing Si IGBT with SiC MOSFET. Cradle-to-gate refers to processes from raw material extraction to delivery to the production house until the final product is ready. The model intends to show the dominant impacts of the module's manufacturing phase. The module has a power rating defined in the functional unit, namely the switching of one Si IGBT power module with a power rating of 1200V, 450A for converter applications. The model results are intended to provide designers with the module's dominant impacts through its manufacturing phase which can assist with environmentally friendly component, material, and technology selection. The final and most important objective is to expand the power electronics LCA field.

The study utilizes cradle-to-gate processes of the module with Germany as a primary manufacturing route, Europe as secondary when obtaining data for Germany is not feasible and global average as a complementary route whenever data on the first two is not available with the utilized tools. Europe representation as per GaBi's methodology considers the European average of the 28 countries (EU-28) in terms of energy consumption and resource utilization. Complete cradle-to-gate processes are included in the study within the utilized software (GaBi) databases scope.

4.2 Life Cycle Inventory

Before going into how the LCI was constructed, some definitions are essential to understand the construction methodology. Some of these definitions are adapted from ISO14040 and GaBi software, while other definitions are unique for this thesis (marked with *):

1. Flows: inputs and outputs of a process within a system.
2. Elementary flow: a flow that is in direct contact with the environment i.e., no further treatment is needed.
3. Tracked flow: a flow that requires/passes through extra treatment before obtaining the final impacts associated with it.
4. Process: list of flows elementary and/or tracked.
5. Unit process: smallest element in the LCI in which inputs and outputs are quantified.
6. Sub-process*: a process required to count for a tracked flow's impacts.

7. Main process*: a process that includes all elementary and tracked flows. (Similar to the aggregated process in GaBi)
8. Sub-plan*: Framework that can include multiple processes.
9. Main plan*: Plan that includes all sub-plans within a phase. The total impacts are calculated from the main plan. In GaBi (Both 8 and 9 are referred to as plan)

The data collected for the study is from different sources integrated to conduct the LCI. The main sources are GaBi databases, the Chalmers model, and tearing down a commercial module that is supported by a material content datasheet from the manufacturer. Table 3 shows the utilization of each source of data.

Table 3: Sources of collecting the LCI and their use within the study.

Source	Use
GaBi databases	Elementary flows impact implementation and sub-processes
Chalmers model	Electricity, water, material demands and wastes for most main processes after adapting to GaBi databases
Module teardown	Sizes, weights, and materials of the different parts of the module
Material content datasheet [82]	Confirmation of teardown information

4.2.1 Chalmers Model

Chalmers model was built to provide a scalable and general LCI for manufacturing an inverter unit ranging from 20-200 kW in nominal power which is suitable for personal electric vehicles. The LCI study is built on the base that material sizes and weights are directly proportional to the module power ratings. The minimum and maximum power ratings are 20 kW and 80 kW respectively, with a defined scale factor for each material. For example, aluminium oxide in the power module has a start value of 6.3 grams considering a 20-kW scenario with a scaling factor of 1.30E-01 g/kW. The base assumption of the Chalmers model is not utilized in this study. In this LCA study, the Chalmers model is used to realize elementary flows and tracked flows in their unit processes without prior scaling. In other words, the utilization of the model stops after acquiring flows within unit processes scaled to 1. The unit processes of the model that are applied in this study are summarized in Appendix A.

The idea is to acquire flows constructed by the Chalmers model that complies with the module of discussion. Then build processes based on flows within the scope of GaBi databases. The processes are scaled based on the teardown information. Figure 24 shows the inventory collection methods and utilization of GaBi software. LCIA methods used are described later in this chapter. Different manufacturing plans utilized to construct the LCA model are described in the results section.

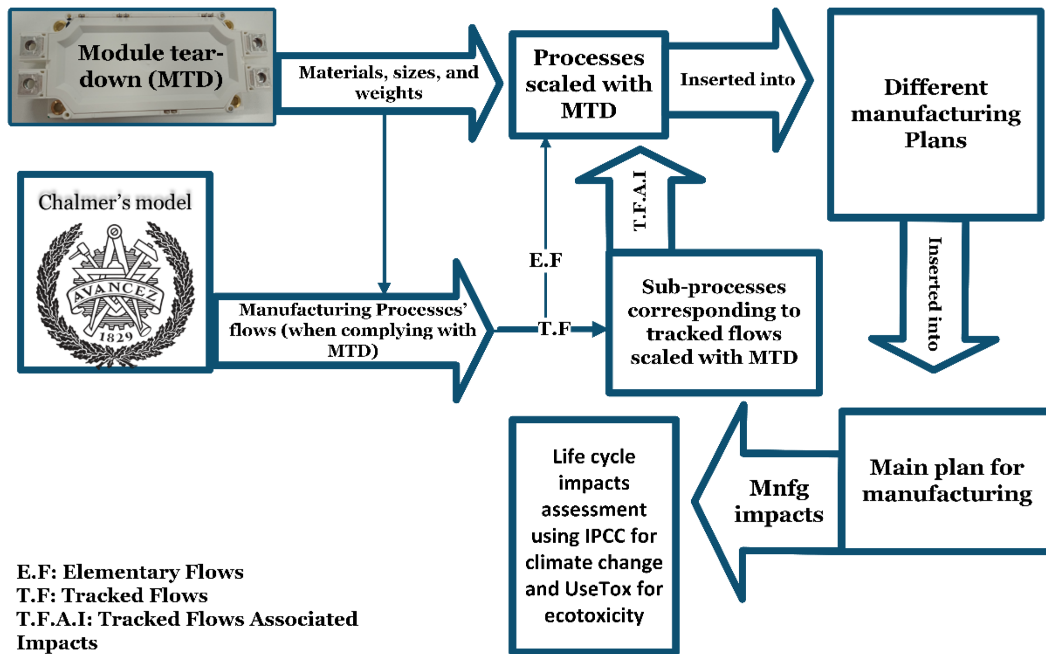


Figure 24: Inventory collecting strategy.

4.2.2 Module Teardown

This master thesis is done under the KDT JU PowerizeD project, a commercial power module with the ratings mentioned in the functional unit is used for this analysis. The module is manufactured by Infineon and is commercially available. Figure 25 shows the module after removing the lid. The power module has the ratings stated in the functional unit and is packaged in Econodual3. The module has six IGBT chips with one FWD chip for each IGBT as shown in the figure.

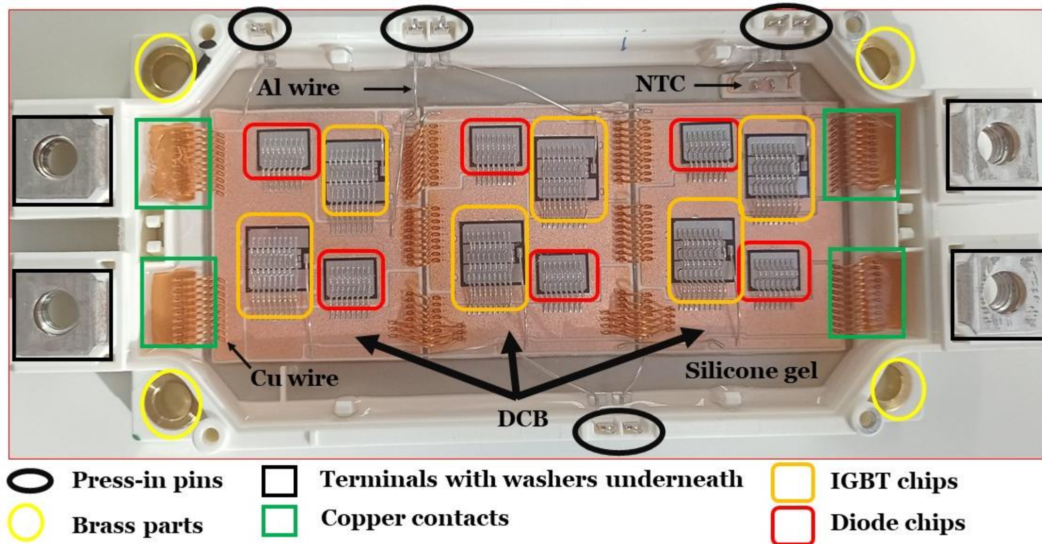


Figure 25: The module under discussion with an open lid.

The teardown is performed to acquire information on materials, sizes, and weights of the different parts of the module. Material information is used to confirm unit processes that comply with Chalmers's model and to build processes that do not comply with the model. Sizes and weights are used interchangeably with density relationships to scale the unit processes. The teardown starts by removing the lid of the module with a hand tool, followed by removing the silicone gel encapsulating the module. The silicone gel is removed by a non-chlorinated silicone rubber remover as per the datasheet instructions [81].

From Figure 22 it is obvious that the metals are inseparable from the plastic frame without damage. Consequently, the plastic frame is sacrificed to obtain the metal connectors, metal wires, and the substrate altogether with the baseplate and the chips. The plastic frame weight is acquired by subtracting the weights of every other part from the original module weight. Multiple cross-sections are then prepared for microscopy and spectroscopy analysis.

Measurement tools and methods of the study are digital scale, digital calliper, optical microscopy alongside image processing software, Scanning Electron Microscopy (SEM), and Energy Dispersive X-ray Spectroscopy (EDS). A digital scale with 0.01 g precision is utilized after every disassembly. The following weights were obtained: The module, the lid, the module after removing the silicone gel and the lid, the metal parts, the substrate with the baseplate, and the copper wires. Al wires masses cannot be directly calculated since the wires are hard to remove, in addition to having very small masses that cannot be measured accurately with the scale of the mentioned precision. Consequently, a proxy is utilized and is explained in the next chapter. A digital calliper is used in this study to provide the starting point for the image

processing software (J-software) by measuring the average surface areas of the IGBT and FWD chips. The average areas are inserted into an image processing software as a reference to detect the sizes of the other parts of the module. Moreover, the digital calliper is used to obtain the areas of the upper copper and J-software is used to obtain the pattern, copper is then used with its mass in the LCA model after conversion. The density information is obtained by Granta EduPack software, which is a database supported by Ansys. On the other hand, an optical microscope is used for sizes less than one millimetre i.e., to acquire the cross sections of Al wires.

SEM is utilized to acquire the thicknesses of the substrate layers, chip and system solder thicknesses, and metals' plating thicknesses. SEM-EDS is implemented to detect material information of solder composition, metal parts, their plating, and the plating of the baseplate. It is mentioned in the material document datasheet that there is a fluctuation margin of less than 25%, in terms of weight deviation, which would have caused the same margin of uncertainty in the LCI scaling if the datasheet is used alone. Instead, the teardown is used as the primary source of information and the document is utilized to confirm the teardown output. In other words, in principle, the same study could be performed without the teardown step but in that case, the study's scaling will be built on estimations which, if done correctly, will still hold a scaling uncertainty value of 25% or less.

4.2.3 Software Implementation

LCA for experts, formerly/commonly known as GaBi, is used in this study as the main tool for modelling and assessing the environmental impacts. The modelling is done through multiple processes that imitate the processes that the device passes through in its manufacturing phase. GaBi is one among multiple popular LCA software. The software is developed by Sphera [83], and it offers a broad range of LCA datasets embedded within the software databases integrated into different GaBi databases. The datasets include environmental impacts of unit processes, aggregated data, partly aggregated data, and full life cycle systems.

GaBi databases are from different sources, this includes the core database (GaBi professional database), GaBi extension databases and GaBi data-on-demand datasets. The datasets within the databases are either developed by Sphera or, from external sources that are then adapted to GaBi databases as in the case of ecoinvent datasets. Datasets developed by Sphera are from primary (industry) and secondary sources. Detailed information on handling databases and modelling principles can be found [84]. The software provides the main LCIA methods including ReCiPe 2016 v1.1 mid and endpoints, CML 2001 v. 2016, and TRACI 2.

Choosing the LCIA approach is dependent on different parameters including the goal and scope of the study and the intended audience. The same logic applies to choosing the methodology of calculation. For a better realization of the differences between methodologies an example of an 8-pin DIP-IC is presented here. The example represents the climate change results from cradle-to-gate processes for IC production, knowing that in the documentation of the dataset, it is mentioned that the data is collected from various manufacturers. As seen in Table 4, the ReCiPe 2016 V1.1 endpoint, which is one of many endpoint methods, has unique naming for climate change indicators. The same applies to ReCiPe 2016 V1.1 midpoint and Intergovernmental Panel on Climate Change (IPCC). From the table, it is worthy of noting that both the ReCipe midpoint and IPCC have different naming and values for carbon emissions. Moreover, the same applies to other indicators within different methodologies. The results can change greatly since methodologies can use different time frames [85]. In this study, since uncertainty needs to be reduced to the minimum value, the midpoint approach is used, as midpoint approaches in general hold fewer uncertainties. The approach is also recommended by the European Commission (EC) environmental footprint guideline [86]. Moreover, International Reference Life Cycle Data System (ILCD) did not recommend any method for calculating climate change using an endpoint [85].

Since IPCC is a wide consensus for the GWP category and is recommended by the ILCD [85], it will be used as the characterization method for GWP in this study. Moreover, IPCC uses three indicators for climate change: 20 years, 100 years, and 500 years. The 100-year time horizon will be used as per the Kyoto Protocol commitment [87]. The second category of analysis was detected after running the results with different LCIA methods and detecting the most overall significant impact category, then choosing a specific LCIA method that complies with ILCD recommendations. The impact category that was found to hold the most significance (quantitively) is ecotoxicity and the chosen LCIA is USEtox 2.12. Ecotoxicity refers to toxicity that affects the ecosystem and is divided into damage to terrestrial, freshwater, and marine ecosystems. The unit for calculating ecotoxicity is comparative toxic unit equivalent per kg emitted (CTUe/kg emitted) which equals to potentially affected fraction of species multiplied by time and volume per unit mass of the emitted chemical. USEtox is a multimedia fate model. It counts for the three mentioned divisions, and it was developed by the United Nations Environmental Program (UNEP)- Society of Environmental Toxicology and Chemistry (SETAC) [88]. ILCD recommend using the technique for freshwater ecotoxicity representations but does not recommend any methodology for calculating freshwater ecotoxicity or terrestrial ecotoxicity.

Table 4: climate change results from cradle-to-gate processes for IC production using different methodologies.

RECIPE 2016 V1.1 climate change Endpoint INDICATORS	**VALUE**
ReCiPe 2016 v1.1 Endpoint (H) - Climate change Freshw Ecosystems, default, excl biogenic carbon [species.yr]	1,80E-14
ReCiPe 2016 v1.1 Endpoint (H) - Climate change Freshw Ecosystems, incl biogenic carbon [species.yr]	1,80E-14
ReCiPe 2016 v1.1 Endpoint (H) - Climate change Human Health, default, excl biogenic carbon [DALY]	2,19E-07
ReCiPe 2016 v1.1 Endpoint (H) - Climate change Human Health, incl biogenic carbon [DALY]	2,19E-07
ReCiPe 2016 v1.1 Endpoint (H) - Climate change Terrest Ecosystems, default, excl biogenic carbon [species.yr]	6,61E-10
ReCiPe 2016 v1.1 Endpoint (H) - Climate change Terrest Ecosystems, incl biogenic carbon [species.yr]	6,60E-10
RECIPE 2016 V1.1 Midpoint climate change INDICATORS	**VALUE**
ReCiPe 2016 v1.1 Midpoint (H) - Climate change, default, excl biogenic carbon [kgCO2eq]	0,23
ReCiPe 2016 v1.1 Midpoint (H) - Climate change, incl biogenic carbon [kgCO2eq]	0,23
IPCC AR6 GWP Midpoint INDICATORS	**VALUE**
IPCC AR6 GWP 100, incl biogenic CO2 [kgCO2eq]	0,16
IPCC AR6 GWP 20, incl biogenic CO2 [kgCO2eq]	0,17
IPCC AR6 GWP 500, incl biogenic CO2 [kgCO2eq]	0,15

As a continuation to Figure 24, Figure 26 shows the methodology of utilizing the software for constructing the related processes with a closer look at how a unit process from the Chalmers model is treated. All unit processes from the Chalmers model do not exist readily in GaBi databases.

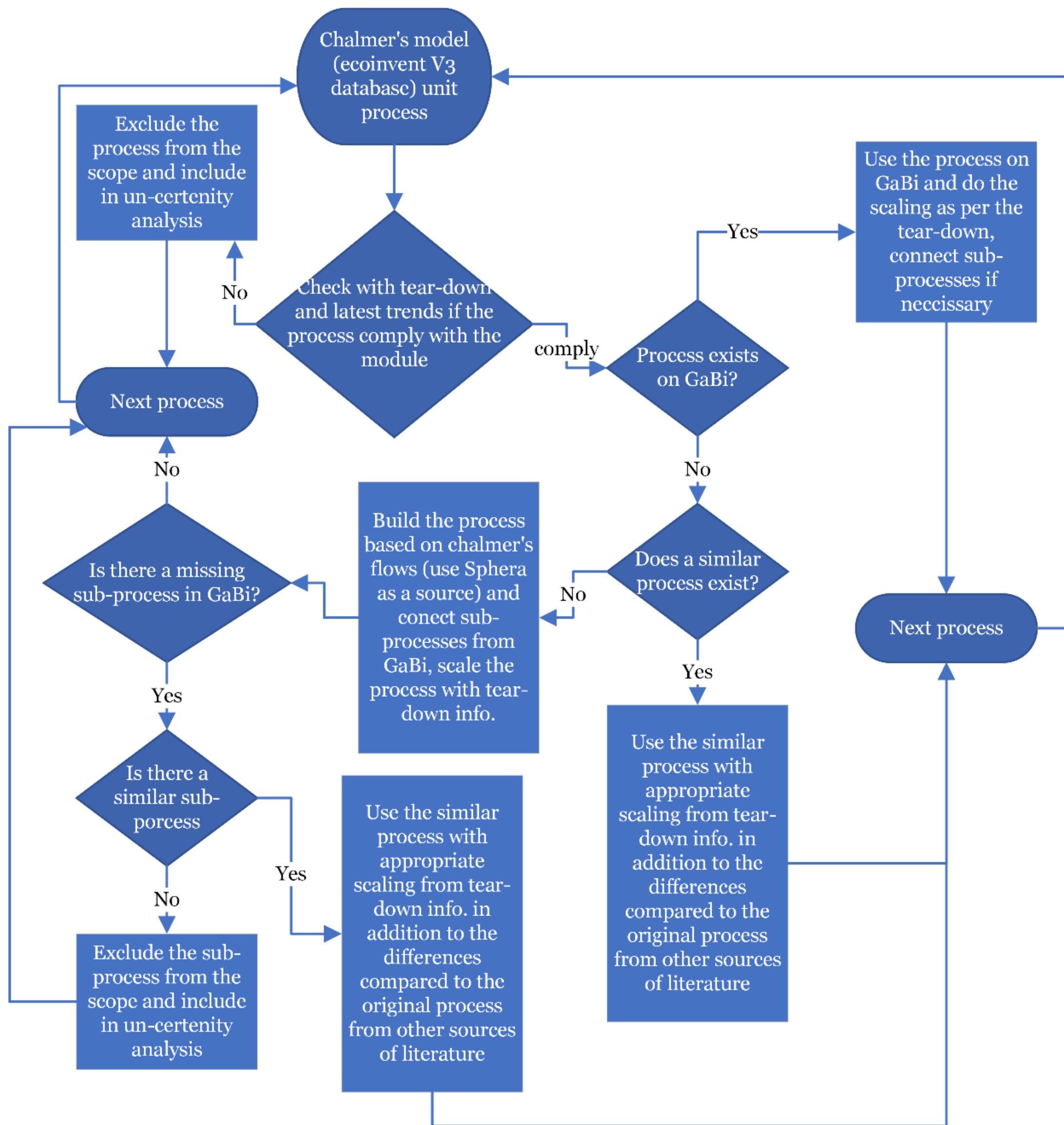


Figure 26: The methodology of utilizing the software for constructing the related processes.

A proxy was implemented using the software to scale the diodes. A power diode was taken as a reference from GaBi databases, the reference diode has a volume of 35.6 mm^3. The die size is 80% of the package size. The die volume was calculated to be 28.4 mm^3. The total GWP caused by manufacturing one diode is 0.027 kgCO2eq, if one considers 80% of the total GWP impacts is from the front end and 20% from the back end; front-end carbon dioxide emissions are:

$$0.027 * 0.8 = 0.022 \ kg \ CO2 \ eq. \quad (1)$$

The reference power diode cannot be used directly in the model since the packaging technology is much different from the module under discussion. The volume of one diode of the module from the teardown information is considered. From Infineon's innovative structure presented in Chapter 2, which is the expected structure for the diode under discussion, a rough estimate of the mask count was considered with the reference diode. Scaling CMOS 130nm node logic process to 0.50 (counting for 0.5 cm^2 of active chip area) results in GWP of 0.61 kgCO2eq, using the equation:

$$X\ (scale\ factor) = X_{cmos130nm}\ (scale\ of\ the\ cmos\ process)\frac{expected\ GWP\ of\ one\ diode}{GWP\ resulting\ from\ X_{cmos130nm}} \quad (2)$$

The scale factor for the diodes was estimated. A scaling method similar to the method used for scaling the diode could be utilized for the IGBT chips. Nonetheless, the manufacturing assumptions including mask count are not disclosed. Based on that, the IGBT chips are scaled directly with their active surface area.

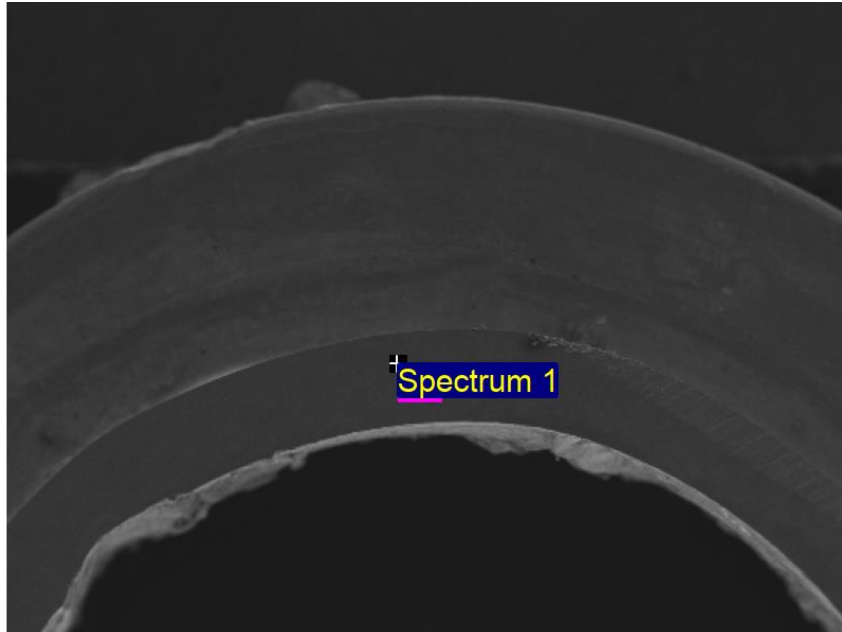
5 Results and Discussion

In this chapter, the results of the teardown process, constructed model and the results of the constructed model are presented and discussed.

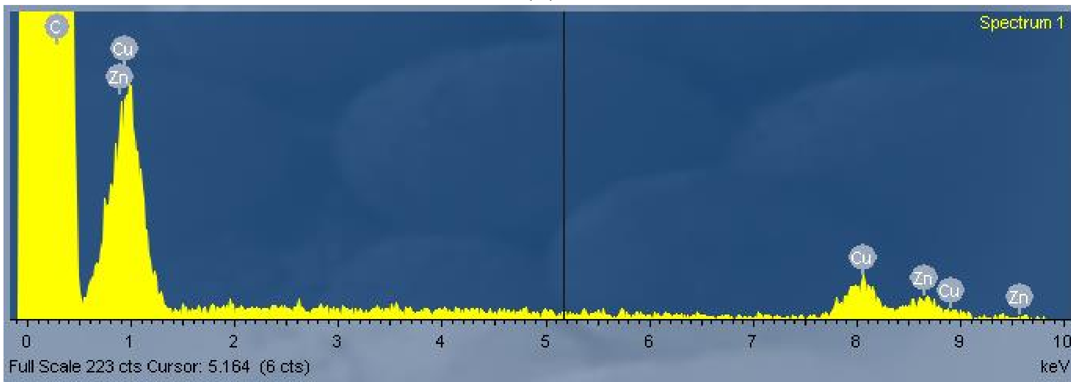
5.1 Teardown Results

To have a more practical and easier understanding of the utilization of the teardown for the LCA model, the module is divided into three clusters. The first cluster is composed of metal connectors, the second is based on a cross-section used for the analysis, and the third cluster is composed of the remaining parts. The clusters are presented in Tables 5, 6, and 7 respectively. As mentioned in Chapter 4, the teardown is the primary source for scaling, so unless stated otherwise, material information, weights, and sizes, used in the model are extracted from the analysis and are then confirmed with the material content datasheet. The reason for that is to reduce the uncertainty of the study. The other way around in terms of having the material content datasheet as a primary source and then having verification analysis would result in similar output. Unless stated otherwise, the confirmation from the document is based on material information and relative weights only.

The composition and plating of metal connectors in addition to their plating sizes were detected with SEM and SEM-EDS. Brass is a metal made of copper and zinc with different ratios. Figure 27 shows the SEM micrograph and the corresponding EDX analysis for one point of the brass part. The ratio of copper to zinc was found to be 65:35. Secondly, the SEM-EDS analysis of press-in pins has shown that the pins are made of copper plated with nickel and a final plating with tin on top of that. Figure 28 shows the spectrum of materials and the corresponding thicknesses of plating. The thicknesses are rounded to 1 μm tin and 2 μm nickel for the model. Thirdly, the analysis of the terminals has shown the same results as press-in pins in terms of material composition. The exact thicknesses could not be identified since an Intermetallic Compound (IMC) was formed between tin and nickel. In contrast with press-in IMC, the IMC in the case of terminals has caused uncertainty to the exact thicknesses. Nevertheless, the spectrum was enough to estimate the thicknesses of nickel that are used to determine the weight of the plating used in the model which is presented in Table 5. Finally, after running the analysis on one washer, the washer was found to be made of iron coated with zinc. A trace of nickel was also identified. Nevertheless, the peak was too small to be considered. Table 5 summarizes the information used in the LCA model from the results of the digital calliper with SEM and SEM-EDS. The weights correspond to all part counts.



(a)



(b)

Figure 27: (a) SEM micrograph of a brass part and (b) the corresponding EDX analysis for one point of the brass part.

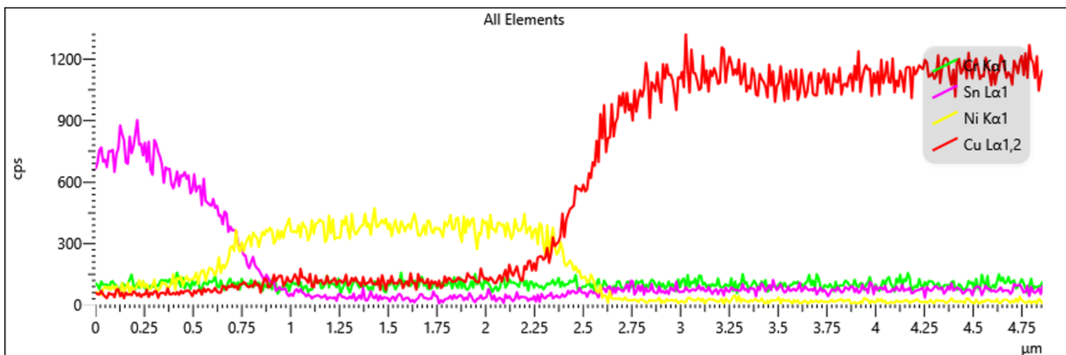


Figure 28: SEM-EDX analysis of press-in pins

Table 5: Selected weights of the first cluster.

Part	Material	Weight (g)	Total Nickel-plating weight (g)
Brass parts	65Cu:35Zn	4.9	0.3
Press-in pins	Cu plated with Ni and Sn	1.1	
Terminals	Cu plated with Ni and Sn	21.6	
Washers	Fe plated with Zn	9.6	

The second cluster is based on a cross section through an IGBT die soldered on a DCB substrate as shown in Figure 29. There was no need to analyse the similar cross-section prepared with the diode chip, the microscope analysis was enough to detect the thickness of the diode.

The insulator in the DCB was confirmed to be Al_2O_3 by SEM-EDS. The area of the insulator shown in Table 6 is used directly in the model. For alumina production, the mass of the insulator presented in the same table is used. The areas detected by the digital calliper and J-software as explained in Chapter 4 are utilized with the thicknesses here to get the volume and then the mass of copper to be used in the LCA model. The mass of the total copper and its removed pattern is presented in Table 6. It was assumed that the edges of the copper layer were not removed in the patterning step, but rather the copper parts are already manufactured with a size less than that of the insulator and only the pattern is etched.

By EDX analysis, the chip and system solders were found to compose of tin, silver, and copper (SAC). Different SAC solders have similar elemental compositions. The exact SAC type could not be identified since some errors could have been induced by grinding. The solder composition is not mentioned in the material content datasheet. Both chip and system solder are closest to SAC405. However, the only available SAC type that was found in GaBi databases is SAC305, so it is used instead, having awareness that the manufacturing of different SAC types is expected to have very close environmental impacts. The total mass of the solder used in the model is presented in Table 6.

The final element of the cluster is the baseplate. The baseplate is made of copper that is plated with tin and nickel as shown in Figure 31. The mass of the plated nickel, which was detected by volume mass conversion with the digit calliper for area, and optical microscope for thickness is considered alongside all other nickel plating which is presented in Table 5. The baseplate copper mass is presented in Table 6.

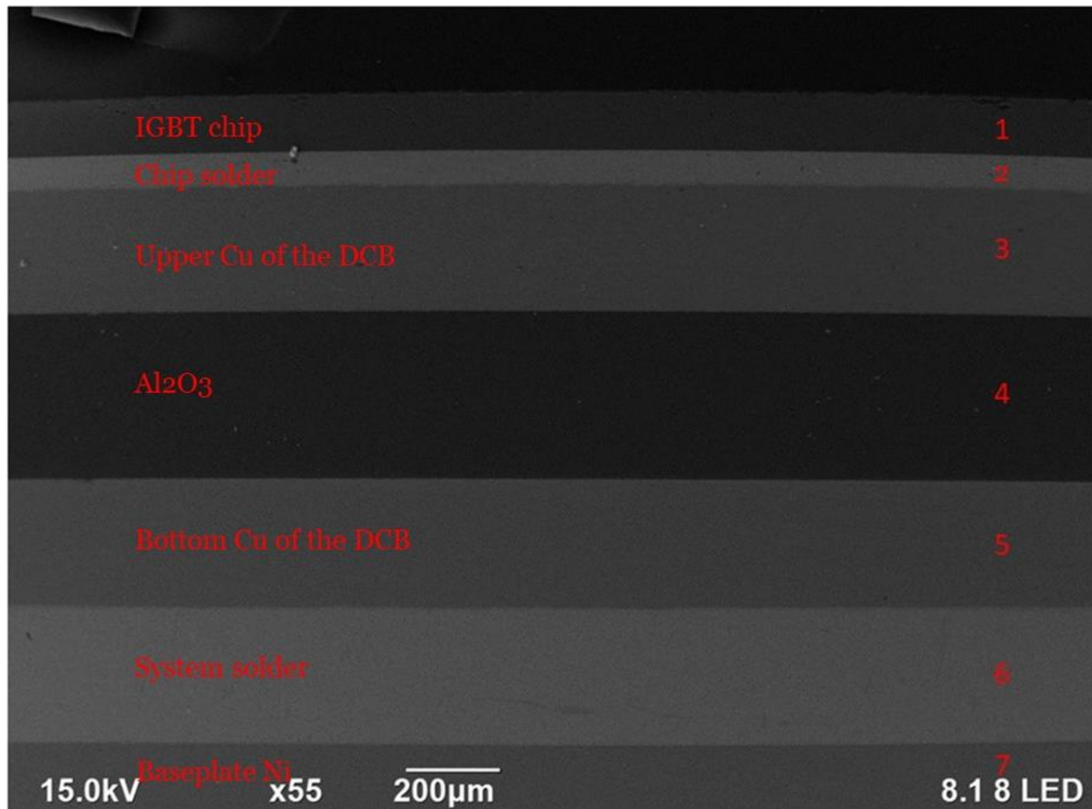
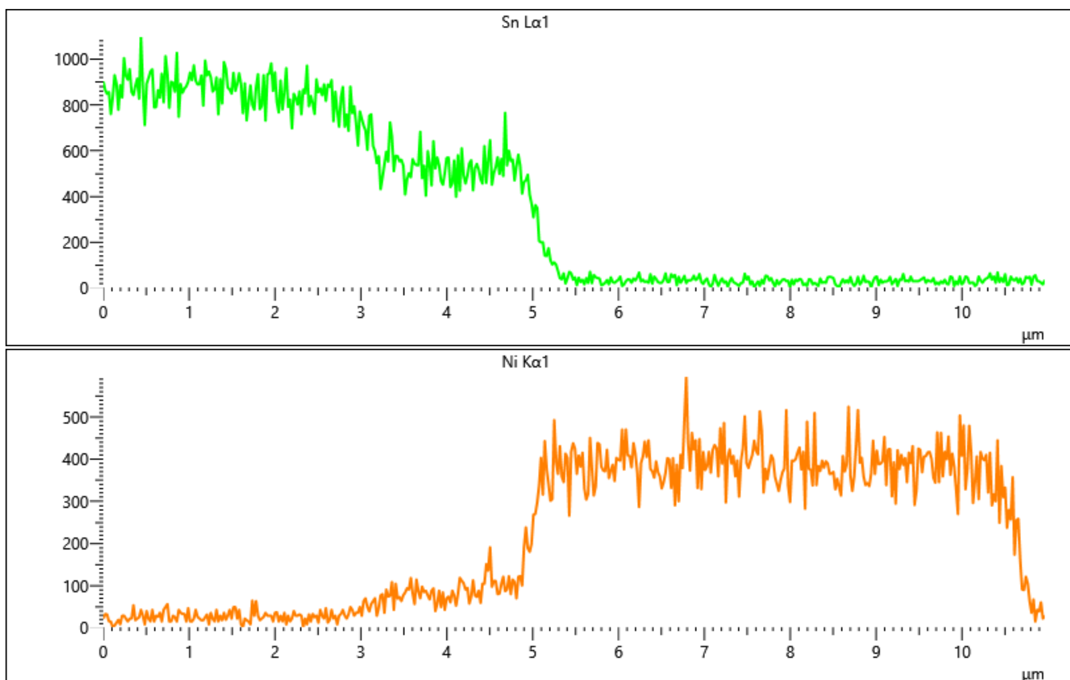


Figure 29: Second cluster's cross-section with an IGBT chip soldered on a DCB substrate.



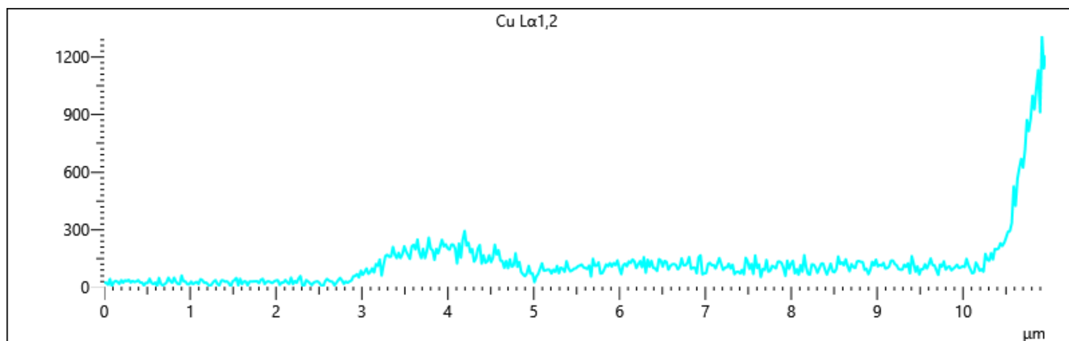


Figure 30: EDX analysis showing the baseplate material composition.

Table 6: Selected weights of the components in the second cluster.

Part	Surface area (mm^2)	Weight (g)
Al2O3 insulator	3780.0	5.7
Copper in DCB substrate	--	16.3
Removed copper	--	0.5
Solder paste	--	8.2
Baseplate	--	204.0

The third and final cluster contains information about the wires, housing, potting, and encapsulation. The module contains copper and aluminium wire bonds. The copper wires were divided into two types based on their function. The first type is used to connect the three DCB substrates, the wires in this case are of two different lengths. The second type is used to connect copper contacts to one DCB substrate. Copper wires were weighted directly and are used in the model with their masses. The total mass used in the model for all copper wires is presented in Table 7. Aluminium wires are also represented by their mass in the model, see Table 7. Nevertheless, the digital scale's precision was not enough to directly weigh the wires as mentioned in the previous chapter. Moreover, Al wire welding makes it very hard to remove the wires. Consequently, the different cross sections of the wires were identified by the optical microscope, the lengths were detected by the image processing software and finally, the density information was used to convert the volumes into masses. The weight of the silicone gel was measured by weighing the module before and after silicone gel removal. Since the weight of the gel is directly stated in the material content datasheet, it was compared to the teardown information and a difference of 0.7 g was found. Finally, the plastic part was treated as a frame and a lid. Both the frame and lid weights are shown in Table 7. The lid was weighed directly, whereas the frame's weight was calculated by subtraction from the total weight as mentioned in Chapter 4. The materials used (PBT, resins, and glass fibre) and their ratio to form the plastic part, are taken directly from the material content datasheet.

Table 7: Selected weights of the third cluster.

Part	Weight (g)
Copper wires	2.0
Aluminium wires	0.5
Silicone potting gel	32.7
Plastic frame with resin	37.0
Lid	13.6

5.2 Model Construction and Scaling

To construct a representative model, prior knowledge of silicon IGBT power modules manufacturing processes presented in the literature, or a study of the Chalmers model [74], [75], [76] is necessary. The model constructed here is divided into six different plans, each plan presents a set of processes that lead to an output product/s. The plans are built using GaBi software, each plan represents a set of fabrication processes that imitate those required for fabricating the module. The plans are the software framework that the environmental impacts are calculated based on. All the manufacturing and processing mentioned in the table refer to cradle-to-gate, meaning that sub-processes fabrications and processing are counted for (unless stated otherwise) but not mentioned in this table. The sub-processes are mentioned in the detailed plan's graph/table shown later in this section. The plans, their main representation and output products are summarized in Table 8:

Table 8: Plans that are used to construct the LCA model and their output product.

Plan: number and name	Output product	Representation
1. Direct copper bond	Un-patterned DCB substrate	The plan represents manufacturing of the DCB substrate
2. Chlorine patterning	Patterned DCB substrate	Represents the patterning of the DCB substrate
3. Baseplate, press pins, and terminals	Nickel-plated copper baseplate Plated copper of DCB	Represents the cleaning of the metals, nickel electroplating and fabrication of the baseplate, press-in

	Cleaned metal connectors and nickel-plated press-in and terminals	pins, and terminals with copper contacts
4. IGBTs and FWDs	Module without frame	Represents IGBT and FWD fabrication, chip, and system soldering
5. Frame, washers, and brass parts	Module with frame and metal connectors	Represents plastic frame fabrication and attachment, Negative Temperature Coefficient (NTC), washers, and brass parts fabrication
6. Wires and silicone	Power module (final product)	Represents wire bonding, potting and lid attachment processes

Appendix A summarizes the adaptation of Chalmers model unit processes, the geographical representation, and excluded processes. Unless stated otherwise, the sub-processes used from GaBi databases are all cradle-to-gate processes, meaning that the scope of the main processes covers all necessary steps from raw material extraction to the final product from factories.

The geographical representation, in general, is completed considering that manufacturing and processing take place in Germany (DE), and in Europe in general (EU/RER) where the process is not available with German representation. Besides, if the process is not available with German or European representation, it is presented globally (GLO). Electricity for production and water consumed during production are always represented by DE. Notwithstanding, the exact locations of manufacturing, processing and assembly for the other parts could not be identified. That does not affect the goals of the study greatly. Since the geographical representation can vary greatly from one manufacturer to another, the model is built such that modifying the geographical representation can be performed easily with the software.

The direct copper bond plan (plan 1) represents the fabrication of the DCB substrate as a process, in addition to the embodiment of pre-requisite processes. The plan includes two main processes, whereby one is a prerequisite for the other. The two main processes altogether required 11 subprocesses, excluding electricity and water supplies. Figure 31 shows the structure of the plan with the included processes. A copper sheet is used here as a representation of the top and bottom copper layer of the DCB substrate. The sheet is the closest representation found within the available datasets (processes) offered by the software's local database used for the study. The

process (RER: Alumina production) has eight tracked flows to offer flexibility to the user to choose the representation that corresponds to the study scope. The tracked flows were connected to pre-requisite processes as shown in the figure, with only significant flows connected. Processes marked in green have GaBi databases as a source including water and electricity marked with different colours, whereas processes marked in grey are adapted processes from the Chalmers model, this applies to all the presented plans. The adaptation and scaling of the main processes are done as per Appendix A and the teardown information presented earlier.

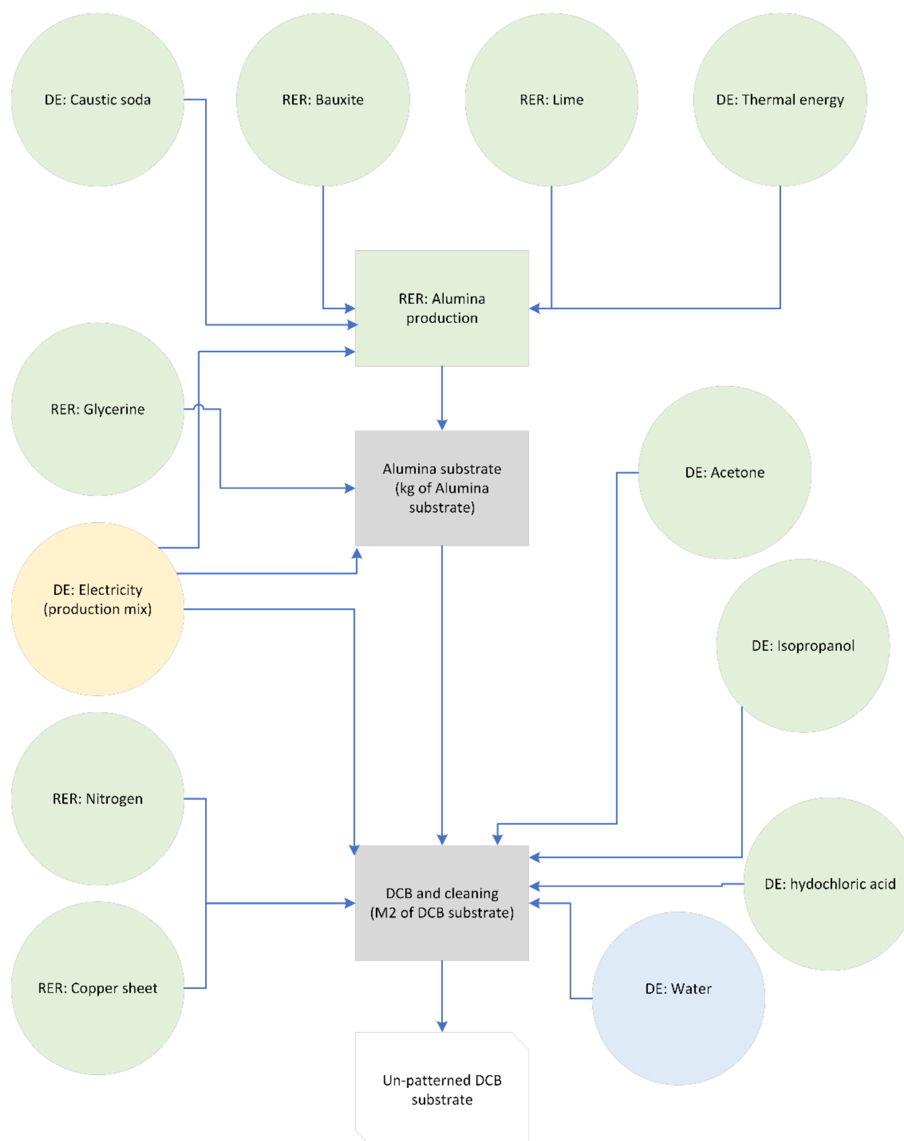


Figure 31: Processes used to construct the first plan.

After obtaining the DCB substrate, the top copper of the substrate is bound to nickel plating as per the Chalmers model and the confirmation from the teardown analysis. The patterning technique chosen by Chalmers's model is chloride re-generative etching. The plan's unit processes, sub-processes and output product are presented in Table 9. Two main processes correspond to the Chalmers model, the total number of subprocesses for the two main plans is 6 excluding water and electricity. Another product is not considered here which is cupric chloride that can be used for a closed loop re-generative etching.

Table 9: Processes used to construct the second plan.

Unit process	Sub-processes	Output product
Copper etching (kg of copper removed)	DE: HCL DE: Chlorine	Cupric chloride
Photolithography	DE: Acetone DE: Isopropanol DE: Ethylene glycol RER: Polymethylmethac-rylate DE: Water DE: Electricity (produc-tion mix)	Patterned DCB substrate

The third plan is a parallel one alongside the first and second plans, the plan contains the processes needed to fabricate the baseplate, terminals, and press-in pins, besides the cleaning of the baseplate, metal connectors, and top copper of the DCB, in addition to nickel electroplating. Nickel electroplating does not just correspond to the plating of the connectors, but rather all nickel plating within the module which also contains the baseplate plating and the top copper plating. The information on plating is discussed in the teardown section. Table 10 shows unit processes in the third plan, sub-processes, and output products. There are two main processes with 4 subprocesses excluding water and electricity. The copper sheet is again used to present the copper of the baseplate, press-in, and terminals for the same reason discussed previously. Tin plating has been excluded from the scope of the study as a process for plating tin or even pure tin as a substance was not available within the local database of the software.

Table 10: Processes used to construct the third plan.

Unit process	Sub-processes	Output product
Metal cleaning (sqm of cleaned metals)	RER: Copper sheet DE: Sulphuric acid DE: Sodium hydroxide DE: Water	Cleaned metals

	DE: Electricity (production mix)	
Nickel electroplating (kg of plated nickel)	DE: Nickel class 1 DE: Water DE: Electricity (production mix)	-Nickel-plated press-in pins and terminals -Nickel-plated DCB's top Cu -Nickel-plated baseplate

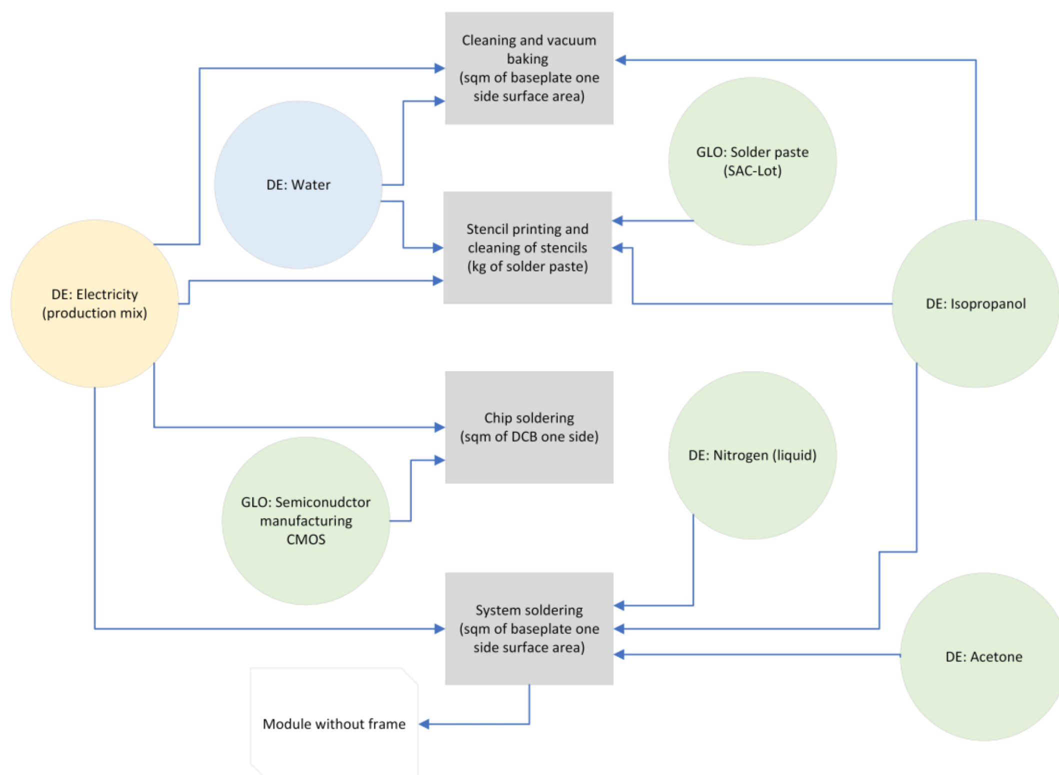


Figure 32: Processes used to construct the fourth plan.

The fourth plan is built with four main processes that comply with Chalmers's model and the teardown information. The plan counts for the fabrication of the semiconductor chips, chip and system soldering processes including a stencil printing process, and cleaning and vacuum baking before soldering. The plan is illustrated in Figure 32. GaBi offers a wide range of semiconductor chips that are integrated into packages that do not comply with the module under discussion. A model for CMOS 130 nm node logic fabrication is used and scaled to model both the IGBT and diode chips. The process is the closest representation to the module of discussion. The process chosen covers all necessary steps from raw material extraction, silicon ingot growth, and front-end fabrication of the wafer using 130 nm logic equivalent processes until wafer dicing. Wafer dicing is not included in the process and was neglected since the impact is insignificant [76]. In Chapter 2, general

common processes for silicon semiconductors were introduced, CMOS and Double-Diffused MOS (DMOS) are considered to share similar processes as per the literature presented in the chapter. Since the process is designed for CMOS logic, differences at the wafer processing level are expected. Nonetheless, apart from the technology node, the chosen model is the closest representation to model silicon growth for both the IGBT and diode chips, knowing that the differences between the processes in terms of energy demand and chemical use at the wafer processing level are sources of uncertainty. 130 nm node is considered an average value in terms of GWP compared to other nodes, see Figure 17. From the volumes and mask count differences (1.3 estimated scale factor), using the results of equation (1) the expected GWP is upscaled to 0.026 kgCO2eq, into equation (2):

$$X\ (scale\ factor) = 0.50 * \frac{0.026}{0.610} = 0.021\ CMOS\ scale/diode \qquad (3)$$

For all the diode chips:

$$X_{total} = 0.021 * 6 = 0.12\ scale\ factor\ for\ the\ cmos\ process \qquad (4)$$

Nonetheless, there is a big extent of uncertainty for the used technique since the exact structures of the power diode/power transistors that are recorded in the model's documentation are not reported. As mentioned in Chapter 4, the IGBT chips are modelled directly with the active chip area, approximately 5.2 cm^2 as the sum of the six IGBT chips (active chip area, the total chip area is larger). The final scale for both the IGBT chips and diodes is 5.3 which corresponds to 5.3 cm^2 of CMOS 130 nm logic active chip area.

Plan number five is presented in Figure 33. The plan counts for the impacts of manufacturing the plastic frame, brass parts, washers, and NTC thermistor and integrating the frame with the module, in addition to post-plasma cleaning after the frame attachment. The plastic type (PBT) was identified from the module's material content and was not analysed further. The weight of the frame was used directly to scale DE: PBT process shown in the figure. The teardown showed that the metal connectors are fixed inside the plastic, based on that, the metal connectors integration was not counted for further, as the integration was assumed to be done alongside injection moulding. Injection moulding is the only valid representation found in GaBi databases for creating the plastic shape, and the process is used only for its electricity representation. The ratios of glass fibre to PBT are modelled in the same manner as the Chalmers model, which corresponds to the material content datasheet. Antimony trioxide was modelled as a flow, but no corresponding process was found. The impacts of producing antimony trioxide are excluded from the study.

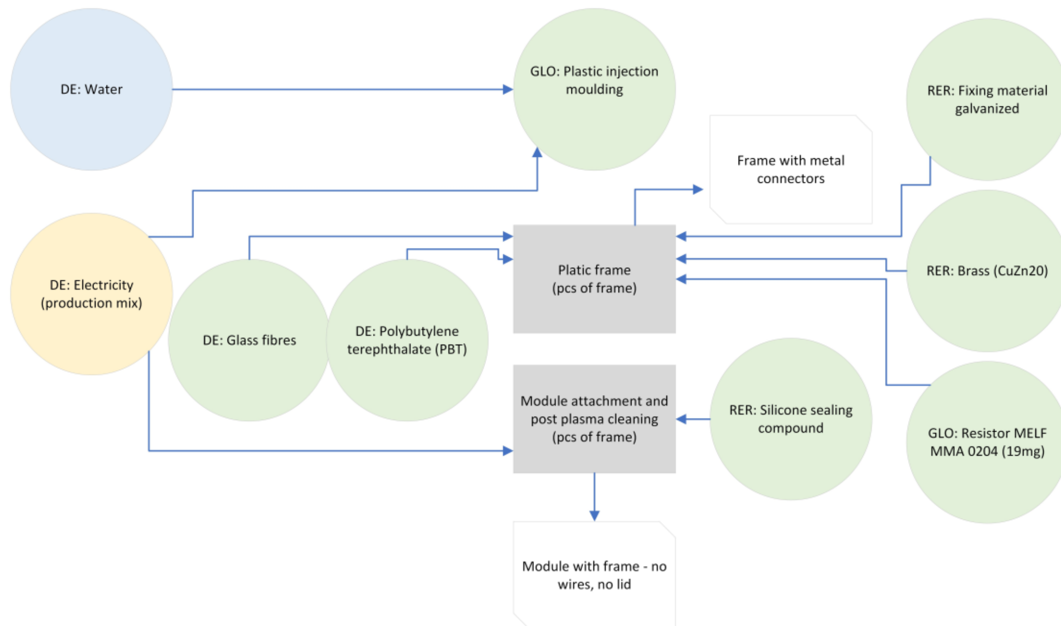


Figure 33: Processes used to construct the fifth plan.

The closest ratio found in GaBi databases to mimic the brass parts is 80Cu:20Zn and is used to model the parts' manufacturing processes, which is expected to be close to the processes used to manufacture 65Cu:35Zn brass. Furthermore, the washers which are made of iron galvanized with zinc were modelled using an already existing process in GaBi databases for manufacturing iron galvanized with zinc to shape M6 screws. The shape of the output product is irrelevant since the process is scaled with the metal mass. The NTC thermistor was modelled using a Metal Electrode Leadless Face (MELF) resistor with the same dimensions as the NTC used in the module. The MELF resistor is manufactured using ceramic as the case of the NTC under discussion. Finally, silicone is used to represent the sealing compound which was not identified through the teardown since it is not expected to affect the LCA model's results for its small quantity.

The final plan counts for wire bonding and welding inside the same process, potting of the silicone gel, UV curing and finally the sealing compound to attach the lid. The plan's unit processes, sub-processes, and output products are shown in Table 11. Al wires did not exist in the local databases used. Consequently, aluminium extrusion is used to model the manufacturing of the Al wires used in the module, whereas copper wires are modelled directly with EU-25 (when the member states were 25 "from 2004-2007"). Both wires are represented with the weights shown earlier. Aluminium extrusion is modelled with North America (RNA) because it is the only available dataset, the overall representation of this specific process is not the optimal way to represent the Al wires. Nonetheless, the process impacts compared to the

whole model are negligible, meaning that the results are not affected greatly by this process.

Table 11: Processes used to construct the sixth plan.

Unit process	Sub-processes	Output product
Wire bonding (Pcs of the module with frame “un-wired”)	EU-25: Copper wire RNA: Aluminium extrusion DE: Sodium hydroxide DE: Electricity (production mix)	Power module wired without silicone and lid
Potting and UV curing (kg of silicone gel)	DE: Silicone fluids (low viscous) DE: Electricity (production mix)	Power module without a lid
Lid attachment (Pcs of the module without lid)	RER: Silicone sealing compound	The power module finished and ready for shipping

Chalmers model could not be used for modelling wire bonding/welding, since it was assumed that “an area equal to total chip area is bonded in each module” [76] which doesn’t comply with the module teardown information, in addition to using only copper wires. The module includes both Al and Cu wire bonds. The ultrasonic bonding process for aluminium can also be adopted for copper since wire bonding electricity consumption is insignificant compared to the total electricity consumption of the power module fabrication. It was found sufficient to estimate the welding electricity consumption from commercially available wire bonding machines. The average was taken, considering different scenarios. The scenarios include two different commercially available wire bonding machines, one is used for aluminium wire bonding with a diameter of 100-500 µm [89], which corresponds to the cross-sections of the module under discussion, and the second is for copper wires with 300-500 µm and aluminium ribbons [90]. Considering different bonding times of 1 bond/sec and 3 bonds/sec including the feeding and cutting time [91]. The power rating taken into consideration is an average between 240 watts and 2400 watts with intervals. The final estimation for the average power consumption of both bonding Al and Cu = 0.14 kWh per module.

Low viscous silicone fluid is used to model the potting gel. The potting material was identified to be silicone gel by the material content datasheet and was confirmed by the silicone removal step. Low viscous silicone is chosen here to comply with a commercial silicone gel manufactured in Germany for Si IGBT power modules [92], knowing that Chalmers model used

"silicone products" as a flow which is a more generic representation than the one specified here.

5.3 Model Limitations and Uncertainty

Uncertainties in general can be induced by many factors including data uncertainties, model uncertainty, and completeness uncertainty among other sources including errors that could differ for different studies [93]. Mainly, there are ways to reduce uncertainty sources within an LCA study, by doing more research or obtaining primary data, whereas there are ways to incorporate uncertainties within a study, usually done with statistical approaches such as Monte Carlo analysis [94]. The ways of reducing uncertainty were followed where possible. That can be reflected by choosing to tear down the module instead of using the material content datasheet and choosing one database to ensure consistency. Statistical uncertainty analysis was left for future work due to data and time limitations.

Chalmers's model included Geometric Standard Deviation (GSD) per unit process as a qualitative method to calculate uncertainty in alignment with ecoinvent database methodologies and principles. The analysis is taken from ecoinvent documentation and other original values calculated within the model framework. Nevertheless, apart from the methodology used, since the primary source of the Chalmers model is the ecoinvent database and literature, the GSD cannot correspond to the actual statistical deviations that can only be known when the real possible potential values of the flows are known, like GaBi's databases and modelling principles method example [60]. Consequently, the GSD analysis of the Chalmers model was not considered. Moreover, beyond statistical uncertainty analysis that needs at least a strong assumption for the possible deviations, errors from Chalmers model authors and the original authors of the used literature should also be considered. Running Monte Carlo analysis is doable within the current scope of the study. Nevertheless, with the current data, Monte Carlo analysis cannot be representative because the deviation of flows is unknown. Consequently, with the available data in the field, it was found that the best way to show the overall uncertainty within a study is to transparently show how the study was conducted and transparently show the sources used for the study.

Uncertainty sources within the study are summarized in Table 12. The severity of the sources is built on their estimations from analysing the model and is unique for this study. The number ranges from 1-5. 5 being the most severe, having a severity of 5 means excluding the source of uncertainty from the study. The severity of 1 does not mean 0 uncertainty but rather the least uncertainty compared to other sources. The reference of the highest severity within the study is the front-end fabrication with a severity of 4. The severity

of 4 was given on the basis that the graphical representation is the global average (GLO) rather than Germany or Europe as the case for other processes, besides, the manufacturing assumptions used in the GaBi model are not disclosed. On the other hand, a severity of 5 was not given for the model because of CMOS and DMOS fabrication similarities presented in the literature. The reference of the least severity was given to GaBi databases for it being verified by ILCD. The complete Sources of uncertainty are not represented but rather the utilized external sources and the most severe process (GLO: CMOS). No data was found for the model's further graphical representation as described earlier. The graphical representation can affect the model greatly, the severity of 4 instead of 5 was given on the basis that GaBi databases build processes based on real manufacturing routes that by chance might be the routes of manufacturing the module under discussion. The model can be modified in terms of graphical representation to represent many other manufacturing routes including a generic route that counts for the average global emissions as in the case of front-end fabrication.

Table 12: Uncertainty source and the corresponding study unique severity score

Uncertainty source	Severity
GLO: C-MOS (Front end fabrication)	4
Chalmers model	2
GaBi databases	1
Excluded sub-processes, appendix A	2
Replaced sub-processes, appendix A	3
User-induced (using the software)	1
Geographical representations	4
Teardown information (Scaling)	1

5.4 LCIA

The cradle-to-gate results are presented in compliance with the six explained plans. The plans are divided such that understanding the plans and the method of constructing the model is an essential step to be able to comprehend and make use of the results. The first environmental impact category as described in the method is GWP. Figure 34 shows the GWP in kgCO2eq, resulting from manufacturing one module using IPCC AR6 GWP 100,

including the biogenic LCIA method. As explained in the method section, the second category (ecotoxicity) is chosen based on being the most significant category. Figure 35 shows the overall ecotoxicity represented in CTUe resulting from manufacturing the power module. The LCIA method as explained is USEtox2.12. Since one of the study's goals is to help designers make sustainable decisions in the early design stages, the detailed GWP impact using the same LCIA method for each plan is presented in Appendix B. The appendix can be utilized directly after knowing the LCIA method and understanding the plans constructions and model limitations for detecting the hotspots of the module fabrication.

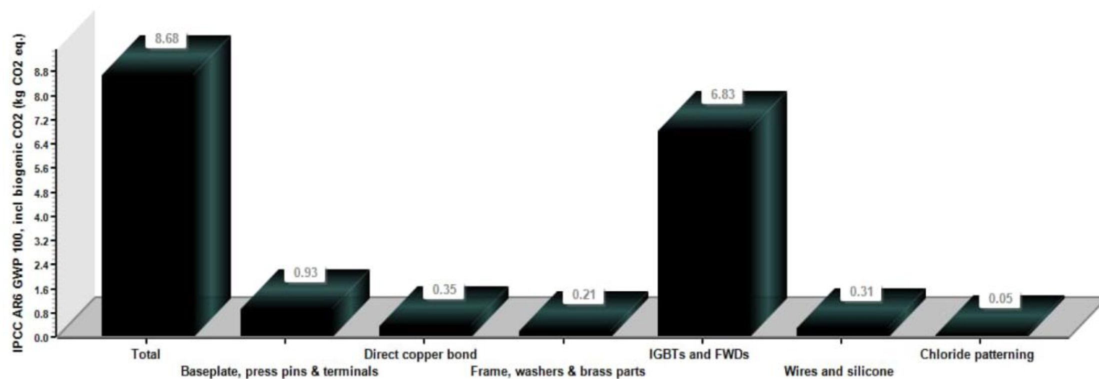


Figure 34: GWP in kgCO2eq from manufacturing one module mentioned in the functional unit, using IPCC AR6 GWP 100 LCIA method.

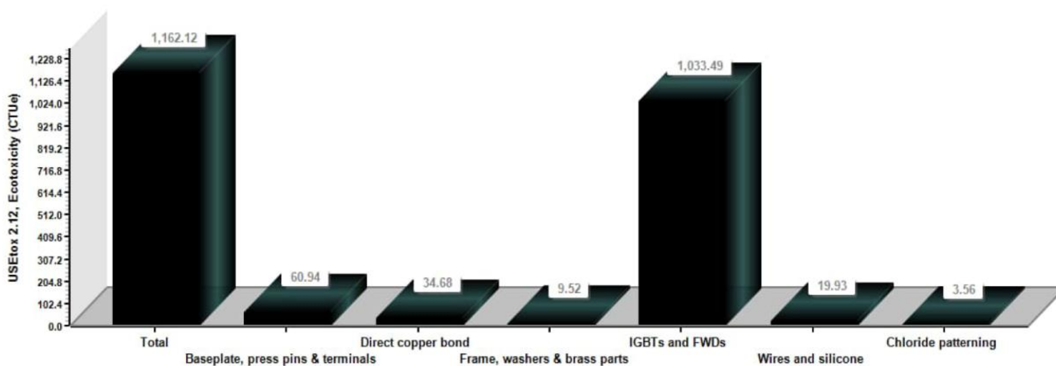


Figure 35: Ecotoxicity in CTUe from manufacturing one module mentioned in the functional unit, using USEtox2.12 LCIA method.

6 Conclusions

A cradle-to-gate LCA study methodology was presented in the highest level of detail possible including results obtained from tearing down and analysing the module under discussion. The LCIA results and interpretation are summarized in the next sections. The dominant conclusion is that to use LCA studies to assess the environmental impacts of electronics, transparent presentation of the method and sources of data is mandatory. The teardown work has shown that modularity is not considered for repair or end-of-life treatment for the module under discussion, meaning that the module is treated as one block. Increasing the modularity would introduce more sustainable scenarios for end-of-life treatment, one of which can be the reuse of the module's sub-parts in a second cycle of manufacturing. This by default would eliminate the impacts of these parts in the second cycle.

Despite the extensive datasets for ICs, GaBi software offers only limited applicable models for power electronics applications. All needed processes to fabricate a power module do not readily exist in the software databases. Moreover, looking at the literature presented in Chapter 3, there is no available database that has a better representation of power electronics applications, including the databases integrated into Simapro and OpenLCA software (both use ecoinvent as a primary database).

6.1 LCIA Interpretation

For the first category (GWP), the most obvious hotspot in the module fabrication phase is front-end fabrication comprised of both the IGBT and diode chips included in plan 4. Front-end fabrication alone counts for 6.8 kgCO2eq, knowing that the process is represented by average global impacts, this also induces a big level of uncertainty that has been discussed. The second hotspot is the copper of the baseplate that counts for 0.9 kgCO2eq, see Appendix B, figure B3. For the second category (ecotoxicity), front-end fabrication recorded the highest value of 1033.5 CTUe. Followed by nickel class 1 in plan 3, which counts for 48.1 CTUe.

6.2 Future Work and Recommendations

The use and end-of-life phases were left for future work for the study's limited time. The model can be used to compare conventional processes/designs with new/innovative designs including modularity scenarios that were not considered in the current model due to teardown information that revealed a non-modular design. After necessary modifications to reduce uncertainties, the model can be utilized as a reference to represent the impacts of Si IGBT

power module manufacturing as a whole or a picked sub-section of the module's fabrication. After necessary modifications to reduce uncertainties, the model can be used to compare the technology of Si IGBT with other technologies like SiC MOSFET. Moreover, the comparison with SiC IGBT is possible after the mature development of the technology and the packaging solutions. All comparisons are in terms of environmental impacts. To have a more accurate (less uncertainty) representation of the environmental impacts, the following steps are recommended:

i. A process to fabricate the IGBT and diode chips should be developed with a manufacturing route that complies with the rest of the module, in terms of having Germany the main manufacturing route and Europe, in general, the second.
ii. The model's graphical representation can be modified to represent specific manufacturing and use scenarios when such data is available.
iii. Statistical uncertainty analysis could be performed after obtaining/estimating the potential of the input and output flows. Another type of uncertainty analysis can be performed by building the same model with another database, namely ecoinvent, and comparing the results.

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A. Utilization of Chalmers Model Unit Processes

Unit process in Chalmers model	Flow scaling to	Adaptation	Justification	Unavailable (excluded) processes	Geographic representation
1. Alumina substrate fabrication	1 m^2 of Alumina substrate of 500 µm thick	Area to mass conversion. Scaled according to process 2	The Alumina substrate in the model of discussion is not 500 µm thick	-Acrylic binder -Acrylic dispersion -Insignificant thermal energies for Alumina production	RER: Alumina production, glycerin, DE: Electricity
2. Direct copper bonding	1 m^2 of DCB substrate	Area to mass conversion. Scaled to 1 kg of DCB substrate	Same as 1	None	RER: Copper sheet, Nitrogen DE: Isopropanol, Acetone, HCL, Electricity, water
3. Photolithographic regenerative etching of the upper copper foil of the DCB	1 kg of copper etching	1 kg of copper removed	--	None	DE: Electricity, water, Chlorine, HCL
3.1. Photolithography	1 m^2 of DCB	1 m^2 of DCB	--	None	DE: Ethylene glycol, Acetone, Isopropanol, RER: photoresist
4. Cleaning of metal surfaces before electroplating	1 m^2 area of three subcomponents that go to the process separately but with the same procedure	1 m^2 of cleaned metal (with mass area proxy to scale) (For all copper (baseplate	The process is used for one component at a time by dividing the input/output flows / into 3	None	DE: Water, Electricity, Sulphuric acid, sodium hydroxide. RER: Copper sheet

Unit process in Chalmers model	Flow scaling to	Adaptation	Justification	Unavailable (excluded) processes	Geographic representation
		+Copper parts))			
5. Nickel electroplating	1 Kg of Nickel	1 Kg of Nickel (the process count for all the nickel plating)	--	None	DE: Electricity, water GLO: Nickel class 1
6. Pre-solder cleaning, including vacuum baking	1 m^2 of the baseplate (one side)	1 m^2 of the baseplate (one side)	--	None	DE: electricity, water, Isopropanol
7. Stencil printing and soldering (both steps)	1 kg of lead-free solder	1 kg of SAC solder.	--	None	DE: Electricity, water, Isopropanol GLO: solder paste
8. Soldering (Vacuum VPS diffusion soldering for chip attachment)	1 m^2 of DCB (area on one side)	1 m^2 of DCB (area on one side)	--	None	DE: Electricity GLO: CMOS
9. Soldering (System soldering)	1 m^2 of the baseplate (one side)	1 m^2 of the baseplate (one side)	--	None	DE: Acetone, Nitrogen
10. Post-solder solvent cleaning	Same as 9	Same as 9 (the same process in the constructed model)	--	None	DE: Water, Isopropanol.
Extra (plastic injection moulding)	--	PBT weight.	Plastic injection moulding is used (for availability)	None	DE: PBT, tap water, Electricity
11. Frame and lid	1 kg of moulding mixture	Direct weights (same	Modules mismatch	Antimony trioxide	DE: glass fibre

Unit process in Chalmers model	Flow scaling to	Adaptation	Justification	Unavailable (excluded) processes	Geographic representation
		process as 12, the moulding electricity is counted for with Extra)			
12. Attachment of plastic frame	1 piece	Scaled with the plastic frame weight (direct scaling) 1 (1 is the resistor)	The scale is done directly with the teardown information	None	RER: Silicone sealing compound
13. Plasma cleaning	1 piece	1 piece	Integrated with 12 in the same process	Argon Gas (negligible)	DE: Electricity
Extra 2 (metals and NTC)	--	Direct scaling	To count for metals and NTC production (Extra 2 is integrated with the frame and lid process)	Tin plating of metals	RER: Brass CuZn20, galvanized screws "washers" GLO: Resistor MELF,
14. Ultrasonic bonding of wires and **terminals**	1 $cm^2$of IGBT chip area	Direct scaling (1 piece of the module)	The assumptions in Chalmers model don't comply with the module in discussion	Copper and aluminium bonding differences, the attachment of terminals is counted	DE: Electricity RER: Copper wire mix RNA: Aluminium extrusion RER: Copper wire mix
15. Potting and curing with UV light (2 processes)	1 kg of silicone	1 kg of silicone	--	None	DE: Electricity, Silicone fluid (low viscous)

Unit process in Chalmers model	Flow scaling to	Adaptation	Justification	Unavailable (excluded) processes	Geographic representation
16. Attachment of plastic lid	1 piece	1 piece	The process can be neglected because the amount of adhesion is very small.	None	RER: Silicone sealing compound

B. Detailed GWP Impact from Module Production

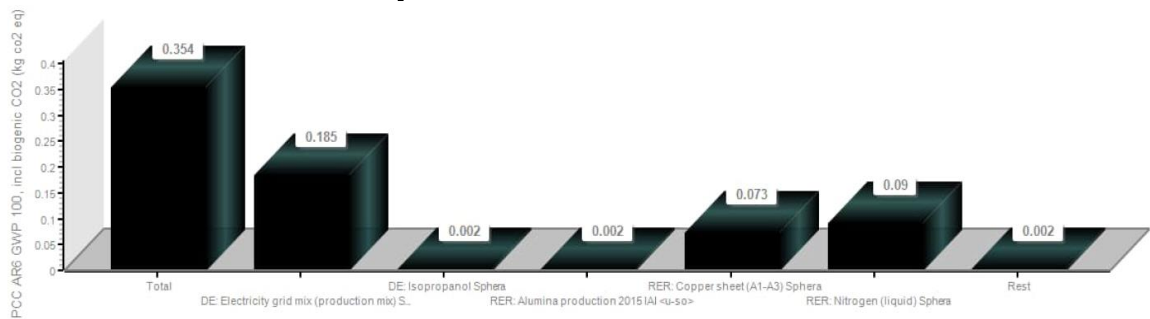

Figure B.1: GWP impact represented in kgCO2eq resulting from the manufacturing processes of the first plan.

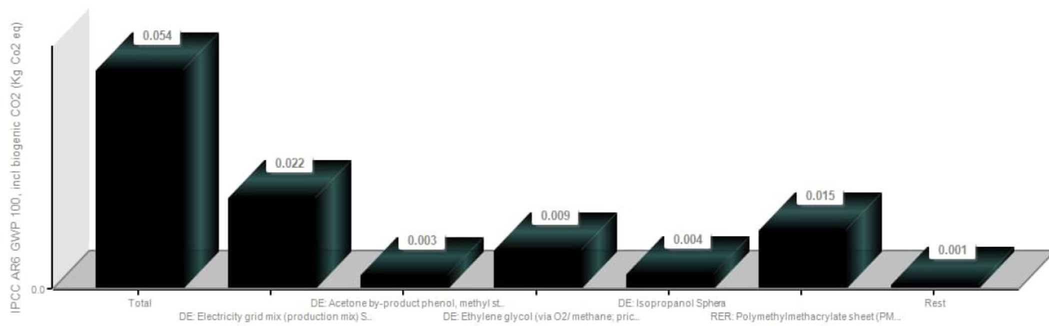

Figure B.2: GWP impact represented in kgCO2eq resulting from the manufacturing processes of the second plan.

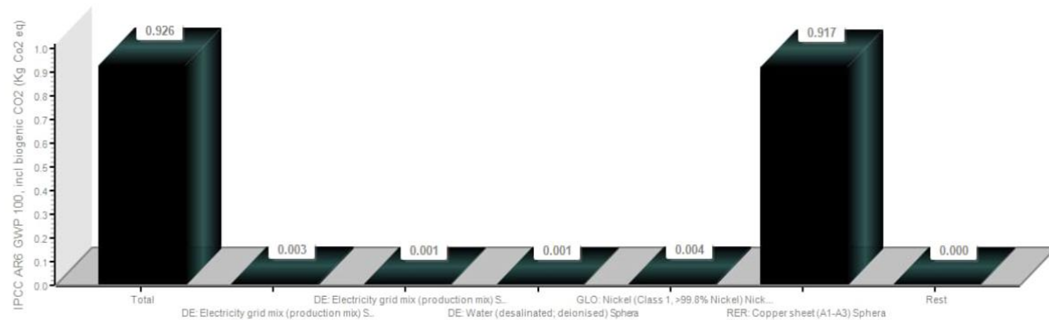

Figure B.3: GWP impact represented in kgCO2eq resulting from the manufacturing processes of the third plan.

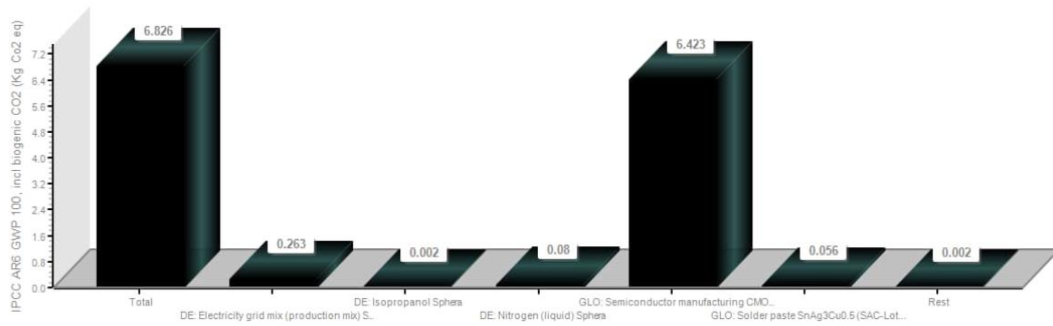

Figure B.4: GWP impact represented in kgCO2eq resulting from the manufacturing processes of the fourth plan.

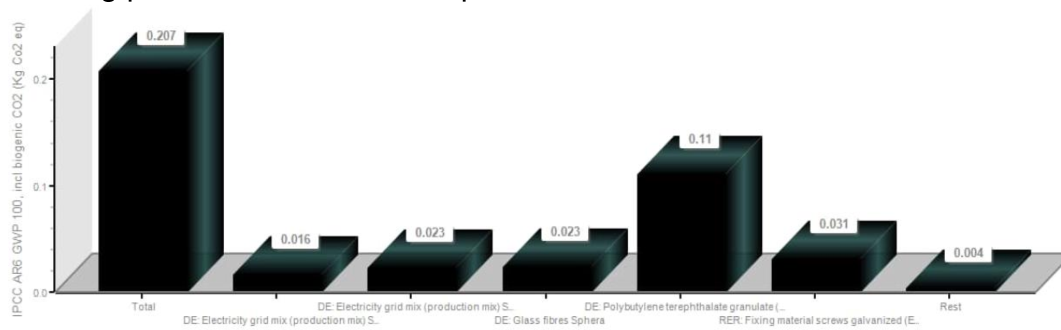

Figure B.5: GWP impact represented in kgCO2eq resulting from the manufacturing processes of the fifth plan.

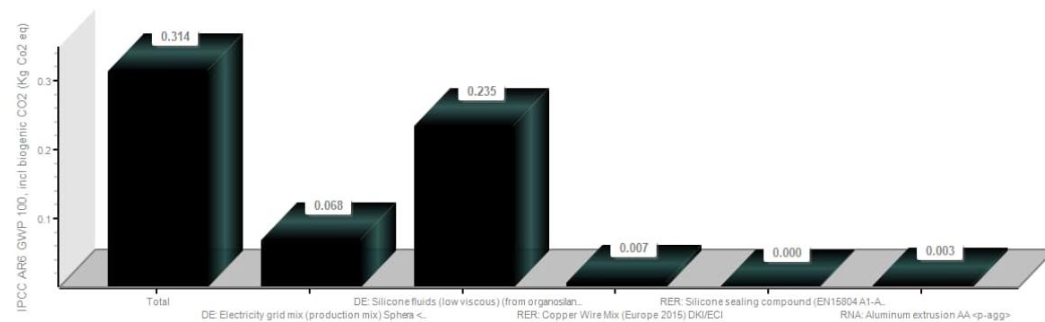

Figure B.6: GWP impact represented in kgCO2eq resulting from the manufacturing processes of the sixth plan.