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TOPOLOGICAL ISSUES IN SINGLE-PHASE POWER FACTOR CORRECTION

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Abstract

The equipment connected to an electricity distribution network usually needs some kind of power conditioning, typically rectification, which produces a nonsinusoidal line current due to the nonlinear input characteristic. With the steadily increasing use of such equipment, line current harmonics have become a significant problem. Their adverse effects on the power system are well recognized. They include increased magnitudes of neutral currents in three-phase systems, overheating in transformers and induction motors, as well as the degradation of system voltage waveforms. Several international standards now exist, which limit the harmonic content due to line currents of equipment connected to electricity distribution networks. As a result, there is the need for a reduction in line current harmonics, or *Power Factor Correction - PFC.*

In this dissertation, we address several issues concerning the application to single-phase PFC of various high-frequency switching converter topologies. The inherent PFC properties of second-order switching converters operating in Discontinuous Inductor Current Mode – DICM are well known, and Boost converters are widely used. However, their output voltage is always higher than the amplitude of the rectified-sinusoid input voltage. In addition, it is expected that the level of the differential-mode EMI is much higher in DICM, as compared to the Continuous Inductor Current Mode – CICM. Therefore, we first investigated the requirements for the EMI filter for a PFC stage based on a Boost converter operating in DICM.

The high-level of differential-mode EMI that is associated with DICM operation prompted our interest to investigate the application of two-switch fourth-order converters for PFC. The switching cell of these converters contains two inductors, which can operate in DICM or in CICM, and one capacitor, which can operate in Discontinuous Capacitor Voltage Mode – DCVM or in Continuous Capacitor Voltage Mode – CCVM. As a consequence, in these topologies several combinations of operating modes can be obtained, which have characteristics that otherwise cannot be obtained in second-order switching converters.

We analyze three fourth-order topologies operating in DCVM and CICM, which have both an input current with reduced high-frequency content and an inherent PFC property. One of the converters, i.e. the Buck converter with an LC input filter, is then selected for a more detailed analysis. In addition, a fourth-order topology with galvanic isolation and operating in DCVM and CICM is presented and analyzed, as well.

We also consider the operation in CCVM and CICM, which is analyzed for a fourth-order topology with step-down conversion ratio. The ‘zero-ripple’ technique is applied to obtain an input current having a very low high-frequency content, and average current mode control is used to shape the input current.

Methods for improving the efficiency of the PFC stage are addressed, too. We compare several Boost-type topologies that have lower conduction losses than the combined diode bridge and Boost converter, as well as one fourth-order topology that is able to operate with bipolar input voltage, in other words it can perform direct AC/DC conversion.

Finally, we propose a novel Zero Voltage Transition – ZVT topology, which reduces the switching losses by creating zero voltage switching conditions at the turn-on of the active switch. This topology can be used in a variety of converters, for DC/DC or PFC applications.

Preface

It has been a pleasure for me to work on this dissertation. I hope the reader will find it not only interesting and useful, but also comfortable to read.

The research reported here has been carried out at the Helsinki University of Technology (HUT), Espoo, Finland, at the Power Electronics Laboratory. I am greatly indebted to many persons for helping me complete this dissertation.

First and foremost, I am most grateful to my advisor, Professor Jorma Kyyrä, whose valuable scientific guidance and encouraging attitude have motivated much of the research described in this dissertation. Jorma is a very gifted and dedicated professor, and I consider myself fortunate to have worked under his guidance. He created an environment extremely favorable for research and paved my way in every possible mode. I can only wish him all the best for the future. Thank you for everything, Jorma.

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I am grateful to my parents and sister for their moral support and understanding. They are very important to me.

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Helsinki, November 2001

Vlad Grigore

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List of Publications

This dissertation consists of an introductory part and the following eight publications, which are referred to by [P1]-[P8] in the text:

[P1] V. Grigore, J. Rajamäki, J. Kyyrä, "Input filter design for power factor correction converters operating in discontinuous conduction mode," in *Record of the 1999 IEEE International Symposium on Electromagnetic Compatibility*, Seattle, WA, USA, 1999, pp. 145-150.

[P2] V. Grigore, J. Kyyrä, "Properties of DC/DC converters operating in discontinuous capacitor voltage mode," in *Proceedings of the IEEE Nordic Workshop on Power and Industrial Electronics, NORPIE/98*, Espoo, Finland, 1998, pp. 19-24.

[P3] V. Grigore, J. Kyyrä, "High power factor rectifier based on Buck converter operating in discontinuous capacitor voltage mode," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1241-1249, Nov. 2000.

[P4] V. Grigore, J. Kyyrä, "Analysis of a high power factor rectifier based on discontinuous capacitor voltage mode operation," in *Record of the 30th IEEE Power Electronics Specialists Conference, PESC'99*, Charleston, SC, USA, 1999, pp. 93-98.

[P5] V. Grigore, J. Kyyrä, "A step-down converter with low-ripple input current for power factor correction," in *Proceedings of the 14th IEEE Applied Power Electronics Conference, APEC'00*, New Orleans, LA, USA, 2000, pp. 188-196.

[P6] V. Grigore, J. Kyyrä, "Topologies for unity power factor AC/DC conversion with reduced conduction losses," in *Proceedings of the 8th European Conference on Power Electronics and Applications, EPE'99*, Lausanne, Switzerland, 1999, CD-ROM, 10 pages.

[P7] V. Grigore, J. Kyyrä, "A new zero-voltage-transition PWM Buck converter," in *Proceedings of the 9th IEEE Mediterranean Electrotechnical Conference, MELECON'98*, Tel-Aviv, Israel, 1998, pp. 1241-1245.

[P8] V. Grigore, J. Kyyrä, "A 500W (50V@10A) ZVT Forward Converter", in *Proceedings of the 13th IEEE Applied Power Electronics Conference, APEC'98*, Anaheim, CA, USA, 1998, pp. 614-619.

List of Abbreviations

The abbreviations listed here are used in the introductory part of this dissertation. The abbreviations used in [P1]-[P8] may be publication specific and are defined within each publication.

AC	Alternating Current
BIFRED	Boost Integrated with Flyback Rectifier Energy storage DC-DC converter
CCVM	Continuous Capacitor Voltage Mode
CENELEC	European Committee for Electrotechnical Standardization
CICM	Continuous Inductor Current Mode
CISPR	International Committee for Radio Interference
DC	Direct Current
DCVM	Discontinuous Capacitor Voltage Mode
DICM	Discontinuous Inductor Current Mode
EMI	Electromagnetic Interference
FCC	Federal Communications Commission
IEC	International Electrotechnical Committee
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
LC	Circuit composed of an inductor L and a capacitor C
LCD	Circuit composed of an inductor L, a capacitor C and a diode D
LISN	Line Impedance Stabilization Network
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCC	Point of Common Coupling
PFC	Power Factor Correction
PWM	Pulse Width Modulation

QR	Quasi-Resonant
RC	Circuit composed of a resistor R and a capacitor C
RMS	Root Mean Square
SEPIC	Single Ended Primary Inductance Converter
VDE	German Association for Electrical, Electronic & Information Technologies
ZCS	Zero Current Switching
ZCT	Zero Current Transition
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

List of Symbols

The symbols listed here are used in the introductory part of this dissertation. The symbols used in [P1]-[P8] may be publication specific and are defined within each publication.

$\langle \bullet \rangle_{T_s}$	average of variable $\bullet$, over one switching period T_s
$\hat{\bullet}$	small perturbations of variable $\bullet$ around the operating point
C	ideal capacitor
C	capacitance of C
C_{DS}	drain-source capacitance of a MOSFET
d	duty-cycle
$\hat{d}(s)$	Laplace transform of $\hat{d}$
d_1	normalized discharge time of a capacitor in DCVM
d_2	normalized discharge time of an inductor in DICM
D	diode
D	constant duty-cycle d
D_1	constant normalized discharge time of a capacitor in DCVM
f_s	switching frequency
G_H	transfer function of the compensator in the high-bandwidth current loop
G_L	transfer function of the compensator in the low-bandwidth voltage loop
H_f	transfer function of the EMI filter
H_{i_1-d}	control-to-input-current transfer function
H_{i_S-d}	control-to-switch-current transfer function
i	instantaneous current *or*
	index variable
$\hat{i}(s)$	Laplace transform of $\hat{i}$

$i_{\bullet,\mathrm{n}}$	current $i_{\bullet}$ normalized to the load current
I	constant current *or*
	amplitude of current i
$I_{1,\mathrm{rms}}$	RMS of the fundamental component of the line current
$I_{\mathrm{D,av}}$	average diode current
$I_{\mathrm{D,rms}}$	RMS diode current
$I_{i,\mathrm{rms}}$	RMS current of the active switch S_i
I_{L}	maximum demand load current (fundamental frequency component) at PCC
$I_{n,\mathrm{rms}}$	RMS of the *n*-th harmonic component of the line current
I_{pk}	peak value of the line current
I_{rms}	RMS of the nonsinusoidal line current
I_{sc}	maximum short-circuit current at PCC
$I_{\mathrm{S,rms}}$	RMS drain current of a MOSFET
Im	imaginary axis
$\mathbf{I}$	phasor representation of a sinusoidal current
k	coupling factor *or*
	number of active switches
k_{zr}	‘zero-ripple’ coupling factor
K	characteristic coefficient
$K_{\mathrm{D}}^{\mathrm{SIN}}$	secondary diode voltage stress coefficient, for operation with rectified-sinusoid input
K_{p}	purity factor of the line current
K_{PFC}	coefficient for assessing the inherent PFC properties
$K_{\mathrm{S}}^{\mathrm{SIN}}$	switch voltage stress coefficient, for operation with rectified-sinusoid input
L	ideal inductor
L	inductance of the ideal inductor L
L_{12}	mutual inductance

L_{m}	magnetizing inductance
M_{SIN}	conversion ratio for operation with rectified-sinusoid input
n	turns-ratio
n	index variable
N	number of turns
p_{S}	instantaneous active switch power dissipation
P	active power in a sinusoidal system *or*
	load power
$P_{\mathrm{D,cond}}$	diode conduction losses
$P_{\mathrm{S,cond}}$	active switch conduction losses
PF	power factor
Q_{r}	recovered charge
r_{1}	average input resistance of the PFC stage
r_{D}	diode resistance, in the simplified on-state model
r_{DS}	drain-to-source resistance, in the simplified on-state model of a MOSFET
R	ideal resistor
R	resistance of the ideal resistor R
R_{1}	constant average input resistance r_{1} of the PFC stage
Re	real axis
s	complex frequency
S	active switch
S	apparent power
S_{a}	total active switch stress coefficient
t	time
T_{f}	equivalent loop gain
T_{L}	line period

T_{off}	off-time of an active switch
T_{on}	on-time of an active switch
T_{s}	switching period
Th	thyristor
THD_i	total harmonic distortion of the line current
THD_v	total harmonic distortion of the line voltage
U_{a}	active switch utilization factor
v	instantaneous voltage
$v(s)$	Laplace transform of voltage v
$v_{1,\text{n}}$	line voltage v_1, normalized to the amplitude V_1
V	constant voltage *or*
	amplitude of voltage v
V_{CM}	peak voltage on capacitor C, when operating in DCVM
V_{D}	forward voltage drop, in the simplified on-state model of a diode *or*
	voltage stress of the secondary side diode
$V_{i,\text{max}}$	voltage stress of active switch S_i
V_{rms}	RMS value of the purely sinusoidal line voltage
V_{S}	switch voltage stress
$\mathbf{V}$	phasor representation of a sinusoidal voltage
X	multiplicator input
X	reactance
XY	multiplicator output
Y	multiplicator input
Z_{ic}	input impedance of the PFC stage
Z_{of}	output impedance of the EMI filter
α	firing-angle *or*

	dead angle
β	angle where the line current, normalized to its amplitude, is 0.35
φ	displacement angle
η	efficiency
ω_L	angular line frequency

1 Introduction

1.1 Nonlinear loads and their effect on the electricity distribution network

The equipment connected to an electricity distribution network usually needs some kind of power conditioning, typically rectification, which produces a nonsinusoidal line current due to the nonlinear input characteristic. The most significant examples of nonlinear loads are reviewed next.

Line-frequency diode rectifiers convert AC input voltage into DC output voltage in an uncontrolled manner. Single-phase diode rectifiers are needed in relatively low power equipment that need some kind of power conditioning, such as electronic equipment (e.g. TVs, office equipment, battery chargers, electronic ballasts) and household appliances. For higher power, three-phase diode rectifiers are used, e.g. in variable-speed drives and industrial equipment. In both single- and three-phase rectifiers, a large filtering capacitor is connected across the rectifier output to obtain DC output voltage with low ripple. As a consequence, the line current is nonsinusoidal. Line-frequency phase-controlled rectifiers are used for controlling the transfer of energy between the AC input and the adjustable DC output. They are applied, for example, in some DC and AC motor drives with regenerative capabilities, or for controlling the light intensity in incandescent lamps or the temperature in resistive heaters. In every case, the line current is nonsinusoidal. Gas-discharge lamps with line-frequency ballast are nonlinear loads, as well. Hence, their line current is nonsinusoidal.

In most of these cases, the amplitude of odd harmonics of the line current is considerable with respect to the fundamental. As an example, a single-phase diode rectifier is presented in Fig. 1.1, together with its line current and voltage waveforms. The odd harmonics of the line current, normalized to the fundamental, are shown in the same figure. The normalized amplitudes of the 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonics are significant.

While the effect of a single low power nonlinear load on the network can be considered negligible, the cumulative effect of several nonlinear loads is important. Line current harmonics have a number of undesirable effects on both the distribution network and consumers [IEE92], [Red95], [Red96a], [Red97]. These effects include:

- Losses and overheating in transformers, shunt capacitors, power cables, AC machines and switchgear, leading to premature aging and failure.

- Excessive current in the neutral conductor of three-phase four-wire systems, caused by odd triplen current harmonics (triple-*n*: 3rd, 9th, 15th, etc.). This leads to overheating of the neutral conductor and tripping of the protective relay.
- Reduced power factor, hence less active power available from a wall outlet having a certain apparent power rating.
- Electrical resonances in the power system, leading to excessive peak voltages and RMS currents, and causing premature aging and failure of capacitors and insulation.
- Distortion of the line voltage via the line impedance, as shown in Fig. 1.1, where the typical worst-case values, $R_{\text{line}} = 0.4\Omega$ and $L_{\text{line}} = 800\mu\text{H}$ [Red01], have been considered. The effect is stronger in weaker grids. The distorted line voltage may affect other consumers connected to the electricity distribution network. For example, some electronic equipment is dependent on accurate determination of aspects of the voltage wave shape, such as amplitude, RMS and zero-crossings.
- Telephone interference.
- Errors in metering equipment.
- Increased audio noise.
- Cogging or crawling in induction motors, mechanical oscillation in a turbine-generator combination or in a motor-load system.

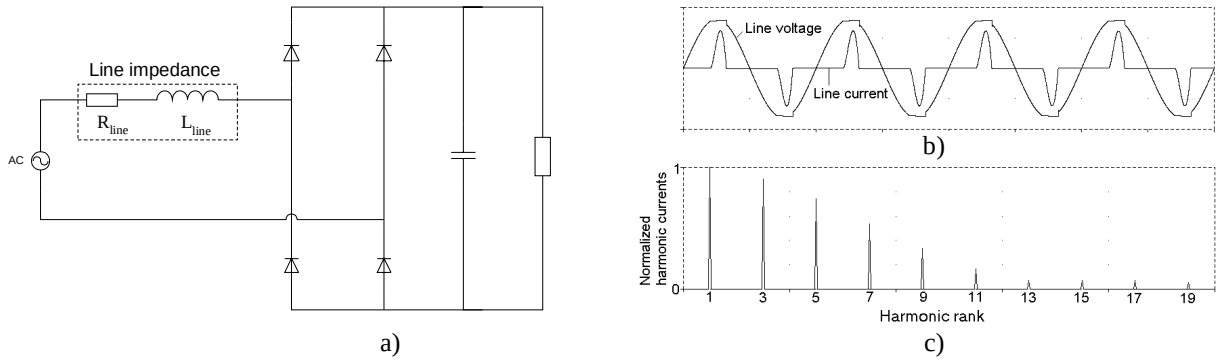


Fig. 1.1 Single-phase diode bridge rectifier: a) Schematic; b) Typical line current and voltage waveforms; c) Odd line current harmonics normalized to the fundamental.

1.2 Standards regulating line current harmonics

The previously mentioned negative effects of line current distortion have prompted a need for setting limits for the line current harmonics of equipment connected to the electricity distribution network. Standardization activities in this area have been carried out for many years. As early as 1982, the International Electrotechnical Committee - IEC published its standard IEC 555-2 [IEC82], which was also adopted in 1987 as European standard EN 60555-2, by the European Committee for Electrotechnical Standardization - CENELEC. Standard IEC 555-2 has been replaced in 1995 by standard IEC 1000-3-2 [IEC95], also adopted by CENELEC as European standard EN 61000-3-2.

Standard IEC 1000-3-2 applies to equipment with a rated current up to and including $16A_{rms}$ per phase which is to be connected to 50Hz or 60Hz, $220\text{-}240V_{rms}$ single-phase, or $380\text{-}415V_{rms}$ three-phase mains. Items of electrical equipment are categorized into four classes (A, B, C and D), for which specific limits are set for the harmonic content of the line current. The standard has been revised several times and a second edition was published in 2000 [IEC00] with an amendment in 2001 [IEC01]. Next, we present the current harmonic limits and the present status in equipment classification, with a discussion on the changes in the definition of Class D equipment. We want to point out that the standard defines also a procedure for applying the limits, as well as exceptions and special provisions which should be taken into account when assessing conformity. Most notably, the limits do not apply for equipment with rated powers of 75W or less (it may be reduced to 50W in the future), other than lighting equipment.

Class A includes: balanced three-phase equipment; household appliances, excluding equipment identified as Class D; tools, excluding portable tools; dimmers for incandescent lamps; and audio equipment. Equipment not specified in one of the other three classes should be considered as Class A equipment. The limits for Class A are presented in Table 1.1.

Class B equipment includes: portable tools; and nonprofessional arc welding equipment. The limits for this class are those shown in Table 1.1, multiplied by a factor of 1.5.

Class C includes lighting equipment. For an active input power greater than 25W, the harmonic currents should not exceed the limits presented in Table 1.2 (except for dimmers for incandescent lamps, which belong to Class A). Discharge lighting equipment having an active input power smaller than or equal to 25W should comply with one of the following two sets of requirements: the harmonic currents should not exceed the Class D power-related limits, shown in Table 1.3, column 2; or, the third harmonic current, expressed as a percentage of the fundamental

current, should not exceed 86% and the fifth should not exceed 61%, with the input current waveform satisfying a special provision of the standard.

The harmonic limits for Class D are presented in Table 1.3. They are defined in both power-related and absolute terms. Initially, Class D included equipment having an active input power less than or equal to 600W, and an input current waveform – normalized to its peak value, I_{pk} – which stays within the envelope shown in Fig. 1.2 for at least 95% of the duration of each half-period, assuming that the peak of the line current waveform coincides with the center line M [IEC95]. For example, devices which comply with this definition are equipment having a front-end composed of a diode bridge and filtering capacitor as shown in Fig. 1.1a), and having an input current as shown in Fig. 1.1b). Class D equipment was penalized indiscriminately by the power-related harmonic limits, regardless of its impact on the electricity distribution system. In addition to that, the definition based on the Class D envelope allowed for techniques aiming merely at changing the classification of the equipment from Class D to Class A by modifying the shape of the input current, to avoid the Class D power-related limits. However, the definition of Class D has been changed [IEC01], to include equipment that can be shown to have a significant impact on the electricity distribution network. Under current definition, Class D includes equipment having an active input power less than or equal to 600W, of the following types: personal computers, personal computer monitors; and television receivers.

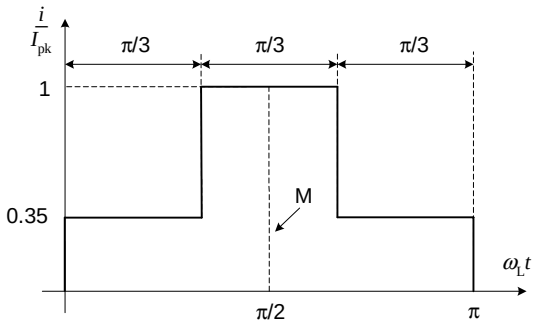


Fig. 1.2 Envelope of the input current used to classify Class D equipment, as defined in the first edition of IEC 1000-3-2.

Table 1.1 Limits for Class A equipment in standard IEC 1000-3-2.

Harmonic order n	**Maximum permissible harmonic current** A
Odd harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \le n \le 39$	$0.15 \cdot \frac{15}{n}$
Even harmonics	
2	1.08
4	0.43
6	0.30
$8 \le n \le 40$	$0.23 \cdot \frac{8}{n}$

Table 1.2 Limits for Class C equipment in standard IEC 1000-3-2.

Harmonic order n	**Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency** %
2	2
3	$30 \cdot PF^{*}$
5	10
7	7
9	5
$11 \le n \le 39$ (odd harmonics only)	3
PF^{*} is the circuit power factor	

Table 1.3 Limits for Class D equipment in standard IEC 1000-3-2.

Harmonic order n	**Maximum permissible harmonic current per watt** mA/W	**Maximum permissible harmonic current** A
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$13 \le n \le 39$	$\frac{3.85}{n}$	As in Class A

Besides standard IEC 1000-3-2, there are also other documents addressing the control of current harmonics. Standard IEC/TS 61000-3-4 [IEC98] [1] gives recommendations applicable to equipment with rated current greater than $16A_{rms}$ per phase and intended to be connected to 50Hz or 60Hz mains, with nominal voltage up to $240V_{rms}$ single-phase, or up to $600V_{rms}$ three-phase.

Standard IEEE 519-1992 [IEE92] gives recommended practices and requirements for harmonic control in electrical power systems, for both individual consumers and utilities. The limits for line current harmonics are given as a percentage of the maximum demand load current I_L (fundamental frequency component) at the Point of Common Coupling – PCC at the utility. They decrease as the ratio I_{sc}/I_L decreases, where I_{sc} is the maximum short-circuit current at the PCC, meaning that the limits are lower in weaker grids. The standard covers also high voltage loads, of much higher power, which are not addressed by IEC 1000-3-2.

This subchapter reflects the status at the moment of writing. However, standards are evolving and changes are expected to them in the future.

The dissertation focuses on methods to achieve compliance with standard IEC 1000-3-2 in single-phase systems.

1.3 Power Factor Correction - PFC

Reduction of line current harmonics is needed in order to comply with the standard. This is commonly referred to as the Power Factor Correction – PFC, which may be misleading. Therefore, some clarification is needed.

The power factor, *PF*, is defined as the ratio of the active power *P* to the apparent power *S*:

$$PF = \frac{P}{S}. \tag{1.1}$$

For purely sinusoidal voltage and current, the classical definition is obtained:

$$PF = \cos\varphi, \tag{1.2}$$

where $\cos\varphi$ is the displacement factor of the voltage and current. In a classical sense, PFC means compensation of the displacement factor.

[1] As of 1st of January 1997, all IEC publications have been issued with a designation in the 60000 series.

We assume the line voltage to be sinusoidal, since in most cases the total harmonic voltage distortion is quite low, e.g. the total harmonic distortion of the line voltage shown in Fig. 1.1 is $THD_v \cong 2\%$. However, the line current is nonsinusoidal when the load is nonlinear. Therefore, the classical definition of the power factor does not apply. For sinusoidal voltage and nonsinusoidal current, (1.1) can be expressed as:

$$PF = \frac{V_{\text{rms}} I_{1,\text{rms}} \cos\varphi}{V_{\text{rms}} I_{\text{rms}}} = \frac{I_{1,\text{rms}}}{I_{\text{rms}}} \cos\varphi = K_{\text{p}} \cos\varphi . \tag{1.3}$$

The factor

$$K_{\text{p}} = I_{1,\text{rms}} / I_{\text{rms}} \text{ , } K_{\text{p}} \in [0,1], \tag{1.4}$$

describes the harmonic content of the current with respect to the fundamental. In this case, the power factor depends on both harmonic content and displacement factor. It appears that there is no standard term which can be used to denote the factor defined by (1.4). Some authors refer to it as the ‘purity factor’ [Kel92], while others as the ‘distortion factor’ [Red94a]. We believe that ‘purity factor’ describes its meaning more accurately, as the factor is unity for a pure sinusoidal current, and it decreases as the harmonic content increases. Moreover, defining it as ‘distortion factor’ is in contradiction with the definition given by the IEEE Standard Dictionary on Electrical and Electronics Terms [IEE96, pp. 306], which considers it as a synonym for the total harmonic distortion factor, the latter being defined for the line current as:

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,\text{rms}}^2}}{I_{1,\text{rms}}}. \tag{1.5}$$

It is straightforward to show that the relation between K_{p} and THD_i is:

$$K_{\text{p}} = \frac{1}{\sqrt{1 + THD_i^2}}. \tag{1.6}$$

Standard IEC 1000-3-2 sets limits on the harmonic content of the current but does not specifically regulate the purity factor K_{p} or the total harmonic distortion of the line current THD_i.

The values of K_p and THD_i for which compliance with IEC 1000-3-2 is achieved depend on the power level. For low power level, even a relatively distorted line current may comply with the standard. In addition to this, it can be seen from (1.6) that the distortion factor K_p of a waveform with a moderate THD_i is close to unity (e.g. $K_p = 0.989$ for $THD_i = 15\%$). Considering (1.3) as well, the following statements can be made:

- A high power factor can be achieved even with a substantial harmonic content. The power factor *PF* is not significantly degraded by harmonics, unless their amplitude is quite large (low K_p, very large THD_i).
- Low harmonic content does not guarantee high power factor (K_p close to unity, but low $\cos\varphi$).

Most of the research on PFC for nonlinear loads, including the research reported in this dissertation, is actually related to the reduction of the harmonic content of the line current. There are several solutions to achieve PFC [Red94a]. Depending on whether active switches (controllable by an external control input) are used or not, PFC solutions can be categorized as *passive* or *active.* In *passive* PFC, only passive elements are used in addition to the diode bridge rectifier, to improve the shape of the line current. Obviously, the output voltage is not controllable. For *active* PFC, active switches are used in conjunction with reactive elements in order to increase the effectiveness of the line current shaping and to obtain controllable output voltage. The switching frequency further differentiates the active PFC solutions into two classes. In *low-frequency* active PFC, switching takes place at low-order harmonics of the line-frequency and it is synchronized with the line voltage. In *high-frequency* active PFC, the switching frequency is much higher than the line-frequency. An overview of methods for PFC is presented in Chapter 2.

1.4 Aim of this dissertation

To better define the scope of the research reported in this dissertation, let us consider the widely used block diagram of a power supply that is shown in Fig. 1.3, where PFC is performed by a high-frequency switching DC/DC converter that shapes the input current as close as possible to a sinusoidal waveform which is in phase with the line voltage. Thus, from the electrical point of view, the equipment connected to the line behaves like a resistive load. The voltage on the storage capacitor at the output of the PFC stage has a ripple at twice the line-frequency (e.g. 100Hz for a European line). Therefore, a second DC/DC switching converter is used to provide a tightly regulated output voltage and, eventually, to provide galvanic isolation. As an example, a typical

telecom power supply uses a Forward DC/DC converter to convert the 380-400V_{dc} output voltage of the PFC stage, to 48V_{dc} output voltage, as well as to provide galvanic isolation. The load of the PFC stage can be also an inverter in AC drives applications.

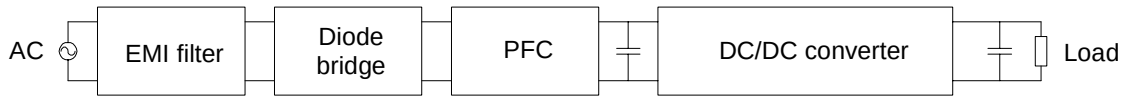


Fig. 1.3 Block diagram of a power supply with active PFC.

While the high-frequency switching PFC stage reduces the line current harmonics, it also has drawbacks, such as: it introduces additional losses, thus reducing the overall efficiency; it increases the EMI, due to the high-frequency content of the input current; and it increases the complexity of the circuit, with negative effects on the reliability of the equipment, as well as on its size, weight and cost. The general aim of this dissertation is to investigate high-frequency switching circuit topologies and methods to be applied in the PFC stage, which would alleviate some of the aforementioned drawbacks. The research addresses several aspects which can be divided into three topics.

First, we investigate input filter requirements for a PFC stage based on a Boost converter operating in Discontinuous Inductor Current Mode – DICM, focusing on the interaction between the input filter and the PFC stage. The background related to this topic is presented in the next chapter, in Subsection 2.3.4, and results are reported in publication [P1], which is summarized in Section 5.1.

Second, we explore the possibilities of realizing a PFC stage having characteristics such as: input current with reduced high-frequency content, to minimize the input current filtering requirements; inherent PFC property, to simplify the control circuit; step-down characteristic, to obtain an output voltage lower than the amplitude of the rectified-sinusoid input voltage. To this objective, fourth-order switching converters are investigated. Research related to this area is reviewed in Chapter 3. The results of our research are reported in publications [P2]-[P5] and are summarized in Sections 5.2 and 5.3.

Third, we study circuit techniques to improve the efficiency of the PFC stage by lowering the conduction losses and/or the switching losses. The background related to this area is presented in Chapter 4. Conduction losses in the combined diode bridge and PFC stage can be diminished, in

principle, by having less switches in the power path, and/or by reducing their average and RMS currents. Four Boost-based PFC stages, as well as the use of one fourth-order switching converter which is able to operate with bipolar input voltage (thus eliminating the need for a diode bridge), are evaluated in publication [P6], which is summarized in Section 5.4. Switching losses can be reduced using soft-switching techniques. A novel Zero Voltage Transition – ZVT technique, which can be applied to both the converter used in the PFC stage and the downstream converter for output voltage regulation, is presented in publications [P7] and [P8] which are summarized in Section 5.5.

2 Overview of Methods for PFC

As mentioned in the previous chapter, the diode bridge rectifier, shown again in Fig. 2.1a), has nonsinusoidal line current. This is because most loads require a supply voltage V_2 with low ripple, which is obtained by using a correspondingly large capacitance of the output capacitor C_f. Consequently, the conduction intervals of the rectifier diodes are short and the line current consists of narrow pulses with an important harmonic content.

The simplest way to improve the shape of the line current, without adding additional components, is to use a lower capacitance of the output capacitor C_f. When this is done, the ripple of the output voltage increases and the conduction intervals of the rectifier diodes widen. The shape of the input current becomes also dependent on the type of load that the rectifier is supplying, resistive or constant power, as opposed to the case of negligible output voltage ripple where the type of load does not affect the line current. This solution can be applied if the load accepts a largely pulsating DC supply voltage and it is used, for example, in some handheld tools. The concept is highlighted by the simulated waveforms shown in Fig. 2.1b), for two values of the output capacitor and assuming constant power load. The shape of the input current is improved to a certain extent with the lower capacitance, at the expense of increased output voltage ripple, as can be seen also from the results listed in the caption of Fig. 2.1.

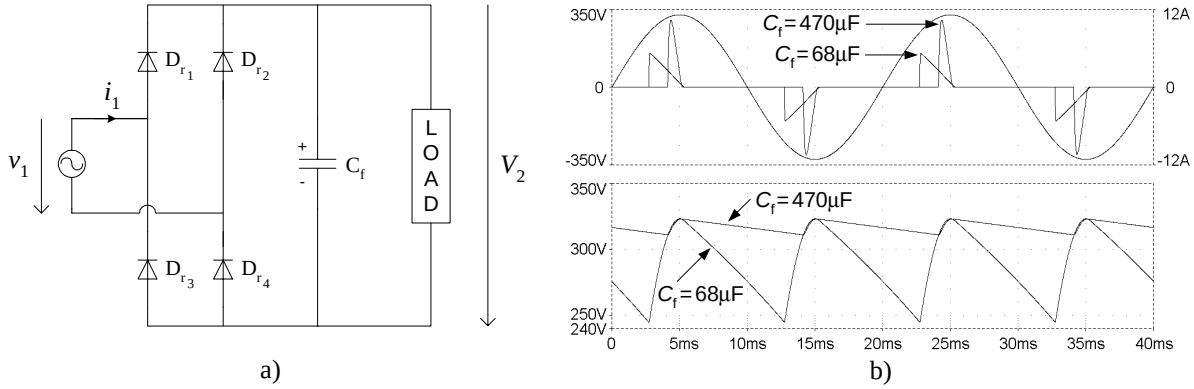


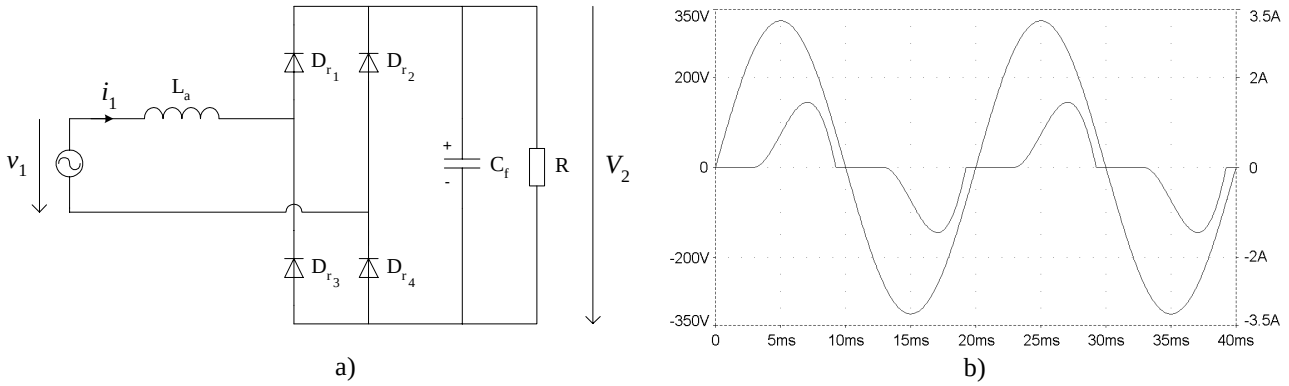
Fig. 2.1 Diode bridge rectifier: a) Schematic; b) Line voltage and line current (upper plot), and output voltage (lower plot), with $V_1 = 230\text{V}_{\text{rms}}$ and constant power load $P = 200\text{W}$. With $C_f = 470\mu\text{F}$, the line current has $K_p = 0.409$, $\cos\varphi = 0.991$ and $PF = 0.405$, and the output voltage ripple is $\Delta V_2 = 12\text{V}$. With $C_f = 68\mu\text{F}$, the line current has $K_p = 0.619$, $\cos\varphi = 0.910$ and $PF = 0.563$, and the output voltage ripple is $\Delta V_2 = 78\text{V}$.

We would like to clarify here that, throughout this chapter, the purity factor K_p, the displacement factor $\cos\varphi$ and the power factor PF, are given only as basic information on the PFC properties of the simulated circuits, and they are not relevant as such for assessing compliance with standard IEC 1000-3-2.

The method presented above has severe limitations: it does not reduce substantially the harmonic currents and the output voltage ripple is large, which is not acceptable in most of the cases. Several other methods to reduce the harmonic content of the line current in single-phase systems exist, and an overview of the representative ones is presented next.

2.1 Passive PFC

Passive PFC methods use additional passive components in conjunction with the diode bridge rectifier from Fig. 2.1. One of the simplest methods is to add an inductor at the AC-side of the diode bridge, in series with the line voltage as shown in Fig. 2.2a), and to create circuit conditions such that the line current is zero during the zero-crossings of the line voltage [Moh95, pp. 91-94]. The maximum power factor that can be obtained is $PF = 0.76$, with the theoretical assumption of constant DC output voltage. We should note here that in reality, as explained later on in this chapter, the DC output voltage of the PFC circuit has ripple at twice the line-frequency, ripple that is also dependent on the load current. Simulated results for the rectifier with AC-side inductor are presented in Fig. 2.2b), where the inductance L_a has been chosen so as to maximize the power factor.



a) b)

Fig. 2.2 Rectifier with AC-side inductor: a) Schematic; b) Line voltage and line current with $V_1 = 230\text{V}_{\text{rms}}$, resistive load $R = 500\Omega$, $C_f = 470\mu\text{F}$, and $L_a = 130\text{mH}$. The line current has $K_p = 0.888$, $\cos\varphi = 0.855$ and $PF = 0.759$. The output voltage is $V_2 = 257\text{V}$.

The inductor can be also placed at the DC-side, as shown in Fig. 2.3a) [Dew81], [Kel92]. The inductor current is continuous for a large enough inductance L_d. In the theoretical case of near-infinite inductance, the inductor current is constant, so the input current of the rectifier has a square shape and the power factor is $PF = 0.9$. However, operation close to this condition would require a very large and impractical inductor, as illustrated by the simulated line current waveform for $L_d = 1\text{H}$ (without C_a), shown in Fig. 2.3b). For lower inductance L_d, the inductor current becomes discontinuous. The maximum power factor that can be obtained in such a case is $PF = 0.76$, the operating mode being identical to the case of the AC-side inductor previously discussed. An improvement of the power factor can be obtained by adding the capacitor C_a as shown in Fig. 2.3a), which compensates for the displacement factor $\cos\varphi$. A design for maximum purity factor K_p and unity displacement factor $\cos\varphi$ is possible, leading to a maximum obtainable power factor $PF = 0.905$ [Kel89]. This is exemplified by the simulated line current for $L_d = 275\text{mH}$ and $C_a = 4.8\mu\text{F}$, which is shown in Fig. 2.3b).

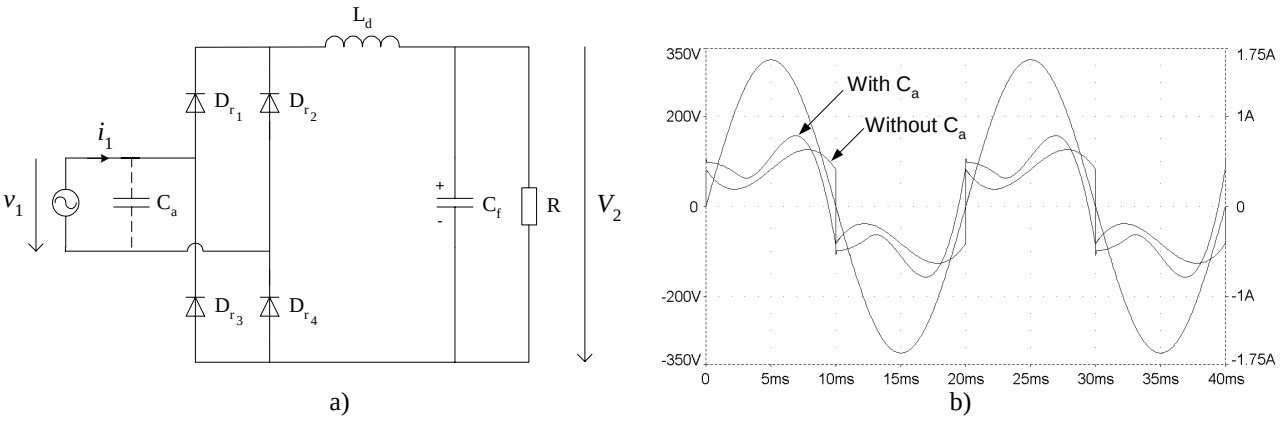


Fig. 2.3 Rectifier with DC-side inductor: a) Schematic; b) Line voltage and line current with $V_1 = 230\text{V}_{\text{rms}}$, resistive load $R = 500\Omega$, and $C_f = 470\mu\text{F}$. With $L_d = 1\text{H}$ and without C_a, the line current has $K_p = 0.897$, $\cos\varphi = 0.935$ and $PF = 0.839$, and the output voltage is $V_2 = 205\text{V}$. With $L_d = 275\text{mH}$ and with $C_a = 4.8\mu\text{F}$, the line current has $K_p = 0.905$, $\cos\varphi = 0.999$ and $PF = 0.904$, and the output voltage is $V_2 = 232\text{V}$.

The shape of the line current can be further improved by using a combination of low-pass input and output filters [Moh95, pp. 488-489]. There are also several solutions based on resonant networks which are used to attenuate harmonics. For example, a band-pass filter of the series-resonant type, tuned at the line-frequency, is introduced in-between the AC source and the load, as

shown in Fig. 2.4 together with simulated waveforms. For 50/60Hz networks, large values of the reactive elements are needed. Therefore, this solution is more practical for higher frequencies, such as for 400Hz and especially 20kHz networks [Vor90a].

The solution using a band-stop filter of the parallel-resonant type [Pra90] is presented in Fig. 2.5 together with simulated waveforms. The filter is tuned at the third harmonic, hence it allows for lower values of the reactive elements when compared to the series-resonant band-pass filter.

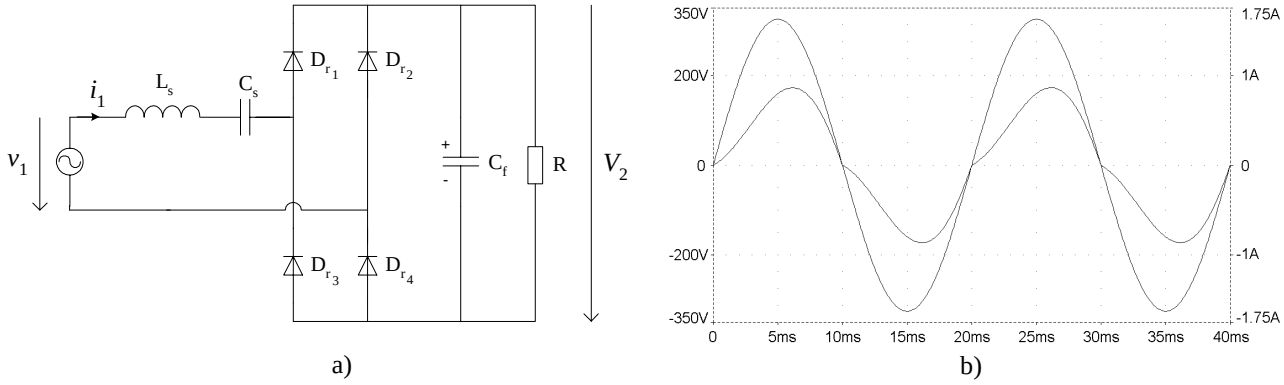


Fig. 2.4 Rectifier with series-resonant band-pass filter: a) Schematic; b) Line voltage and line current with $V_1 = 230\text{V}_{\text{rms}}$, resistive load $R = 500\Omega$, $C_\text{f} = 470\mu\text{F}$, $L_\text{s} = 1.5\text{H}$ and $C_\text{s} = 6.75\mu\text{F}$. The line current has $K_\text{p} = 0.993$, $\cos\varphi = 0.976$ and $PF = 0.969$. The output voltage is $V_2 = 254\text{V}$.

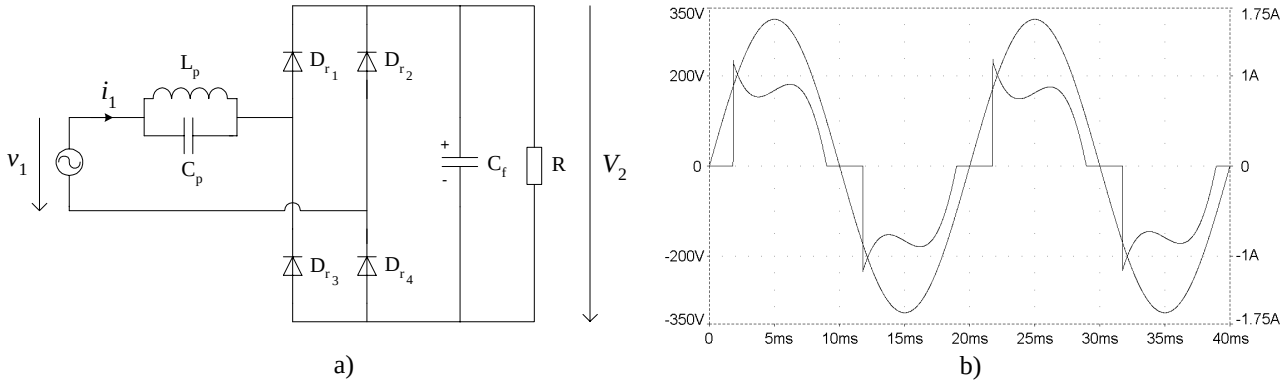


Fig. 2.5 Rectifier with parallel-resonant band-stop filter: a) Schematic; b) Line voltage and line current with $V_1 = 230\text{V}_{\text{rms}}$, resistive load $R = 500\Omega$, $C_\text{f} = 470\mu\text{F}$, $L_\text{p} = 240\text{mH}$ and $C_\text{p} = 4.7\mu\text{F}$. The line current has $K_\text{p} = 0.919$, $\cos\varphi = 0.999$ and $PF = 0.918$. The output voltage is $V_2 = 266\text{V}$.

Another possibility is to use a harmonic trap filter. The harmonic trap consists of a series-resonant network, connected in parallel to the AC source and tuned at a harmonic that must be attenuated [Eri97, pp. 575-582]. For example, the filter shown in Fig. 2.6a)-b) has two harmonic traps, which are tuned at the 3rd and 5th harmonic, respectively, as shown in Fig. 2.6c). As seen from Fig. 2.6d), the line current improvement is very good, at the expense of increased circuit complexity. Harmonic traps can be used also in conjunction with other reactive networks, such as a band-stop filter [Red91].

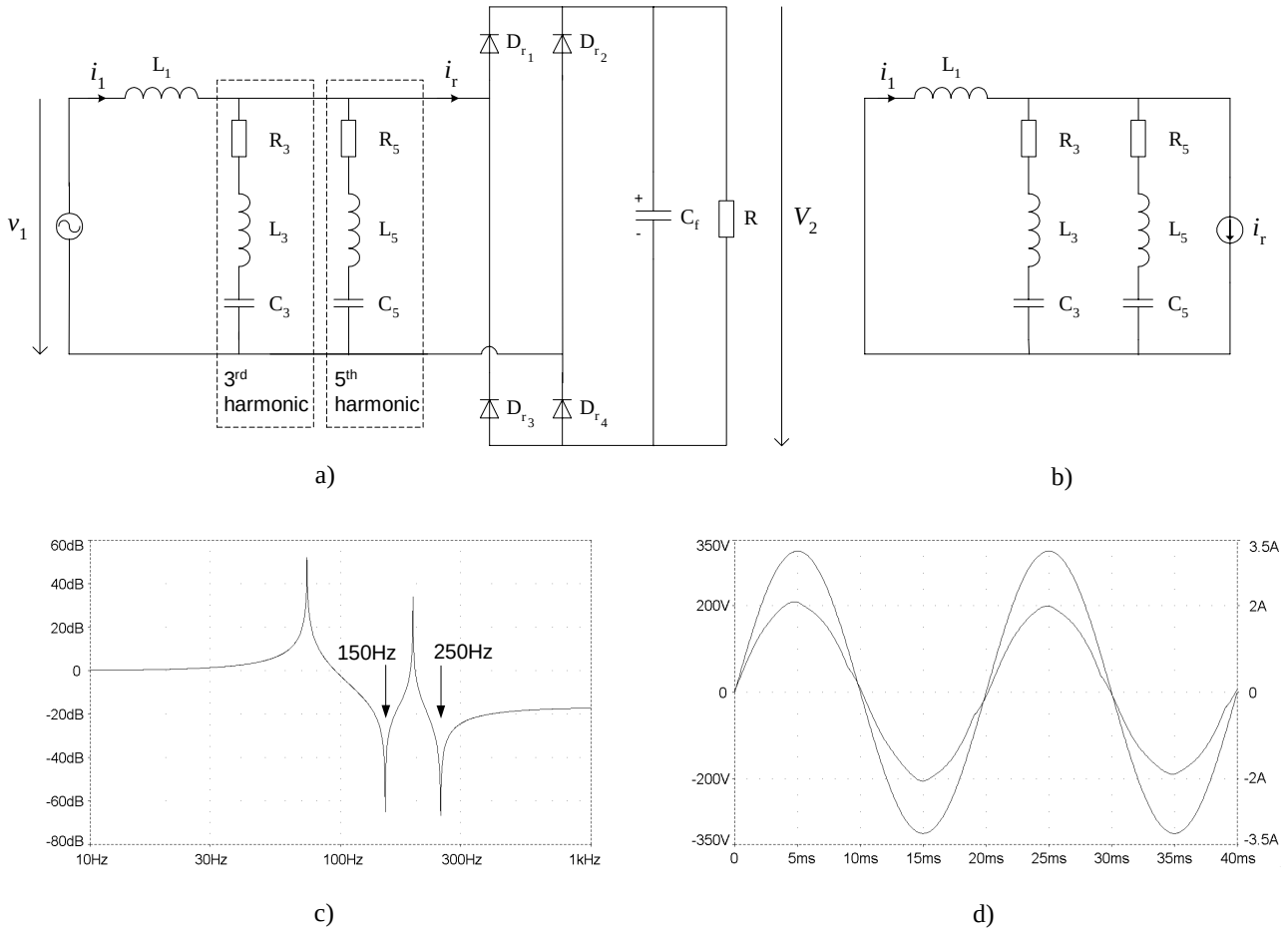


Fig. 2.6 Rectifier with harmonic trap filter: a) Schematic; b) Simulation circuit for the frequency response of the harmonic trap filter; c) Frequency response $\left|i_1(s)/i_r(s)\right|$ of the harmonic trap filter with $L_1 = 400\text{mH}$, $L_3 = 200\text{mH}$, $C_3 = 5.6\mu\text{F}$, $R_3 = 0.1\Omega$, $L_5 = 100\text{mH}$, $C_5 = 4.04\mu\text{F}$, and $R_5 = 0.1\Omega$; d) Line voltage and line current with $V_1 = 230\text{V}_{\text{rms}}$, resistive load $R = 500\Omega$, $C_f = 470\mu\text{F}$, and filter values from c). The line current has $K_p = 0.999$, $\cos\varphi = 0.999$ and $PF = 0.998$. The output voltage is $V_2 = 395\text{V}$.

The capacitor-fed rectifier, shown in Fig. 2.7 together with simulated waveforms, is a very simple circuit that ensures compliance with standard IEC 1000-3-2 for up to approximately 250W input power at a $230V_{rms}$ line voltage. The conversion ratio is a function of X_a/R, where $X_a = 1/(\omega_L C_a)$. Therefore, it is possible to obtain a specific output voltage, which is nevertheless lower than the amplitude of the line voltage and strongly dependent on the load. Despite the harmonic current reduction, the power factor is extremely low. This is not due to current harmonics, but to the series-connected capacitor that introduces a leading displacement factor $\cos\varphi$. An advantage could be that the leading displacement factor $\cos\varphi$ can assist in compensating for lagging displacement factors elsewhere [Sok98].

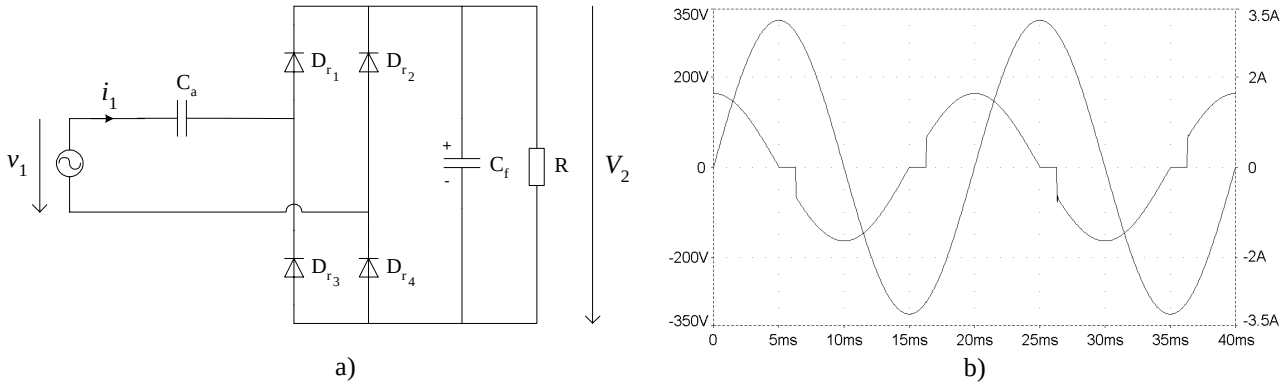


Fig. 2.7 Capacitor-fed rectifier: a) Schematic; b) Line voltage and line current with $V_1 = 230V_{rms}$, resistive load $R = 500\Omega$, $C_f = 4700\mu F$, and $C_a = 16\mu F$. The line current has $K_p = 0.995$, $\cos\varphi = 0.052$ and $PF = 0.0517$. The output voltage is $V_2 = 12V$.

The rectifier with an additional inductor, capacitor, and diode – LCD rectifier – is shown in Fig. 2.8, together with simulated waveforms. The added reactive elements have relatively low values. The idea behind the circuit is linked to the previous definition of Class D of the IEC 1000-3-2 standard, which was based on the envelope shown in Fig. 1.2. The circuit changes the shape of the input current and, while only a limited reduction of the harmonic currents can be obtained, it was also possible to change the classification of the circuit from Class D to Class A. The power-related limits of Class D were avoided and the absolute limits of Class A could be met for low power, in spite of the line current being relatively distorted [Red98]. However, as presented in Chapter 1, the definition of Class D has been changed and techniques aiming at changing the classification of equipment from Class D to Class A have lost their applicability.

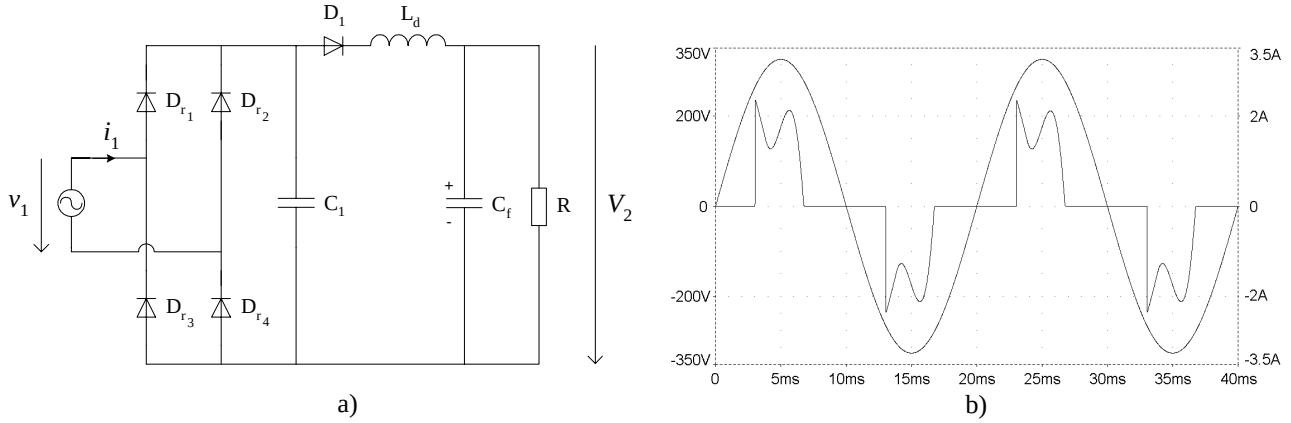


Fig. 2.8 Rectifier with an additional inductor, capacitor and diode (LCD): a) Schematic; b) Line voltage and line current with $V_1 = 230\text{V}_{\text{rms}}$, resistive load $R = 500\Omega$, $C_{\text{f}} = 470\mu\text{F}$, $C_1 = 40\mu\text{F}$, and $L_{\text{d}} = 10\text{mH}$. The line current has $K_{\text{p}} = 0.794$, $\cos\varphi = 0.998$ and $PF = 0.792$. The output voltage is $V_2 = 304\text{V}$.

Finally, the valley-fill rectifier is shown in Fig. 2.9, together with simulated waveforms [Spa91], [Kit98]. The circuit reduces the harmonic content of the line current but the output voltage has a large variation and the load of the rectifier must be able to tolerate it.

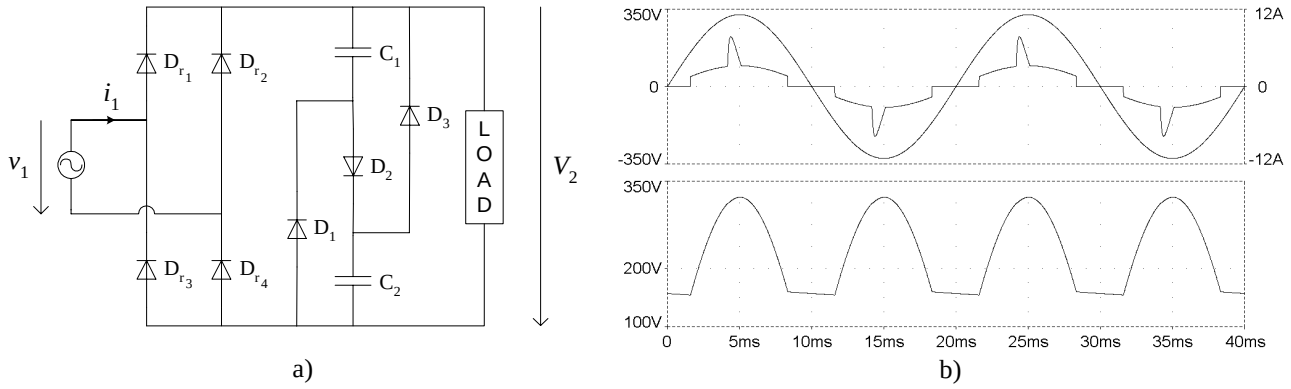


Fig. 2.9 Valley-fill rectifier: a) Schematic; b) Line voltage and line current (upper plot), and output voltage (lower plot), with $V_1 = 230\text{V}_{\text{rms}}$, constant power load $P = 200\text{W}$, and $C_1 = C_2 = 470\mu\text{F}$. The line current has $K_{\text{p}} = 0.921$, $\cos\varphi = 0.999$ and $PF = 0.920$. The output voltage ripple is $\Delta V_2 = 168\text{V}$.

Passive power factor correctors have certain advantages, such as simplicity, reliability and ruggedness, insensitivity to noise and surges, no generation of high-frequency EMI and no high-frequency switching losses. On the other hand, they also have several drawbacks. Solutions based on filters are heavy and bulky, because line-frequency reactive components are used. They also

have poor dynamic response, lack voltage regulation and the shape of their input current depends on the load. Even though line current harmonics are reduced, the fundamental component may show an excessive phase shift that reduces the power factor. Moreover, circuits based on resonant networks are sensitive to the line-frequency. In harmonic trap filters, series-resonance is used to attenuate a specific harmonic. However, parallel-resonance at different frequencies occurs too, which can amplify other harmonics [Eri97, pp. 575-582].

Better characteristics are obtained with active PFC circuits, which are reviewed in the following two subchapters.

2.2 Low-frequency active PFC

Three representative solutions are presented in Fig. 2.10. The phase-controlled rectifier is shown in Fig. 2.10a), and its control signals in Fig. 2.10b). It is derived from the rectifier with a DC-side inductor from Fig. 2.3, where diodes are replaced with thyristors. According to [Kel90], depending on the inductance L_d and the firing-angle α, a near-unity purity factor K_p *or* displacement factor $\cos\varphi$ can be obtained. However, the overall power factor PF is always less than 0.9. In [Kel91], the inductance L_d and firing angle α are chosen to maximize K_p. This implies a lagging displacement factor $\cos\varphi$ that is compensated for by an additional input capacitance C_a. This approach is similar to that used in [Kel89] for the diode bridge rectifier with a DC-side inductor, and discussed in the previous subchapter. This solution offers controllable output voltage, is simple, reliable, and uses low-cost thyristors. On the negative side, the output voltage regulation is slow and a relatively large inductance L_d is still required.

Second-order switching converters are introduced in the next subchapter, as they are mainly used at high switching frequencies. However, it is also possible to use them at low switching frequencies, as explained next. The low-frequency switching Boost converter is shown in Fig. 2.10c). The active switch S is turned on for the duration T_{on}, as illustrated in Fig. 2.10d), so as to enlarge the conduction interval of the rectifier diodes [Zuc97]. It is also possible to have multiple switchings per half line-cycle, at low switching frequency, in order to improve the shape of the line current [Red91]. Nevertheless, the line current has a considerable ripple.

The low-frequency switching Buck converter is shown in Fig. 2.10e) [Red91]. Theoretically, the inductor current is constant for a near-infinite inductance L_d. The switch is turned on for the duration T_{on} and the on-time intervals are symmetrical with respect to the zero-crossings of the line voltage, as illustrated in Fig. 2.10f). The line current is square with adjustable duty-cycle. For a

lower harmonic content of the line current, multiple switchings per line-cycle can be used. However, the required inductance L_d is large and impractical.

To conclude, low-frequency switching PFC offers the possibility to control the output voltage in certain limits. In such circuits, switching losses and high-frequency EMI are negligible. However, the reactive elements are large and the regulation of the output voltage is slow.

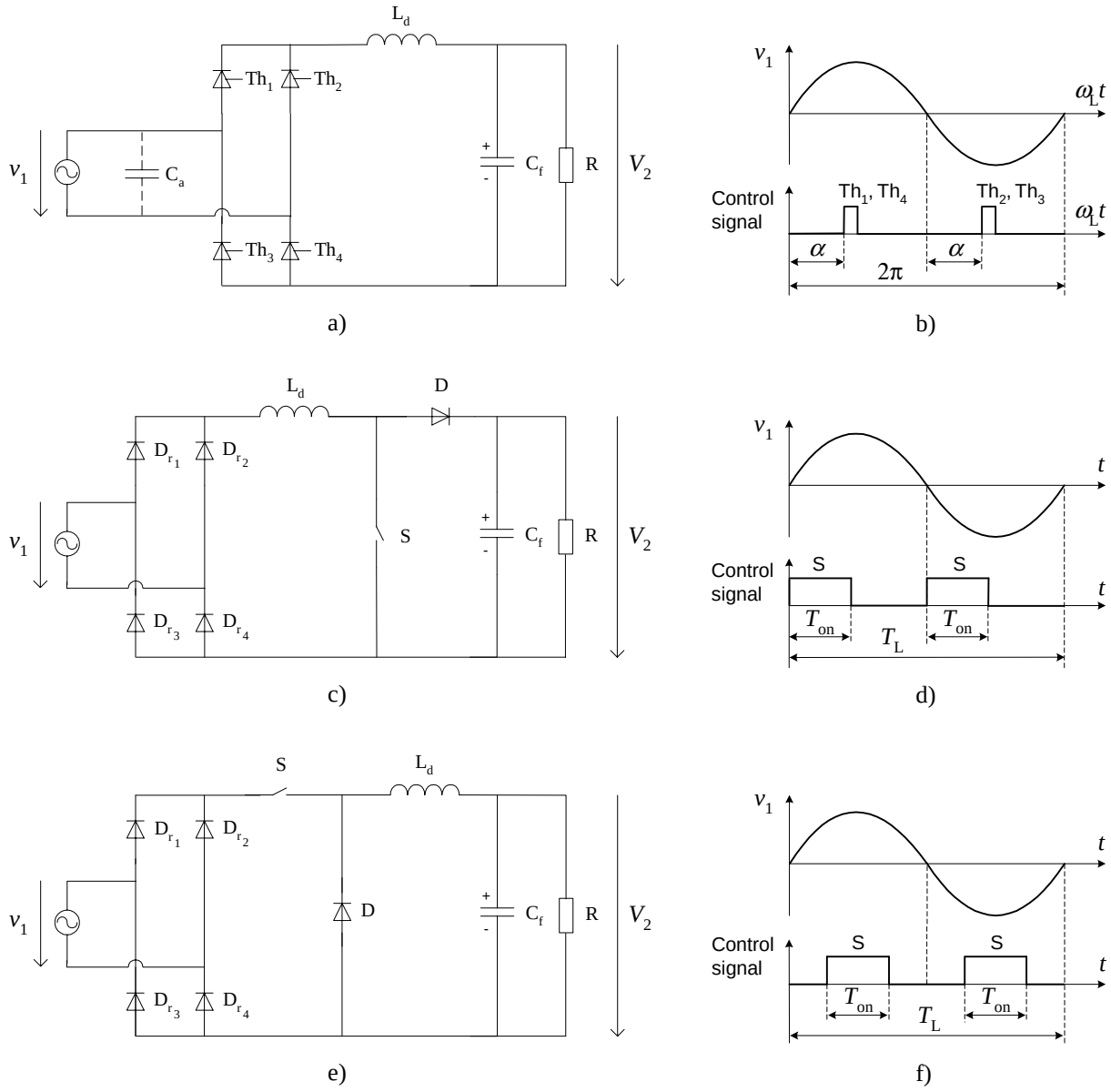


Fig. 2.10 Low-frequency active PFC: a) Controlled rectifier with DC-side inductor, with b) phase-control; c) Boost converter, with d) one commutation per half line-cycle; e) Buck converter, with f) one commutation per half line-cycle.

2.3 High-frequency active PFC

The PFC stage can be realized by using a diode bridge and a DC/DC converter with a switching frequency much higher than the line-frequency. In principle, any DC/DC converter can be used for this purpose, if a suitable control method is used to shape its input current or if it has inherent PFC properties. Regardless of the particular converter topology that is used, the output voltage carries a ripple on twice the line-frequency. This is because, on the one hand, in a single-phase system the available instantaneous power varies from zero to a maximum, due to the sinusoidal variation of the line voltage. On the other hand, the load power is assumed to be constant. The output capacitor of the PFC stage buffers the difference between the instantaneous available and consumed power, hence the low-frequency ripple. Next, we present the application of second-order switching converters for PFC.

2.3.1 Second-order switching converters applied to PFC

The first-order switching cell is shown in Fig. 2.11a). The active switch S is controlled by an external control input. In a practical realization, this switch would be implemented, for example, by a MOSFET or an IGBT. The state of the second switch, which is diode D, is indirectly controlled by the state of the active switch and other circuit conditions. The switching cell also contains a storage element, which is the inductor L.

The basic Buck, Boost and Buck-Boost converters are generated from this switching cell, as shown in Fig. 2.11b), d) and f), respectively. Considering also the output filtering capacitor, they are second-order circuits. The output filtering capacitor can be assimilated to a voltage source. Hence, the ports of the switching cell are connected to voltage sources, a fact which explains why the storage element of the switching cell is an inductor and not a capacitor.

The converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle, or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle. There are specific characteristics associated with these operating modes, which determine the method used to shape the input current in a PFC application. These operating mode-specific characteristics are described in Subsections 2.3.2 and 2.3.3. However, first let us describe three characteristics that are important for a PFC application, which are dependent mainly on the specific topology rather than on the operating mode.

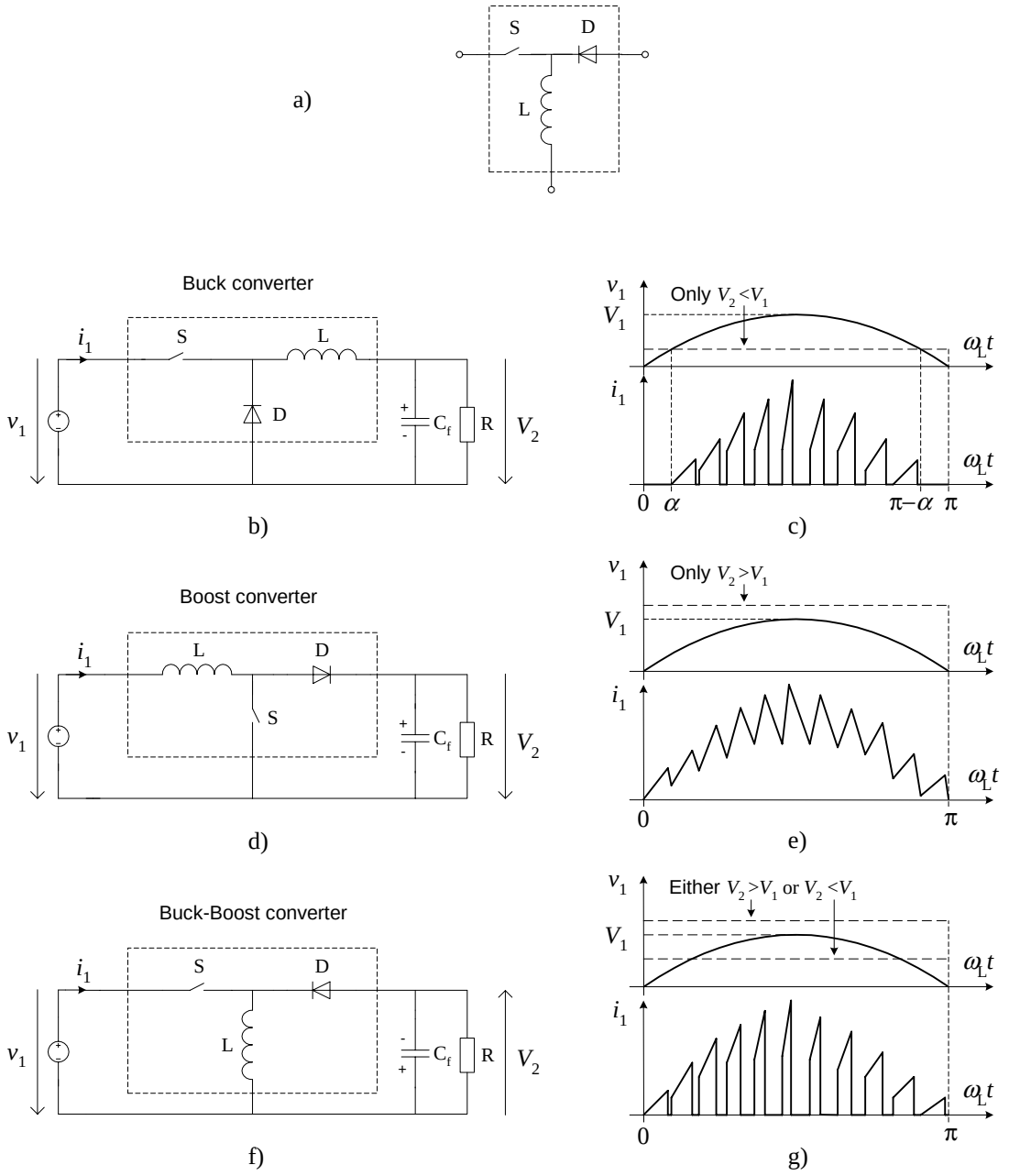


Fig. 2.11 Second-order switching converters and their application for high-frequency active PFC, assuming operation in CICM: a) First-order switching cell, from which second-order switching converter are generated; b) Buck converter, with c) waveforms; d) Boost converter, with e) waveforms; f) Buck-Boost converter, with g) waveforms.

In a PFC application, the input voltage is the rectified line voltage $v_1(t) = V_1 \cdot |\sin \omega_L t|$. The output voltage V_2 is assumed to be constant. The first characteristic, which is determined by the conversion ratio of the converter, is the relation between the obtainable output voltage V_2 and the amplitude V_1 of the sinusoidal input voltage.

The second characteristic refers to the shape of the filtered (line-frequency) input current. If the converter is able to operate throughout the entire line-cycle, a sinusoidal line current can be obtained. Otherwise the line current is distorted, being zero in a region around the zero-crossings of the line voltage where the converter cannot operate.

The third characteristic is related to the high-frequency content of the input current. We consider that the input current is continuous if it is not interrupted by a switching action. This means that the inductor is placed in series at the input and only the inductor current ripple determines the high-frequency content of the input current. For CICM operation, the inductor current ripple can be relatively low, a situation in which the input current has a reduced high-frequency content. Conversely, the input current is discontinuous if it is periodically interrupted by the switching action of a switch placed in series at the input. In such a case, the high-frequency content of the input current is large, even in CICM operation. The terms continuous/discontinuous input current should not be confused with CICM/DICM, which refer to the inductor current.

We now briefly characterize second-order converters in the light of these topology-specific characteristics. The converters are shown in Fig. 2.11 together with waveforms relevant for a PFC application, assuming operation in CICM. We need to clarify here that the given waveforms are only for supporting the explanation of the topology-specific characteristics. In reality, the switching frequency is much higher than the line-frequency and the input current waveform is dependent also on the type of control that is used.

The Buck converter, shown in Fig. 2.11b), has step-down conversion ratio. Therefore, it is possible to obtain an output voltage V_2 lower than the amplitude V_1 of the input voltage. However, the converter can operate only when the instantaneous input voltage v_1 is higher than the output voltage V_2, i.e. only during the interval $\omega_L t \in (\alpha, \pi - \alpha)$, where $\alpha = \arcsin(V_2/V_1)$. Hence, the line current of a power factor corrector based on a Buck converter has crossover distortions, as illustrated in Fig. 2.11c). Moreover, the input current of the converter is discontinuous. Consequently, even in CICM, the input current has a significant high-frequency component that has to be filtered out. Some PFC applications based on this topology are reported in [End92] and [Spi97].

The Boost converter is shown in Fig. 2.11d). It has a step-up conversion ratio; hence the output voltage V_2 is always higher than the amplitude V_1 of the input voltage. Operation is possible throughout the line-cycle so the input current does not have crossover distortions. As illustrated in Fig. 2.11e), the input current is continuous, because the inductor is placed in series at the input.

Hence, an input current with reduced high-frequency content can be obtained when operating in CICM. For these reasons, the Boost converter operating in CICM is widely used for PFC [Eri97, pp. 24-29, pp. 627-645].

The Buck-Boost converter, shown in Fig. 2.11f), can operate either as a step-down or a step-up converter. This means that the output voltage V_2 can be higher or lower than the amplitude V_1 of the input voltage, which gives freedom in specifying the output voltage. Operation is possible throughout the line-cycle and a sinusoidal line current can be obtained. However, the output voltage is inverted, which translates into higher voltage stress for the switch. Moreover, similar to the Buck converter, the input current is discontinuous with significant high-frequency content, as illustrated in Fig. 2.11g). The topology-specific characteristics are summarized in Table 2.1.

In addition to these basic converters, the two-switch Buck + Boost converter [Gha93], [Eri97, pp. 149] is an interesting solution. It operates as a Buck converter when the input voltage is higher than the output voltage and as a Boost converter when the input voltage is lower than the output voltage. Therefore, operation is possible throughout the line-cycle and the output voltage can be varied in a wide range, in a similar manner to the Buck-Boost converter. Another positive aspect is that, due to its non-inverted output voltage, the voltage stress of the switches is lower than in a Buck-Boost converter. However, this topology has an increased number of switches which leads to higher cost and conduction losses.

Table 2.1. Topology-specific characteristics.

	Conversion characteristic	**Crossover distortions**	**Input current**
Buck	Step-down, $V_2 < V_1$	Yes, because operation is possible only for $\omega_L t \in (\alpha, \pi - \alpha)$, $\alpha = \arcsin \frac{V_2}{V_1}$	Discontinuous
Boost	Step-up, $V_2 > V_1$	No	Continuous
Buck-Boost	Step-down/up $V_2 \gtrless V_1$	No	Discontinuous

Having examined characteristics that are determined mainly by the topology, we describe next characteristics that are determined by the operating mode.

2.3.2 Operation in Continuous Inductor Current Mode - CICM

In this operating mode, the inductor current never reaches zero during one switching cycle and there is always energy stored in the inductor. The *volt·seconds* applied to the inductor must be balanced throughout the line-cycle by continuously changing the duty-cycle of the converter using an appropriate control method.

An example of a control scheme is shown in Fig. 2.12. The low-bandwidth outer loop with characteristic $G_{\mathrm{L}}(s)$ is used to keep the output voltage of the PFC stage constant and to provide the error signal v_{ε}. The high-bandwidth inner loop with characteristic $G_{\mathrm{H}}(s)$ is used to control the input current. A multiplier is used to provide a reference v_{xy}, which is proportional to the error signal v_{ε} and which has a modulating signal with the desired shape for the input current. Fig. 2.12 shows the most common situation, where the modulating signal is the rectified-sinusoid input voltage $|v_1|$. Depending on the topology of the PFC stage, it may be beneficial to use as a modulating signal the difference between the input voltage and the output voltage [Red92a].

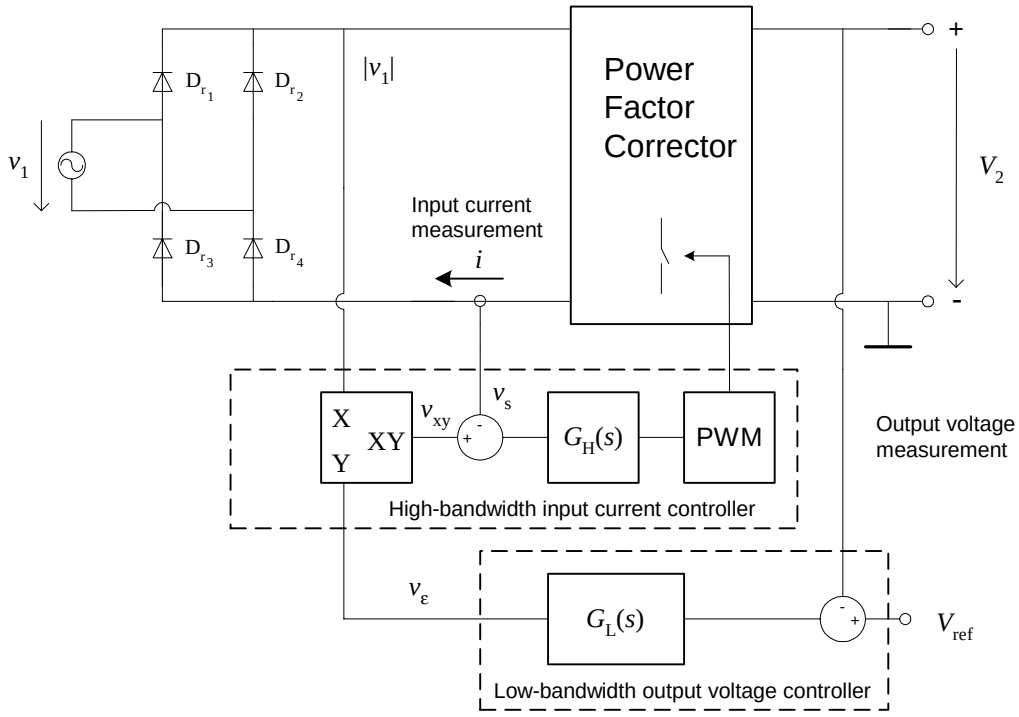


Fig. 2.12 Example of the control scheme for PFC using a switching converter operating in CICM.

The control circuit can be simplified by eliminating the multiplier and the sensing of the line voltage. In this case the modulating signal is $v_{xy} = v_{\varepsilon}$, and it is essentially constant over the line-cycle, because v_{ε} is the control signal from the low-bandwidth output voltage controller. Therefore, the input current is clamped to a value proportional with v_{ε} and its shape approaches a square waveform. The simplification of the control circuit leads to a more distorted line current, but compliance with the standard can be obtained up to approximately 500W for a $230V_{rms}$ input voltage. Furthermore, if the edges of the line current waveform are softened, thus obtaining a nearly trapezoidal waveform, compliance up to several kW can be obtained [Red96b].

There are several ways to implement the high-bandwidth inner loop [Eri97, pp. 636-639]. In peak current mode control, well-known from DC/DC converters, the active switch is turned on with constant switching frequency, and turned off when the upslope of the inductor current reaches a level set by the outer loop. This gives instant over-current switch protection, but also makes the control very sensitive to noise. Moreover, the control is inherently unstable at duty-cycles exceeding 0.5; a compensating ramp must be added to the inductor ramp to solve this problem. Finally, in peak current mode control there is an inherent peak to average current error. Consequently, the average inductor current cannot follow accurately the current reference signal set by the outer loop. In a Boost-based PFC converter with sinusoidal reference, this leads to crossover distortions and line current harmonics [Red94b]. However, if the simplicity of the control circuit is of primary interest, rather than the quality of the line current waveform, then peak current mode control with input current clamping is attractive [Mak95], [Can96].

A better control method is the average current mode control, where the average of the inductor current, instead of the peak, is compared to the current program level. This offers better noise rejection and stability, when compared to peak current mode control. Because the average of the current is controlled, a line current waveform of a very good quality can be obtained. Consequently, average current mode control is widely used in PFC applications [Dix90a], [Dix90b]. Its implementation is somewhat more complicated when compared with that of the peak current mode control, because an additional operational amplifier is needed in the current loop.

Yet another method is hysteretic control, where the inductor current is kept within a regulation band [Zho90]. Its main advantage is its simple implementation. However, the variable switching frequency associated with it is a drawback.

Finally, charge nonlinear carrier control is an approach where the integral of the current through the switch is compared with a nonlinear carrier voltage generated by the controller.

Alternatively, the peak of the switch current is used for comparison in peak current nonlinear carrier control, which has nevertheless higher noise sensitivity. These methods offer the advantage of eliminating the multiplier from the control circuit, and the need for sensing the sinusoidal input voltage. Furthermore, no operational amplifier is needed in the current loop. However, the nonlinear carrier is obtained assuming that the controlled converter operates in CICM, which explains the main drawback of the method: the line current is distorted in DICM operation, i.e. at light load and around the zero-crossings of the line voltage [Mak96].

2.3.3 Operation in Discontinuous Inductor Current Mode - DICM

In this operating mode, for second-order converters shown in Fig. 2.13a), the inductor current i_L varies from zero to a maximum and returns back to zero before the beginning of the next switching cycle, as presented in Fig. 2.13b).

Throughout this dissertation, we will use the term 'input resistance' r_1 of a switching converter to refer to the average input resistance calculated as the ratio of the average input voltage and the average input current, over one switching cycle T_s. The input voltage v_1 can be considered to be constant during one switching period T_s, because the switching frequency is much higher than the line-frequency. Hence, as depicted in Fig. 2.13a), the input resistance of the analyzed converters can be defined as:

$$r_1(t) = \frac{v_1(t)}{\langle i_1(t) \rangle_{T_s}}, \tag{2.1}$$

where $\langle i_1(t) \rangle_{T_s}$ is the average of the input current i_1 over one switching period T_s [Eri97, pp. 370-381]. Based on the operating principle of the converters and on the waveforms shown in Fig. 2.13b), as well as assuming a rectified-sinusoid input voltage v_1, it is straightforward to calculate the expressions $r_1(t)$ of the input resistance that are presented in Table 2.2.

The input resistance of the Buck-Boost converter depends only on inductance L, switching period T_s and duty-cycle d. If operation in DICM is ensured throughout the line-cycle and if d is kept constant, then the input resistance r_1 is constant. As a consequence, the average input current $\langle i_1(t) \rangle_{T_s}$ tracks the shape of the input voltage and the converter has an *inherent* PFC property. In contrast to CICM operation, in DICM there is no need for the controller to adjust the duty-cycle over the line-cycle to perform PFC.

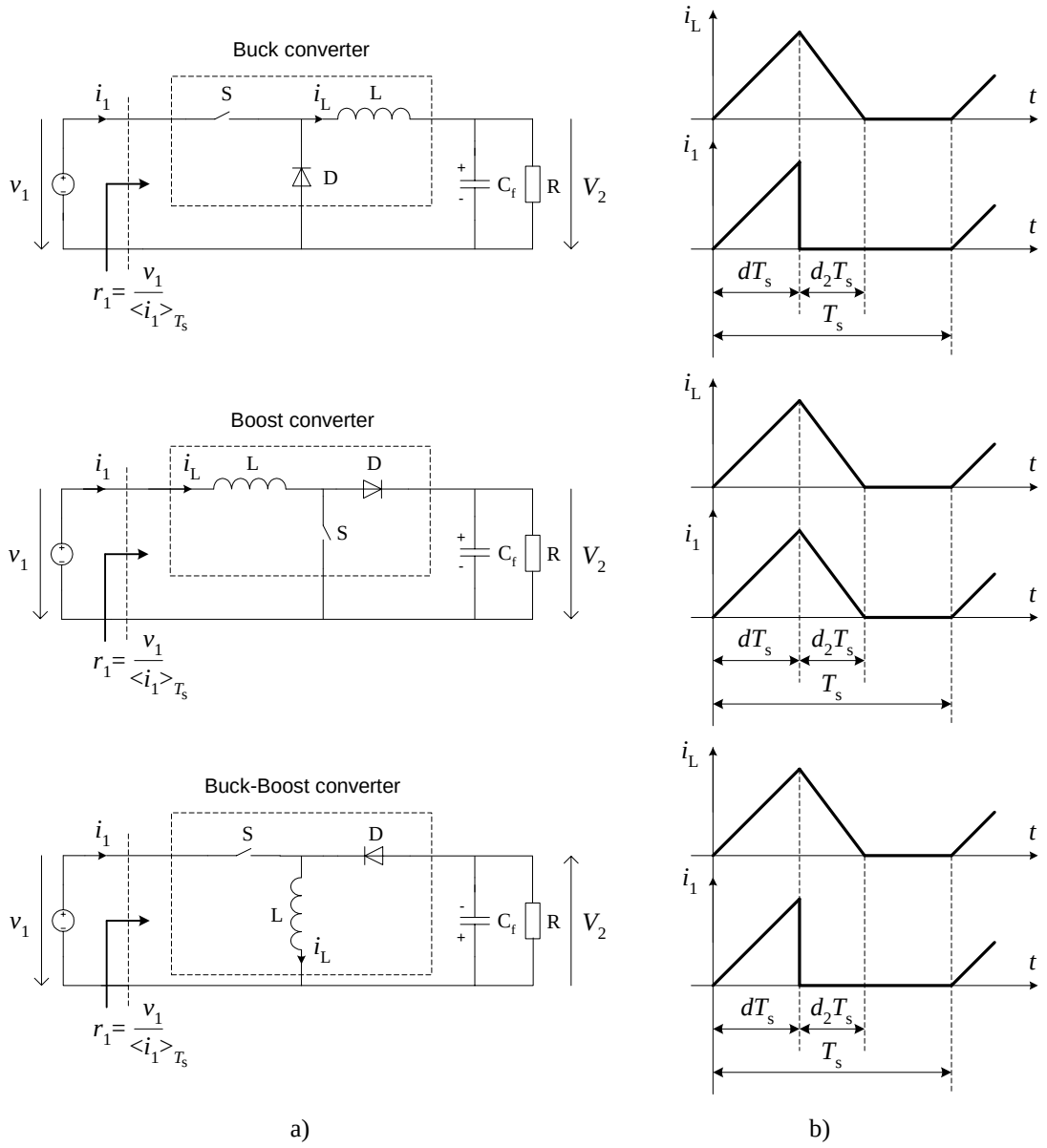


Fig. 2.13 Second-order switching converters: a) Definition of the input resistance $r_1(t)$; b) The inductor current $i_L(t)$ and the input current $i_1(t)$, when operating in DICM.

As can be seen in Table 2.2, the input resistance of the Buck converter is not constant throughout the line-cycle. However, its variation decreases and inherent PFC property improves, when the ratio V_2/V_1 is decreased. As explained previously, the line current has crossover distortions too, which are however less disturbing when the ratio V_2/V_1 is decreased. However, compliance with standard IEC 1000-3-2 can be obtained up to a relatively high power, when the output voltage V_2 is low enough when compared to the amplitude V_1 of the sinusoidal input voltage [Spi97].

Table 2.2. Inherent PFC properties of second-order switching converters operating in DICM.

	Input resistance $r_1(t)$	**Inherent PFC**
Buck	$r_1(t)=\frac{2L}{d^2T_s}\left(\frac{1}{1-\frac{V_2}{V_1\sin\omega_L t}}\right),\ \omega_L t\in(\alpha,\pi\text{-}\alpha),\ \alpha=\arcsin\frac{V_2}{V_1}$	**Fair** Improves when V_2/V_1 is decreased
Boost	$r_1(t)=\frac{2L}{d^2T_s}\left(1-\frac{V_1\sin\omega_L t}{V_2}\right),\ \omega_L t\in(0,\pi)$	**Fair** Improves when V_2/V_1 is increased
Buck-Boost	$r_1(t)=\frac{2L}{d^2T_s},\ \omega_L t\in(0,\pi)$	**Excellent**

The Boost converter has an imperfect inherent PFC property, as well. Its input resistance changes throughout the line-cycle, but the variation decreases and inherent PFC property improves when the ratio V_2/V_1 is increased. Taking into account the fact that the line current does not have crossover distortions, compliance with the standard is achieved comfortably.

The inherent PFC property of second-order switching converters operating in DICM can be explained by the fact that the *volt·seconds* applied to the inductor are inherently balanced every switching cycle, so the duty-cycle d can be kept constant. The excellent inherent PFC property of the Buck-Boost converter is explained by the very good control of the quantity of energy that is transferred in each switching cycle from input to output. During the on-time of the active switch, energy is transferred only from the input voltage source to the inductor. During the off-time of the active switch, there is only energy transfer from the inductor to the output, until the energy stored in inductor is depleted. The quantity of energy transferred during each switching cycle depends only on the input voltage v_1 and the input resistance r_1. In the Buck converter there is as well a 'parasitic' transfer of energy from input to output, during the on-time of the active switch. Likewise, in the Boost converter there is a 'parasitic' transfer of energy from input to output during the off-time of the active switch. This 'parasitic' transfer is dependent on the V_2/V_1 ratio, which explains the degradation of the inherent PFC property in these converters.

The main advantage of using switching converters operating in DICM for PFC applications is the simplicity of the control method. Since there is no need to continuously adjust the duty-cycle d to perform PFC, only a voltage loop is needed to regulate the voltage across the storage capacitor. The bandwidth of the voltage loop has to be low (e.g. 10-15Hz), in order to filter out the output voltage ripple at twice the line-frequency. The simple control of converters with inherent PFC makes them attractive for low-cost applications. They can be used in a power conversion chain as shown in Fig. 1.3 or as stand-alone converters, if their low-frequency output voltage ripple can be tolerated. In the latter case, the Flyback converter, which offers isolation and is functionally equivalent to the Buck-Boost converter, is often used [Tan93].

Besides these applications, converters with inherent PFC are essential for integrating the PFC stage with the output voltage regulation stage into a so-called *single-stage* converter. An example is the BIFRED converter (Boost Integrated with Flyback Rectifier/Energy storage/DC-DC converter) [Mad92], which is shown in Fig. 2.14. The input stage is a Boost converter operating in DICM for PFC, and the output stage is a Flyback converter for output voltage regulation. The active switch is shared by the two stages. Capacitor C is the energy storage capacitor and sees the low-frequency (e.g. 100Hz) and the high-frequency switching ripple, while C_f is the output capacitor seeing only the high-frequency switching ripple. This is potentially a low-cost solution, since there is only one switch and one control circuit. However, DICM operation translates into a high peak current through the switch, which has a negative impact on efficiency. As a consequence, the concept is advantageous only for low power applications, for example up to a few hundred watts, when compared to the two-stage approach. Several single-stage converters have been developed based on similar principles. For example, a Boost input stage is used in [Tak91], [Red94c] and [Hub97], while [Oba98] uses a Buck-Boost input stage.

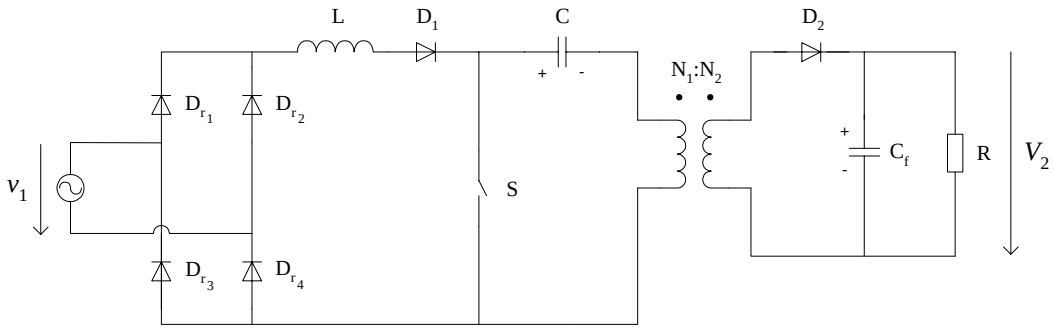


Fig. 2.14 Example of a single-stage converter with PFC: the BIFRED converter.

2.3.4 EMI filter requirements

The high-frequency ripple of the input current of switching converters generates differential-mode EMI, while the common-mode EMI is a result of secondary, usually parasitic, effects [Tih95, pp. 150]. Typically, the differential-mode EMI is dominant below 2MHz, while the common-mode EMI is dominant above 2MHz [Wu96]. In this dissertation, one important aspect when analyzing various converter topologies is the high-frequency ripple of the input current; hence, we only address the differential-mode EMI and the requirements for the input filter that are related to it.

A high-frequency active PFC stage significantly increases the differential-mode EMI, typically by 30dB to 60dB according to [Red96a], and an EMI filter must be used to comply with EMI standards. There are three main requirements concerning the design of the EMI filter for a PFC stage [Vla96]. To discuss them, let us consider a one-stage LC filter, as shown in Fig. 2.15a).

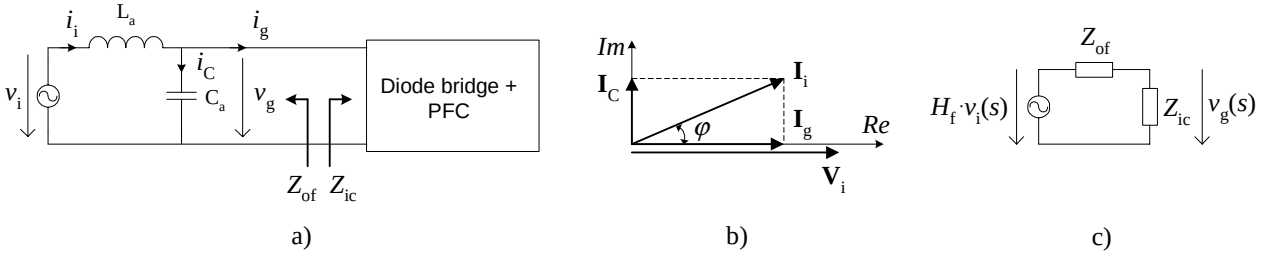


Fig. 2.15 One-stage LC filter for attenuating differential-mode EMI: a) Schematic; b) Phasor diagram of line-frequency components of the system currents and voltages; c) The Thévenin equivalent circuit.

The first requirement for the EMI filter is to provide the required attenuation, in order to ensure compliance with the EMI standards.

Fig. 2.15b) shows the phasor diagram of the line-frequency components of the system currents and voltages. We assume that the input current i_g of the PFC stage is sinusoidal and in phase with the input voltage v_g which, assuming that the voltage drop across the filter inductor L_a is very small at line-frequency, is essentially equal to the line voltage v_i. The capacitive current $\mathbf{I}_C$, which is proportional to C_a, introduces a displacement angle φ between the line current $\mathbf{I}_i$ and the line voltage $\mathbf{V}_i$, which degrades the power factor.

This leads to the second requirement for the EMI filter: the displacement angle φ must be kept low. Hence, the capacitance C_a that can be used is upper limited

$$C_a < C_{max}, \tag{2.2}$$

where C_{max} is a function of the acceptable displacement factor $\cos\varphi$. As a consequence, the inductance L_a is lower limited

$$L_a > L_{min}, \tag{2.3}$$

in order to have a product $L_a C_a$ that gives the required attenuation.

The third requirement is related to the overall stability of the system. It is known that unstable operation may occur due to the interaction between the EMI filter and the power stage. This phenomenon is analyzed in several publications, including [Jan92] for peak current mode controlled DC/DC converters, and [Red92b] and [Spi99] for power factor correctors with average current mode control. To explain it, let us consider the Thévenin equivalent circuit shown in Fig. 2.15c), of the EMI filter/PFC stage interconnection from Fig. 2.15a). H_f is the transfer function of the filter, Z_{of} is the output impedance of the EMI filter and Z_{ic} is the input impedance of the PFC stage. From the equivalent circuit, we can write:

$$\frac{v_g(s)}{v_i(s)} = \frac{H_f(s)}{1+\dfrac{Z_{of}(s)}{Z_{ic}(s)}} = \frac{H_f(s)}{1+T_f(s)}, \tag{2.4}$$

where $T_f = Z_{of}/Z_{ic}$ can be considered as a loop gain that must satisfy the Nyquist criterion for stability. The interaction between the EMI filter and the power converter is minimized and no instabilities can arise in the system, if $|T_f| \ll 1$. This means that the modulus of the output impedance of the EMI filter must be much lower than the modulus of the input impedance of the power converter, $|Z_{of}| \ll |Z_{ic}|$. This criterion has been largely used especially for DC/DC converters [Mid76], [Mid78]. However, the aforementioned condition may be difficult to fulfill in a PFC application. This is because, at the resonant frequency of the EMI filter, the modulus of the output impedance $|Z_{of}|$ has a maximum that is proportional to $\sqrt{L_a/C_a}$, which cannot be set arbitrarily low since C_a is upper limited according to (2.2) and L_a is lower limited according to (2.3). Hence,

in a PFC application it is possible to have $|T_f| > 1$, especially at low $|Z_{ic}|$, i.e. at low line voltage and high load current. Therefore, if the input impedance Z_{ic} shows an excessive positive phase shift, then $T_f = Z_{of} / Z_{ic}$ may not satisfy the Nyquist criterion for stability and instabilities occur [Spi99]. For this reason, it is important to know the input impedance Z_{ic} of the PFC stage, in order to be able to perform the stability analysis. In publication [P1], we determine the input impedance of a PFC stage based on the Boost converter operating in DICM.

3 Fourth-Order Switching Converters

Several characteristics of second-order switching converters were discussed in the previous chapter, from the PFC application point of view. It is evident that topological and/or operating mode related properties impose some constraints when applying these topologies to PFC.

To begin with, it is not possible to have inherent PFC property and a reduced high-frequency content of the input current at the same time. Indeed, the inherent PFC property is obtained in DICM operation, which leads naturally to a significant high-frequency content of the input current that has to be filtered out. Moreover, high peak and RMS switch currents are associated with DICM operation, thus increasing the rating of the switches, as well as the conduction losses.

Secondly, an output voltage that is lower than the amplitude of the input voltage could be useful in some applications, but this characteristic cannot be associated with a reduced high-frequency content of the input current. On the one hand, Buck or Buck-Boost converters could be used to obtain a low output voltage, but their input current is naturally discontinuous. On the other hand, Boost converter operating in CICM would allow a reduced high-frequency content of the input current, but its output voltage is higher than the amplitude of the input voltage, typically 380-400V_{dc} for a PFC application with an universal input voltage of 90-265V_{rms}.

We conclude that input current with reduced high-frequency content, inherent PFC property and step-down conversion ratio are conflicting requirements in second-order converters. This fact constitutes the motivation for investigating the possibility of obtaining such characteristics using more complex converter topologies. Several DC/DC converter topologies are systematically generated in [Tym88], including converters with more than two switches and/or of higher order. Converters with more than two switches are not considered in this dissertation, because of the higher semiconductor component count and possibly increased control complexity. Therefore, two-switch converters of higher order are considered next.

Third-order converters could be obtained from second-order switching cells, which, in their turn, could be obtained by adding an inductor or a capacitor to the first-order switching cell shown in Fig. 2.11. However, it can be seen from Fig. 2.11 that the voltage applied at any of the switching cell's ports has a DC component. Therefore, an inductor cannot be added in parallel with any of these ports. It is not possible to add the inductor in series with one of the switches either, because there would be no path for the current to flow when the switch turns off. Finally, an inductor added

in the branch already containing inductor L would be redundant. Let us now consider a capacitor, this cannot be added in series to any branch of the switching cell, because the conduction is unidirectional and the current through every branch has a DC component. Furthermore, a capacitor connected in parallel at any of the ports of the switching cell is actually connected in parallel to the input voltage source, or to the output capacitor, or to the series connection between the input voltage source and the output capacitor, which makes it redundant. Having said this, fourth-order converters, which are generated from third-order switching cells, are investigated in the next section.

3.1 Generation of fourth-order switching converters

Two-switch third-order switching cells are composed of one active switch, one passive switch (diode), two inductors and one capacitor. There are many switching cells that can be obtained by combining these elements. However, according to [Tym88], only those five shown in Fig. 3.1 are distinct (the notation *Cell C – Cell G* is as in [Tym88]). That is to say, other two-switch third-order switching cells are electrically equivalent to one of these five cells.

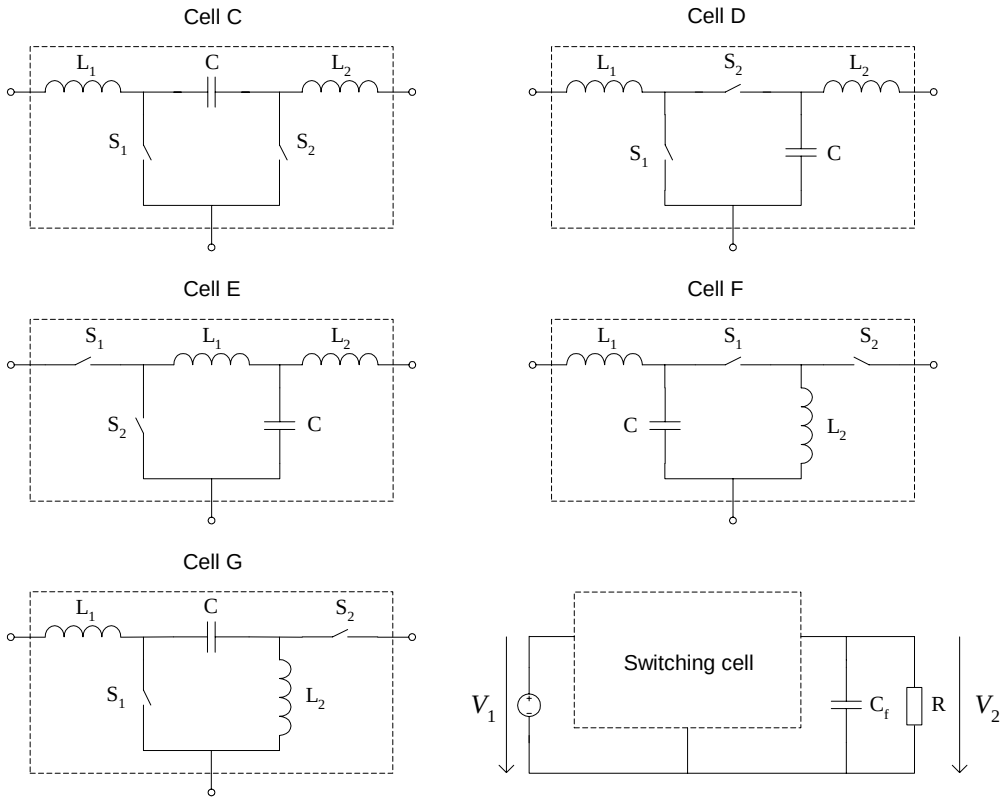


Fig. 3.1 Third-order switching cells and generation of fourth-order converters.

As shown in Fig. 3.1, a switching cell is placed in-between the input voltage source and the output capacitor and load. A family of converters is obtained by rotating the switching cell in all possible combinations. A total of 27 different two-switch fourth-order converters can be obtained [Tym88, *Cell C – Cell G*]. The switches are shown as generic components in Fig. 3.1. The resulting converter topology defines the conduction direction of the switches and determines which is the active one.

Several two-switch fourth-order topologies have been known and used in DC/DC applications for many years. It is not surprising that they are, in fact, members of a larger family of converters generated from one of the switching cells shown in Fig. 3.1. For example, the well-known Ćuk converter [Cuk77a] and the two-inductor Boost and Buck converters [Whi87] belong to the family generated from *Cell C*. The SEPIC converter belongs to the family generated from *Cell G*.

3.2 Characteristic properties of fourth-order switching converters

Fourth-order converters have some characteristics, which are described next, that cannot be obtained in second-order topologies.

- It is possible to associate continuous input current with a step-down or step-down/up conversion ratio. This is not possible in Buck or Buck-Boost converters. In addition to that, in some of the topologies, the output current is continuous, as well. For example, the two-inductor Buck converter presented in [Whi87] is a topology with step-down characteristic and continuous input/output currents. The Ćuk converter is an example of a step-down/up topology where both input and output currents are continuous.

- Converters generated from *Cell G* have conversion ratios that are not encountered at all in second-order converters. The SEPIC converter has a step-down/up conversion ratio without having an inverted output voltage, as opposed to both the Buck-Boost and Ćuk. Other two topologies belonging to this family can operate with bipolar input voltage (though, both switches must be active and must allow reverse conduction, e.g. through the body diode or an anti-parallel diode). Therefore, it is possible to obtain AC/DC conversion without the need of a diode bridge.

- By properly coupling the inductors, the ripple of the current in one of the inductors can be reduced to a great extent. This is discussed in more detail in Section 3.3.

- More than two operating modes are possible in fourth-order converters, as described in [Cuk79] and [Mak91]. Each of the inductors L_1 and L_2 can operate in CICM or DICM. In addition

to that, while the voltage on the output capacitor of the switching converter is assumed to be constant over one switching cycle, capacitor C belonging to the switching cell has two possible operating modes. In Continuous Capacitor Voltage Mode – CCVM, the voltage on the capacitor is never clamped to a certain level during one switching cycle. This behavior is similar to that of an inductor in CICM. Conversely, in Discontinuous Capacitor Voltage Mode – DCVM, the voltage on the capacitor is clamped to a certain value during one switching cycle. This operating mode is described in more detail in Section 3.5. Similarly to DICM, DCVM offers inherent PFC property, which is discussed in Section 3.6.

- The increased order of the circuit implies more complex dynamics, as it has been shown for example in [Cuk77a], [Mid79] and [Vor96].

3.3 The 'zero-ripple' technique

The coupled inductor technique can be applied in a DC circuit in order to reduce the current ripple in an inductor. It can be used, for example, to reduce the ripple of the input/output current of a switching converter. The underlying principle is described next.

Let us consider the coupled inductors L_1 and L_2 as shown in Fig. 3.2. This winding arrangement can be described by the equations:

$$v_{L_1} = L_1 \frac{di_1}{dt} + L_{12} \frac{di_2}{dt}, \tag{3.1}$$

$$v_{L_2} = L_2 \frac{di_2}{dt} + L_{12} \frac{di_1}{dt}. \tag{3.2}$$

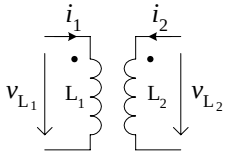


Fig. 3.2 Coupled inductors.

The mutual inductance L_{12} is given by

$$L_{12} = k\sqrt{L_1 L_2}\,, \tag{3.3}$$

where k is the coupling factor of the inductors. If we now consider that equal voltages

$$v_{\mathrm{L}_1} = v_{\mathrm{L}_2}\,, \tag{3.4}$$

are applied to the inductors, it follows from (3.1) and (3.2) that

$$\left(L_1 - L_{12}\right)\frac{di_1}{dt} = \left(L_2 - L_{12}\right)\frac{di_2}{dt}. \tag{3.5}$$

From (3.5) it can be seen that the ripple of the current in either of the inductors can be cancelled, if the inductors are suitably coupled. Ripple in inductor L_1 can be cancelled if $L_2 = L_{12}$. Considering (3.3), this is equivalent to having a ‘zero-ripple’ coupling factor

$$k_{\mathrm{zr}} = \sqrt{\frac{L_2}{L_1}}\,. \tag{3.6}$$

Similarly, ripple in inductor L_2 can be cancelled if $L_1 = L_{12}$, which is equivalent to having a ‘zero-ripple’ coupling factor

$$k_{\mathrm{zr}} = \sqrt{\frac{L_1}{L_2}}\,. \tag{3.7}$$

Having two inductors, fourth-order switching converters offer the opportunity to apply this technique, provided that the voltages applied to the inductors fulfill the condition in (3.4). ‘Zero-ripple’ input or output current can be obtained, depending on the topology and on the requirements of the application. Moreover, a single integrated magnetic component can be used to realize the coupled inductors. As a consequence, a reduction of size and cost can be potentially obtained as compared to using two separate inductors.

In order to illustrate how the ‘zero-ripple’ technique can be applied in fourth-order converters, let us consider the Ćuk converter that is shown in Fig. 3.3, for which this technique has been presented in [Cuk77b]. If capacitors C and C_f are modeled as ideal voltage sources (infinite capacitance), and if resistive voltage drops are neglected, it can be easily seen that the voltages applied to inductors L_1 and L_2 are always equal. Therefore, cancellation of the current ripple in either of the inductors can be obtained. In reality, C and C_f have finite capacitance, so the voltage across them has a certain ripple. As a consequence, the condition $v_{L_1} = v_{L_2}$ cannot be accurately fulfilled. For this reason, the current ripple can be reduced to a great extent but it cannot be cancelled. Hence, the quotation marks in ‘zero-ripple’ have been used. In addition to that, it is difficult to ensure that a coupling factor as defined by (3.6) or (3.7) is obtained with precision in a practical implementation.

The ‘zero-ripple’ technique is presented in some detail in [Sev85, pp. 273-282]. A more comprehensive analysis is made in [Kol97], where it is shown that ‘zero-ripple’ structures correspond to an integration of an LC filter into the respective converter structure. This leads possibly to a higher power density when compared to a separate arrangement of filter and converter. However, it has to be pointed out that, in several fourth-order topologies, the filtering capacitor of the integrated LC filter acts also as an essential element for the energy transfer between the input and output (e.g. in the Ćuk converter).

The application of this technique can be found in a number of other publications, as well. In [Cap88] it is pointed out that the ‘zero-ripple’ technique can be applied to two-inductor Buck and Boost converters in [Whi87]. Applications of these topologies for DC/DC conversion and using the ‘zero-ripple’ technique are also discussed in [Mar91] and [Zha93]. Finally, in [Wan96], the ‘zero-ripple’ technique is applied to a fourth-order modified Boost converter.

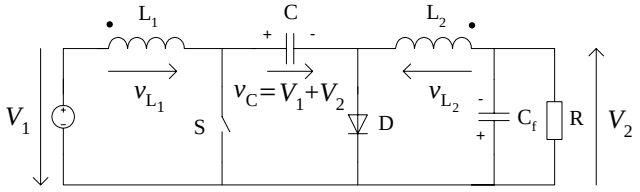


Fig. 3.3 Ćuk converter with coupled inductors.

3.4 Application for PFC with operation in CICM and CCVM

As stated in Chapter 1, one aim of the research reported in this dissertation is to investigate converter topologies having an input current with reduced high-frequency content. For this reason, the research concentrates on CICM operation for both inductors L_1 and L_2, and on those topologies having an inductor in series at the input side. Besides operation in CICM for L_1 and L_2, in this section we also consider the case when capacitor C is operating in CCVM. The first aspect to be discussed is that the converter does not have inherent PFC properties in this operating mode. Similar to second-order converters operating in CICM, the duty-cycle of the switch must be controlled, in order to shape the line current. In principle, any of the control methods described in Subsection 2.3.2 can be applied, but the more complex dynamics of a fourth-order converter have to be taken into account.

Let us consider as an example the SEPIC converter, which is shown in Fig. 3.4. Its application for PFC, with average current mode control, is discussed in [Dix93a]. As can be seen, there is a loop consisting of the input voltage source, inductor L_1, capacitor C and inductor L_2, in which the only damping is provided by the parasitic resistances. This explains the pair of (practically) undamped complex conjugated poles in the control-to-switch-current transfer function [Dix93b]. In a DC/DC application, the capacitance C may be in a similar range as that of the output filtering capacitor. Therefore, the pair of undamped complex conjugated poles would be at a low enough frequency, where the control loop has enough gain to damp any resonance that might occur. However, the situation is different in a PFC application, where the voltage on capacitor C varies over the line-cycle (e.g. in the SEPIC converter the capacitor voltage follows the shape of the rectified line voltage). As a consequence, the capacitance C that can be used is limited to a value (e.g. a few μF) that is much lower than it would be in a DC/DC application. The position of the undamped complex conjugated poles is at a much higher frequency, where the gain of the current loop is insufficient to damp oscillations. Therefore, an RC series network placed in parallel to the capacitor is needed, to provide effective damping of the complex conjugated poles. A PFC based on Ćuk and SEPIC converters is discussed also in [Spi94a], where average current mode control and a damping RC network are used to obtain stable operation, as well as in [Jay98], where inductors are coupled and nonlinear carrier control is applied.

The second aspect to be considered is that the limited capacitance C that can be used in a PFC application has a negative effect also on the effectiveness of the ‘zero-ripple’ technique, when compared to a DC/DC application. This is explained by the larger voltage ripple on capacitor C or,

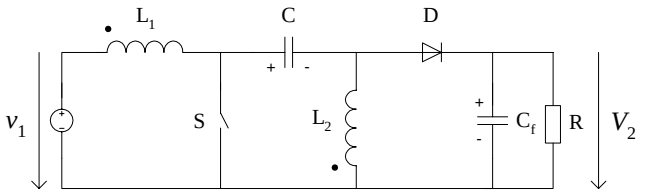


Fig. 3.4 SEPIC converter.

from another point of view, by the higher resonant frequency of the LC filter that is embedded in the converter structure. However, the results can still be very good. In [Wal00] we have applied the fourth-order modified Boost converter from [Wan96] for PFC, and obtained a reduction of the input current ripple from almost 1A to approximately 50mA. In [P5], we discuss the PFC application of a fourth-order step-down topology with coupled inductors, which is useful to achieve a step-down conversion ratio, as well as an input current with very low ripple.

3.5 Discontinuous Capacitor Voltage Mode – DCVM

Let us consider in more detail how DCVM can be obtained and explain how it can be considered as the dual of DICM. Both operating modes are illustrated in Fig. 3.5.

DICM is obtained in second-order converters by periodically switching the inductor between a positive voltage source V_+ and a negative voltage source V_-. This makes the current i_L increase linearly from zero to its peak value and then to decrease linearly back to zero. The current cannot reverse direction and it is clamped to zero. This is because conduction through inductor L is always unidirectional, as it can be seen from Fig. 2.11. The unidirectional conduction is illustrated in Fig. 3.5 by the diode D placed in series with inductor L.

DCVM can be obtained if a capacitor C is periodically switched between a positive current source I_+ and a negative current source I_-. This makes the voltage v_C increase linearly from zero to its peak value and then to decrease linearly back to zero. When it reaches zero, the voltage is clamped, which is illustrated in Fig. 3.5 by the diode D placed in parallel across the capacitor.

The previous two paragraphs only explain the underlying principle for discontinuous operating modes. In fourth-order switching converters, depending on the actual topology, the current/voltage may be clamped to a different level. Still, the operating mode that is obtained is discontinuous. It has to be pointed out also that the ideal sources, the changeover switch and the

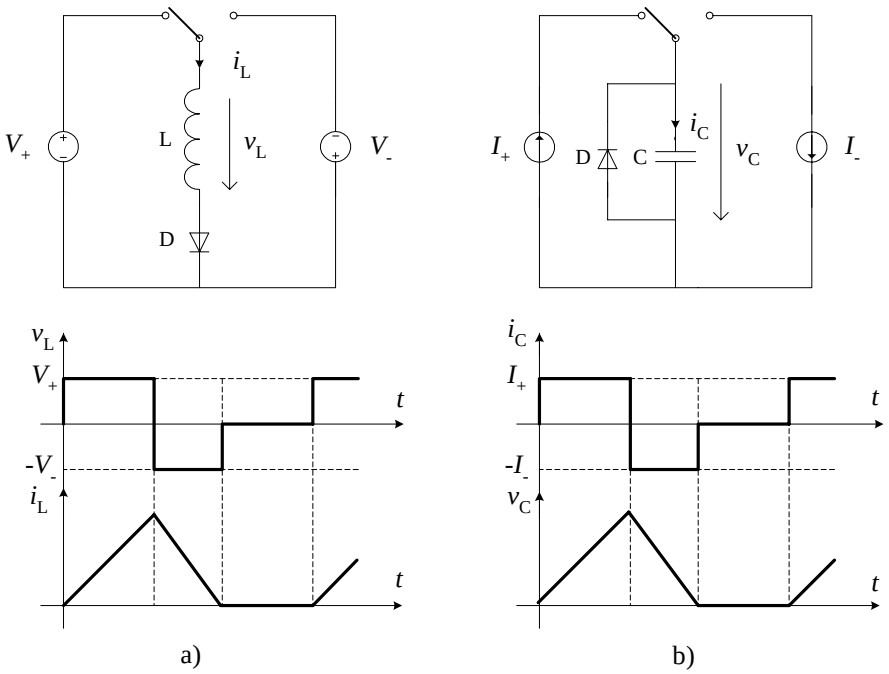


Fig. 3.5 Illustration of discontinuous operating modes: a) DICM; b) DCVM.

diode in Fig. 3.5 are not actual components of the analyzed converters. The circuits are only intended to illustrate the principle and their operation should not be considered in a strict way.

It can be seen that DCVM can be considered as a dual of DICM. For DICM, two voltage sources and one inductor are needed, whereas to obtain DCVM, two current sources and one capacitor are required. DCVM can be obtained in fourth-order converters if the following conditions are met:

- The topology allows for a charge and discharge sequence of capacitor C, as shown in Fig. 3.5b).
- Capacitance C is low enough to allow the voltage variation shown in Fig. 3.5b). In addition to that, inductors L_1 and L_2 from Fig. 3.1 operate in CICM, and they implement the current sources from Fig. 3.5. These issues are discussed in detail in publications [P2]-[P4].

3.6 The inherent PFC property

It has been pointed out in [Tse97a] and [Tse98a] that the inherent PFC property is related to operation in a discontinuous conduction mode. That is to say, inherent PFC can be achieved in either DICM or DCVM. We shall discuss separately the use of discontinuous conduction modes in fourth-order switching converters to achieve the inherent PFC property.

3.6.1 Operation in DICM and CCVM

In this case, the inherent PFC property is obtained using DICM for inductors L_1 and L_2, while capacitor C operates in CCVM. The current through the inductors is not necessarily clamped to zero. For example, in a Ćuk converter with both inductors operating in DICM, the currents are clamped periodically at a non-zero value. However, the sum of the currents is zero during the clamping intervals, therefore their combined dynamics is reduced [Tse97a]. The inherent PFC property can be demonstrated in the same manner as that used for second-order converters.

A number of applications can be found in the literature: based on the Ćuk converter in [Brk92], on Ćuk and SEPIC converters in [Pom94], and on the SEPIC converter in [Spi94b]. However, an input current with reduced high-frequency content, which is one aim of the research presented in this dissertation, cannot be obtained using DICM. Therefore, this combination of operating modes will not be addressed further.

3.6.2 Operation in DCVM and CICM

Inherent PFC can be obtained also by using DCVM operation for capacitor C and CICM operation for inductors L_1 and L_2 [Tse97a], [Tse98a]. Moreover, if one of the inductors is placed in series at the input of the converter, we can produce an input current with reduced high-frequency content. As stated in Chapter 1, these are two of the characteristics we would like to obtain for the PFC stage. However, there are few publications addressing the operation of fourth-order converters in DCVM and CICM. Therefore, we explored this topic further. Reference [Ism92] investigates the application of DICM or DCVM to achieve PFC in a three-phase rectifier. A Ćuk converter operating in DCVM is analyzed in [Lin97], and [Tse97b] presents a single-stage converter based on this operating mode. DCVM operation of the Buck converter with an LC input filter is addressed in [Lee97], but we provide a more comprehensive analysis in publications [P2] and [P3]. Furthermore, in [P4] we present and analyze a Flyback-derived isolated converter operating in DCVM.

4 Methods for Improving the Efficiency

The PFC stage performs an additional power processing operation, and therefore it has a negative impact on the overall efficiency of the power supply. In this dissertation, we aim at improving its efficiency by reducing the switch conduction losses in the combined diode bridge and PFC stage, as well as on circuit techniques for reducing the switching losses.

4.1 Reduction of conduction losses

Conduction losses are caused by the current flowing through a non-ideal switching device in the on-state, which determines a certain voltage drop on the device. A static model of the switching device is useful for estimating the conduction losses [Kre98, pp. 454-464]. Static models are presented in Fig. 4.1, for on-state diode and MOSFET, devices that are considered in publication [P6] for comparing the conduction losses of the analyzed topologies.

Fig. 4.1 Static models for an on-state switching device: a) Diode; b) MOSFET.

As shown in Fig. 4.1, the static characteristic of the on-state diode can be modeled as a voltage source V_D in series with a resistor r_D. On the other hand, the appropriate static model for the on-state MOSFET is just a resistor r_{DS}. With these models, it is straightforward to calculate the conduction losses of diode D:

$$P_{D,\,cond} = V_D\, I_{D,\,av} + r_D\, I_{D,\,rms}^2, \tag{4.1}$$

where $I_{D,\,av}$ and $I_{D,\,rms}$ are the average and RMS diode currents, respectively. Similarly, the conduction losses of switch S (MOSFET) are expressed as:

$$P_{S,\,cond} = r_{DS}\, I_{S,\,rms}^2, \tag{4.2}$$

where $I_{S,\,rms}$ is the RMS switch current.

Naturally, the total conduction losses of the combined diode bridge and PFC stage are the sum of the individual conduction losses of the switches. Considering also (4.1) and (4.2), we can conclude that one way to diminish the total conduction losses is to reduce the number of switches that are in the power path and/or to reduce the average/RMS currents flowing through the switches, assuming that the r_{DS} of MOSFETs and the V_D and r_D of diodes remain unchanged. In our research, which is reported in publication [P6], we take mainly this circuit-oriented approach. A second possibility is the device-oriented approach, i.e. using MOSFETs with lower r_{DS} and diodes having lower V_D and r_D. The two approaches are interrelated, in the sense that circuit techniques can be used to lower the voltage stress of the switches, thus allowing the use of switches having lower losses. A good example of this is the three-phase Vienna rectifier which, being a three-level topology, allows the use of devices with lower voltage rating [Kol94]. On the other hand, as shown in publication [P6], the circuit-oriented approach may lead to topologies that have fewer switches in the power path, but also impose a higher voltage stress on them. As a result, switches with higher voltage rating and therefore with higher losses need to be used.

4.2 Reduction of switching losses

The commutation process of real switching devices takes a certain time, during which the instantaneous power dissipated in the device can be very large. Therefore, switching losses are a major reason for decreased efficiency in converters. To discuss the reasons for them, let us consider once more the first-order switching cell and the Buck converter, which are shown again in Fig. 4.2.

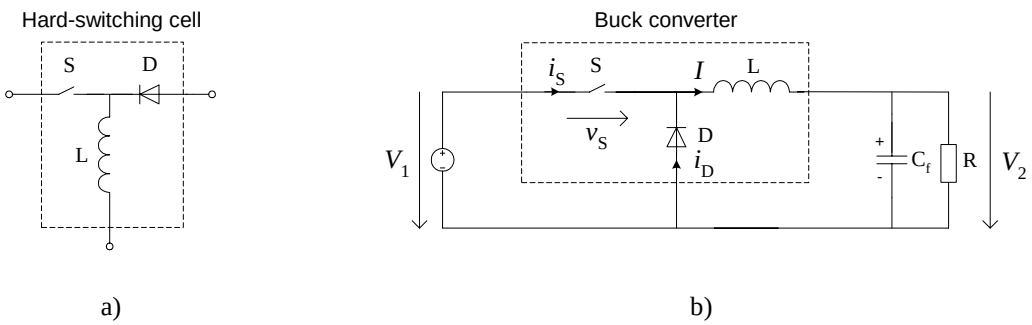


Fig. 4.2 a) Hard-switching cell; b) Buck converter.

The switching cell is labeled ‘hard-switching cell’, because there is no mechanism in place to decrease the switching losses. The inductor current I is assumed to be constant, fact which gives specific characteristics to the switching mechanism. In addition, the switching mechanism depends for certain aspects on the types of switching devices that are used. We will discuss here the cases where the active switch S is either a MOSFET or an IGBT, and the passive switch is a *p-n* type silicon diode. The sources of switching losses [Eri97, pp. 94-104] are summarized next.

- During turn-on and turn-off of the active switch S, the switch voltage v_S and the switch current i_S have simultaneously non-negligible values, so a significant instantaneous power $p_S = v_S\, i_S$ is dissipated in the switch. The energy lost at turn-off is particularly significant in IGBTs, due to the current tailing that occurs during this transition.

- Some amount of minority charge is stored in diode D while it is conducting. When the diode turns off, the stored charge must be removed during the reverse recovery process, before it can establish a reverse biased operating point. While some of the charge is removed by recombination within the diode, a part Q_r is recovered through a negative current i_D, which flows through the active switch as well. On the other hand, while this process takes place, the active switch voltage is practically $v_S = V_1$, because the diode remains forward biased. As a consequence, the reverse recovery process of the diode induces switching losses in the active switch S.

- When the active switch S is turned on, its parasitic capacitance, e.g. for a MOSFET the drain-source capacitance C_{DS}, is shunted and the energy stored in it is dissipated in the switch.

- When a switch is conducting, inductances effectively in series with it, e.g. the leakage inductance of a transformer, the interconnection and the package inductances, store energy, which is dissipated at turn-off.

Switching losses can be reduced using soft-switching techniques. To begin with, switching losses induced by the diode reverse recovery are proportional to the stored charge Q_r. At its turn, Q_r depends on the on-state diode current $i_D = I$, as well as and on the rate of variation di_D/dt at turn-off, which is limited only by the external circuit; the higher I and di_D/dt are, the higher Q_r is. However, Q_r is reduced if the rate of variation of the diode current is limited, typically $di_D/dt < 100\,\mathrm{A/\mu s}$ [Jan98]. As a result, switching losses are reduced, as well. This technique is used in some passive snubbers, e.g. in [Lev97], where a small auxiliary inductor is used to limit the rate of variation of the diode current.

The capacitive turn-on losses can be theoretically eliminated and the overlap of non-negligible active switch voltage and current can be avoided at turn-on, by using the Zero Voltage Switching – ZVS technique. Basically, this technique consists of forcing to zero the active switch voltage, prior to its turn-on, by creating a resonance between an inductor and a capacitor. The inductor also limits the rate of variation of the diode current, so losses due to the reverse recovery are reduced as well. The ZVS technique has been applied in a variety of topologies, such as the resonant and quasi-resonant – QR converters [Eri97, pp. 659-707, pp. 726-731]. The ZVS-QR switching cell is depicted in Fig. 4.3a), and a ZVS-QR Buck converter where the active switch S is a MOSFET, is shown in Fig. 4.3b). The resonant process involves capacitor C_r, which consists of the output capacitance of the switch with possibly an auxiliary parallel-connected capacitor, and the inductor L_r. It starts after the active switch S is turned off and diode D begins conducting. The switch voltage has essentially a sinusoidal variation and it returns to zero after a certain time T_{off}, instance when the active switch S is turned on again with zero voltage on it. ZVS is achieved, but

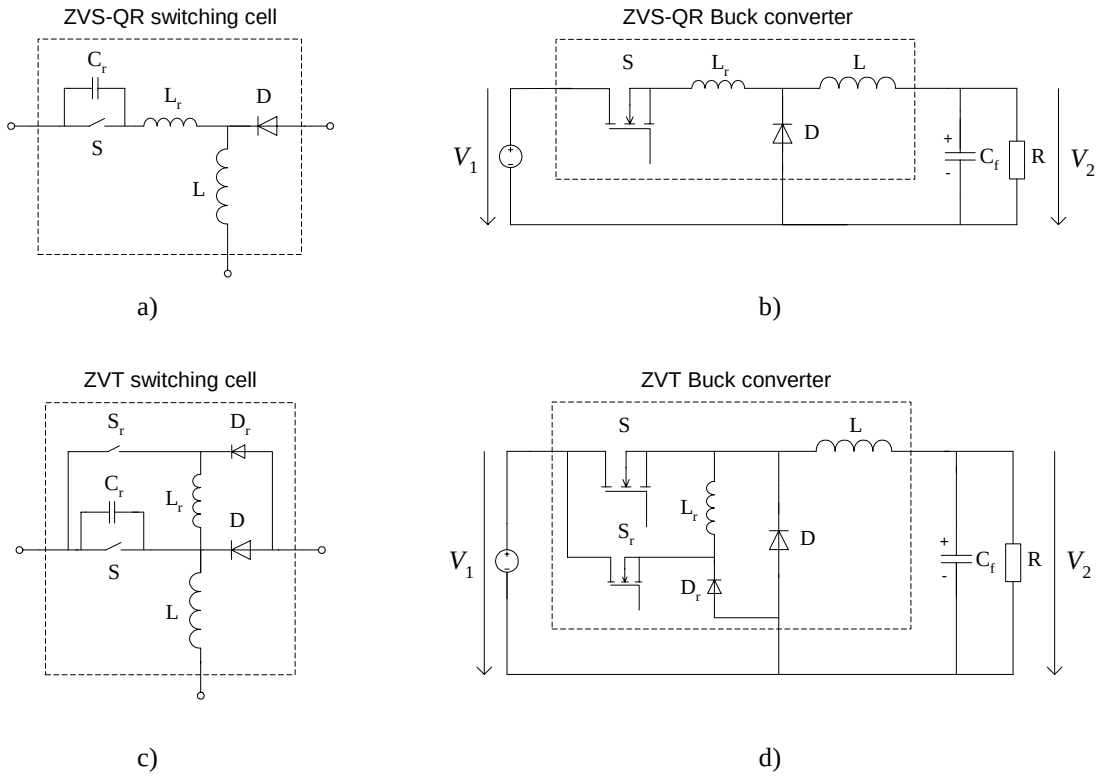


Fig. 4.3 ZVS topologies: a) ZVS-QR switching cell; b) ZVS-QR Buck converter; c) ZVT switching cell; d) ZVT Buck converter.

the off-time T_{off} of the active switch is practically fixed. Therefore, the control of the converter has to be done using variable switching frequency, instead of fixed switching frequency. Moreover, while the active switch S is blocked, its peak voltage is higher in the ZVS-QR converter, when compared to its hard-switching counterpart, e.g. in the ZVS-QR Buck converter the switch voltage stress is higher than the input voltage V_1. Higher switch voltage stress and variable-frequency control are the main drawbacks of the ZVS-QR converters. A modified quasi-resonant topology has been proposed in [Hua95], which solves the problem of variable-frequency control, at the expense of increased complexity. In this solution, an auxiliary active switch is used to shunt the resonant inductor L_r, thus interrupting the resonant process for a certain interval in order to enable operation with fixed switching frequency. Nevertheless, the problem of increased switch voltage stress remains.

Better characteristics are obtained in Zero Voltage Transition – ZVT topologies, at the expense of increased complexity. Here, to achieve ZVS, switch voltage and current waveforms are changed only during commutation intervals, the behavior of the ZVT converter being otherwise identical to that of the hard-switching converter. In converter topologies having only one active switch, the ZVT technique is implemented with an auxiliary circuit, which consists of an additional active switch, an auxiliary inductor, for the resonant process that discharges the drain-source capacitance of the switch and for limiting the rate of change of the diode current at turn-off, as well as a few other passive components. Several ZVT topologies have been published, e.g. in [Fre93], [Hua94], [Mos95], [Jou96] and [Smi97]. The topology from [Hua94] is presented in Fig. 4.3c)-d), as an example. The auxiliary switch S_r is turned on before turning on the main active switch S. This initiates a resonant process, which creates zero voltage switching conditions for the main active switch. The time intervals where the auxiliary circuit is active are very short when compared to the switching period; hence, except for the commutation intervals, the waveforms of the ZVT Buck converters are the same as those of the hard-switching Buck converter.

The ZVS and ZVT techniques presented above reduce the switching losses which are due to the reverse recovery of the diode and to the capacitive discharge when the active switch turns on, and they can be applied also when the main active switch is an IGBT. On the other hand, the switching losses at turn-off due to the current tailing of the IGBT can be reduced using the Zero Current Switching – ZCS technique, which consists of forcing to zero the active switch current, prior to its turn-off. This technique can be considered as a dual of the ZVS technique, and it is used, for example, in resonant and quasi-resonant converters [Eri97, pp. 659-707, pp. 712-726]. The

ZCS-QR switching cell is depicted in Fig. 4.4a), and a ZCS-QR Buck converter where the active switch S is an IGBT, is shown in Fig. 4.4b). The resonant process, involving the capacitor C_r and the inductor L_r, starts when the active switch S is turned on and diode D ceases conducting. The switch current has an essentially sinusoidal variation, and it returns back to zero after a certain time T_{on}. The on-time T_{on} of the active switch is practically fixed, and a variably-frequency control must be used to control the output voltage. In addition to this, the peak switch current is higher in a ZCS-QR converter, when compared to its hard-switching counterpart. It can be seen that ZVS-QR and ZCS-QR converters have dual behavior. A modified ZCS-QR switching cell, which solves the problem of variable-frequency control, has been proposed in [Hua95]. An auxiliary switch is used in series with the resonant capacitor C_r, to interrupt the resonant process for a certain interval, thus allowing for fixed-frequency operation. The idea is similar to that used by the same authors in their modified ZVS-QR switching cell and discussed previously. However, the solution still has the drawback of high peak switch current.

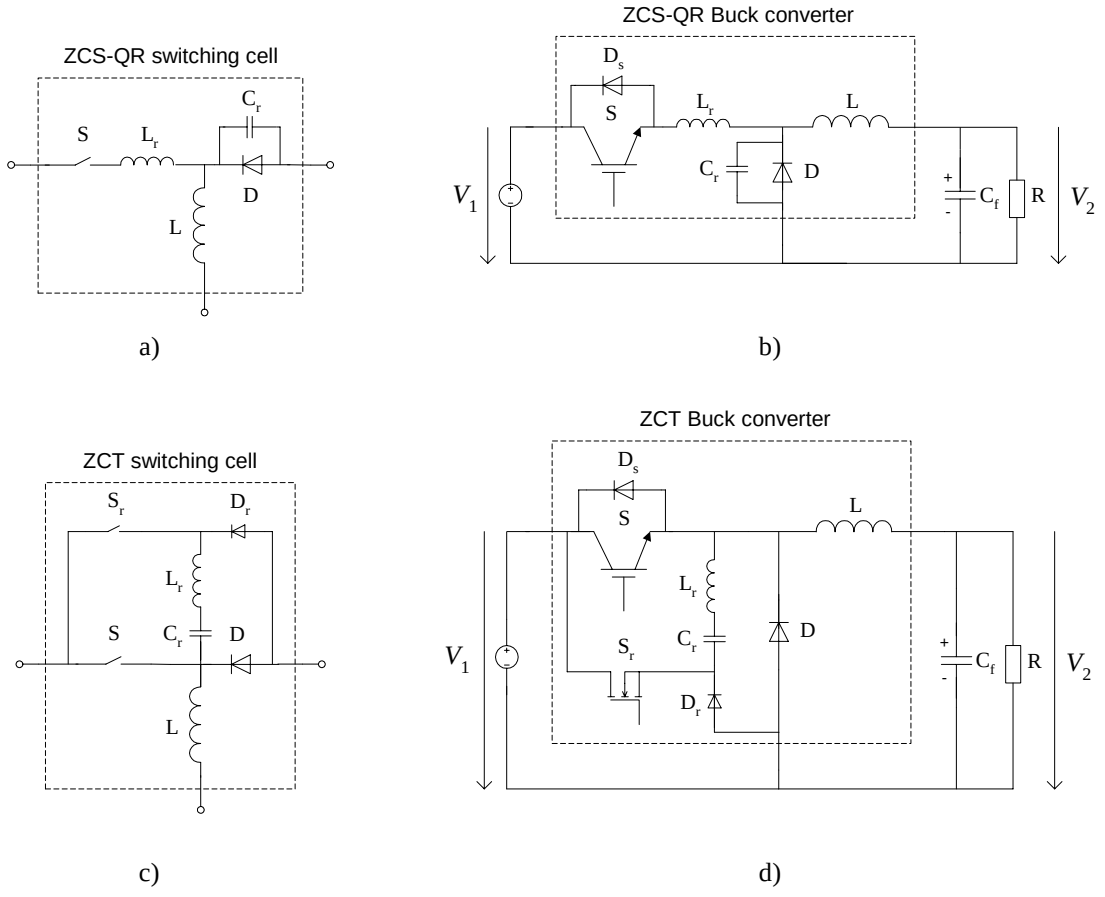


Fig. 4.4 ZCS topologies: a) ZCS-QR switching cell; b) ZCS-QR Buck converter; c) ZCT switching cell; d) ZCT Buck converter.

Zero Current Transition – ZCT topologies, working on similar principles as the ZVT topologies, have been proposed as well. An example is the topology shown in Fig. 4.4c)-d) [Hua95]. The auxiliary switch S_r is turned on prior to turning off the main switch S, and it initiates a resonant process that shapes to zero the current through S. In this way, the main switch can be turned off with zero current through it.

While having increased complexity as a main drawback, ZVT and ZCT topologies have also clear advantages. The switching losses are reduced, without the need to alter the switch waveforms during the conduction intervals of the main switches. In addition to this, because the operation of the original hard-switching converter is altered only during switching intervals, the design of the converter itself and of its control circuit can be made in a similar manner as for the original hard-switching converter.

Our research concerning the reduction of switching losses, which is reported in this dissertation, focused on ZVT topologies. In publication [P7], we present a novel ZVT Buck converter. The ZVT operating principle can be applied to other converters as well, for example to the forward converter as presented in publication [P8], or to a PFC Boost converter as presented in [Bar98].

5 Summary of Publications

In this chapter, we present a summary of the original publications which constitute this dissertation and which are attached in Appendix A.

The publications are divided into five categories. In Section 5.1, we summarize publication [P1], in which input filtering requirements for a PFC stage based on Boost converter operating in DICM are examined. In the following two sections, research is extended to fourth-order switching converters. In Section 5.2, we summarize publications [P2]-[P4], in which fourth-order switching converters operating in DCVM and CICM are investigated and their application for PFC is analyzed. Furthermore, PFC based on a fourth-order switching converter operating in CCVM and CICM is analyzed in publication [P5] and summarized in Section 5.3. The last two sections address methods to improve the efficiency of the PFC stage. Section 5.4 summarizes publication [P6], which examines the possibility of improving its efficiency by reducing the conduction losses in the combined diode bridge and PFC stage. Finally, Section 5.5 summarizes publications [P7] and [P8], which present a ZVT technique that improves the efficiency by reducing switching losses to a great extent.

The author's contribution to the work is stated in Section 5.6 and the major conclusions of the work are postponed until Chapter 6.

5.1 EMI filter requirements

5.1.1 Publication [P1]

In Subsection 2.3.4, we discussed the general requirements for the EMI filter of a PFC stage. In this publication, we analyze the particularities of these requirements when the PFC stage is a Boost converter operating in DICM.

We first present a case analysis for a 100W PFC stage based on a Boost converter, operating with a $220V_{rms}$ rectified input voltage and having a $380V_{dc}$ output voltage. The differential-mode EMI is determined by simulation and the model of a $50\Omega/50\mu H$ Line Impedance Stabilization Network – LISN [Tih95, pp. 36] is used to measure it. Three cases are considered: operation in DICM with constant on-time and constant switching frequency, operation in DICM with constant on-time and variable switching frequency (DICM borderline operation) and, as a reference for

comparison, operation in CICM with average current mode control. Not surprisingly, at constant switching frequency, the differential-mode EMI is higher when operating in DICM when compared to operation in CICM, with approximately $20\text{dB}\mu\text{V}$ for the analyzed case. On the other hand, in variable-frequency DICM operation, the differential-mode EMI is lower when compared to the fixed frequency DICM operation, but it extends to a lower frequency, i.e. to the minimum switching frequency.

We proceed by discussing the EMI filter requirements for DICM operation. The requirements of providing the necessary switching noise attenuation, while ensuring low displacement angle φ, apply in the same way as for CICM operation. Therefore, we focus on the third requirement discussed in Subsection 2.3.4, namely ensuring overall system stability.

As explained in Subsection 2.3.4, it is important to know the input impedance Z_{ic} of the PFC stage, in order to check if $T_{\text{f}} = Z_{\text{of}} / Z_{\text{ic}}$ satisfies the Nyquist criterion for stability, where Z_{of} is the output impedance of the EMI filter. To calculate the input impedance Z_{ic}, a time-invariant model of the converter is needed, this can be obtained by using an averaging method. Low-frequency models for PFC converters operating in DICM were developed in the past by averaging signals over half line-cycle, models which are useful for designing the low-bandwidth voltage control loop [Rid89], [Gla95]. However, the resonant frequency of the EMI filter is decades above the line-frequency; hence, a high-frequency model of the PFC stage is needed to study the interaction with the EMI filter. For this, we use the averaged 'PWM switch' approach, in which the active switch and the diode are replaced by a time-invariant equivalent circuit that is obtained by averaging quantities over one switching period T_{s} [Vor90b]. It is recognized that in a PFC application, the circuit is not in a stationary state, when considering its operation over one switching cycle, meaning that the current through the output capacitor has a DC component. Therefore, the circuit is first transformed to its stationary state equivalent, in which an additional load resistance models the DC component of the output capacitor current. The nonlinear equations resulting from the circuit are linearized around the operating point and then the input impedance is calculated.

The application of this method is presented in details for a Boost converter operating in DICM and with constant on-time and constant switching frequency, with the constant on-time and variable switching frequency case being similar. The modulus and phase characteristic of the calculated input impedance are shown in Fig. 5.1. The operating point of the converter is changing over the line-cycle, so it only makes sense to consider these characteristics starting from a frequency much higher than the line-frequency, e.g. at least ten times higher. As mentioned before, the resonant

frequency of the EMI filter is much higher than the line-frequency too, so the model is appropriate for studying its interaction with the PFC stage. The input impedance Z_{ic} shows no phase-shift starting from a low frequency, e.g. approx. 100Hz, as can be seen from Fig. 5.1. As a consequence, $T_f = Z_{of} / Z_{ic}$ satisfies the Nyquist criterion and there are no instabilities due to the interaction between the EMI filter and the PFC stage.

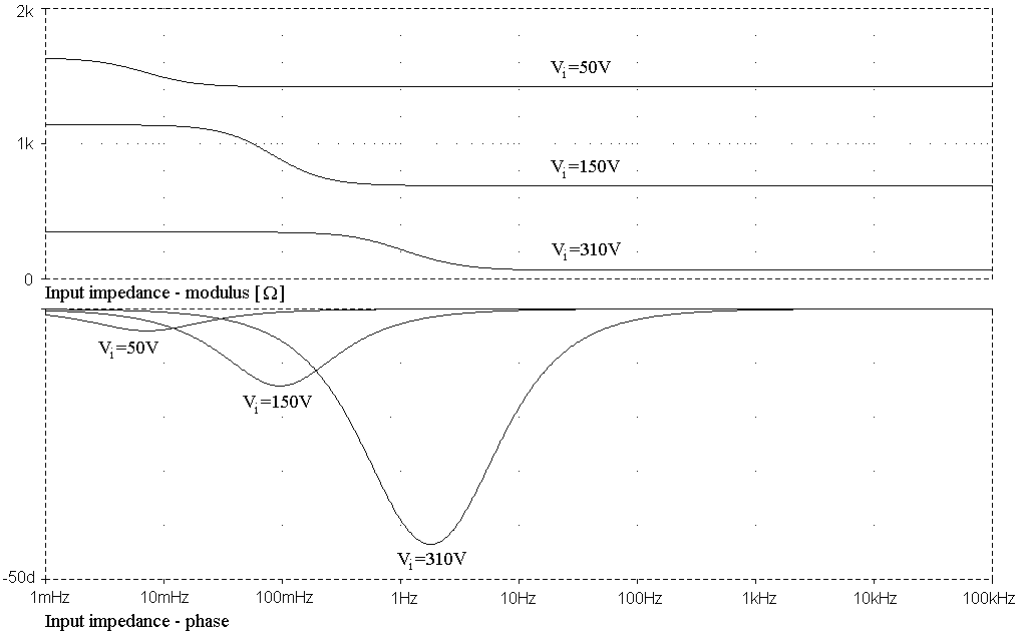


Fig. 5.1 Input impedance Z_{ic} of the Boost converter operating in DICM, with a constant on-time and a constant switching frequency.

5.2 Fourth-order switching converters operating in DCVM and CICM

5.2.1 Publication [P2]

For this publication, we first inspected the two-switch fourth-order topologies from [Tym88, *Cell C – Cell G*], in order to select a number of them for further investigation. Several factors were taken into account, such as the ability to operate in DCVM, the conversion ratio, the voltage and current stress of the switches, as well as the type of input and output currents, i.e. continuous or discontinuous. One topology for each type of conversion ratio, i.e. step-down, step-up and step-down/up was selected, with preference for those topologies in which both input and output currents are continuous. The selected topologies are shown in Fig. 5.2a). Inductor L_1 is a high-frequency

reactive element, whereas L_2 can be either a low- or a high-frequency reactive element. By low-frequency reactive element we mean an inductor or a capacitor that can be modeled at line-frequency as an ideal current or voltage source, respectively. In contrast, a high-frequency reactive element can be modeled as an ideal source at switching frequency, but not at line-frequency.

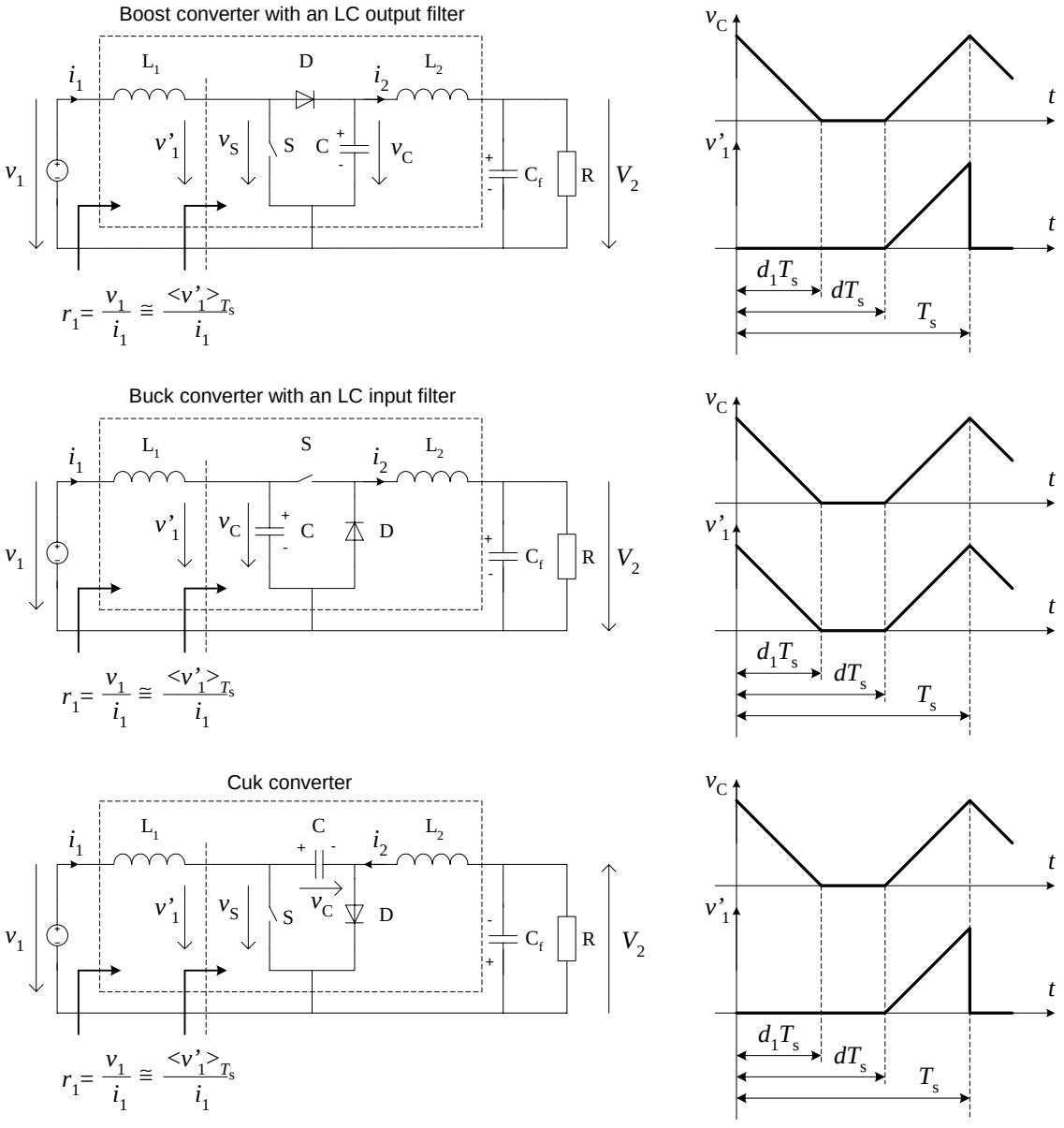


Fig. 5.2 a) Selected fourth-order switching converters; b) Capacitor voltage $v_C(t)$ and voltage $v_1'(t)$ when operating in DCVM.

Let us first examine the operation of the selected converters over one switching cycle. During this interval, currents through L_1 and L_2 can be considered to be constant. Furthermore, capacitor C operates in DCVM and its voltage varies as shown in Fig. 5.2b). The first topology is derived from *Cell D* and it resembles a Boost converter with an LC output filter. If we model the input and output inductors as current sources, it can be viewed as a current step-down converter, having the output current lower than the input current. Therefore, it can be considered as the dual of the voltage step-down Buck converter, which has its output voltage lower than the input voltage. The second topology is derived from *Cell D* as well, and it resembles a Buck converter with an LC input filter. Viewed as a current step-up converter, whose output current is higher than the input current, it is the dual of the voltage step-up Boost converter, which has its output voltage higher than the input voltage. The third topology is derived from *Cell C* and it is the Ćuk converter. If we consider it as a current step-down/up converter, it is the dual of the voltage step-down/up Buck-Boost converter. One conclusion is that topologies in Fig. 5.2 are duals of the second-order topologies from Fig. 2.13, at least if we consider their behavior during one switching cycle.

As shown in Fig. 5.2, the input resistance r_1 is defined as:

$$r_1(t) = \frac{v_1(t)}{i_1(t)}. \tag{5.1}$$

At line-frequency, the reactance of the high-frequency inductor L_1 is low when compared to r_1, so it does not significantly affect the line current waveform; hence, it can be neglected. Therefore, as shown also in Fig. 5.2,

$$r_1(t) = \frac{v_1(t)}{i_1(t)} \cong \frac{\langle v'_1(t)\rangle_{T_s}}{i_1(t)}, \tag{5.2}$$

where $\langle v'_1(t)\rangle_{T_s}$ is the average of v'_1 over one switching period T_s. Based on the operating principle of the converters and on the waveforms shown in Fig. 5.2, we calculated the expressions of $r_1(t)$. These, as well as the inherent PFC properties, are summarized in Table 5.1. The duality between selected fourth-order converters operating in DCVM and second-order converters operating in DICM is further highlighted by comparing Table 5.1 with Table 2.2.

It can be seen from Table 5.1 that DCVM operation offers inherent PFC property and that, from this point of view, the Ćuk converter is the best amongst the selected topologies. Indeed, its

input resistance is only a function of the duty-cycle d, switching period T_s and capacitance C. On the other hand, the input resistance of the other two selected topologies is dependent also on the normalized discharging time d_1 of capacitor C, and consequently on the ratio of inductor currents $i_2(t)/i_1(t)$, a dependence which degrades to a certain extent the inherent PFC property. The expressions of inductor currents $i_1(t)$ and $i_2(t)$ are not defined in Table 5.1, because they depend on whether L_2 is a low- or a high-frequency storage element.

Table 5.1. Inherent PFC properties of selected fourth-order switching converters operating in DCVM.

	Input resistance $r_1(t)$	**Inherent PFC**
Boost with an LC output filter	$r_1(t)=\frac{(1-d)^2 T_s}{2C}\left(1-\frac{i_2(t)}{i_1(t)}\right)$	**Fair** Improves when i_2/i_1 is decreased
Buck with an LC input filter	$r_1(t)=\frac{(1-d)^2 T_s}{2C}\frac{1}{\left(1-\frac{i_1(t)}{i_2(t)}\right)}$	**Fair** Improves when i_2/i_1 is increased
Ćuk	$r_1(t)=\frac{(1-d)^2 T_s}{2C}$	**Excellent**

In publication [P2], we consider that inductor L_2 is a low-frequency storage element. Therefore, i_2 is continuous over the line-cycle, constant for the theoretical case of infinite L_2, and it can be considered as the dual of the constant voltage V_2 in second-order converters. Let us consider also that the input voltage is the rectified line voltage $v_1(t)=V_1\cdot|\sin\omega_L t|$, and that the average input resistance r_1 is constant. Then, the input current has a sinusoidal shape $i_1(t)=I_1\cdot|\sin\omega_L t|$ and it can be considered as the dual of the rectified line voltage $v_1(t)=V_1\cdot|\sin\omega_L t|$ in second-order converters. With these assumptions, we can state that fourth-order converters operating in DCVM and second-order converters operating in DICM have dual behavior not only during one switching cycle, but throughout the line-cycle as well. We use the term *low-frequency duality* to refer to this behavior.

Following this general study, we select for further analysis the Buck converter with an LC input filter, which is redrawn in Fig. 5.3 together with its characteristic waveforms when operating in DCVM. The main reason for selecting it, even if its inherent PFC property is not perfect, is that it has the lowest voltage stress of the switches amongst the converters selected in the first phase. As can be seen from Fig. 5.2, the maximum voltage across the switches is the peak voltage across capacitor C. Hence, switch voltage stress is a major issue in DCVM and it must be minimized.

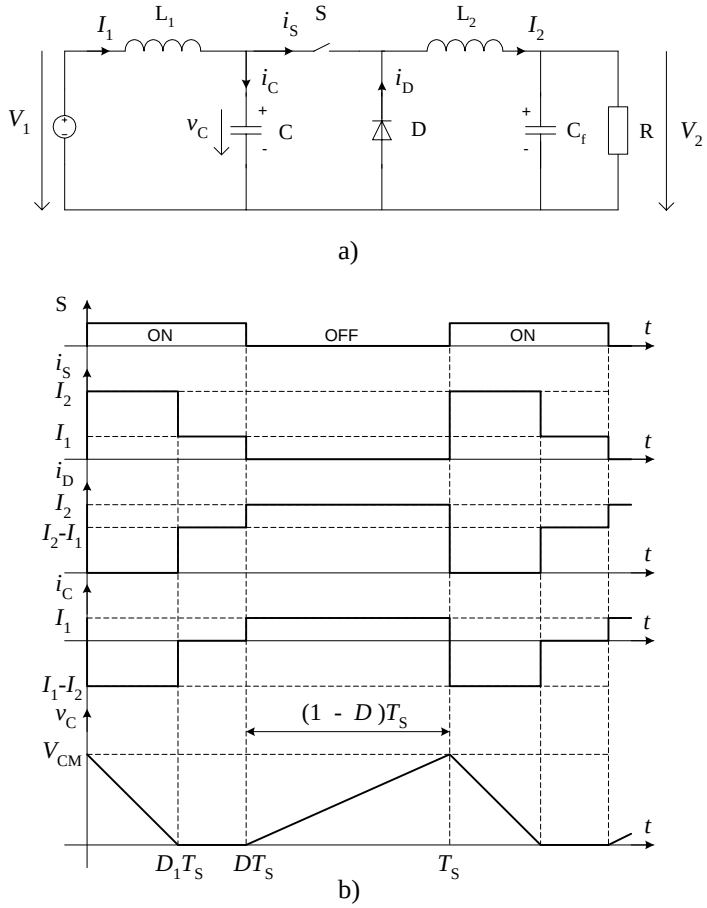


Fig. 5.3 Buck converter with an LC input filter: a) Schematic; b) Characteristic waveforms when operating in DCVM.

First, we make an analysis over one switching cycle, whose main results are the relationships for the normalized discharging time D_1 of capacitor C, the average input resistance R_1 and the voltage stress of the switches. These results are needed for the next step, when the operation with a rectified-sinusoid input voltage is analyzed. In addition, we identify the conditions to minimize the influence of the variable term i_2/i_1 on r_1, in other words the conditions to improve the inherent PFC

property. We define a coefficient $K_{\mathrm{PFC}} = (1-D)/D_1$, which should be as large as possible to minimize the aforementioned influence. It is found that coefficient K_{PFC} increases as the duty-cycle D decreases, and when the coefficient $K = 2T_s/(RC)$ increases. Hence, operation at low duty-cycle D and high K is favorable (e.g. we obtain $K_{\mathrm{PFC}} \cong 8$ with $D = 0.2$ and $K = 500$). In conclusion, inherent PFC property can be improved to a great extent by suitably selecting the operating conditions.

After the analysis over one switching cycle, we extend the analysis to a half line-cycle interval, considering operation with rectified-sinusoid input voltage. We calculate the conversion ratio $M_{\mathrm{SIN}} = V_2/V_1$, where V_2 is the output voltage and V_1 is the amplitude of the rectified-sinusoid input voltage, by equating the input and output energy over a half line-cycle. The conversion ratio is plotted in Fig. 5.4, for several values of coefficient K. The continuous line shows the conversion ratio when we take into account the influence of the variable term in r_1, whereas the dashed line shows the conversion ratio obtained by neglecting the variable term in r_1. As expected, the difference between the two results is very small at low duty-cycle D and high K, where the influence of the variable term in r_1 is minimal, and increases for higher duty-cycle D and/or lower K. Fig. 5.4 shows as well the boundary between DCVM and CCVM operation.

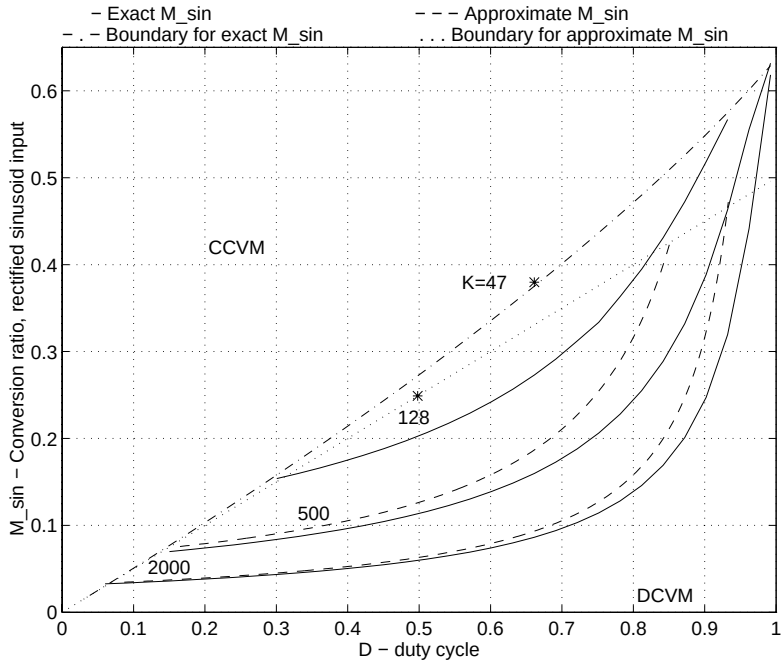


Fig. 5.4 Buck converter with an LC input filter operating in DCVM: the conversion ratio M_{SIN} when operating with a rectified-sinusoid input voltage and with L_2 as a low-frequency storage element.

Fig. 5.5 shows the switch voltage stress coefficient $K_S^{SIN} = V_S / V_1$, where V_S is the voltage stress of the switches and V_1 is the amplitude of the rectified-sinusoid input voltage. It can be seen that the voltage stress of the switches is quite high. The minimum switch voltage stress is $K_S^{SIN} = 2$, twice the amplitude of the rectified-sinusoid input voltage. It occurs when operating on the DCVM boundary, which is the horizontal axis in Fig. 5.5. The dashed line shows the limit of K_S^{SIN} when $K \to \infty$.

Finally, simulated waveforms for a 120W converter operating with a $220V_{rms}$ rectified input voltage and having a $24V_{dc}$ output voltage are presented in Fig. 5.6. They highlight the fact that, when the output inductor L_2 is a low-frequency storage element, operation is possible throughout the line-cycle and the input current does not have crossover distortions. This is due to the fact that the converter is actually a current step-up converter, which can operate whenever the input current is lower than the output current, and there is a low-frequency duality with the voltage step-up Boost converter.

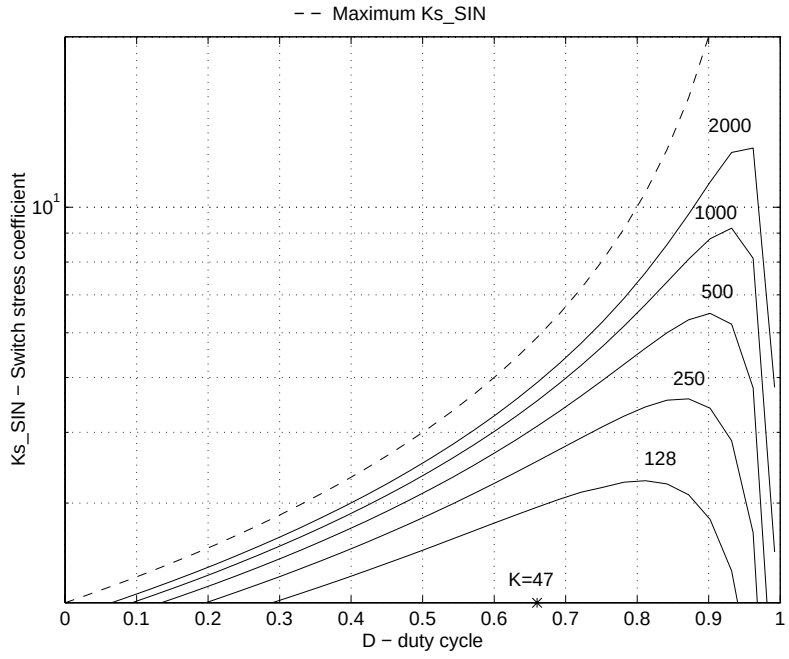


Fig. 5.5 Buck converter with an LC input filter operating in DCVM: the switch voltage stress coefficient K_S^{SIN} when operating with a rectified-sinusoid input voltage and with L_2 as a low-frequency storage element.

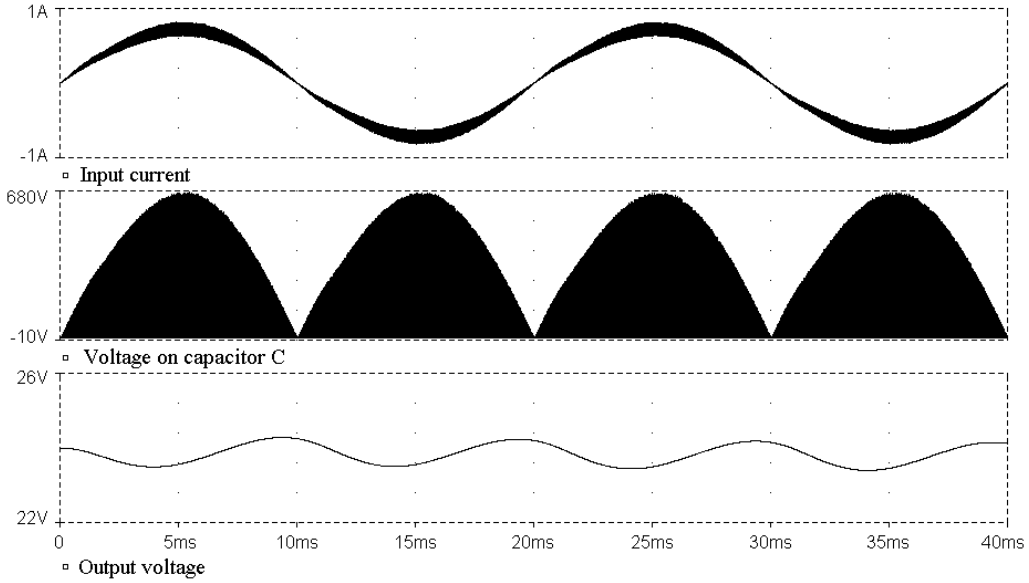


Fig. 5.6 Simulated waveforms: input current – upper trace; voltage on capacitor C – middle trace; output voltage – lower trace.

5.2.2 Publication [P3]

The low-frequency duality assumed in publication [P2] is obtained with L_1 as high-frequency and L_2 as low-frequency storage elements. However, this leads to a very large and impractical inductor L_2. Therefore, this assumption is relaxed in publication [P3], where we assume that both L_1 and L_2 are high-frequency storage elements, which leads to an easier implementation in practice. With this assumption, we present a comprehensive analysis of the converter from Fig. 5.3, when operating in DCVM as a high power factor rectifier. We determine important characteristics such as the conversion ratio, the boundary between DCVM and CCVM operation and the switch voltage stress, which are not presented in [Lee97]. When L_2 is a high-frequency storage element, the analyzed converter is the dual of the Boost converter operating in DICM only when we consider its operation over one switching cycle. We use the term *high-frequency duality* to describe this behavior.

First, we make an analysis over one switching cycle. Naturally, the characteristic waveforms are the same as those in publication [P2] and shown in Fig. 5.3 because, over one switching cycle, the converter behaves in a similar manner. Moreover, the analysis over one switching cycle is, to a great extent, similar.

Second, we extend the analysis to a half line-cycle interval and consider operation with rectified-sinusoid input voltage $v_1(t) = V_1 \cdot \left|\sin \omega_L t\right|$ and constant output voltage V_2. Inductor L_2 is only a high-frequency storage element, so its current varies over a half line-cycle from zero to a maximum. Consequently, the converter behavior over half line-cycle is different from that presented in publication [P2]. To be more precise, the converter behaves like a voltage step-down Buck converter, rather than a current step-up converter. As a result, it cannot operate when the instantaneous input voltage is lower than the output voltage. Hence, as shown in Fig. 5.7, the line current is zero outside the interval $t \in (t_1, T_L/2 - t_1)$, where $t_1 = \omega_L^{-1} \cdot \arcsin M_{SIN}$ and $M_{SIN} = V_2/V_1$ is the conversion ratio when operating with rectified-sinusoid input voltage. Operation with capacitor C in DCVM is possible only during the interval $t \in (t_2, T_L/2 - t_2)$, where $t_2 = \omega_L^{-1} \cdot \arcsin(M_{SIN}/D) > t_1$. It would appear that the inherent PFC property is lost during interval $t \in (t_1, t_2) \cup (T_L/2 - t_2, T_L/2 - t_1)$. However, the PFC property is maintained because inductor L_2 operates in DICM during this interval. By properly selecting inductance L_2, the input resistance with L_2 in DICM can be set close to the input resistance with C in DCVM, thus obtaining a smooth line current transition from one interval to the other, as depicted in Fig. 5.7.

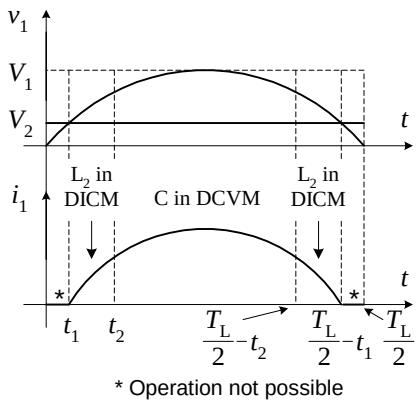


Fig. 5.7 Operating modes during a half line-cycle.

Considering the aforementioned issues, we determine the analytical expressions for the input resistance r_1, as well as for the inductor currents i_1 and i_2. Afterwards, the analysis proceeds in a similar manner as in publication [P2], by equating the input and output energy over a half line-cycle. In this publication we take into consideration the converter efficiency η, as well. We obtain the conversion ratio M_{SIN}, which is plotted in Fig. 5.8 for several values of the coefficient $K = 2T_s/(RC)$, and for two efficiencies, $\eta = 1$ and $\eta = 0.8$. Obviously, at a certain duty-cycle D,

the conversion ratio decreases for lower efficiency. The plot also shows the boundary between DCVM and CCVM operation. From Fig. 5.8, we can also see that, when the output current decreases (load resistance R increases, coefficient K decreases), the operating point moves upwards and eventually enters the CCVM region. Hence, DCVM operation is possible from a minimum load current upwards.

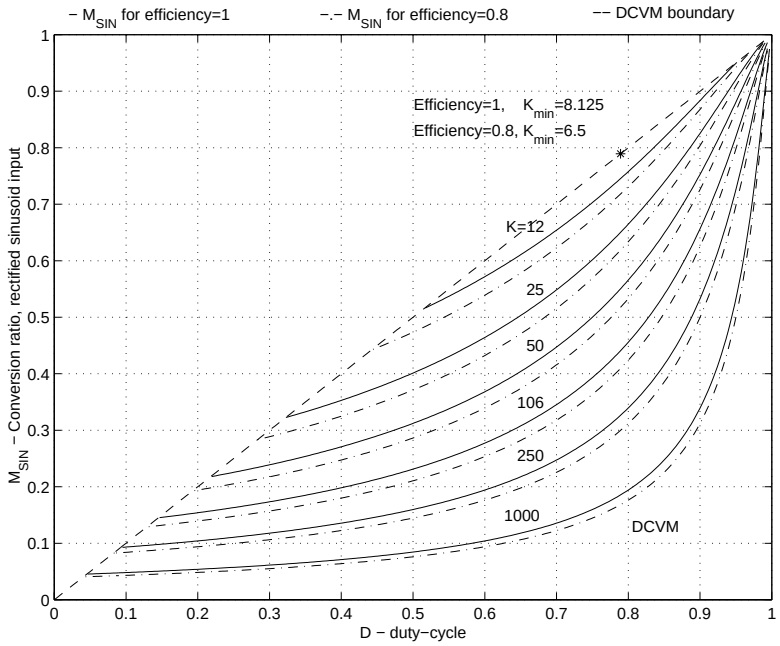


Fig. 5.8 Buck converter with an LC input filter operating in DCVM: the conversion ratio M_{SIN} when operating with a rectified-sinusoid input voltage and with L_2 as a high-frequency storage element.

The switch voltage stress coefficient $K_{\mathrm{S}}^{\mathrm{SIN}} = V_{\mathrm{S}}/V_1$ is plotted in Fig. 5.9. The boundary between DCVM and CCVM operation is at $K_{\mathrm{S}}^{\mathrm{SIN}} = 2$ and the dotted line identifies the limit of $K_{\mathrm{S}}^{\mathrm{SIN}}$ when $K \to \infty$. The switch voltage stress is dependent on the operating point and it is quite sensitive to its variations. For this reason, it is advantageous to keep the operating point fixed, in order to have both a constant conversion ratio and a well-defined switch voltage stress, when the load resistance R changes. This can be done by keeping the duty-cycle D constant and by changing the switching period T_{s}, in order to keep constant the coefficient $K = 2T_{\mathrm{s}}/(RC)$. In other words, fixed duty-cycle variable-frequency control should be used.

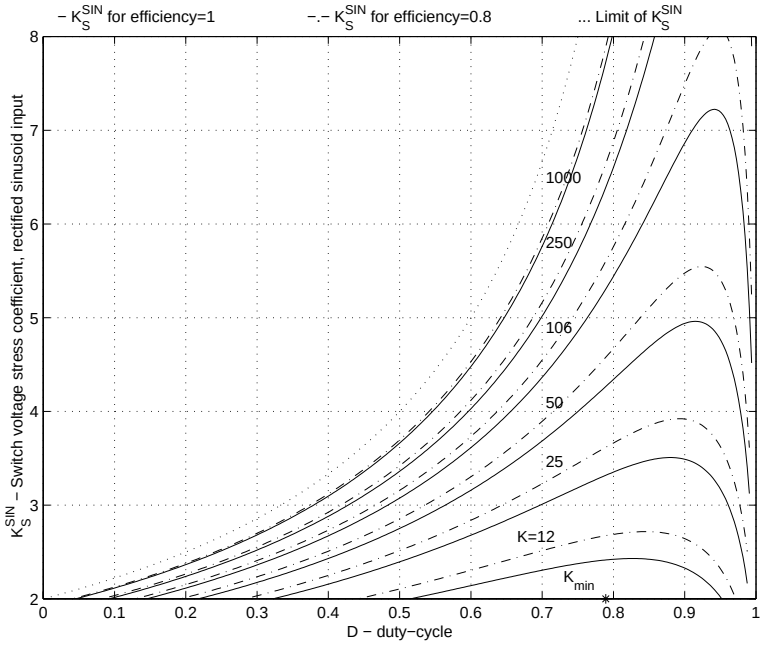


Fig. 5.9 Buck converter with an LC input filter operating in DCVM: the switch voltage stress coefficient K_S^{SIN} when operating with a rectified-sinusoid input voltage and with L_2 as a high-frequency storage element.

Based on the analytical results, we designed and constructed a 100W high power factor rectifier having a $48V_{dc}$ output voltage and operating with a $90\text{-}265V_{rms}$ universal input voltage. Theoretical and experimental results agree reasonably well for practical purposes. Operation in DCVM has a negative impact on efficiency. The turn-on of the active switch with high voltage across it greatly increases switching losses. In addition, the switches must be rated at a higher voltage as compared to CCVM operation; hence, they tend to have larger conduction losses. The measured efficiency is in the range of 80% for 100W output power and 100kHz switching frequency, and 85% for 50W output power and 50kHz switching frequency.

Line current waveforms are presented in Fig. 5.10. It can be seen that the line current has crossover distortions, as expected. However, its harmonic content is well below the limits specified in the IEC 1000-3-2 standard for Class A equipment. Generally speaking, the maximum power level for which compliance with the standard can be achieved decreases as the conversion ratio M_{SIN} increases: a larger M_{SIN} leads to longer interval where the converter cannot operate, hence to a higher harmonic content and a lower power for which compliance is achieved.

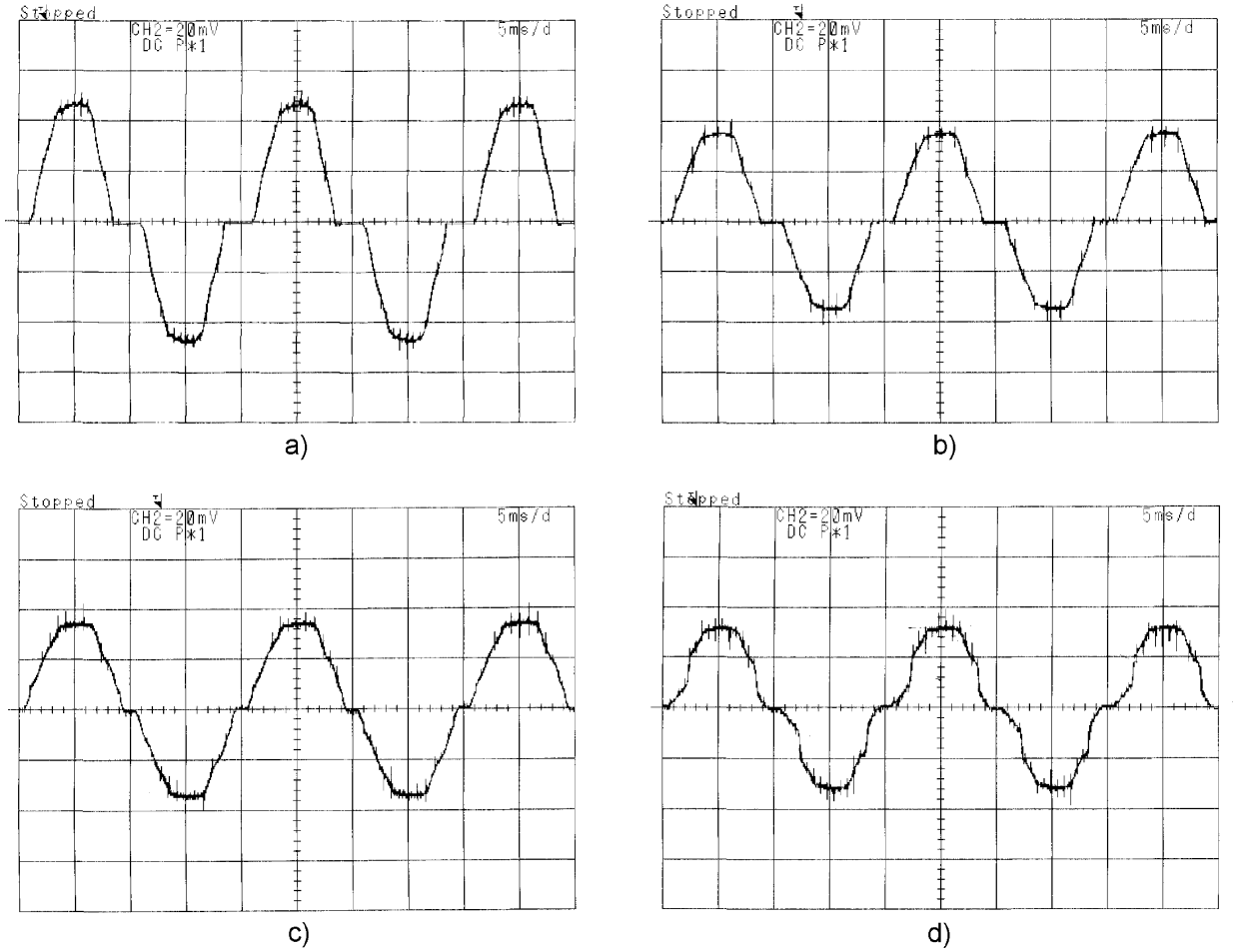


Fig. 5.10 Experimental line current at full load (100W) for: a) $90V_{rms}$ input, 1A/div; b) $110V_{rms}$ input, 1A/div; c) $220V_{rms}$ input, 0.5A/div; d) $255V_{rms}$ input, 0.5A/div. Time scale: 5ms/div.

5.2.3 Publication [P4]

The converters that are analyzed in publications [P2] and [P3] do not have galvanic isolation. This prompted our interest to investigate the possibility of implementing galvanic isolation, in addition to the general aims of this dissertation. In this publication, we analyze a Flyback-derived fourth-order converter. The converter and its characteristic waveforms when operating in DCVM are presented in Fig. 5.11. While the topology is similar to that of the BIFRED converter [Mad92], shown in Fig. 2.14, its operation is radically different. In the analyzed converter, both the input inductor and the magnetizing inductance of the transformer are high-frequency reactive elements and operate in CICM. The primary side capacitor operates in DCVM to ensure an inherent PFC property. In contrast, in the BIFRED converter, the primary side capacitor is a low-frequency storage element,

i.e. its voltage can be considered constant, and the input inductor operates in DICM to ensure an inherent PFC property.

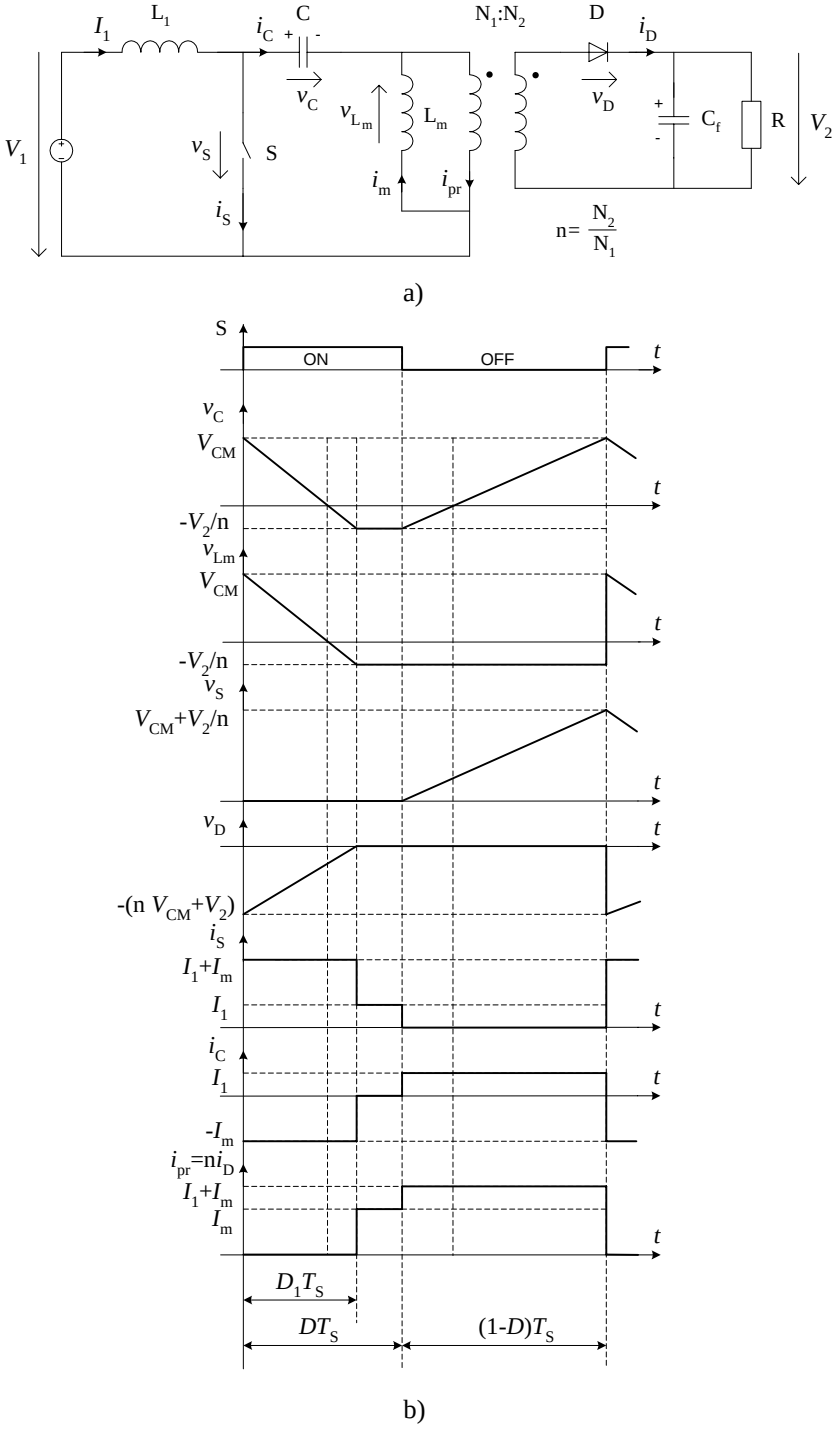


Fig. 5.11 Flyback-derived converter: a) Schematic; b) Characteristic waveforms when operating in DCVM.

First, an analysis over one switching cycle is made. This analysis reveals that the average input resistance of the converter is constant, meaning that the inherent PFC property is excellent. On the other hand, the voltage stress of the active switch is $V_S = 2V_1/(1-D)$. This is higher than for the Buck converter with an LC input filter operating in DCVM, in which the switch voltage stress is $V_S = 2V_1$ when operating on the DCVM border.

The analysis is then extended to a half line-cycle interval considering the operation with a rectified-sinusoid input voltage $v_1(t) = V_1 \cdot |\sin \omega_L t|$ and a constant output voltage V_2. The line current is sinusoidal because, besides having a constant average input resistance, the converter is able to operate throughout the line-cycle. These properties are similar to those of the Ćuk converter operating in DCVM, which were summarized in Table 5.1. With these considerations, we equate the input and output energy, taking into account the converter efficiency η, as well. The purpose is to calculate the conversion ratio $M_{SIN} = V_2/V_1$, the boundary between DCVM and CCVM operation, as well as the voltage stress coefficient $K_S^{SIN} = V_S/V_1$ of the active switch and the voltage stress coefficient $K_D^{SIN} = V_D/V_1$ of the secondary side diode. The conversion ratio M_{SIN} is plotted in Fig. 5.12 for several values of the coefficient $K = 2T_s/(RC)$ and for two efficiencies, $\eta = 1$ and $\eta = 0.8$. It is natural that the conversion ratio for a certain duty-cycle D decreases when the efficiency is lower. Interestingly, the conversion ratio is not dependent on the turns-ratio of the Flyback transformer. This can be easily explained by taking into account the fact that the output voltage V_2 is only a function of the input energy and of the load resistance R. Moreover, the input energy is determined by the average input resistance of the converter, which is not dependent on the turns-ratio.

However, the border between DCVM and CCVM operation is dependent on the turns-ratio $n = N_2/N_1$. From Fig. 5.12 we can see that the available DCVM operating area increases as the turns-ratio n increases. This is explained by the fact that the magnetizing current I_m, which discharges capacitor C as seen from Fig. 5.11, is proportional to the turns-ratio n. A higher n means a higher discharging current I_m; hence, a lower normalized discharging time D_1 and a larger area where the condition $D_1 < D$ is fulfilled and operation in DCVM is possible.

On the other hand, as seen from Fig. 5.13, the diode voltage stress coefficient K_D^{SIN} increases as well, as the turns-ratio n increases. In conclusion, while a larger n increases the area where DCVM is possible, it also raises the voltage stress of diode D. Hence, a trade-off must be made. However, the turns-ratio n does not affect the active switch voltage stress coefficient K_S^{SIN}, which, as seen from Fig. 5.13, is dependent only on the duty-cycle D.

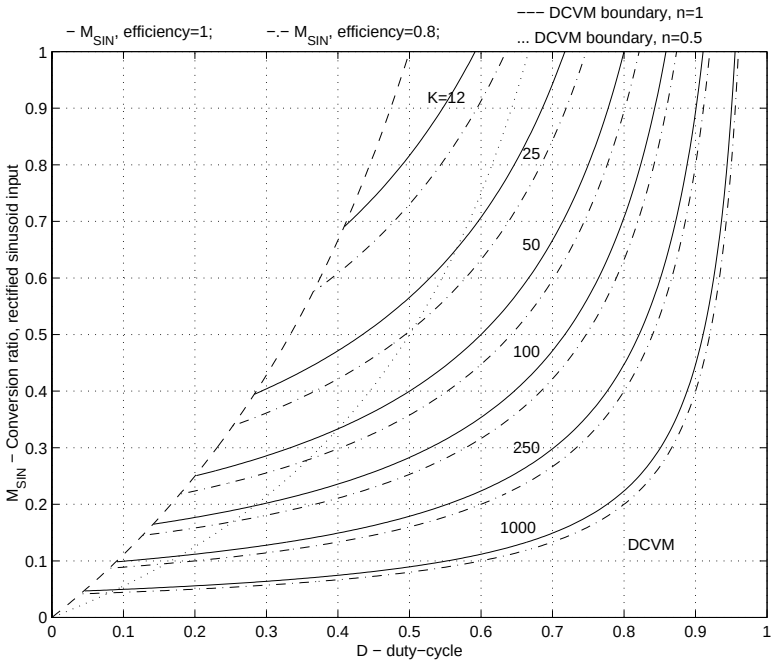


Fig. 5.12 Flyback-derived fourth-order converter operating in DCVM: the conversion ratio M_{SIN} when operating with a rectified-sinusoid input voltage.

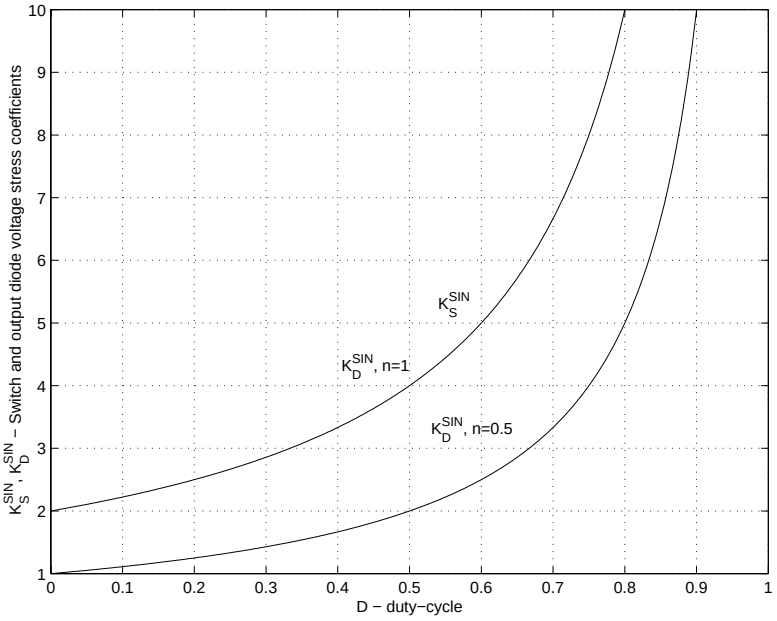


Fig. 5.13 Flyback-derived fourth-order converter operating in DCVM: the active switch voltage stress coefficient $K_{\mathrm{S}}^{\mathrm{SIN}}$ and the diode voltage stress coefficient $K_{\mathrm{D}}^{\mathrm{SIN}}$ when operating with a rectified-sinusoid input voltage.

As seen from Fig. 5.12, the operating point tends to leave the DCVM operating area when the load current decreases (load resistance R increases, coefficient K decreases). At the same time, as can be seen from Fig. 5.13, the switch voltage stress coefficients are dependent on the operating point, as well. This behavior is similar to that of the converter analyzed in publication [P3], and an analogue reasoning can be used to conclude that it is more advantageous to compensate for load variations by using fixed duty-cycle variable-frequency control, thus keeping the operating point fixed and having a well-defined switch voltage stress.

Based on the analytical results, an experimental circuit has been designed and built, with the purpose of validating the concept. The converter has $f_s = 100\text{kHz}$ switching frequency, a 50V_{rms} input voltage and a 20Ω load. The experimental output voltage is 10.5V_{dc}, while the theoretical value for $\eta = 0.8$ is 12.7V_{dc}. As for the experimental results from publication [P3], the difference between the experimental and theoretical results can be explained mainly by the fact that capacitor C is not operating in DCVM over the entire half line-cycle. The experimental results from Fig. 5.14 prove the inherent PFC property of the circuit and its ability to operate throughout the entire line-cycle.

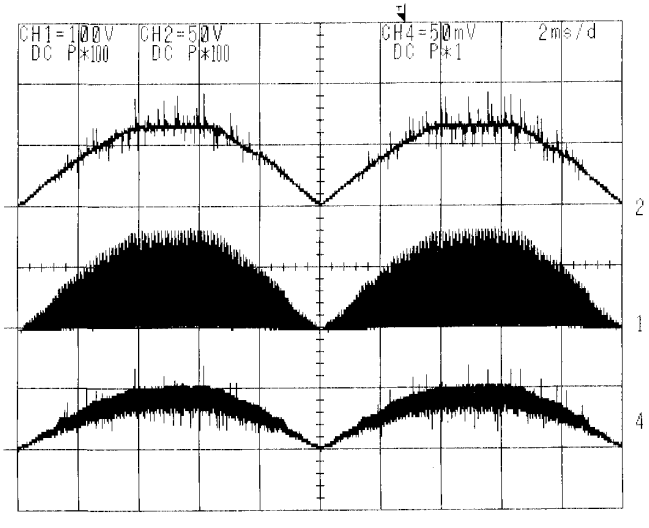


Fig. 5.14 Experimental waveforms: rectified line voltage – upper trace, 50V/div; switch voltage v_S – middle trace, 100V/div; inductor current i_1 – lower trace, 0.5A/div. Time scale: 2ms/div.

5.2.4 Conclusions of publications [P2]-[P4]

Publications [P2]-[P4] cover several aspects concerning the application of DCVM for PFC: an analysis of suitable fourth-order topologies, analysis of inherent PFC property offered by DCVM operation, the application of low-frequency and high-frequency duality, and the possibility of obtaining galvanic isolation. Besides the specific characteristics presented in each publication, several general conclusions can be drawn, regarding the operation of fourth-order converters in DCVM and their application for PFC.

- By choosing a suitable topology and using DCVM, it is possible to obtain simultaneously characteristics such as input and output currents with reduced high-frequency content, inherent PFC property, and step-down characteristic, aims that are stated in Chapter 1 of this dissertation. In addition, galvanic isolation can be implemented.

- DCVM operation is possible from a minimum load current upwards. The converter enters CCVM for a load current below the minimum. Conversely, DICM operation in second-order switching converters is possible up to a maximum load current. The converter enters CICM for a load current above the maximum.

- High switch voltage stress is associated with DCVM operation. Conversely, DICM operation implies high switch current stress.

- In DCVM, the active/passive switch turns off/on with zero voltage across it. Conversely, in DICM the active/passive switch turns on/off with zero current through it.

- In both DCVM and DICM, the operating point is load dependent. In DICM, variable duty-cycle fixed-frequency control can be used to compensate for load variations. However, analysis shows that in DCVM it is advantageous to use fixed duty-cycle variable-frequency control to compensate for load variations. Thus, the operating point is fixed and the switch voltage stress is well defined.

The characteristics of DCVM operation are summarized in Table 5.2 and compared with those of DICM operation, highlighting their duality. We can conclude that an inherent PFC property can be obtained while having an input current with reduced high-frequency content, at the expense of a high switch voltage stress and the need to use fixed duty-cycle variable-frequency control.

Table 5.2. Comparison of DICM and DCVM characteristics.

	DICM	**DCVM**
Switch stress	High current	High voltage
Discontinuous mode possible	From no load up to a certain maximum load current	From maximum load current down to a certain minimum load current
Control	Fixed-frequency Variable duty-cycle	Variable-frequency Fixed duty-cycle

5.3 Fourth-order switching converters operating in CCVM and CICM

5.3.1 Publication [P5]

In this publication, we investigate the application for PFC of a fourth-order converter having step-down characteristic and operating in CCVM and CICM. The topology, shown in Fig. 5.15 together with characteristic waveforms, has been presented in [Whi87] as a two-inductor Buck converter, and later on in [Tym88], with little or no analysis. Its application as a DC/DC converter has been reported in [Zha93]. We consider it interesting for a PFC application because it has a step-down characteristic and a continuous input current, which are two of the aims of this dissertation. Moreover, we apply the 'zero-ripple' technique in order to obtain an input current with very low ripple. Due to its operation in CICM and CCVM, the converter does not have an inherent PFC property, so a suitable control method (e.g. as shown in Fig. 2.12) has to be used to shape its input current.

Similar to the Buck converter, the converter under consideration cannot operate when the instantaneous voltage is lower than the output voltage. Therefore, when applying it for PFC, the resulting line current has crossover distortions. In the beginning, the aim is to select a modulation strategy. Several modulation strategies, which can be used when applying a step-down converter for PFC, are reviewed in this publication [Red92a], [Red96b]. They are differentiated by the method used to generate the reference for shaping the line current (v_{xy} in Fig. 2.12).

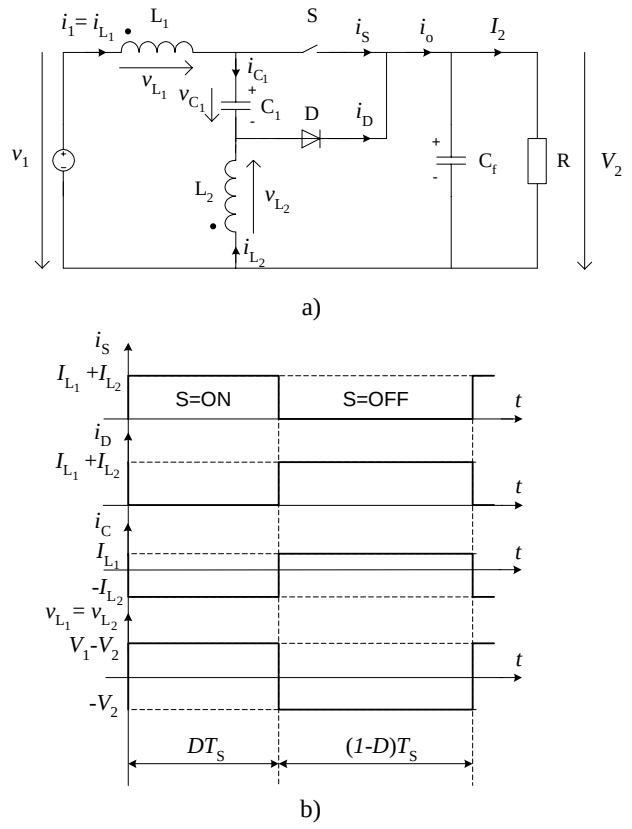


Fig. 5.15 Two-inductor Buck converter: a) Schematic; b) Characteristic waveforms when operating in CCVM.

We select the modified sine wave modulation, where the reference signal is proportional to the difference between the rectified line voltage and the output voltage. The main reason for this selection is that we choose to reference the control circuit to the positive output rail from Fig. 5.15, in order to avoid the need for an isolated gate driver for the active switch S. In this case, the difference between the rectified line voltage and the output voltage is readily available, and the modified sine wave modulation can be implemented easily.

The shape of the line current when using modified sine wave modulation is shown in Fig. 5.16. We compare it with the Class D template as defined by the first version of standard IEC 1000-3-2 [IEC95], with the purpose of determining the maximum output voltage that can be specified while having an operation in Class A. Although the definition of Class D has been changed recently, as explained in Chapter 1, the analysis was relevant at the time when [P5] was published, and therefore it is summarized here. Analysis shows that the line current with modified sine wave belonged to Class A if $V_2 < 0.7294 \cdot V_1$, where V_2 is the output voltage and V_1 is the amplitude of the rectified-sinusoid input voltage so, from this point of view, there was a relatively

large degree of freedom in specifying the output voltage. It is also shown that modified sine wave modulation gives compliance with Class A limits for a significant maximum input power, over a wide range of output voltages (e.g. almost 5kW for $230V_{rms}$ input voltage and $48V_{dc}$ output voltage).

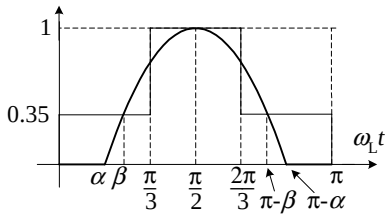


Fig. 5.16 Modified sine wave and Class D template.

Having considered the modulation issues, the analysis proceeds by determining the expressions of several important waveforms, which are plotted in Fig. 5.17, considering that the inductor currents and the voltage on capacitor C are constant over one switching cycle. The purpose of calculating the aforementioned expressions is twofold. First, the voltage and/or current stress of various components of the circuit can be calculated. Second, we obtain information concerning the variation of the operating point throughout the line-cycle, which is very important for the small-signal analysis that follows.

The small-signal analysis is made for the purpose of calculating transfer functions of the converter, which are needed to design the current loop of the control circuit (e.g. the characteristic $G_H(s)$ of the high-bandwidth controller in Fig. 2.12). The analysis is made using the averaged 'PWM switch' approach, in which the active switch S and the diode D are replaced with a time-invariant equivalent circuit that is obtained by averaging quantities over one switching period T_s. The resulting nonlinear circuit equations are linearized around the operating point and then the required transfer functions are calculated [Vor90b]. We calculate the control-to-input-current $H_{i_1-d}(s) = \hat{i}_1(s) / \hat{d}(s)$ transfer function, which is needed if the input current is sensed, as well as the control-to-switch-current $H_{i_S-d}(s) = \hat{i}_S(s) / \hat{d}(s)$ transfer function, which is needed if the switch current is sensed. The '^' character denotes small perturbations of the quantity around the operating point where the analysis is made. If we examine the circuit in Fig. 5.15, and take into account that we reference the control circuit to the positive output rail, it appears advantageous to sense the switch current in our application, so we use the control-to-switch-current transfer function.

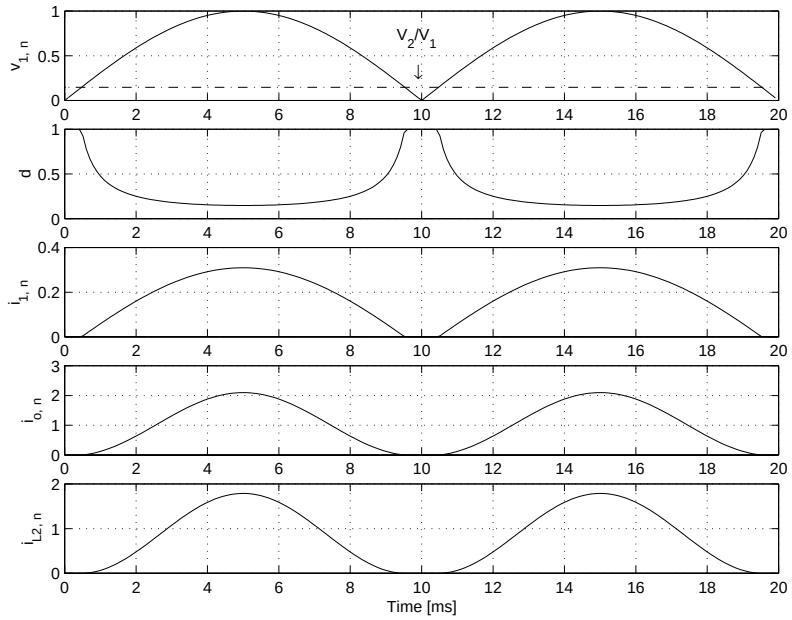


Fig. 5.17 Theoretical normalized waveforms of the two-inductor Buck converter when operating with a rectified-sinusoid input voltage, for $V_2 = 48\text{V}_{\text{dc}}$ and $V_1 = 230\text{V}_{\text{rms}}$. From the upper to the lower trace: $v_{1,\text{n}}$ - rectified-sinusoid input voltage v_1 normalized to the amplitude V_1; d - duty-cycle; $i_{1,\text{n}}$ - input current i_1 normalized to the load current I_2; $i_{\text{o,n}}$ - output current i_{o} normalized to the load current I_2; $i_{\text{L}_2,\text{n}}$ - current i_{L_2} normalized to the load current I_2.

In our analysis, we also take into account the fact that inductors L_1 and L_2 are coupled with coupling coefficient k, with the purpose of implementing the 'zero-ripple' technique. However, it would be unrealistic to consider that a coupling factor having exactly the 'zero-ripple' value k_{zr}, given by (3.6), can be implemented in practice. Therefore, we assume that k approaches k_{zr}, $k \to k_{\text{zr}}$.

The calculated transfer functions reveal the complex dynamics of the converter, which can be summarized as follows:

- The transfer functions' coefficients are functions of the duty-cycle D and of the normalized output current $i_{\text{o,n}}$, both of which have a large variation over a half line-cycle, as seen from Fig. 5.17. Therefore, the transfer functions are time-varying and their shapes change throughout the line-cycle. Under such circumstances, the stability of the converter can be assessed by using the quasi-static approximation, i.e. assuming that its dynamics are much faster than the variation of its operating point, and by checking the phase margin at several operating points throughout the line-cycle.

- The relative position of a zero in the control-to-switch-current transfer function is dependent on whether the coupling coefficient k is smaller or larger than the 'zero-ripple' value k_{zr}.

- Both transfer functions exhibit a pair of undamped complex conjugated poles, which may generate instabilities, as explained in Section 3.4.

Based on the theoretical analysis, we have designed and built a 200W rectifier, having a $48V_{dc}$ output voltage and operating with a $230V_{rms}$ input voltage and 100kHz switching frequency. Average current mode control was implemented successfully in the high-bandwidth controller. We used a series RC network connected in parallel to capacitor C_1, in order to damp the aforementioned complex conjugated poles. In this case, the control-to-switch-current transfer function was obtained by PSpice simulation and by using the average model of the converter. Experimental waveforms are presented in Fig. 5.18. As expected, the line current has crossover distortions, but compliance with standard IEC 1000-3-2 is comfortably achieved. By using the 'zero-ripple' technique, an input current with less than 50mA ripple was obtained. Finally, the measured efficiency was in the range of 88.5-92%.

In conclusion, we present in this paper the application for PFC of a fourth-order step-down converter, where 'zero-ripple' technique was applied. With this topology, we can achieve an output voltage lower than the amplitude of the line voltage, as well as an input current with very low ripple.

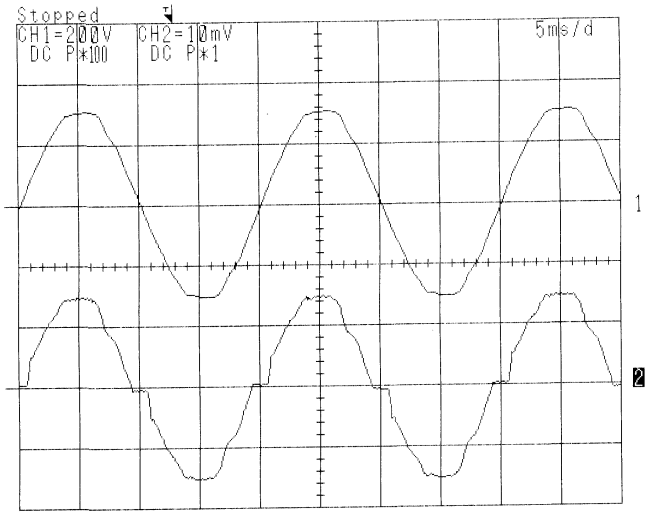


Fig. 5.18 Experimental waveforms: line voltage – upper trace, 200V/div; input current – lower trace, 1A/div. Time scale: 5ms/div.

5.4 Reduction of conduction losses

5.4.1 Publication [P6]

In this publication, we investigate the possibility of lowering the conduction losses of the AC/DC conversion stage with PFC, by reducing the number of switches in the power path. Four second-order topologies and a fourth-order one are analyzed and their conduction losses are estimated. We assume operation in CICM for the second-order topologies and operation in CICM and CCVM for the fourth-order one.

The well-known topology consisting of a cascaded diode bridge and a Boost converter is shown in Fig. 5.19, where $v_1(t) = V_1 \sin \omega_L t$. In this topology, which we use as a reference, there are always three switches in the power path, i.e. two diodes in the bridge plus one of the switches in the Boost converter.

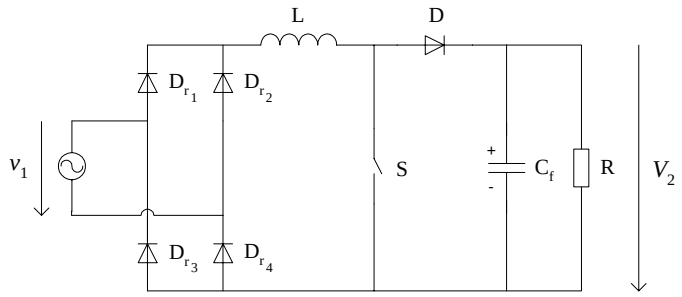


Fig. 5.19 Cascaded diode bridge and Boost converter PFC stage.

Topologies having fewer switches in the power path are presented in Fig. 5.20. Among them, those shown in Fig. 5.20 a)-c) are Boost-type. Their operation is essentially the same as that of the cascaded diode bridge and Boost converter; hence, the relationship between the conversion ratio and the duty-cycle d of the active switch(es) is:

$$\frac{V_2}{V_1 \left| \sin \omega_L t \right|} = \frac{1}{1-d}. \qquad (5.3)$$

The Boost-type PFC stage with a modified diode bridge, shown in Fig. 5.20a), has been presented in [Cho98]. There are three switches in the power path when the active switch S is conducting, i.e. D_a, S and D_{r_4} when $v_1 > 0$, or D_b, S and D_{r_3} when $v_1 < 0$. On the other hand,

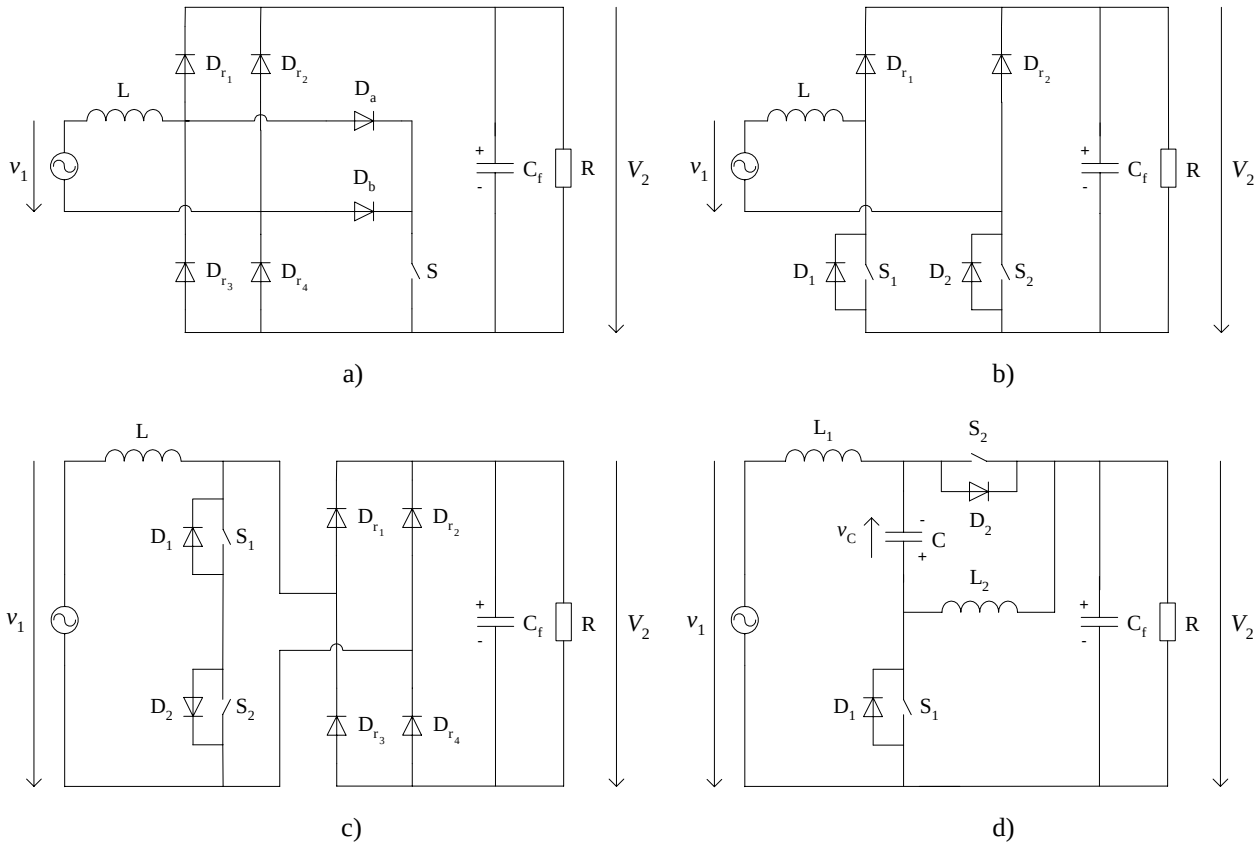


Fig. 5.20 Topologies for AC/DC conversion with PFC, having fewer switches in the power path: a) Boost-type PFC stage with a modified diode bridge; b) Boost-type PFC stage with two active switches; c) Boost-type PFC stage with a bi-directional switch; d) Fourth-order switching converter able to operate with a bipolar input voltage.

there are only two switches in the power path when the active switch S is not conducting, i.e. D_{r_1} and D_{r_4} when $v_1 > 0$, or D_{r_2} and D_{r_3} when $v_1 < 0$. It can be seen from (5.3) that the duty-cycle d is lower around the peak of the sinusoidal input voltage, when compared to the zero-crossings region. Assuming a sinusoidal variation of the line current, this means that the duty-cycle d is low when the line current is high; hence, much of the energy is transferred to the load during the off-time of the active switch S, when only two switches are in the power path. As a consequence, a good reduction in the conduction losses is expected.

The Boost-type PFC stage with two active switches, shown in Fig. 5.20b), has been presented in [Mar96]. In this topology, there are always only two switches in the power path. Therefore, conduction losses are reduced to an even greater extent, at the expense of an additional active switch. Similar observations apply for the Boost-type PFC stage with a bi-directional switch [Vin98], shown in Fig. 5.20c).

Let us now reconsider the topology from Fig. 5.19. We can see that the bipolar input voltage is first rectified, and then the resulting unipolar voltage is applied to the Boost converter. The Boost-type topologies from Fig. 5.20a)-c) rely on a rectification action, as well. The question arose if there is any switching converter topology that is able to operate with a bipolar input voltage while having unipolar output voltage, without relying on a rectification action, that is to say having a bipolar conversion ratio. The answer is positive: two fourth-order switching converters generated by *Cell G* from Fig. 3.1, i.e. *G1* and *G3* in [Tym88], are able to operate with bipolar input voltage and unipolar output voltage. Among them, topology *G3*, shown in Fig. 5.20d), is advantageous for a PFC application because its input current is continuous, while in the other one the input current is discontinuous.

During the positive half line-cycle, the active switch S_1 is controlled with duty-cycle *d*, and D_2 is the free-wheeling diode. The conversion ratio is:

$$\frac{V_2}{v_1} = \frac{1-d}{1-2d} \in (1, \infty), \quad v_1 > 0, \quad d < 0.5 . \tag{5.4}$$

On the other hand, during the negative half line-cycle, the active switch S_2 is controlled with the duty-cycle *d* and D_1 is the free-wheeling diode. In this case, the conversion ratio is:

$$\frac{V_2}{v_1} = -\frac{d}{1-2d} \in (0, \infty), \quad v_1 < 0, \quad d < 0.5 . \tag{5.5}$$

At first sight, this topology may offer a possibility to reduce the conduction losses, because only one switch is in the conduction path at any moment.

To compare the described topologies, we first determine the voltage and current stress of the switches. We consider sinusoidal variation of the input voltage $v_1(t) = V_1 \sin \omega_L t$ and constant output voltage V_2. We also assume that a control circuit shapes the input current to the sinusoidal waveform $i_1(t) = I_{1,\mathrm{rms}} \sqrt{2} \sin \omega_L t$, and that the duty-cycle *d* varies according to (5.3), (5.4) or (5.5), depending on the specific topology. With these assumptions, we determine the maximum voltage and current of the switches and, using the method described in [Eri97, pp. 604-608], we calculate the average and RMS currents of the switches. A first observation is that the maximum voltage and current of the switches are considerably larger in the topology from Fig. 5.20d), when compared to

the Boost-based topologies. For a topology with *k* active switches, a total active switch stress coefficient can be defined,

$$S_{\mathrm{a}} = \sum_{i=1}^{k} V_{i,\max} I_{i,\mathrm{rms}} , \tag{5.6}$$

where $V_{i,\max}$ is the maximum voltage and $I_{i,\mathrm{rms}}$ is the RMS current of the active switch S_i [Eri97, pp. 177]. Moreover, considering the converter load power P, an active switch utilization factor can be defined as:

$$U_{\mathrm{a}} = \frac{P}{S_{\mathrm{a}}} . \tag{5.7}$$

This factor depends not only on the voltage and current stress of the switches, but also on the number of active switches that are required; hence, it is a good measure for comparing various topologies. Factor U_{a} is plotted in Fig. 5.21 for the analyzed topologies, considering an universal input voltage $V_1 = 90 - 265\mathrm{V}_{\mathrm{rms}}$ and $V_2 = 400\mathrm{V}_{\mathrm{dc}}$ output voltage. The best switch utilization factor is achieved by the Boost-type topologies having only one active switch, followed by the Boost-type topologies having two active switches. The converter able to operate with bipolar input voltage has the lowest active switch utilization factor, due to the large voltage and current stress of the switches.

We then consider a case study, to compare the analyzed topologies from the conduction losses point of view. Besides the aforementioned input and output voltage specifications, we assume $P = 200\mathrm{W}$ and 100% efficiency. Conduction losses are estimated with the static models for on-state switching devices that are described in Section 4.1, and using in (4.1) and (4.2) the calculated expressions for the average and RMS currents of the switches. As device parameters, we used $V_{\mathrm{D}} = 0.6\mathrm{V}$ and $r_{\mathrm{D}} = 0.015\Omega$ for diodes, and $r_{\mathrm{DS}} = 0.8\Omega$ for the MOSFETs. The estimated conduction losses are plotted in Fig. 5.22, normalized to the conduction losses of the basic topology from Fig. 5.19, which is used as a reference for our analysis. The best reduction of the conduction losses is achieved by the two-switch Boost-type topologies from Fig. 5.20b)-c). Less improvement is obtained in the Boost-type PFC stage from Fig. 5.20a), which has nevertheless a better active switch utilization coefficient U_{a}. Finally, the converter which is able to operate with bipolar input voltage has higher conduction losses than the cascaded diode bridge and Boost converter. Even if it has only one switch in the power path, the conduction losses are high due to the larger current stress

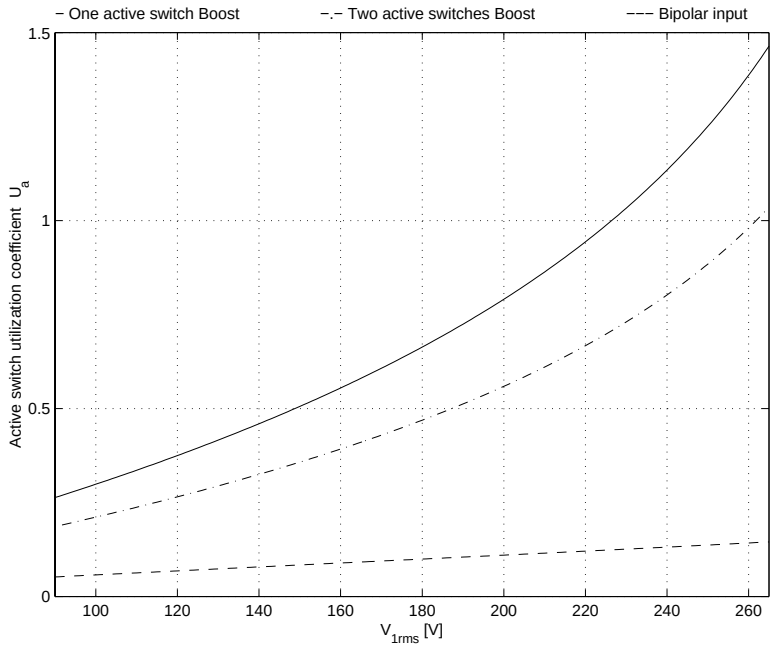


Fig. 5.21 Active switch utilization coefficient U_a .

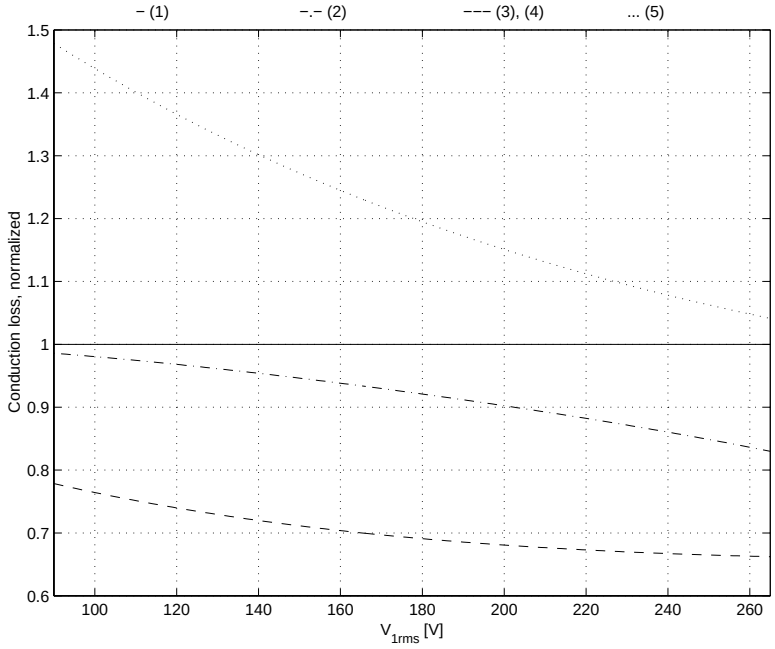


Fig. 5.22 Conduction losses for (1) cascaded diode bridge and Boost PFC stage from Fig. 5.19, (2) Boost-type PFC stage with a modified diode bridge from Fig. 5.20a), (3) Boost-type PFC stage with two active switches from Fig. 5.20b), (4) Boost-type PFC stage with a bi-directional switch from Fig. 5.20c) and (5) fourth-order switching converter able to operate with a bipolar input voltage from Fig. 5.20d). The values are normalized to the conduction losses of (1).

of the switches. We must also point out that this result has been obtained when using the same device parameters for all the analyzed topologies. However, higher voltage rated switches would have to be used in the converter that can operate with bipolar input, switches that tend to have even larger conduction losses.

5.5 Reduction of switching losses

5.5.1 Publication [P7]

In this publication, we present a novel ZVT Buck converter. The topology is shown in Fig. 5.23, where the load and the output filtering capacitor are modeled by the voltage source V_2. We assume that the active switch is a MOSFET, which is modeled by the ideal switch S_1, the body diode D_1 and the drain-source capacitance C_{DS}, which in Fig. 5.23 is included in C_1. ZVT is implemented by an auxiliary circuit, which we first reported in [Gri97]. The auxiliary circuit creates ZVS conditions for the active switch S_1 and limits the rate of change of the current through diode D at turn-off. It consists of the active switch S_r, diodes D_r and D_2, inductor L_r and capacitors C_1 and C_2. Besides C_{DS}, capacitor C_1 may eventually include an additional paralleled capacitor. When the main switch is turned off, the additional capacitor provides an alternative path for the current to reduce turn-off losses, and limits the rate of change of the switch voltage to reduce the EMI noise [Tse98b].

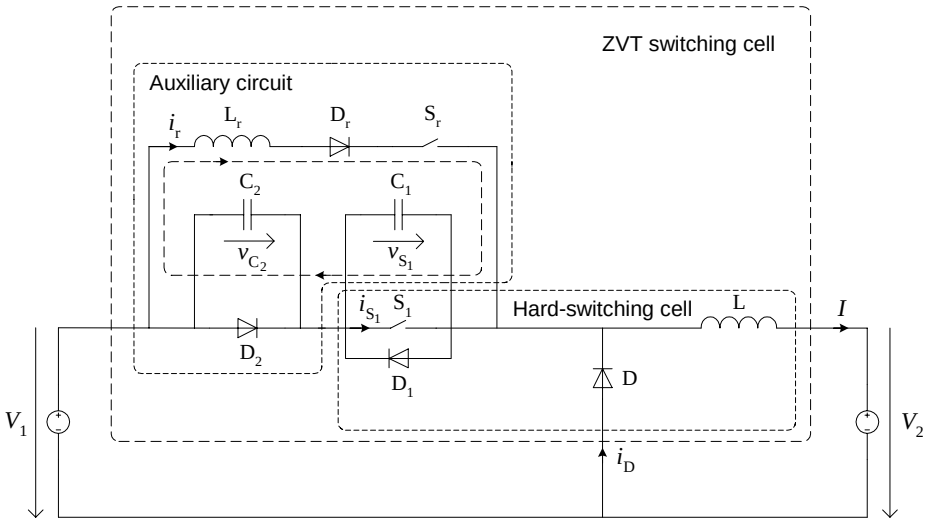


Fig. 5.23 ZVT Buck converter.

The operating principle is highlighted by the simulated waveforms from Fig. 5.24. The proposed topology basically makes use of a half-wave resonance, to transfer the energy from C_1 to the auxiliary capacitor C_2, from where it is recovered afterwards. The main switch S_1 turns on with ZVS, the auxiliary switch S_r turns off with ZCS, and the diode D has a controlled reverse recovery. When compared to other ZVT topologies having partially similar operating principle, the presented topology has certain advantages and disadvantages.

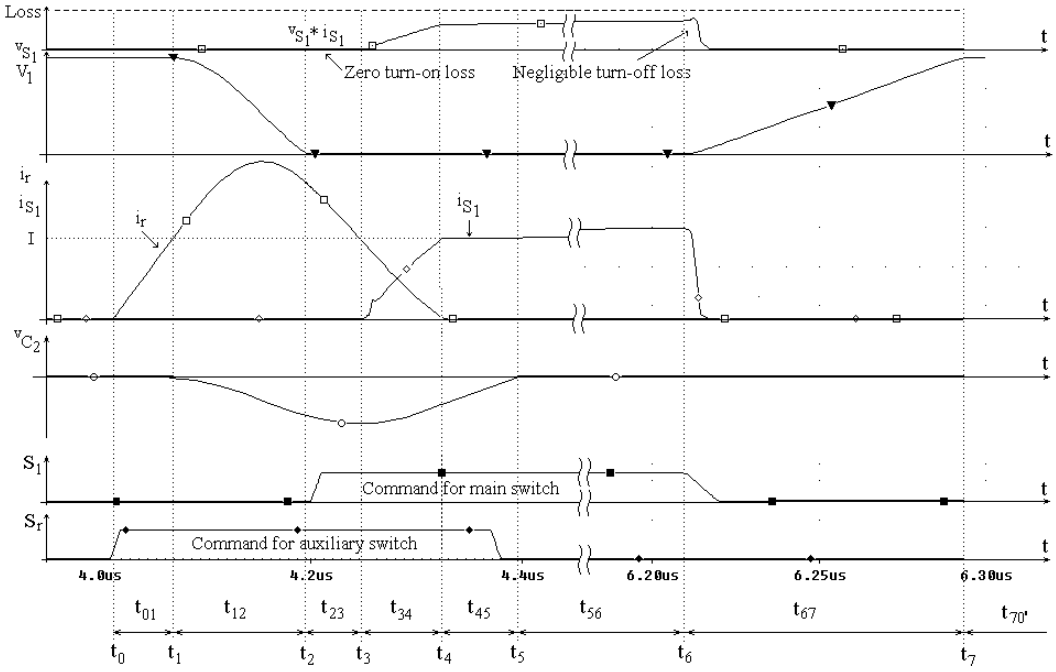


Fig. 5.24 Relevant simulated switching waveforms.

- The topologies presented in [Fre93] and [Hua94] make use of a half-wave resonance as well, to discharge capacitor C_1. However, in those topologies, the resonance is interrupted when C_1 is completely discharged and when there is still some energy left in the resonant inductor. In [Fre93], to ensure that this energy is recovered after the resonant process ends, the ratio V_2/V_1 of the output and input voltages must satisfy a condition that is dependent on the specific converter topology [Smi97]. For example, the condition is $V_1 < V_2/2$ in a Boost converter, which is major drawback for a PFC application. Nevertheless, the auxiliary switch turns off with ZCS. In [Hua94], there is no constraint on V_2/V_1, but the auxiliary switch turns off under hard-switching conditions. On the other hand, the topology presented in this publication has no constraint on V_2/V_1, and the auxiliary switch turns off with ZCS.

- The topology presented in [Mos95] uses an additional capacitor as well, to store temporarily the energy removed from C_1. However, it uses a full-wave resonance. i.e. the resonant current is allowed to reverse. During the negative half cycle, the resonant current flows through the main switch, increasing its current stress and the conduction losses. On the other hand, in the proposed topology there is no additional current stress for the main switch.

- The main disadvantage of the proposed topology is the diode D_2 placed in the power path, because it introduces additional conduction losses. In addition, the voltage stress of diode D_2 adds to the voltage stress of diode D. However, these drawbacks can be reduced to a certain extent. The voltage stress of D_2 is a function of the capacitances ratio C_2/C_1, the higher this ratio, the lower the voltage stress. Thus, by selecting a higher ratio C_2/C_1, the voltage stress of diode D_2 is reduced, and consequently the additional voltage stress of diode D. As a result, a diode rated at a lower voltage can be selected for D_2, with resultant reduced forward voltage drop and less conduction losses. On the other hand, the larger ratio C_2/C_1 translates into a longer resonant interval t_{14}, so a tradeoff must be made.

To conclude, we present in this publication a novel ZVT Buck topology, in which the main switch S_1 turns on with ZVS, the diode D has a controlled reverse recovery and the auxiliary switch S_r turns off with ZCS. The operating principle of the proposed topology can applied to a variety of switching converters, for either DC/DC or PFC applications, for example to the forward converter as presented in publication [P8], and to the PFC Boost converter as presented in [Bar98].

5.5.2 Publication [P8]

In this publication, we apply to a forward converter the ZVT technique described in publication [P7], with the aim of evaluating the benefits in terms of efficiency. As an application for the converter, we consider a 500W power factor corrected rectifier for telecommunications equipment. The schematic of the analyzed converter is shown in Fig. 5.25, where the auxiliary circuit for implementing ZVT has been added to the hard-switching converter.

The efficiencies of the hard-switching and ZVT forward converters are evaluated by simulation, which is done using MicroSim PSpice software and taking into account only the losses in the switching devices. The graphs of estimated efficiencies are plotted in Fig. 5.26, considering a 50-500W load range. The switching frequency is 110kHz. It can be seen that the efficiency is improved, approximately from 2% at light load to 5.5% at full load. The graphs of total losses in the hard-switching and in the ZVT forward converter are plotted in Fig. 5.27, which shows also the

distribution of losses between the main circuit and the auxiliary circuit in the ZVT converter. It can be concluded that, even if the auxiliary circuit for implementing ZVT introduces additional losses, the total losses are lower in the ZVT case when compared to the hard-switching case, hence the efficiency is improved.

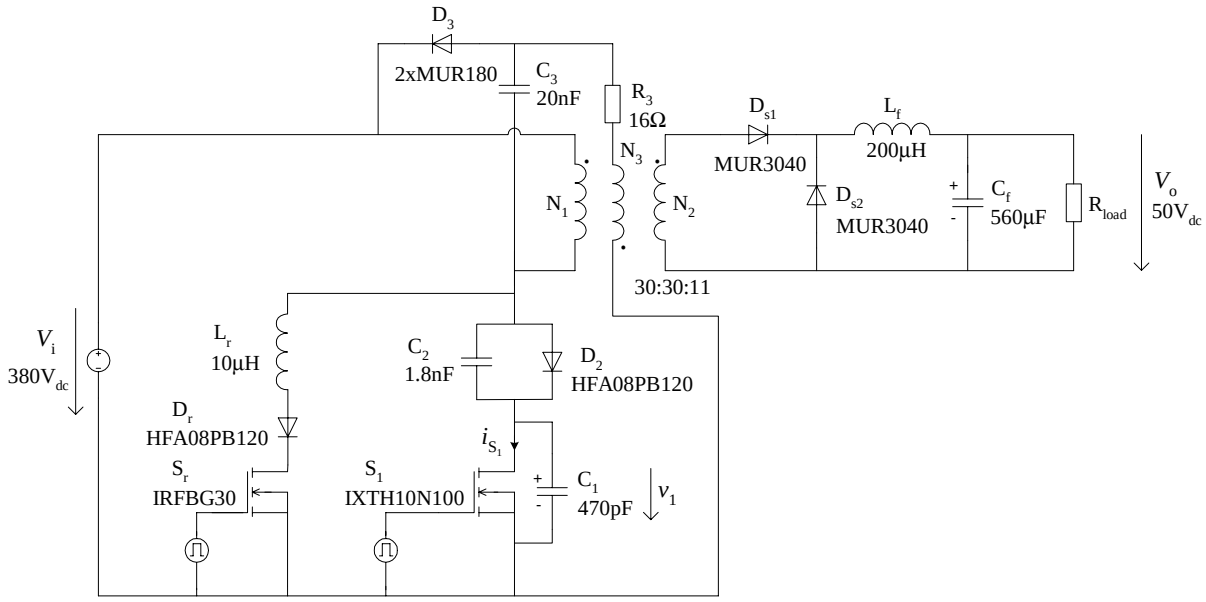


Fig. 5.25 ZVT Forward converter.

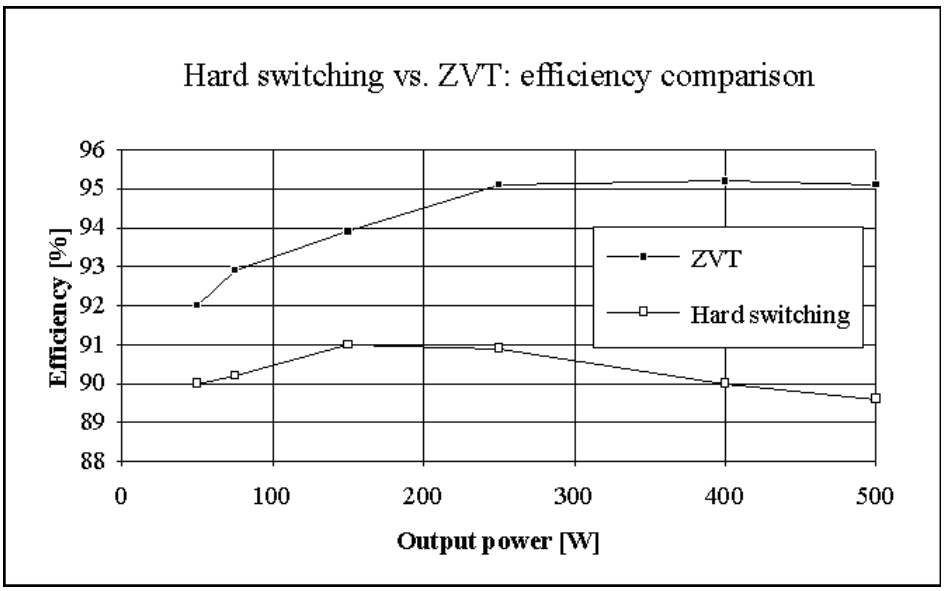


Fig. 5.26 Hard-switching vs. ZVT forward converter: efficiency comparison (simulated).

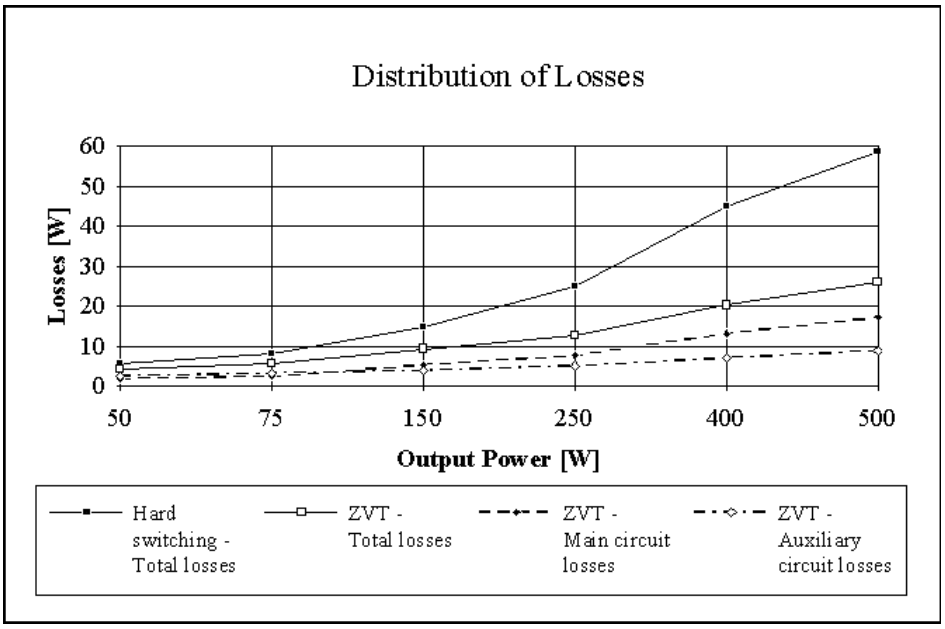


Fig. 5.27 Total losses with hard-switching vs. ZVT, and distribution of losses between the main circuit and the auxiliary circuit of the ZVT forward converter (simulated).

5.6 Contribution of the author

The author carried out the research work reported in publications [P1]-[P8] and, except for publication [P1], wrote the manuscripts alone. In publication [P1], the author wrote the major part of the manuscript. Lic. Tech. Jyri Rajamäki wrote the part that refers to the composite IEC (CISPR), FCC and VDE conducted EMI limits, as well as the part that summarizes the input filter design criteria. He also read the final text and commented it.

All the research work has been done under the guidance of Prof. Jorma Kyyrä, who provided valuable and constructive ideas. The regular academic discussions held with him played an important role in advancing the research process and the publication work. Prof. Kyyrä also read the manuscripts, gave useful scientific comments, and revised the language and the writing style.

The co-authors have seen the aforementioned description of the contributions and agree with it. None of the publications have been used as part of someone else's academic thesis or dissertation.

6 Conclusions and Discussions

This chapter summarizes the main results of the research. We also assess the scientific importance of the work and discuss possible future research topics.

6.1 Main results

We first analyzed the requirements for the EMI filter of a PFC stage based on a Boost converter operating in DICM. As expected, the differential-mode conducted EMI is larger in DICM when compared to CICM, when constant switching-frequency is used and for the same power level, which supports our motivation to investigate higher-order topologies. It was also shown that for both the constant and the variable switching-frequency cases, the input impedance of the converter is practically purely resistive and no instabilities can arise from the interaction with the EMI filter.

After that, we extended our research by examining two-switch fourth-order topologies, the aim being to explore the possibility of realizing a PFC stage having an input current with reduced high-frequency content, inherent PFC property and an output voltage lower than the amplitude of the sinusoidal input voltage.

We first considered the operation in DCVM and CICM, and three topologies were initially selected, i.e. the Boost converter with an LC output filter, the Buck converter with an LC input filter and the Ćuk converter. It was shown that, when operating in DCVM and CICM, the selected topologies have both inherent PFC properties and an input current with reduced high-frequency content. We also showed that, if both inductors are high-frequency storage elements, there is a high-frequency duality, i.e. over one switching cycle, between the selected topologies and the second-order topologies operating in DICM. On the other hand, if the output inductor is a low-frequency storage element, then a low-frequency duality is obtained, meaning that the duality applies for the behavior over the line-cycle as well. After these considerations, we selected the Buck converter with an LC input filter for further investigation, because it has the lowest switch voltage stress of the topologies selected in the first phase, and an output voltage lower than the amplitude of the sinusoidal input voltage can be obtained. We present an extensive analysis of both the operation with low-frequency and high-frequency output inductor. Important characteristics are determined, such as the conversion ratio and the switch voltage stress when operating with a rectified-sinusoid input voltage, as well as design criteria. A simulation example is presented for the low-frequency output inductor case, showing that a nearly sinusoidal line current can be obtained in this case. For

the high-frequency output inductor case, a prototype has been designed and built. As expected, the line current has crossover distortions, but the harmonic content is well below the standard limits. The simulated and experimental results confirm the analytical ones, as well as the functionality of the Buck converter with an LC input filter as a power factor corrector, when operating in DCVM and CICM.

The possibility of implementing galvanic isolation has been addressed, as well. We presented a Flyback-derived fourth-order topology operating in DCVM and CICM, for which an extensive analysis was performed and a prototype has been built. The converter has excellent inherent PFC properties and the line current is sinusoidal, as confirmed by the experimental waveforms.

A major conclusion from the analysis of fourth-order converters operating in DCVM and CICM is that, while offering both inherent PFC properties and an input current with reduced high-frequency content, this operating mode leads to high switch voltage stress. Nevertheless, the switch voltage stress can be minimized to a certain extent by properly selecting the operating point of the converter.

Operation in CCVM and CICM was considered as well, for a two-switch fourth-order topology having both step-down conversion ratio and continuous input current. The ripple of the input current can be reduced to a great extent by coupling the two inductors with a suitable coupling coefficient, i.e. by using the ‘zero-ripple’ technique. Small-signal analysis was used to derive the control-to-input-current and the control-to-switch-current transfer functions, which are needed to close the high-bandwidth current loop. The transfer functions reveal the complex dynamics of the converter, and the existence of a pair of complex conjugated poles that need to be damped to avoid instabilities. A prototype has been designed and built, in which average current mode control has been implemented successfully and an input current with very low ripple has been obtained by using the ‘zero-ripple’ technique.

The focus of the research then shifted towards reducing the conduction losses in the combined diode bridge and Boost converter. Therefore, we investigated topologies having fewer switches in the power path: one Boost-type topology with a modified diode bridge, two Boost-type topologies having two active switches, as well as a fourth-order topology that is able to operate with a bipolar input voltage. At first sight, the fourth-order converter topology is very attractive, because it has only one switch in the power path. It can realize direct AC/DC conversion with PFC, without the need for a diode bridge to perform the rectification of the input voltage. The conclusion of this analysis is that the best reduction of the conduction losses is obtained in the Boost-type topologies

having two active switches, while the Boost-type topology with modified diode bridge is a good cost/performance tradeoff. The fourth-order topology, while initially attractive, is subjected to high voltage and current stress of the switches. Therefore, even if it has only one switch in the power path, it has higher conduction losses.

Finally, we concentrated on reducing the switching losses by using ZVS and we proposed a novel ZVT Buck converter. We then applied the proposed technique to a 500W forward converter, for which simulations show an efficiency improvement approximately from 2% at light load to 5.5% at full load. Even if the technique is presented for DC/DC applications, its versatility allows the application to converters used for PFC applications as well.

6.2 Scientific importance of the author's work

In this dissertation, we have investigated several issues concerning the application of various topologies in single-phase PFC. We considered in the beginning the application of the DICM Boost converter for PFC, for which we used an averaging method to calculate the input impedance characteristic. It has been recognized that in a PFC application the converter is not operating in a stationary state, meaning that the current through the output capacitor has a DC component, when we consider the operation over one switching cycle. Therefore, a stationary state equivalent circuit must be used.

After that, special attention has been given to fourth-order topologies, as means for obtaining characteristics that otherwise cannot be obtained in second-order ones. All the two-switch fourth-order topologies that can be generated from the switching cells presented in Section 3.1 have been carefully examined. Among them, those considered as representative for our aims were selected and analyzed in our publications.

We have pointed out the duality that exists between the selected fourth-order converters operating in DCVM and CICM, and second-order converters operating in DICM. A thorough analysis of the Buck converter with an LC input filter operating in DCVM and CICM has been made, which enables a very good understanding of the advantages and disadvantages offered by this operating mode. In addition, the analytical results represent a concrete design tool, which was not available previously. We have also analyzed a fourth-order topology with galvanic isolation, operating in the DCVM in CICM, operating mode that has not been considered before for this topology.

The fourth-order topology with step-down characteristic and operating in CCVM and CICM has been used in the past in DC/DC applications. However, its application for PFC has not been proposed nor studied. We demonstrate its applicability as a power factor corrector, when an output voltage lower than the amplitude of the input voltage, as well as a low high-frequency content of the input current, are needed. The small-signal analysis was particularly useful, as it shows the complex dynamics of the converter. The analysis takes into account the coupling factor used to reduce the ripple of the input current, as well as the variation of the operating point of the converter throughout the line-cycle.

Besides comparing several Boost-type topologies with lower conduction losses, we have pointed out the possibility of performing direct AC/DC conversion with PFC. This can be done by using a fourth-order topology able to operate with a bipolar input voltage, the aim being the reduction of the conduction losses. Unfortunately, the analysis shows that conduction losses are not decreased, because of the higher current stress of the switches.

Even if the analyzed fourth-order topologies cannot be considered as being new, several aspects concerning their application for PFC, which have been discussed in this section, are original. The number of topologies that are analyzed in our papers is inherently limited. However, the information concerning the characteristics of a specific operating mode is of course useful when analyzing other fourth-order topologies in the same operating mode. In addition, the methodology that is used in our publications can be applied to the entire class of fourth-order converters, be it for example an analysis of the DCVM and CICM operation, or the small-signal analysis of the CCVM and CICM operation.

Finally, we have presented an original ZVT topology, which is based on the principle of creating a half-wave resonance to transfer the charge from the parasitic capacitance of the active switch to an auxiliary capacitor, from where it is recovered afterwards. This technique can be used in a variety of converters, for either DC/DC or PFC applications.

6.3 Topics for future research

In this dissertation, we have analyzed the application for PFC of only few of the fourth-order topologies. Other topologies might offer characteristics that are interesting for specific applications and therefore could be worth investigating. We have also seen that the ‘zero-ripple’ technique can be applied in fourth-order converters. However, in a PFC application, its effectiveness is restricted

by the limited amount of capacitance that can be used in the fourth-order switching cell. This is an issue that it is worth investigating in more detail.

Finally, more specific design criteria for the proposed ZVT Buck converter should be derived. In addition to that, the application of the proposed ZVT technique to other types of converters is worth investigating. Its operating principle might also prove useful in developing other types of ZVT converters.

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