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Hardware implementation of an energy adaptive resource-scalable wireless sensor node

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ABSTRACT OF THE
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In this thesis, hardware implementation of an energy adaptive resource-scalable wireless sensor node is presented. The node is designed by using commercial off-the-shelf components. Special attention is paid on minimizing the total power consumption in order to find out what levels are achievable with current state-of-the-art devices.

The designed node holds many advantages over conventional wireless sensor nodes which are often strictly application-specific and require extensive hardware and software modifications when used for other applications. Re-usability of the node hardware reduces the required effort and cost when developing new applications. Sensors or additional resources can be easily attached to the node as separate boards.

Part of energy adaptivity is the possibility for energy autonomous operation. The node can harvest ambient energy through specific elements that convert physical phenomena into electricity. Required conditions for energy autonomous operation are studied and analysed in the thesis. Power consumption of the node is characterized by performing measurements with different clock and power -related settings. The results show that the minimum power consumption of the node is approximately 140 μW while the maximum power consumption is approximately 85 mW. Measurement results are presented in the thesis and are used to estimate required size for the harvesting element.

Keywords: Wireless sensor node, modularity, energy adaptivity, resource scaling, energy autonomous operation, energy harvesting

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Tässä työssä esitellään kaupallisesti saatavilla oleviin komponentteihin perustuva langattoman, energia-adaptiivisen anturilaitteen toteutus. Laitteen laskentaresurssit ovat määriteltävissä laskentatarpeen mukaan. Keskeinen optimoitava suure suunnittelussa on laitteen kokonaistehonkulutus, mikä on pyritty minimoimaan, jotta laite voisi toimia autonomisesti keräten tarvitsemansa energian sisätilavalosta. Työssä on myös selvitetty laitteen eri osien vaikutus tehonkulutukseen.

Suunnitellulla anturilaitteella on monia etuja tavanomaiseen langattomaan anturilaitteeseen nähden. Tyypilliset toteutukset ovat sovelluskohtaisia ja niiden muuntaminen toiseen käyttötarkoitukseen edellyttää suuria muutoksia laitteistossa ja ohjelmistoissa. Tässä työssä toteutettua anturilaitetta voidaan käyttää ilman laitteistomuutoksia moniin eri tarkoituksiin ja sen ominaisuuksia voidaan laajentaa yksinkertaisilla laajennusmoduuleilla.

Olennainen osa energia-adaptiivisuutta on kyky toimia autonomisesti. Anturilaite kykenee keräämään ympäristöstään energiaa käyttäen elementtejä, jotka muuntavat valosähköisen, mekaanisen tai termisen energian sähköiseksi tehoksi. Tämän työn tavoitteena on määritellä laiteen minimienergiankulutusvaatimukset ja energiantuotantokapasiteettivaatimukset energiakeräimelle autonomisen toiminnan mahdollistamiseksi. Laitteen tehonkulutus on mitattu useilla kellotaajuus- ja toimintatila-asetuksilla. Tulokset osoittavat, että pienin saavutettavissa oleva tehonkulutus on noin 140 μW ja maksimitehonkulutus noin 85 mW. Työssä esiteltyjen mittausten perusteella voidaan määritellä laitteen tarvitseman energiankeräimen koko.

Avainsanat: Langaton anturilaite, modulaarisuus, energia-adaptiivisuus, laskentaresurssien skaalaaminen, autonominen toiminta, energian kerääminen

Preface

I would like to thank Department of Micro- and Nanosciences of Aalto University for the possibility of doing the thesis. I would also like to express my gratitude to my instructors Marko Kosunen and Hüseyin Yiğitler and to my thesis supervisor Jussi Ryynänen for providing good guidance throughout the project. The whole project has been a valuable learning experience for me and has taught me to become a better engineer.

Finally, I want to thank my family, friends and colleagues for their support. Lastly, I want to express my deepest gratitude to my fiancée Linda, without whose support any of this wouldn't be possible.

Otaniemi, 19.5.2015

Jani Hevosoja

Contents

Symbols and Abbreviations

Abbreviations

ADC	Analog-to-Digital Converter
BLE	Bluetooth Low Energy
CPU	Central Processing Unit
CPWG	Coplanar Waveguide with Lower Ground Plane
DMA	Direct Memory Access
FPGA	Field-Progammable Gate Array
GPIO	General Purpose Input/Output
IC	Integrated Circuit
ISM	Industrial, Scientific and Medical frequency band
LDO	Low-Dropout Regulator
LiPo	Lithium-Polymer
LLWU	Low-Leakage Wake-Up Unit
LNA	Low-Noise Amplifier
MAC	Media Access Control
MCU	Micro-Controller Unit
MEMS	Micro-Electro-Mechanical Systems
MPPT	Maximum Power Point Tracking
PA	Power Amplifier
PCB	Printed Circuit Board
PMU	Power Management Unit
PPC	Power Path Controller
PV	Photovoltaic
RAM	Random Access Memory
RF	Radio Frequency
RTOS	Real-Time Operating System

SFD	Start-of-Frame Delimiter
SoC	System-on-Chip
SPI	Serial Peripheral Interface
TEG	Thermoelectric Generator
TRCB	True Reverse Current Blocking
UART	Universal Asynchronous Receiver/Transmitter
WSN	Wireless Sensor Network

1 Introduction

Recent years have witnessed an increasing interest in Wireless Sensor Networks (WSNs) driven by advances in wireless communications, sensor technologies and digital electronics [1]. New energy-efficient protocols for different layers of WSNs are constantly being studied on and developed [2, 3]. As for sensors, advances in technologies such as Micro-Electro-Mechanical Systems (MEMS) have made it possible to manufacture low-cost, high-performance sensors that can be easily integrated in small size. Finally, the advances in digital electronics, combined with improved energy harvesting techniques, have made long-term deployment of wireless elements without a mains connection possible. With the aforementioned advances, WSNs have become a cost-effective alternative to traditional wired networks.

WSN consists of small low-cost devices called *nodes*, often also referred to as *motes*. These nodes are equipped with sensors to monitor physical and environmental conditions and a radio frequency (RF) transceiver to enable wireless communication between, for example, sensor node and a sink node. Sometimes it becomes desirable for the node to be able to make decisions and carry out actions based on gathered information. These nodes may require much better computational performance and more communication power than typical sensor nodes and are often more complex to design [4]. Significant trade-offs between power consumption and computational capacity must be made in such use-cases.

A large amount of literature has been published presenting various implementations of wireless sensor network nodes [5–11]. These nodes traditionally employ small batteries as a power supply. Once the battery depletes, it has to be manually replaced. In large networks, deployment and replacement costs can be magnitudes higher than the hardware costs [12]. This makes energy harvesting an ideal option for long-term deployment of such networks [13]. However, energy harvesting itself might not always be able to provide enough power to the system due to, for example, changes in ambient conditions. This is particularly harmful for applications where real-time operation is critical as a fading node might require reorganization of the network.

Many of the existing wireless sensor node implementations are strictly application-specific and require extensive hardware and software redesign if used for other applications. Some implementations utilize modularity [5, 8] to support a wider range of sensors and applications. Typically, these implementations allow only minor configurability outside of the sensor boards and may fail to provide the flexibility and extendibility required by an application [9, 11]. Since different parts of the network may have different requirements for processing and memory resources, it might become necessary to completely redesign certain modules.

This thesis presents hardware implementation of an energy adaptable resource-scalable wireless sensor node to address the aforementioned issues. The node is designed by using commercial off-the-shelf components. The design presented emphasizes on minimizing power consumption of the node in order to find out how low total power consumption can be reached with commercially available components. In addition to designing a power consumption optimized sensor node, an important

goal of this work is to identify and characterize the power consumption contributors of the sensor node in various operation modes. The characterization can be used to determine the required size and power output for the harvesting element. Furthermore, power consumption characterization identifies the most important points of development for IC and System-on-Chip (SoC) designers to further improve the building blocks of the node.

The designed node holds many advantages over traditional wireless sensor nodes which are typically designed for a single use-case scenario or support only a low number of sensors. This leads to low design re-usability since the system has to be designed all over for a different use-case scenario. Furthermore, extendibility of traditional wireless sensor nodes is low or non-existent. They also offer limited resource scalability and hardware flexibility. The node presented in this thesis addresses these by providing options for resource scaling, such as increased processing capability for computationally intensive applications, and hardware flexibility through sensor interface connectors, voltage-level translators and configurable supply voltages. Furthermore, the designed node supports energy autonomous operation so it can be deployed to places without mains connection or when the battery life-time is an issue.

Special emphasis is placed on energy autonomous operation of the node. Since available ambient energy levels can be extremely low especially in indoor conditions, the node is designed for the lowest possible power consumption. Any additional increase in the power consumption lowers the maximum attainable duty cycle. Furthermore, the node is able to function without assuming a pre-charged storage element by utilizing a robust automated zero-charge start-up unit. This unit improves efficiency during the initial charging phase and guarantees that the system is powered up only when there is sufficient power available.

The thesis is organized as follows. Next chapter presents an overview of the key areas of the design to provide necessary background information to the reader. Concepts energy adaptivity and resource scalability are introduced and discussed. In addition, limitations of the existing wireless sensor node implementations are discussed. Implemented node is presented in detail in Chapter 3. Finally, Chapter 4 presents measurement results for the designed node and defines the minimum power that an energy harvesting element must produce in order to achieve energy autonomous operation.

2 Background

This chapter of the thesis presents necessary background information to understand the design and operation of an energy adaptable resource-scalable wireless sensor node. First, the fundamental functional blocks of any wireless sensor node are presented and discussed briefly. The key features, namely, modularity, resource scalability and energy adaptivity of the proposed platform are discussed next. The chapter is concluded by introducing additional important considerations that must be addressed in the hardware design.

Implementation of an adaptable wireless sensor node that provides hardware modification flexibility and resource scalability to meet the requirements of different WSN applications has been published [9]. For many parts of the design, principles presented in the aforementioned publication are followed. This publication classifies the design challenges of such nodes around the following areas:

- Power management
- Timing management
- Inter-processor communications
- Abstraction software development.

Implementing an adaptable node platform requires both hardware and special software components. In this thesis, only the hardware is discussed in detail. Later in this Chapter, a brief overview of the software architecture is given.

2.1 Fundamental components of wireless sensor nodes

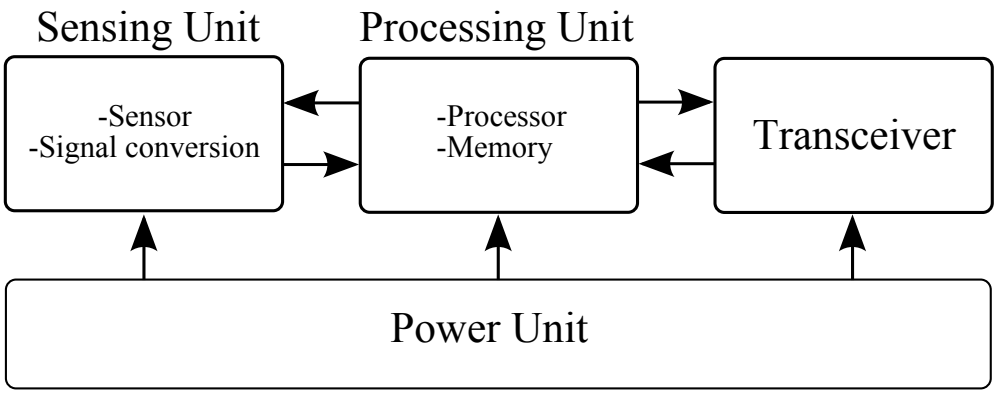

Figure 1: Fundamental components of wireless sensor nodes.

Figure 1 presents the fundamental components of a wireless sensor node [1]. Minimal implementation of a sensor node must include at least a sensing unit, processing unit, transceiver and a power unit. Sensing unit can consist of one or more sensors. Processing unit contains a processor core, memory for storing the

compiled program and variables and the necessary peripherals to interface with the sensor unit and the transceiver. Power unit, on the other hand, is responsible for generating appropriate supply voltages to the system from a selected power source which can be, for example, a battery or an energy harvester.

Depending on the level of integration, two or more of these fundamental units may be available as a single SoC solution. Modern commercial transceivers are often built around microcontrollers (MCUs) which provide processor core, memory and programmable I/O peripherals. For example, the transceiver used in the designed node is built around 8051-based MCU that provides various timers, serial interfaces and general-purpose input/output (GPIO) ports. The sensing unit can be connected directly to the appropriate pins of the SoC. The power unit, however, cannot be integrated since it must provide the power source to the system.

2.1.1 Transceiver

A wide range of different RF transceivers have been used in the published implementations. In works [5] and [10], a sub-1 GHz transceiver operating at 868 MHz industrial, scientific and medical (ISM) band is used. Work [6] on the other hand uses a special 315 MHz non-ISM band transceiver. Many commercial wireless sensor nodes, such as MICAz and TELOSB, are based on an IEEE 802.15.4 compliant RF transceiver operating at 2.4 GHz [14, 15]. Overall, the 2.4 GHz ISM band is by far the most used frequency band in WSN applications.

A sensor node conveys the collected information by means of wireless transceiver unit. Generally, these units can be selected based on the following list of the most important decision criteria:

- Estimated transmission range
- Required data rate
- Power consumption
- Level of integration.

Estimated transmission range can be used to solve the best frequency band for the transceiver. When the distance between sending and receiving node grows, lower frequencies may become desirable since attenuation is frequency-dependent. Required data rate sets a minimum requirement for throughput of the transceiver. Node may also be under strict power constraints which can set a limit for maximum allowed power consumption. Level of integration, on the other hand, defines how many external components are required to provide the necessary transceiver functionality.

2.1.2 Sensing unit

While in the early days sensors were bulky and expensive and effectively limited adoption of wireless sensor networks [12], MEMS technology enabled manufacturing sensors with physical dimensions in sub-mm scale. These sensors are manufactured

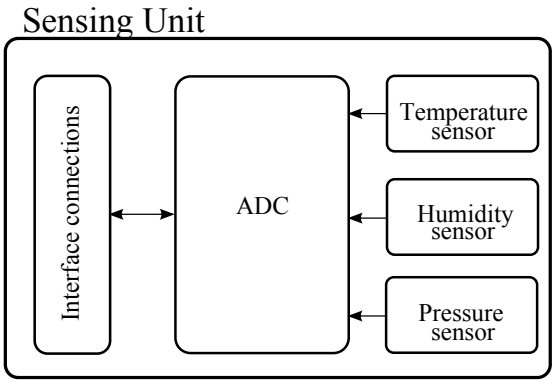

Figure 2: Example of a typical sensing unit.

using a semiconductor technique which also allows integration of electronic components on a single IC. This makes MEMS sensors ideal for wireless sensor network nodes which are often under strict cost and size constraints. However, it should be noted that not all sensors can be miniaturized due to, for example, applied mechanical stress or temperature.

Typical sensing unit of a wireless sensor node consists of at least one sensor, a method to convert output of the sensor to a suitable digital format and a well-defined interface for connections to the processing unit. An example of a such sensing unit is given in Figure 2. All these functionalities along with a small internal memory are integrated in modern sensors. It is easy to find commercial low-cost sensors [16] that provide, for example, a simple serial interface to configure the IC and to read the digitalized measurement result. In this case, to obtain the result, processing unit only has to read a specific memory location in the sensor's internal memory through the interface.

2.1.3 Processing unit

Figure 3 presents very simplified model of a typical wireless sensor node processing unit. Normally, MCUs consist of a central processing unit (CPU), non-volatile program memory, small amount of random access memory (RAM), clock generator and a set of peripherals. Therefore, a single MCU is capable of providing the necessary functions that a wireless sensor node minimally requires from the processing unit.

Increased level of integration has been a key element in reducing size and cost, two critical constraints of wireless sensor nodes. Since MCUs can provide peripherals such as ADCs , timers and serial interfaces, there is usually no need to provide these functionalities externally. As stated earlier, SoCs that combine an MCU and a transceiver are commercially available [17]. Thus, a simple wireless sensor node requires minimally only a few external components to function.

Most node implementations use an MCU-based processing unit. However, field-programmable gate array (FPGA) -based processing unit implementations have also been published [18]. These implementations, though, while providing good flexibility, are limited by power constraints of FPGAs [19]. This makes long-term deployments

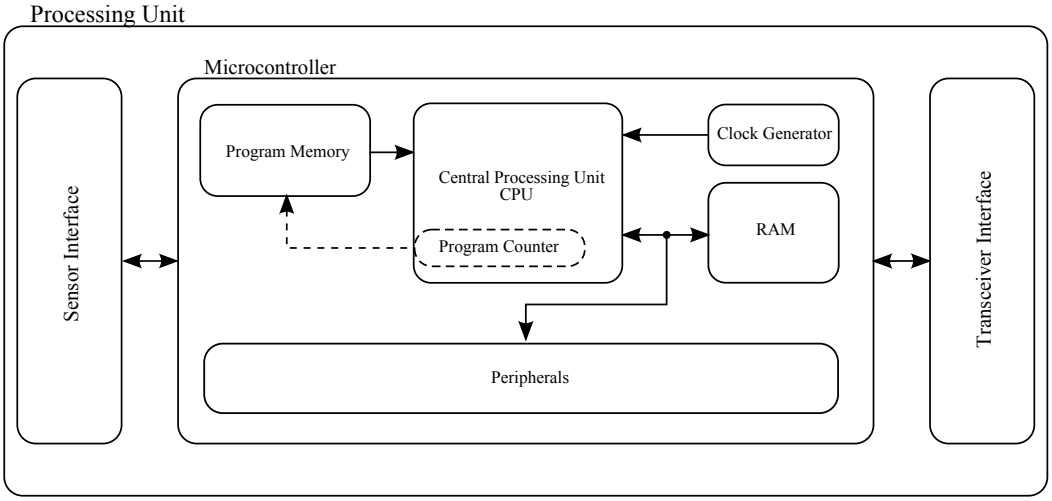

Figure 3: Typical processing unit of a wireless sensor node.

or energy autonomous operation extremely hard to implement with such nodes.

2.1.4 Power unit

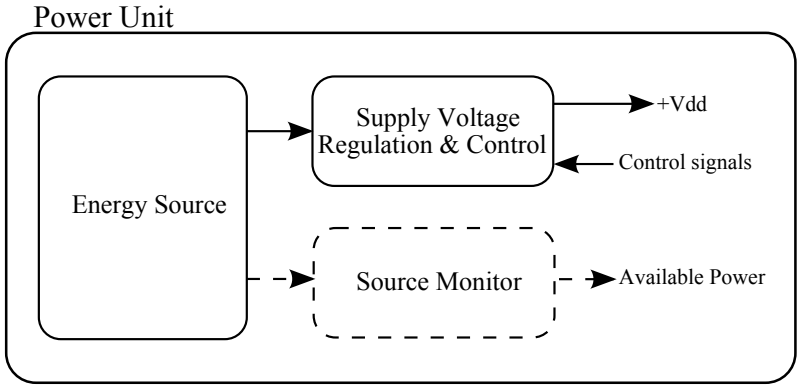

Figure 4: Power unit of a wireless sensor node.

Figure 4 illustrates the contents of a typical wireless sensor node power unit. Most wireless sensor node implementations are powered from a finite source such as a battery. Infinite energy sources, for example solar cells, have also been used successfully [13]. In addition to an energy source, power unit may have controllable regulators or additional circuitry and, optionally, a source monitoring circuitry. These source monitors are rarely implemented in the published node implementations.

Main responsibility of the power unit is to convert the voltage provided by an energy source to a convenient level in order to safely power the system. Switching DC-to-DC converters are often used due to their generally high efficiency compared to low-dropout regulators (LDO) . However, at extremely light loads in μA range, efficiency of the switching DC-to-DC converters tend to drop drastically due to frequency dependent losses [20]. Thus, in order to maximize the energy efficiency,

a power unit has to provide means to control state of the converter. Otherwise, quiescent current consumed by the converter itself becomes dominant while the system is in low-activity sleep mode.

2.2 Adaptive WSN nodes

2.2.1 Resource scalability

Processing and memory resources of wireless sensor nodes are usually predefined and cannot be scaled or extended without significant hardware and software modifications [9]. Traditional modular designs enable rapid prototyping of new sensor boards but do not directly address the resource scaling issues. Depending on the application, redesigning the power, processing or communications module may become necessary. Hence, these designs lack adaptability for the different energy, processing, memory and timing demands of different applications.

Figure 5 presents an example how to increase resource scalability of a SoC-based wireless sensor node. Processing and memory resources of a low-performance, resource-constrained SoC MCU are extended by connecting a high-performance MCU through a high-speed interface. The high-performance MCU, labeled as *main controller* throughout the thesis, provides increased processing performance, better energy efficiency and offers more flexibility than the SoC MCU. Similarly, resources can be extended even further by supporting MCUs on the extension boards. This sets further requirements for the node software, however, since properties such as architecture and connection interface of the MCUs should be kept arbitrary.

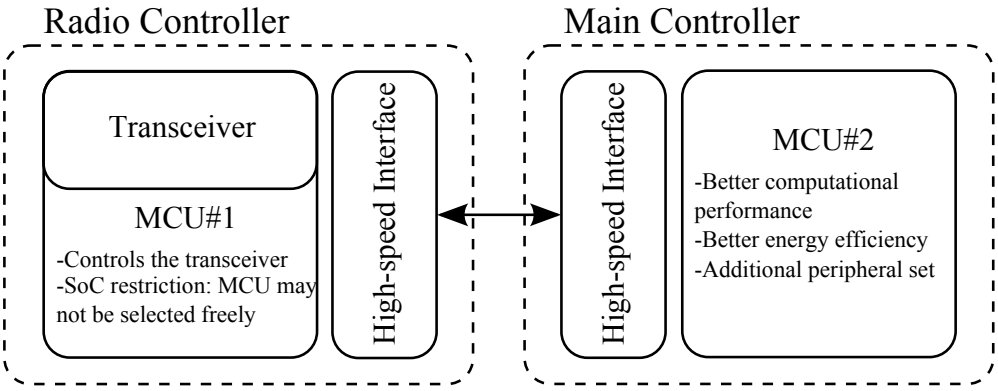

Figure 5: Resource scalability can be improved by supporting multiple MCUs. Here, processing and memory resources provided by a performance-limited transceiver SoC are extended by a high-performance MCU.

Some of the node implementations are based on FPGAs. However, while having great resource scaling capabilities due to fully customizable logic, power consumption has been identified as a bottleneck [19]. Thus, it is not a suitable option for the type of a wireless sensor node that has to be also capable of operating without a battery source, relying only on ambient energy.

2.2.2 Modularity

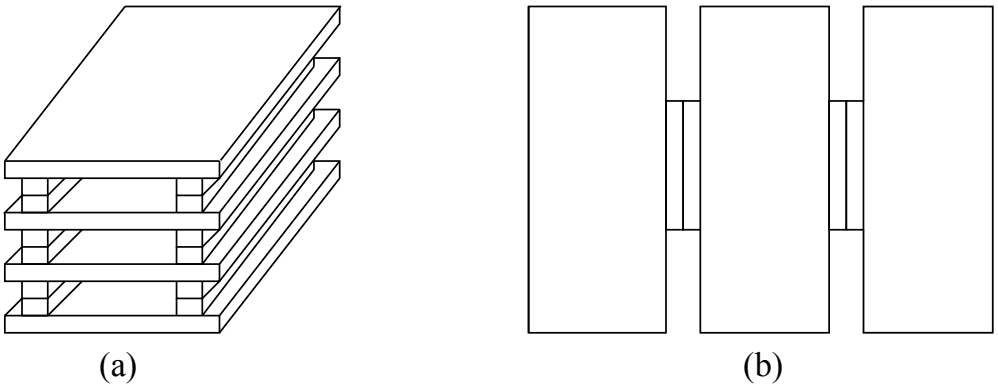

Figure 6: a) Stackable and b) planar modular architecture.

Modularity has been defined as an important feature of wireless sensor nodes [21]. By using a modular architecture, different modules can be redesigned independently according to application requirements. For example, if a different set of sensors is required by an application, a simple sensor module can be designed and manufactured without altering communications, processing or power module. Furthermore, providing resourceful interfaces between different modules further increases design re-usability since these modules can have arbitrary access and configuration interfaces. Manufacturing and development costs when changing the application on a modular wireless sensor node may be brought to a fraction of a complete redesign cost. The end-product can be a simplified version of the modular node in order to reduce the component costs if certain functionalities are not required.

In Figure 6, two typical modular architectures are presented. Stackable modular architecture, as shown in Figure 6 a), consists of vertically connected modules. Order of the modules can be arbitrary if a similar stacking connector layout is followed in each module, that is, if all modules have the same top and bottom side connectors. Figure 6 b) shows another common [22] modular architecture. In this case, different modules are placed in a planar fashion. Here, the order of the modules cannot be arbitrary since the modules do not share a same set of connections. Furthermore, the form factor, an important constraint of a wireless sensor node, for such a device is generally poor compared to a device using stackable architecture. Still, planar architecture has been proven to be a good solution for certain implementations [5].

2.3 Energy adaptive WSN node

Along with resource scalability, energy adaptivity should be considered an important feature of adaptable node platforms due to different power constraints of applications. An application performing extremely demanding computational operations must have a strong power supply since the current drawn is constantly high. On the other hand, applications that require long network life-time benefit from configurability of the power management system. Finally, some applications may ultimately require

more than a decade of network lifetime. In this case, significant trade-offs must be made if the node is powered from a battery [13]. For such applications, energy harvesting becomes an intriguing option.

An energy adaptive node consists of an energy harvester that enables energy autonomous operation and a finite power supply option. It must also provide means to monitor both the finite power supply level and the amount of harvested energy. Furthermore, a power path controller is required to conveniently change between the supplies. Energy harvester should be prioritized since the battery must be replaced once it depletes. Finally, a software component that handles the power management and utilizes the monitors and the controller is required. Thus, an energy adaptive node can be operated completely autonomously, directly from the battery or by using both options to maximize the battery life-time.

It is proposed that sensor network algorithms must be aware of the hardware and able to use the power management features in order to minimize the power consumption [1]. Therefore, it is important to design the energy adaptive node in such a way that it allows software to have as much control over the power management resources as possible.

Main benefit of the proposed node architecture is that it allows a truly adaptable node platform. The architecture allows good hardware flexibility and resource scalability and can be used for applications with diverse energy constraints. Thus, the same node hardware and software can be used for different applications which greatly reduces the required development efforts. Disadvantages of the architecture are hardware costs and complexity. In order to fully utilize the capabilities of the architecture, software and hardware are much more complex than for an application-specific wireless sensor node.

2.3.1 Duty cycling

Existing wireless sensor node implementations can be categorized as either battery powered or energy harvesters. Power consumption of the node in both cases is typically managed by duty cycling where the node is either in a high-power *active mode* or in a low-power *sleep mode*. During a certain period of time T, the node spends a given amount of time in both of these modes. Thus, it is possible to estimate the average power consumption P_{avg} of an application as

$$P_{avg} = \frac{t_a \cdot P_a + t_s \cdot P_s}{T} \tag{1}$$

where t_a is the time spent in active mode, P_a the average power consumption of active mode and t_s and P_s the same values for sleep mode. This equation is a valuable tool when estimating the battery lifetime or required size of an energy harvesting element.

2.3.2 Energy harvesting

An energy adaptive platform must provide a means to produce power without assuming that a finite source, such as a battery, is always connected. This means

that it must include an energy harvester which collects the power required to run the system through different elements that convert ambient energy into electricity.

Table 1 presents different ambient energy sources and typical power levels that can be harvested under given conditions [23]. These power levels are used to estimate size of the harvesting element that is required to ensure continuous operation of the node later in this thesis.

Table 1: Various ambient energy sources, typical harvestable power levels and estimated harvesting element sizes to generate 100 μW of power.

Energy Source	Harvested Power	Estimated Element Size
Vibration/Motion		
`Human`	4 μW/cm^2	25 cm^2
`Industry`	100 μW/cm^2	1 cm^2
Temperature Difference		
`Human`	25 μW/cm^2	4 cm^2
`Industry`	1-10 mW/cm^2	0.1 cm^2
Light		
`Indoor`	10 μW/cm^2	10 cm^2
`Outdoor`	10 mW/cm^2	0.01 cm^2
RF		
`GSM`	0.1 μW/cm^2	1000 cm^2
`Wi-Fi`	1 μW/cm^2	100 cm^2

Harvesting energy from RF emissions is possible but the energy available is much less than for the other options. Vibration-based energy harvesters utilize piezoelectric elements that convert applied mechanical stress into electricity. Temperature difference -based energy harvesters, on the other hand, use thermoelectric generators (TEGs) that exploit the Seebeck effect. However, these harvesting elements suffer from a number of limitations. Mobility of the TEG-based devices is poor since the element must remain connected in a place where a strong temperature difference is present. Practically, they also require a cooling element on the cold side in order to generate the necessary temperature difference. Vibration-based devices, on the other hand, cannot be used in stationary applications since the element must vibrate in order to produce energy. Furthermore, the vibration energy harvesters have a specific resonance frequency outside of which the power produced drops drastically.

Vibration energy harvesters and TEGs are ideal for industrial applications where the operating conditions are either fixed or controllable. For devices that require mobility or easy deployment, using light as the energy source is the most feasible option. Energy of light is converted into electricity with photovoltaic (PV) cells. The amount of electricity produced by a PV cell depends on several factors, such as intensity of light, angle of incidence, ambient temperature and other factors contributing towards the overall efficiency of the cell. For typical commercial PV cells

the peak efficiency is usually rated between 15 % and 20 %, with monocrystalline cells having slightly higher peak efficiencies than cells using polycrystalline silicon [24].

2.3.3 Energy storage elements

While the energy harvester could be designed in such a way that it uses only, for example, a typical Lithium-Polymer (LiPo) battery as a storage element [25], it is not a feasible solution for long-term deployments where the network lifetime is expected to be around or over a decade. Since charging a storage element to its maximum capacity is a slow process due to the available power levels, the process should be constant and independent of user input. However, batteries have a limited number of charge cycles which means that they need to be replaced at regular intervals. As pointed out earlier in this thesis, maintenance and deployment costs are dominant in large-scale and long-term wireless sensor networks.

Supercapacitors are ideal energy storage elements for energy harvesters since they offer virtually limitless number of charge cycles and long operational lifetime [13]. Total time required to charge the supercapacitor to a certain voltage can be estimated from equation

$$t_{charge} = C\frac{(V_{end} - V_{start})}{I_{charge}} \tag{2}$$

where V_{start} and V_{end} are the initial and final voltage over the supercapacitor and I_{charge} the constant current used for charging. Considering that an initially empty ideal 1 F capacitor is charged from a constant current source of 100 μA to a fixed voltage of 1.9 V, the charging time required is over 5 hours. In practice, different losses cause the charging time to be even longer. If the capacitor is charged from a weak power supply, such as a solar cell, even small losses can increase the time significantly. Thus, it is important to minimize losses on the power path between the power supply and the capacitor, as well as design the circuitry connected to the capacitor for lowest possible power consumption.

However, there are some factors related to the supercapacitors that cannot be affected. Diffusion current is typically in order of tens of microamperes for supercapacitors [26], setting requirement for a minimum initial charge current. Diffusion current decreases exponentially with increasing voltage and decays over time. After a certain period of time, the leakage current is said to have settled to its equilibrium value. Because of this, many manufacturers specify leakage currents for their products after a rated voltage has been applied for a certain amount of time, typically 72 hours.

2.3.4 Cold start

In order to support out of the box operation to ease the deployment phase, necessity of a pre-charged energy storage element must be removed for applications that are based on energy harvesting. However, this sets further requirements for the energy harvesting circuitry since it must provide at least

- Reasonable cold start time
- Auto-start operation since the node has no power at the beginning
- Mechanism to connect and disconnect the system load according to available power

Reducing pre-charging time is dependent on the implementation of the energy harvester system. Since there is no power available at the beginning, functionalities such as maximum power point tracking (MPPT) are not usable. Hence, initial charging must be performed at a reduced efficiency. Once the available energy on the storage element has reached a sufficient level, an optimized harvester circuitry should be enabled to take control of the charging.

Energy harvesting system must be capable of completely autonomous operation since, again, no power is available at the beginning. Controlling functionality of the energy harvester is unnecessary and in the beginning even impossible so it must be designed to be reliable. A voltage threshold -based operation is used in the designed node to guarantee robustness of the energy harvester.

2.3.5 Power path control

Power path controller is necessary to fulfil the requirements set by energy adaptivity. It must support at least

- Automated power path selection in the beginning
- Selectable power path once the system is running
- Isolation of different power paths
- Changing a power path without losing system power

and should be designed to be as reliable as possible. Since the primary power supply should be kept arbitrary, the power path manager must guarantee that the system can be automatically powered at the beginning from either power path. Otherwise, the user has to manually connect appropriate power path to the system. Once the node is running, power path should become configurable to enable switching between different power paths in software.

Isolation of different power paths is important because reverse leakages must be prevented. Resistive losses on the power paths should also be minimized. Diodes are not ideal for such a cause because of the associated voltage drops. Furthermore, the system must be guaranteed power while a power path switch is pending. Hence, special load switches are required.

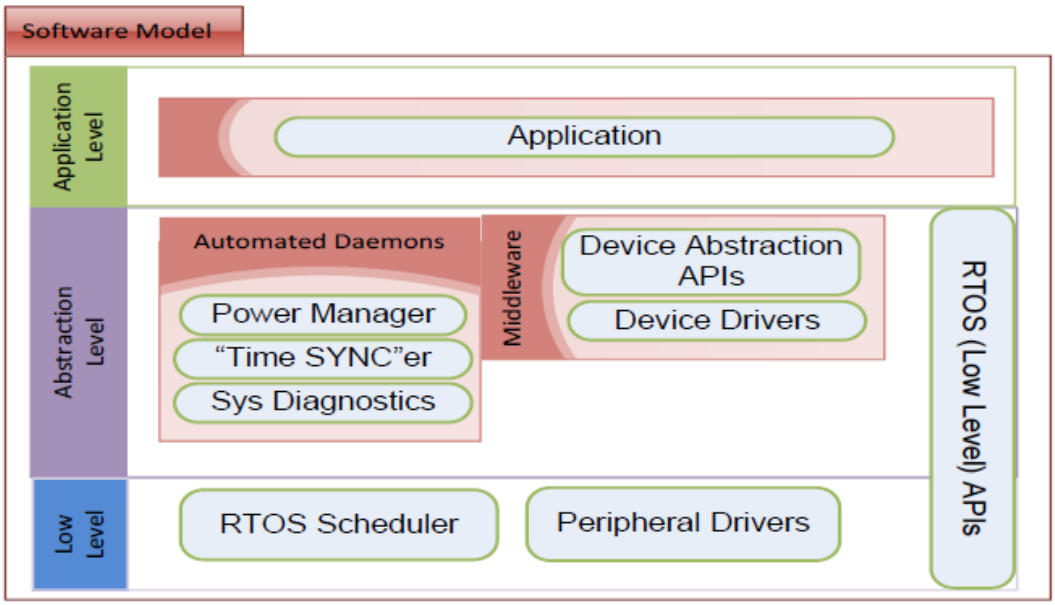

Figure 7: Software model of the node [27].

2.4 Software model

Figure 7 presents software model of the node. Operation of both the radio controller and the main controller is based on FreeRTOS which is a small footprint real-time operating system (RTOS) . The software model consists of three levels: low level, abstraction level and application level. Application developer can make use of the provided APIs when programming the application.

Low level of the software model consists of an RTOS scheduler and a set of peripheral drivers. The scheduler is responsible for allocating processor time to different tasks based on their priorities. Peripherals of the MCUs are controlled by the peripheral drivers which provide the configuration, initialization and ISR functions. These two software components are strictly tied to the underlying hardware and thus, are located on the lowest level of the software model.

Energy adaptivity of the node is handled by the power manager which makes use of the power control resources provided by the hardware. Implementing this functionality is a complex issue and requires knowledge of the complete power characteristics of the node. Providing the power profile for this cause is one of the primary goals of the thesis. Time synchronizer, on the other hand, is responsible for synchronizing operation of the node. Finally, the middleware implements an unified external device access software for the application development.

3 Hardware design

3.1 Overview of the node hardware

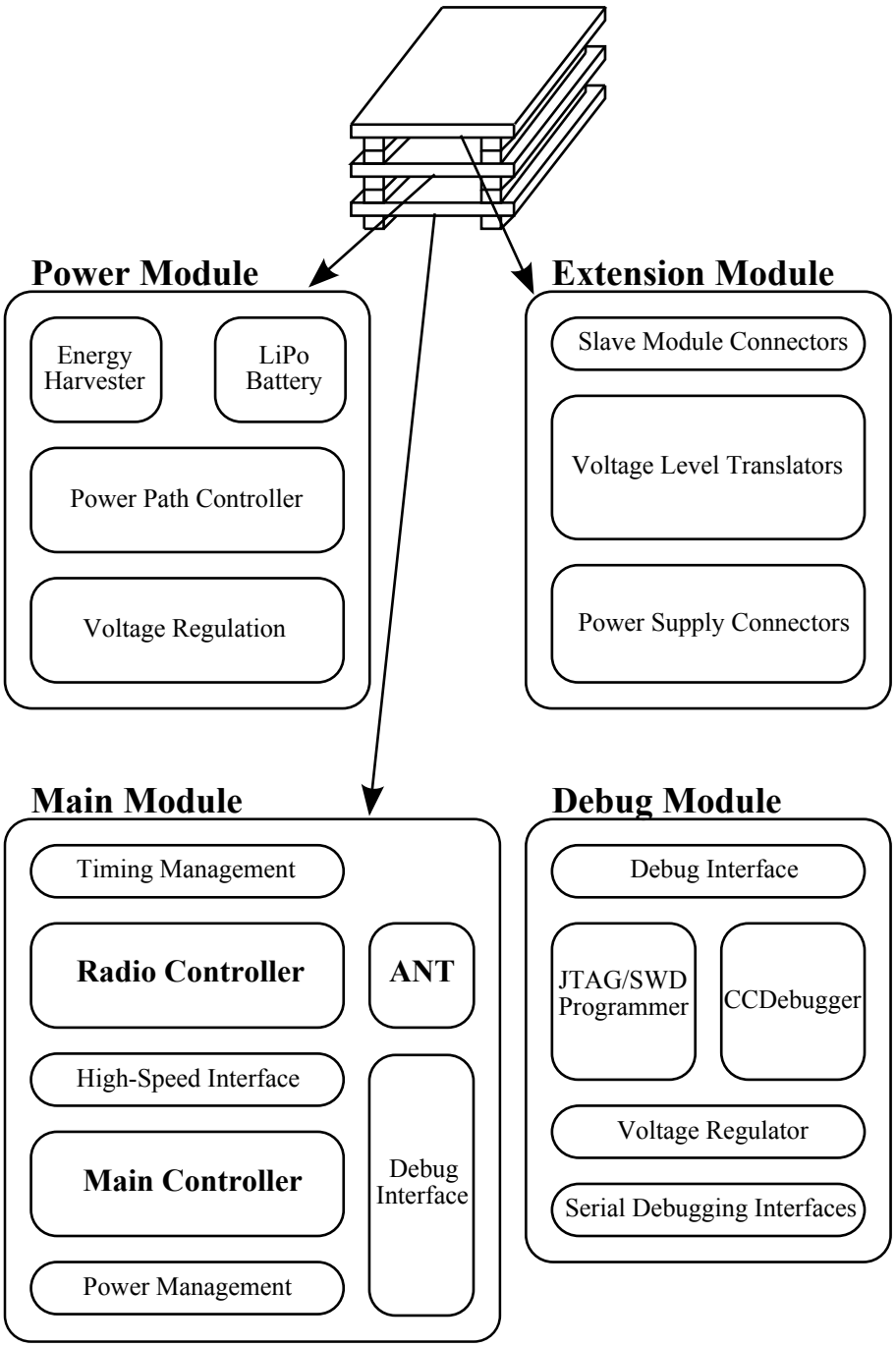

Figure 8: Overview of the node hardware.

This chapter describes the hardware design that aims to fulfil the requirements described in the previous chapter. The designed node uses stackable modular architecture in order to reduce the form factor and enable easy connection of the

modules. Basic module stack consists of a power module, a main module and an extension module. Extension module provides interfaces for connecting the different sensor and actuator modules as well as hardware resource extension modules. These modules are commonly labelled as *slave modules*. Debug module is not part of the normal stack and is used only for programming and debugging purposes.

Figure 8 presents a high-level overview of the different modules and their contents. Power module generates various regulated voltages from the given sources and provides controls for them. Power path controller is also a critical component of the power module; robust autonomous operation is required during the initial start-up. Main module, on the other hand, is responsible for controlling the operation of the node. Both radio and main controller are located in the main module. In addition to the MCUs, main module has an antenna connector and the proper matching circuit, power and timing management subsystems and a simple debug interface.

3.2 Design procedure

Due to the complex nature of the node, a specific procedure was created and followed carefully throughout the design phase in order to minimize the amount of errors. A generalized version of the procedure is presented in Figure 9. It can be used as a guideline when designing similar or otherwise complex hardware. The procedure begins with a conceptual design phase that aims to identify the requirements and possible problems related to the specified project goals. As an example of such, the zero-charge start-up phase and the bypass circuit as the solution is a result of this phase.

At the start of the technical design phase, a top-level block diagram is first derived for each separate module. This block diagram consists of complete functional units without any specific design details. The functional units are then filled with more detailed implementations or spread into even smaller subunits. Designs utilizing this kind of top to bottom -approach are called hierarchical designs.

Since the node has hundreds of components of different types, hierarchical design is feasible because it makes the design more understandable by partitioning the complete design into smaller subunits. Thus, if a problem is detected, it can be often easily corrected within the related subunit. However, in order to effectively utilize a hierarchical design, the interfaces between different subunits must be clearly defined. In this case, since the node hardware is also modular, special attention must be paid when defining the interfaces both between different modules and between different subunits within the modules.

Excel sheets come in particularly handy when allocating pins of the MCUs to different interfaces. Instead of applying time consuming trial-and-error approach directly on the schematics, the pins and their corresponding functionalities can be listed in a sheet. This way, the pins can be allocated before making any modifications on the schematic level. This reduces the probability of errors since different functionalities are clearly visible which is often not the case in the schematics. When modifying pins allocation of the MCUs, changes should be applied first on the Excel sheet and then on the schematics.

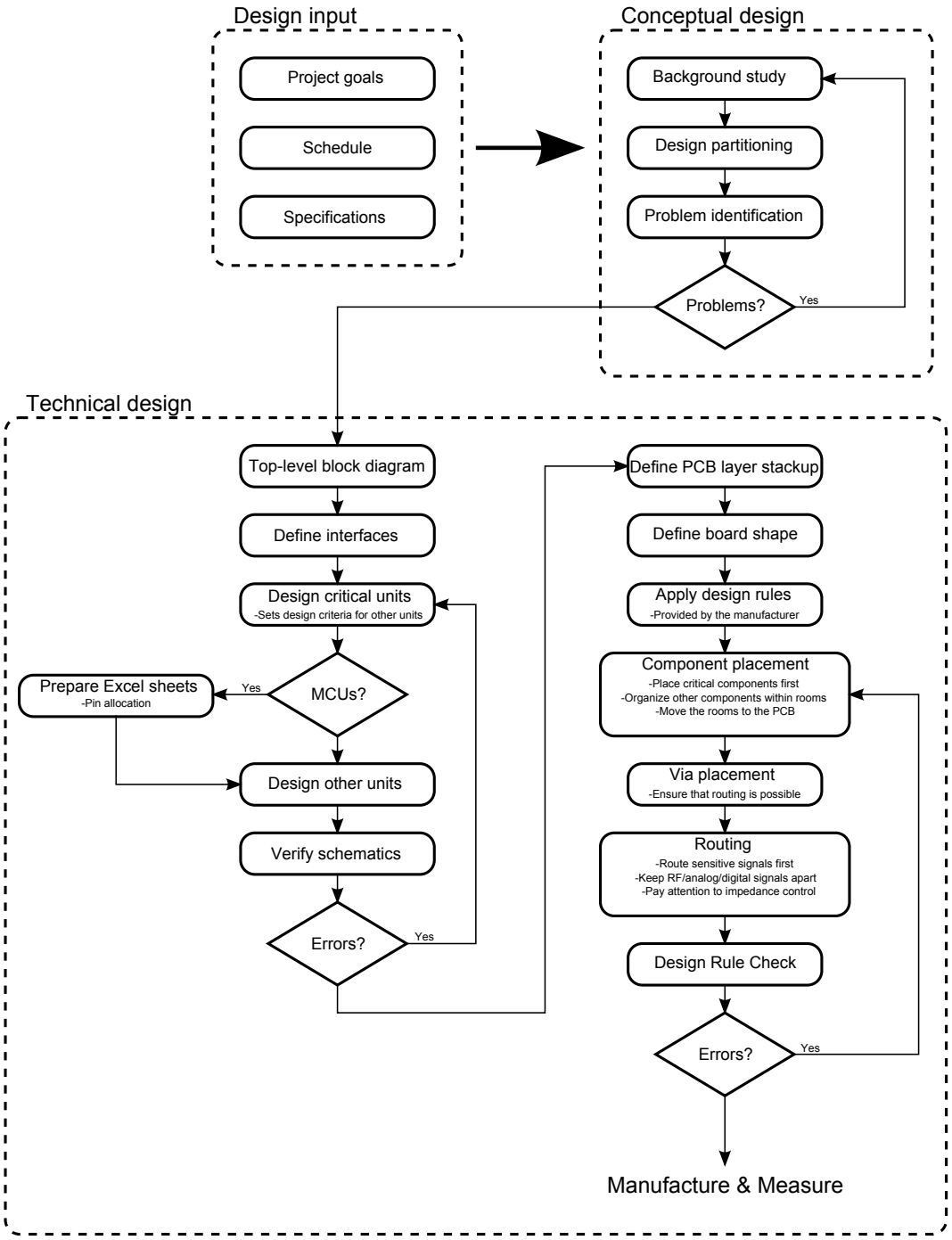

Figure 9: Utilized design procedure. The procedure has been generalized so it can be used as a guideline for other designs.

PCB design is started by defining the layer stackup and the board shape. The layer stackup should be the same for each module in order to allow different modules to share the same panel. This effectively reduces cost of PCB manufacturing since the costs are mainly related to the panels. Design rules provided by the manufacturer should be closely followed. This ensures that the probability of, for example, accidental

short-circuits during manufacturing process is kept minimal.

Finally, the components are placed and routed. Sensitive components, such as radio or high-accuracy analog parts, should be placed first directly to the PCB. Placement for the other components can be done in small rooms outside of the PCB area. Once the placement is completed, the complete room can be moved to the PCB. This is an effective method for simplifying the component placement. Afterwards, vias are placed to critical locations, for example close to power pins of the ICs in order to provide a short connection to the power or ground plane.

3.3 Power module

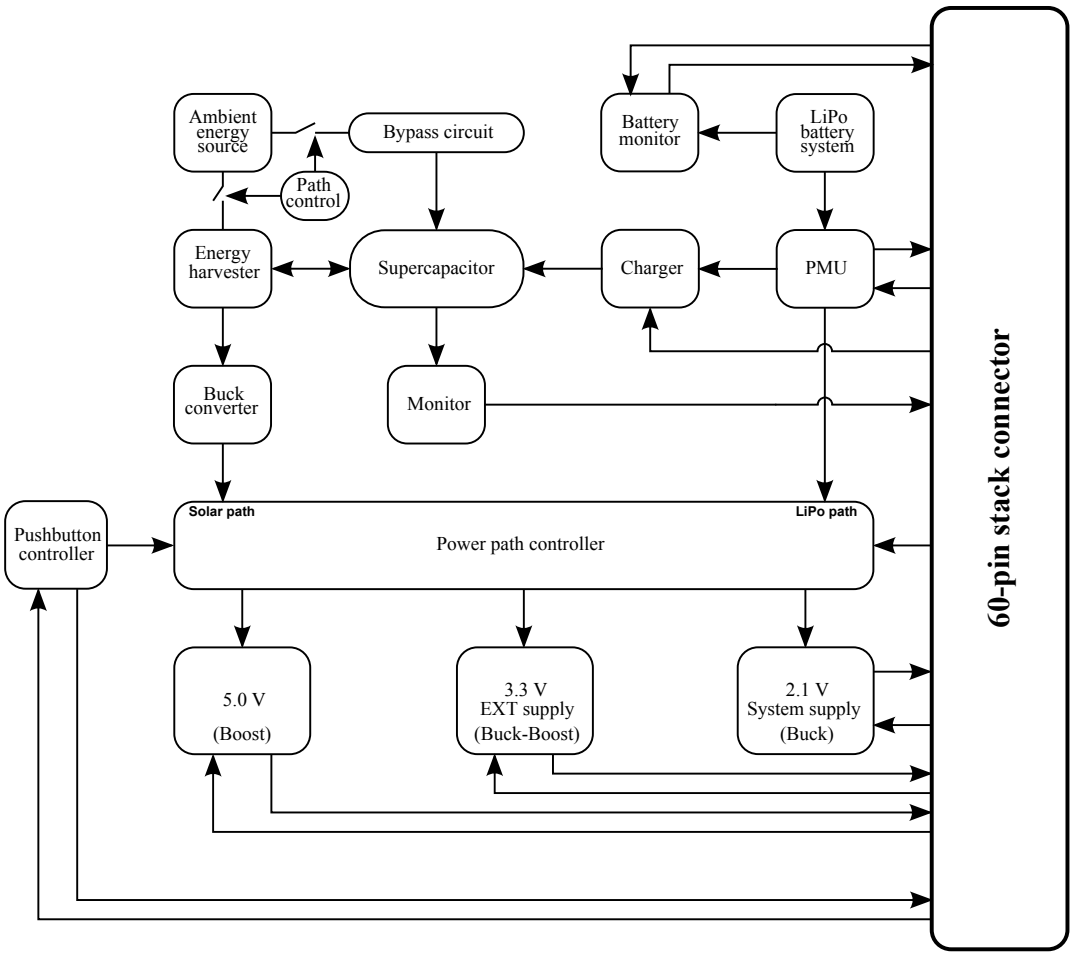

Figure 10: Block diagram of the power module.

A simplified functional block diagram of the power module is presented in Figure 10. Power module features three fixed-voltage outputs and four adjustable ones provided by the power management unit (PMU). Overall, voltage range of 0.8 V to 5.0 V is covered by the various regulators of the power module. An energy harvesting system is provided to gather energy from ambient sources. The energy harvester is optimized for photovoltaic cells with approximately 80 % MPPT ratio.

Supercapacitor is used as a storage element due to the benefits discussed in Chapter 2. No initial charge on the supercapacitor is required. The bypass circuit in parallel with the harvester is used to reduce the initial charging time of the supercapacitor due to the harvester's low efficiency when charging an empty storage element. Additionally, a Lithium-Polymer battery can be used as a power source.

Once the system on the main module is running, it is possible to have full control over many of the power management features. The main power source is controllable through the prioritized power path controller which can provide a huge benefit in power-critical applications. For example, an application can be designed to use a solar cell as the primary source and a LiPo-battery as a back-up source. When lighting level diminishes and the voltage over supercapacitor drops, the PPC can be used to automatically switch the input supply from supercapacitor to the LiPo-battery. Once the supercapacitor voltage exceeds a certain threshold, the power path can be changed again. This kind of approach can extend the battery life significantly. Furthermore, if one of the power supplies becomes permanently unusable, the node can still rely on the other.

Supercapacitor can be charged from the power source connected to the battery system. The charger is controlled by the main controller. The benefit of having such a charger is that the zero-charge start-up phase can be bypassed completely by giving the supercapacitor a sufficient charge before deployment. Furthermore, during experimentations it is often helpful to rapidly charge the supercapacitor when necessary. Both the LiPo and the supercapacitor voltage can be monitored.

3.3.1 Energy harvesting system

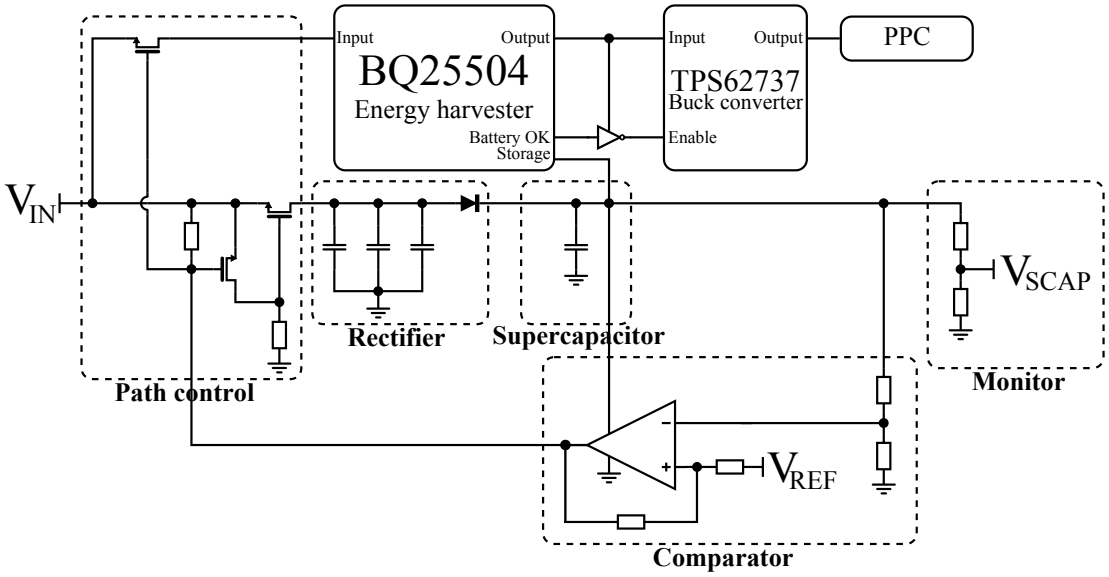

Figure 11: Energy harvesting system of the node.

Energy harvesting system of the node is based on Texas Instruments' BQ25504 with a supercapacitor as a storage element. BQ25504 combines an efficient energy

harvester with an ultra-low power boost converter and an energy storage system. Supercapacitor as a storage element is an ideal choice for this design since it eliminates the need for any pre-charging and strict safety monitoring that are required with the typical batteries. Supercapacitors offer virtually limitless charge cycles and have longer lifetime than, for example, a LiPo battery.

Figure 11 shows implementation of the energy harvesting system used in this design. Initially, when the supercapacitor is empty, the charging is performed through a path formed by path control and rectifier circuits. In this case, the supercapacitor is charged directly from the energy harvesting element. While this is extremely undesired method in normal circumstances, it has benefits in this implementation. This is discussed more in detail in the following section.

The harvester IC first ramps up its output to 1.8 V using the energy stored in the supercapacitor. After the output has reached this level, the main boost regulator becomes operational. Output voltage of the converter is determined by *overvoltage threshold* which is adjustable. Internal charger circuitry remains disabled for a short duration after the main converter is turned on to set the initial reference voltage of MPPT circuitry. Afterwards, the harvester repeatedly disables the charger every 16 seconds to let the input rise to its open-circuit voltage to obtain a new reference voltage. The harvester also indicates when battery level is sufficient for a load to be applied. In this design, an inverted indicator signal is used to drive the enable pin of a buck regulator that produces output voltage of the harvesting system, nominally 2.7 V.

Voltage level of the supercapacitor is monitored by utilizing internal ADC peripheral modules of the microcontrollers. Both MCUs on the main module can supervise the available energy on the supercapacitor. It should be noted that the MCUs do not have a separate supply for the analog peripherals. Thus, since the supply voltage of the MCUs can vary between 2.1 V to 3.3 V, it is important to ensure that the maximum input voltage of the ADC modules stays below 2.1 V in order to avoid incorrect readings and possibly even permanent damage. Hence, a voltage divider, as presented in Figure 11 is required.

Using a voltage divider, however, is not a straightforward matter since using large resistor values in order to minimize the current consumption conflicts with the required current to charge the sampling capacitor of the ADC to provide accurate results. Since the sampled signal, voltage over the supercapacitor, can be assumed to change slowly, a decent sized capacitor can be used in parallel to the ADC input pin of the MCUs. This method causes the parallel capacitor to charge up slowly due to the high-resistance divider but provide accurate results since the amount of droop is decreased when the ADC sampling capacitor charges up. Trade-off of this method is that the maximum sampling rate depends on the external capacitor.

3.3.2 Zero-charge start-up

The energy harvester used in the design has an internal cold-start unit which is essentially an unregulated boost converter. The unit is activated when voltage over the storage element is less than 1.5 V [25]. Based on initial testing performed on

an evaluation board of the harvester, the efficiency during this phase was estimated to be around 10 %. Because of the reduced efficiency, charging time of the supercapacitor during this phase can be very long. To reduce the charging time when the supercapacitor is initially empty, the harvester is bypassed to allow charging directly from the harvesting element.

Once voltage over the supercapacitor has reached approximately 1.9 V, an open-drain comparator turns off the bypass circuit and enables the harvester. After voltage at the output of the harvester is ramped up to the overvoltage threshold, charging of the supercapacitor continues normally until a load can be applied. Afterwards, the energy harvester splits the harvested energy between charging the supercapacitor and powering the output, prioritizing the latter. Should voltage of the supercapacitor drop below 1.9 V, the bypass circuit is reactivated. A small hysteresis is provided by the comparator circuit to ensure that the load transients do not affect the operation.

To maximize effectiveness of the zero-charge start-up mechanism, a special attention on component selection is crucial. Transistors in the power path should have low on-resistance and leakage currents to minimize the losses. The diode protecting solar cells from excessive voltages when the harvester's internal boost regulator becomes operational should feature low forward voltage drop and low reverse leakage. Selecting resistor values properly to minimize the current consumption is also a key element since too large values can lead to excessive offset voltages at certain nodes due to the leakage currents. Nodes affected by these offset voltages in this implementation are mainly gates of the PMOS transistors. Selecting too large values, however, for certain threshold voltage programming resistors of the comparator can cause problems due to its internal circuitry.

3.3.3 Lithium-Polymer battery system

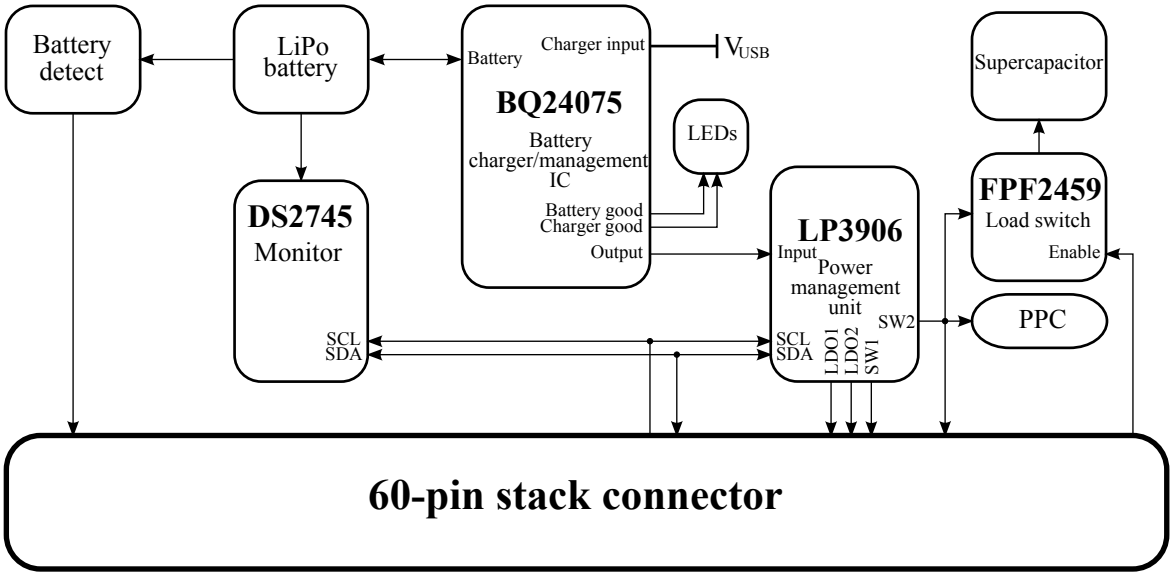

Figure 12: Lithium-Polymer battery system.

The designed node can also be supplied from a Lithium-Polymer battery. Complete battery system is presented in Figure 12. Presence of the battery is indicated to the main module by using a simple transistor-based circuit. Connected battery can be charged directly from a computer's USB port through a USB connector located on the main module. Charging and management of the battery is performed by Texas Instruments' BQ24075 charger IC which features the necessary functions to guarantee safety of the battery during the charging operation.

The charger regulates its output voltage to 5.5 V which would damage the parts of the design that are not 5 V tolerant. Because of this, conversion of the output voltage to a lower level is required to protect the system. Since LiPo-batteries are much stronger power sources than, for example, solar cells, a sophisticated PMU can be used to provide additional flexibility for power management purposes. Naturally, the power consumption of the high-quality PMU used in the design is significantly higher than power consumption of the low-power fixed-output regulators. However, this is not an issue since the LiPo power path is completely isolated from the energy harvester and will be powered down if a battery is not connected. The PMU features two highly efficient step-down DC-to-DC converters and two LDO regulators with programmable output voltage. One of the step-down converters, SW2, is used as the main regulator of the battery system. By default, the output voltage of SW2 is 3.3 V which is low enough to guarantee system safety.

The battery monitor provides voltage, current and temperature measurements. Current is monitored with a small shunt resistor generating a voltage relative to the current passing through. The monitor can be operated in two different modes, active mode and sleep mode. In active mode, each measurement is acquired continuously and the results can be read from the corresponding registers. The sleep mode can be used to conserve power if battery monitoring is not required.

Under normal circumstances the supercapacitor is charged only by the energy harvester. An alternative method for charging to eliminate the zero-charge start-up phase is also provided. The supercapacitor, as shown in Figure 12, is connected to a battery source through a load switch featuring true reverse current blocking (TRCB) and a programmable current limit. Current limiter prevents an empty supercapacitor from draining the source too rapidly which could lead to an overloading condition on the battery side. In addition, TRCB feature prevents the supercapacitor from leaking through the switch.

3.3.4 Pushbutton controller

A pushbutton controller circuit, as shown in Figure 13, is used in the design to control whether or not system load should be connected. Essentially, the pushbutton controller is used to connect or disconnect the load in a similar fashion as is used in a typical mobile phone. By setting proper values for the two external capacitors it is possible to determine the turn-on and turn-off delays of the node. Motivation to use this kind of setup is the immunity to short-term interferences that can occur due to, for example, vibrations, by increasing the stability through controllable device powering.

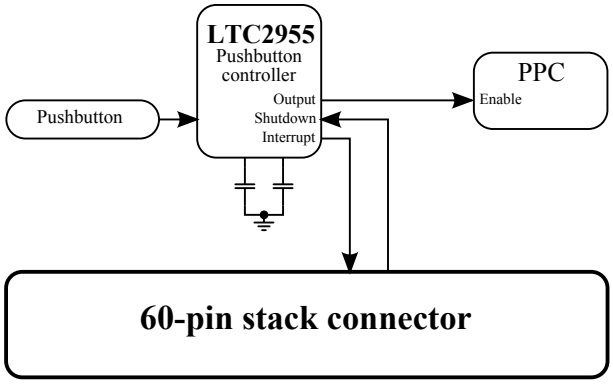

Figure 13: Pushbutton controller used in the node.

The pushbutton controller features interrupt and shutdown signals. Interrupt signal is generated when the pushbutton has been pressed to cut off power from the system. Main controller of node can detect this signal and prepare for incoming power loss. Main controller can also generate a signal for the pushbutton controller to request a complete power down.

3.3.5 Power path controller

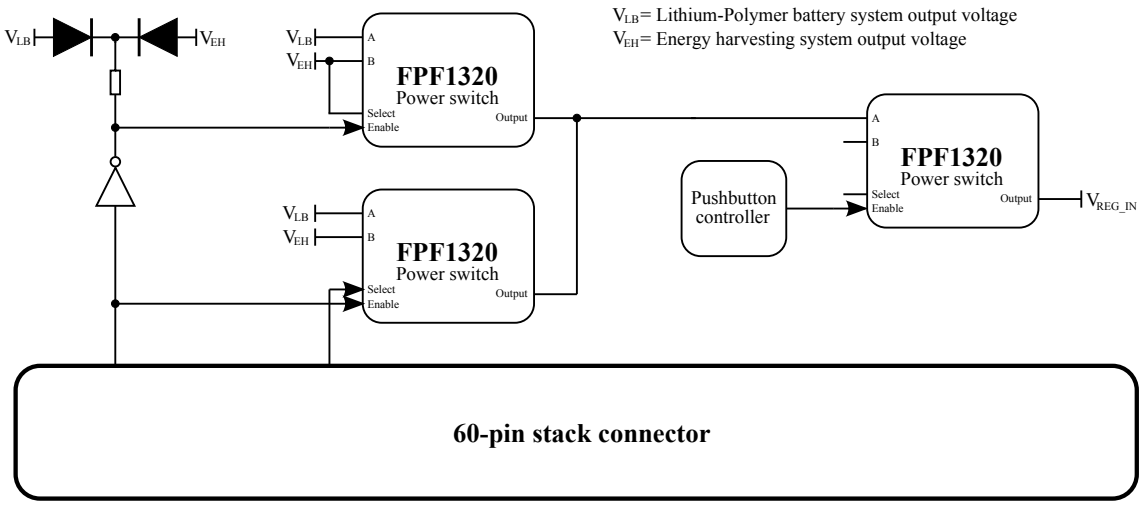

Figure 14: Prioritized power path controller of the power module.

Figure 14 presents the power path controller of the power module. Truth table of the power switches is presented in Table 2. The first stage of the PPC ensures that if either the energy harvesting system or the LiPo battery system is capable of providing power, the power gets fed to the next stage. If both power sources are available, the PPC prioritizes energy harvesting system since it is an infinite source. The operation is completely automatic.

The diode connection ensures that the enable pin gets pulled high if either source has power. This is possible because the energy harvesting system's output voltage

Table 2: Truth table of the FPF1320 power switch.

Enable	Select	Output
Low	Low	Disabled
Low	High	Disabled
High	Low	A
High	High	B

is regulated to 2.7 V while LiPo battery system provides 3.3 V by default. The 0.6 V difference is enough to guarantee that both diodes do not conduct at the same time. Enable pin of the power switch has a 7 MΩ internal pull-down resistor which allows use of a large value resistor at the output of the open-drain inverter. Thus, if the inverter pulls its output low, the power consumption due to the current flowing through the resistor can be kept small.

The PPC is controllable when the system has been powered up. Two control signals, enable and path select, are available. Both microcontrollers of the main module can control the PPC. Timing properties of the power switches guarantee that the power will not be lost when changing the power path. The switches also feature TRCB mechanism which prevents any current flow towards the sources.

3.3.6 DC-to-DC converters

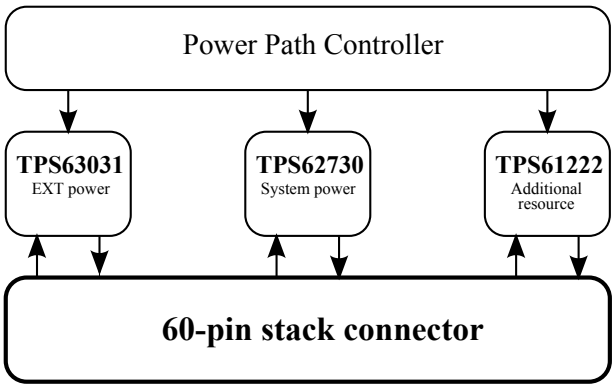

Figure 15: Fixed-output DC-to-DC converters of the power module.

Power module features three fixed-output DC-to-DC converters as shown in Figure 15. TPS62730 is the main regulator through which the power is supplied to the main module. It features an ultra-low power bypass mode where the input is connected to the output directly. When the converter is enabled, the output voltage is regulated to 2.1 V. The main motivation to use this specific regulator to power the main module is the reduced current consumption of the radio controller during RX and TX operations [28].

Converter circuits are designed following the reference designs of each device. The critical components are the inductors and capacitors, for which the datasheets provide selection information. Along with the adjustable outputs of the power management unit described earlier, the outputs of power module cover the range from 0.8 V to 5.0 V.

Each of the regulators has a specific pin input for enabling. By default, 3.3 V regulator is turned on and 5.0 V regulator off. Turning the 5.0 V regulator off forces it into the bypass mode and thus, there is always voltage at the output. In a bypass mode, only the conversion functionality is disabled. In addition, the 3.3 V regulator has a power save input pin which optimizes efficiency for light loads if used. Power save is enabled by default and is not controllable. The main regulator, on the other hand, must be controlled by the MCUs on the main module. It is required to configure the MCU's pin driving the regulator's enable pin properly to initially force a known state on the pin.

3.4 Main module

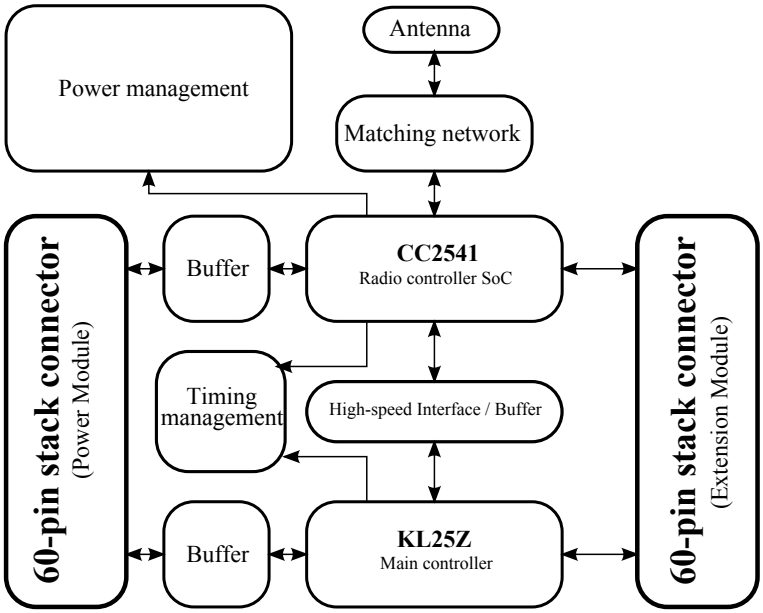

Figure 16: Block diagram of the main module.

This section of the thesis presents design of crucial functional blocks of the main module. In Figure 16, a simplified block diagram of the main module is shown. Purposes and functionalities of the power management and timing management subsystems are explained in detail.

CC2541 is selected as the radio controller because of its low power consumption during RX/TX events and availability of the Bluetooth Low Energy (BLE) protocol stack. The lack of processing performance of CC2541 is compensated with an ARM Cortex-M0+ -based microcontroller which offers very low power consumption with

significantly increased processing capabilities. The microcontrollers communicate through a special interface presented later in this section.

3.4.1 Power control

Power management subsystem is operates independently and decides which supply is used to power the system. A control signal to shut down main controller side completely is also provided and can be an asset for energy-critical applications. Available power sources on the main module are the power module, USB and debug module.

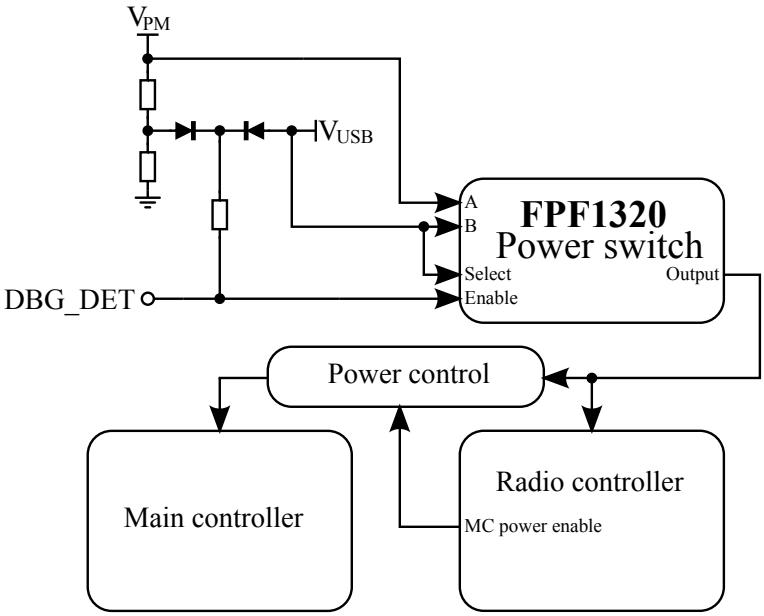

Figure 17: Power management subsystem of the main module.

Operation of the power management subsystem is based on prioritization. Power switch is the same that is used in the power path controller of power module in Section 3.3.5. Power path selection is automatic but the radio controller must be able to control power of the main controller since using the latter is voluntary. Main controller must be allowed to remain completely disabled if it is not required.

A diode-based configuration, as shown in the figure, is used to drive the enable and select pins of the power switch. Since power module's output voltage V_{PM} can also be up to 3.3 V if a LiPo-battery is used, it must be divided down due to the common cathode connection of the diodes. This prevents the diodes to conduct simultaneously and increases stability of the system.

If debug module is not connected, DBG_DET signal is floating. When the module is connected, the signal is pulled to ground, disabling the power switch and cutting of power from the system. The power supply is selected manually on the debug module. A small resistor is required to prevent a short circuit between V_{USB} and DBG_DET which is tied to ground directly. The following list provides a brief summary of the priorities and the reasoning behind them.

1. High priority: Debug module; it must ensure that both microcontrollers have power for programming purposes.
2. Medium priority: USB connector; power is supplied from PC's USB port or by using a wall adapter which are both infinite supplies.
3. Low priority: Power module; the power supply is either a weak energy harvester or a finite battery.

3.4.2 Timing management

In order to provide resource scalability, multiple simultaneous MCUs are supported. However, these MCUs typically have their own notion of time since they are clocked from different sources. As a result, collaborative operation of the MCUs is not time synchronized. Synchronization can be established by generating a global tick signal and performing MCU operations according to it.

It is suggested that the timing management consists of two hardware signals, the start-of-frame delimiter (SFD) indicator and a heartbeat signal. SFD indicator is used to capture the local time of the MCUs by utilizing timer peripherals. Heartbeat signal, on the other hand, is used to maintain hardware-level synchronization. Combined, these can be used to establish and maintain network level synchronization. [9]

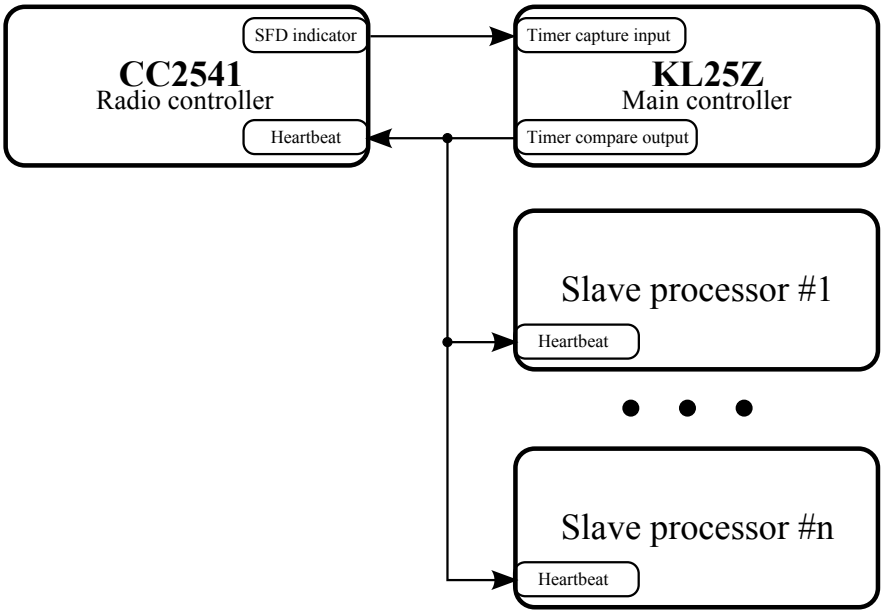

Figure 18: Timing management of the main module.

Figure 18 presents time management hardware components of the designed node. Radio controller has a 40-bit timer peripheral, labelled as media access control (MAC) timer, that is capable of capturing the exact moment of access code reception. The event is relayed to the main controller by using special RF core observation signals provided by the radio controller. Indication of the received access address is captured by a timer on the main controller side.

By using the aforementioned indicator, node-level local time can be captured by the hardware upon packet reception. MCUs of the node, including possible MCUs on the slave modules, can be synchronized to a common heartbeat signal by adjusting their own clocks according to it. In order to maintain network level synchronization, the heartbeat signal can be adjusted to received timing information. [9]

3.4.3 Hardware buffers

The designed node may have multiple different voltage levels present simultaneously. For example, external modules and the main module may have different supply voltages. For many digital components, the maximum safe voltage that can be applied to the I/O pins is close to the current supply voltage. To guarantee safe operation in designs where multiple voltage levels are present, the relevant I/O pins must be protected by using voltage-level translation. The buffers can also be used to isolate a number of signals. This is particularly useful for the power module configuring since both MCUs can access certain functionalities but only one should have access for them at a time. Otherwise, the worst-case scenario might happen, that is, when one of the controllers drives a pin low and the other high. This can even lead to permanent damage on the MCUs.

A wide range of commercial voltage-level translators are available. Some voltage-level translators, however, have weak output drivers, and thus, cannot be used to buffer open-drain signals such as I^2C. Instead, buffers that provide stronger drive capability must be used. It is important to verify that the selected buffers fit within low and high voltage thresholds of the design. Otherwise, the buffers may be forced to operate in a non-specified voltage range and might produce incorrect transitions.

3.4.4 Radio controller

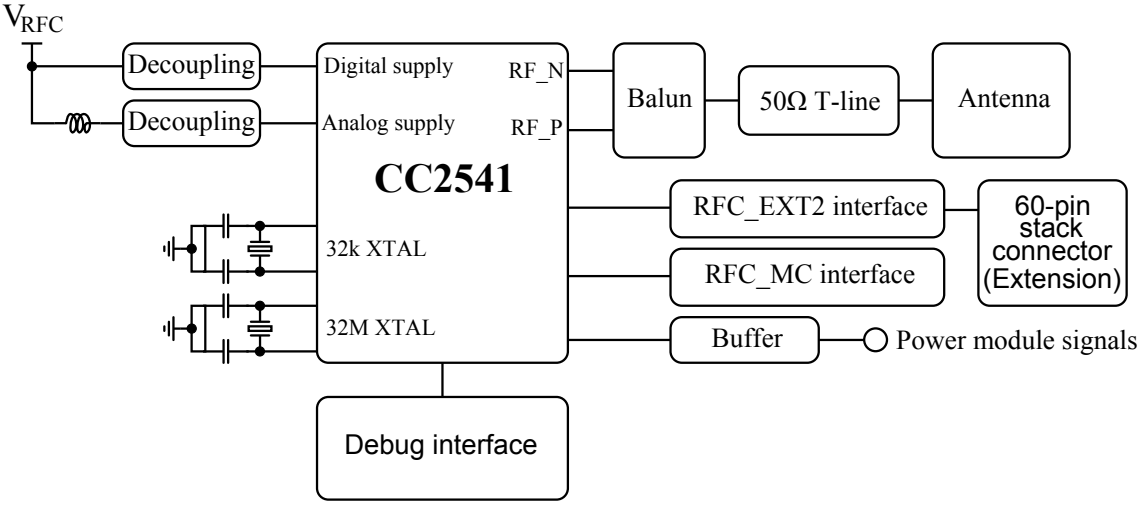

Figure 19: Radio controller of the node.

The designed node uses CC2541 from Texas Instruments as the radio controller.

Most important functional blocks related to the radio controller are shown in Figure 19. Information on the radio performance of the selected radio controller is gathered in Table 3. Poor scalability of the current consumption should be noted. Despite having a difference of 20 dBm in TX power, the difference in power consumption is only 1.4 mA. One big contributor towards this is likely poor efficiency of the power amplifier. Enabling main regulator on the power module during RX/TX events reduces the current consumption of approximately 20 % as was discussed earlier in this thesis.

Radio controller features a number of peripherals such as timers, an 8-channel ADC and communication interfaces. Since the node supports two kinds of operation modes, pins of the radio controller can have multiple functionalities depending on the mode being used. In RFC only -mode, the node behaves like a traditional wireless sensor node simply gathering and sending the measurement data. Of the extensions, only the RFC_EXT2 is usable in this mode. Furthermore, many of the power management features cannot be used while in this mode. In complex applications requiring more processing power or strict timing and power management, the node can be run with both MCUs active.

RFC_EXT2 interface is a collection of signals for the slave modules. The interface provides typical GPIO functionalities, various timer functionalities and serial interfaces. These pins can be multiplexed for other functionalities as well. Similarly, RFC_MC interface is a collection of signals that define the interface through which the radio controller and the main controller communicate.

The radio controller used in the design is a 2.4 GHz BLE SoC combining an RF transceiver and an 8051-based MCU. Supply filtering method shown in the figure follows closely the reference designs in order to ensure good decoupling. Ferrite bead between analog and digital supplies effectively eliminates the switching noise components [29]. The placement of the decoupling capacitors has a strong effect on their performance. In PCB design, the capacitors should be placed as close to the IC as possible in order to minimize the loop formed by the IC's power pins and the capacitors. In a good design, the power is forced to flow through the capacitors' pads before reaching the IC.

There are five different power modes that can be utilized. These modes are aimed to lower the power consumption of the radio controller if required and are particularly useful when duty cycling. SRAM contents are retained in each power mode which is an asset since it enables easy and fast switching between different power modes. It should be noted, though, that most of the peripheral registers lose their contents and cannot be used in the certain low-power modes.

The RF systems are highly dependent on accurate clocks because any deviation in the clock frequency can degrade the RF performance. A 32 MHz external crystal is mandatory since it is used to generate clock for the radio core. On the other hand, a 32.768 kHz external crystal is used for accurate sleep timing to provide support for BLE in low power modes since the standard sets requirements for timing accuracy. The radio controller also features internal 16 MHz and 32 kHz RC-oscillators.

Accurate crystals should be used with radio controller. Accuracy of a crystal consists of multiple factors such as aging, temperature stability and frequency tolerance.

Table 3: Radio performance characteristics of the CC2541.

Parameter	Value
RF TRANSMIT | V_{DD} = 3V and f_C = 2440 MHz	
Output power, maximum	0 dBm
Output power, minimum	-23 dBm
Optimum load impedance	(70 + j30)Ω
TX mode current consumption, 0 dBm	18.2 mA
TX mode current consumption, -20 dBm	16.8 mA
TX mode current consumption with TPS62730, 0 dBm	14.3 mA
TX mode current consumption with TPS62730, -20 dBm	13.1 mA
RF RECEIVE | 1 Mbps, GFSK, 250 kHz deviation, BLE mode	
Input RF level, maximum	10 dBm
Receiver sensitivity, standard mode, BLE	-88 dBm
Receiver sensitivity, high-gain mode, BLE	-94 dBm
RX mode current consumption, standard mode	17.9 mA
RX mode current consumption, high-gain mode	20.2 mA
RX mode current consumption with TPS62730, standard mode	14.2 mA
RX mode current consumption with TPS62730, high-gain mode	16.7 mA

Especially temperature stability can be an inconvenient variable in countries such as Finland since the temperature varies over a wide range during a year. Since crystal frequency deviation is directly transferred to RF deviation, it is important to ensure that the selected crystal meets with the performance requirements set by BLE.

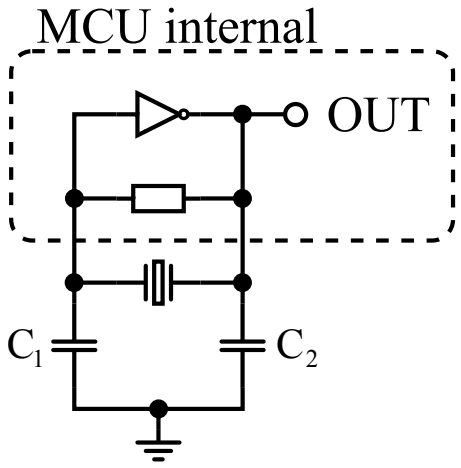

Figure 20: Typical Pierce oscillator circuit of MCUs.

Most of the modern microcontrollers utilize a simple inverter-based Pierce oscillator as shown in Figure 20 to provide an accurate and stable clock for the system.

The crystal in combination with the external capacitors forms a band-pass filter providing a 180 degree phase shift at the resonant frequency of the crystal. The biasing resistor forces the inverter to operate at the linear region where it has high gain. The negative gain of the inverter in combination with the 180 degree phase shift results in a positive feedback circuit causing the oscillation. Because the external capacitors appear as in series, the total load capacitance can be calculated using equation

$$C_L = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}} + C_p \tag{3}$$

where C_p is the sum of all parasitic capacitances. These parasitic capacitances are mainly introduced from crystal port of the MCU and from the PCB itself. The value for C_p is typically between 2 pF and 8 pF. As a rule of thumb, a value of 5 pF is usually used in the calculation. For the selected 32 MHz crystal, the load capacitance is approximately 11 pF and for the 32.768 kHz crystal approximately 12.5 pF. The value should not vary much from the recommended since resonance frequency of the oscillator is dependent on the load capacitance.

The radio controller is programmed via a debug interface which consists of the signals required for programming. Programming is performed through a 2-pin serial interface. Debug interface of the radio controller provides possibility for serial debugging by providing connections for radio controller's universal asynchronous receiver/transmitter (UART) peripheral.

3.4.5 50-Ω transmission line design

Radio controller produces differential RF signals. These signals are used as inputs to low-noise amplifier (LNA) during RX operation and as outputs from power amplifier (PA) during TX. The signal traces must be kept equal in length and symmetric in the PCB design and must also be matched commonly to the antenna connector's impedance. The impedance for many standard antenna connectors is typically 50 Ω. In the design, a 50 Ω SMA edge-mount connector is used. The matching, in case of differential RF signals, is generally done using either lumped elements or a device-specific balun. Matching with lumped elements requires knowledge about using the Smith chart for the best result but provides much better fine tuning options than a balun. As a drawback, such a network will require more room on the PCB.

A balun optimized for CC254x devices is used in this design. To meet with the demand for equal trace length and symmetry, RF_N and RF_P are routed as a differential pair. Because the balanced port differential impedance is matched to the radio controller, the differential properties of the pair are not as important as the trace length. The key is to keep the traces between the balun and the radio controller as short as possible to minimize changes in the matching impedance. Longer traces will eventually start behaving like transmission lines which results in significant degrading of the RF performance as more reflections are caused. As a general rule of thumb, any trace longer than $\lambda/10$ should be treated as a transmission line.

A 50 Ω transmission line is required between the unbalanced port of the balun and the antenna connector for optimal matching. In transmission line theory, a

sudden change in the trace impedance is a point of discontinuity and at each such point reflections are generated, reducing the maximum power that can be transmitted through the antenna.

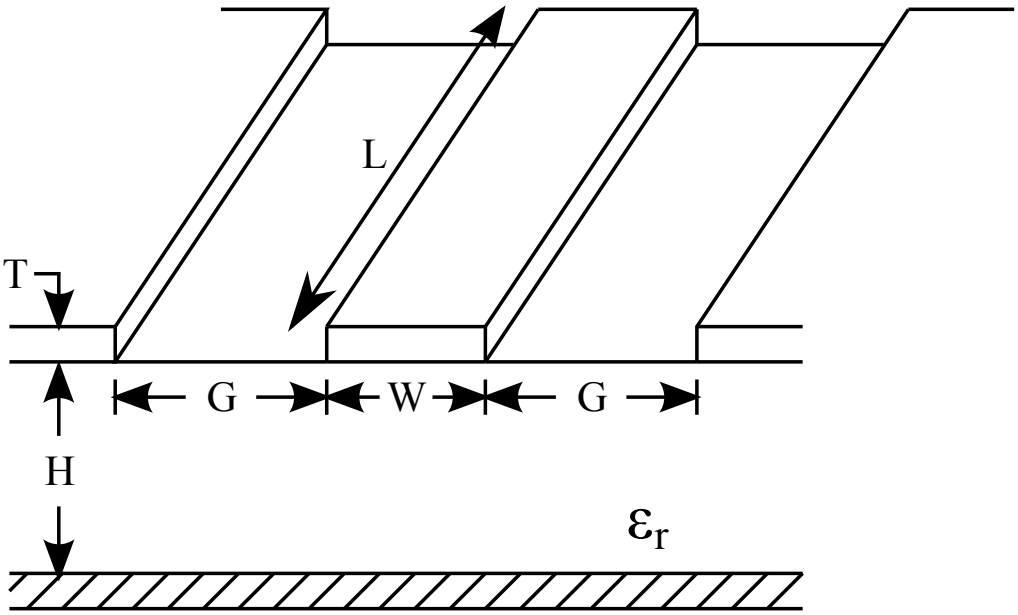

Figure 21: Structure of CPWG.

Table 4: Design parameters of the 50-Ω transmission line.

Parameter	**Variable name**	**Value**
Frequency	f	2.4 GHz
Relative permittivity	ϵ_r	4.1
Height of the substrate	H	0.680 mm
Copper thickness	T	17 μm
Width of the center strip	W	0.762 mm
Gap between ground plane and the center strip	G	0.160 mm
Length of the center strip	L	7.750 mm

The transmission line is modelled as a coplanar waveguide with lower ground plane (CPWG) in Agilent ADS. CPWG structure is presented in Figure 21 and the design parameters of the simulated model in Table 4. Characteristic impedance of the designed transmission line is 49.930 Ω at 2.4 GHz according to ADS. The simulation results are presented in Figure 22.

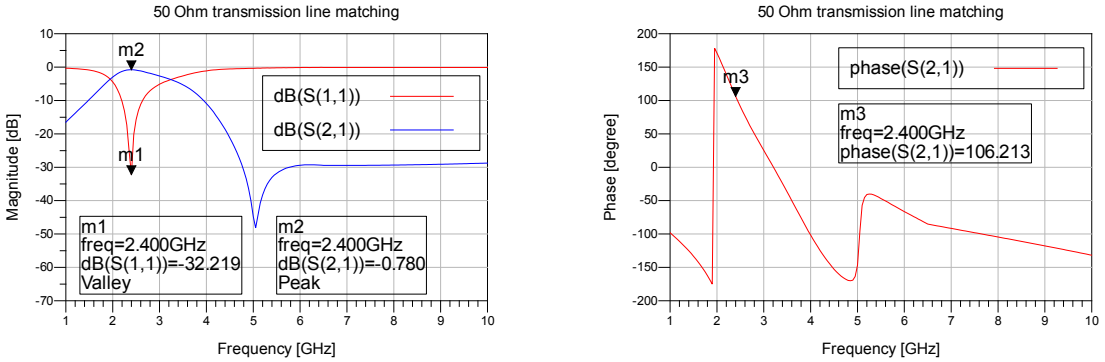

Figure 22: Simulation results for the designed transmission line.

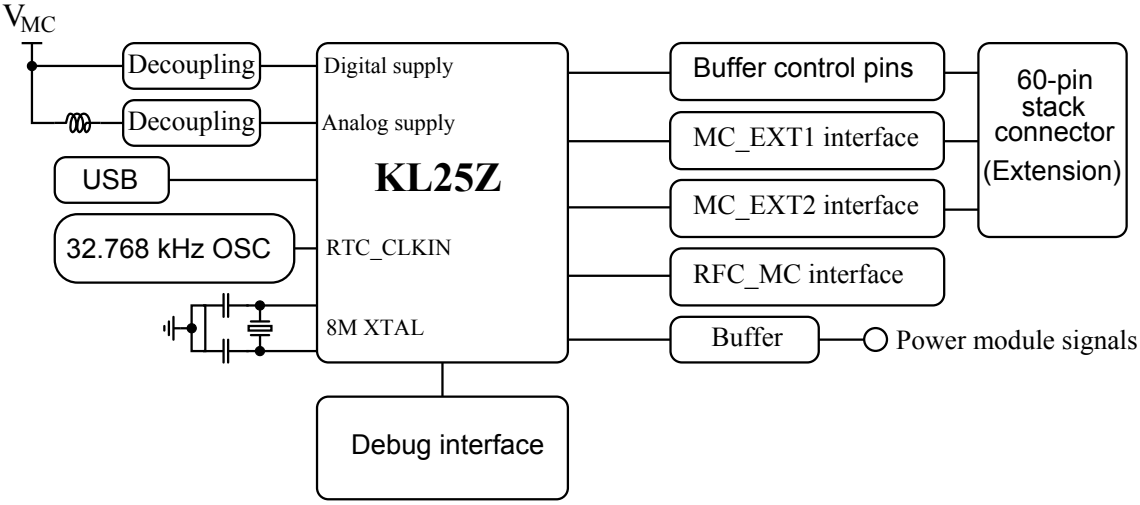

Figure 23: Main controller of the node.

3.4.6 Main controller

Selected main controller, KL25Z from Freescale, is an ARM Cortex M0+ -based MCU which is specially designed for low power applications. Figure 23 shows the hardware components related to the main controller. Main controller features a large variety of low-power peripherals and is highly configurable since most of its pins can be multiplexed up to seven different functions. Fully compliant USB 2.0 OTG module is also integrated. The internal USB regulator is used to provide a 3.3 V output from a USB supply. This output serves as one of the primary supplies for the main module. It enables powering of the main module and all extension modules straight from the USB and thus, removes the absolute requirement for a connected power module.

Clock generation and distribution of the main controller is presented in Figure 24. Flexible clocking network allows the use of various clock sources. There are two internal RC oscillators providing 4 MHz and 32 kHz clocks. Alternatively, external crystals or even oscillators can be used to provide a more accurate and stable clock. An 8 MHz external crystal is connected to enable usage of internal PLL. Internal

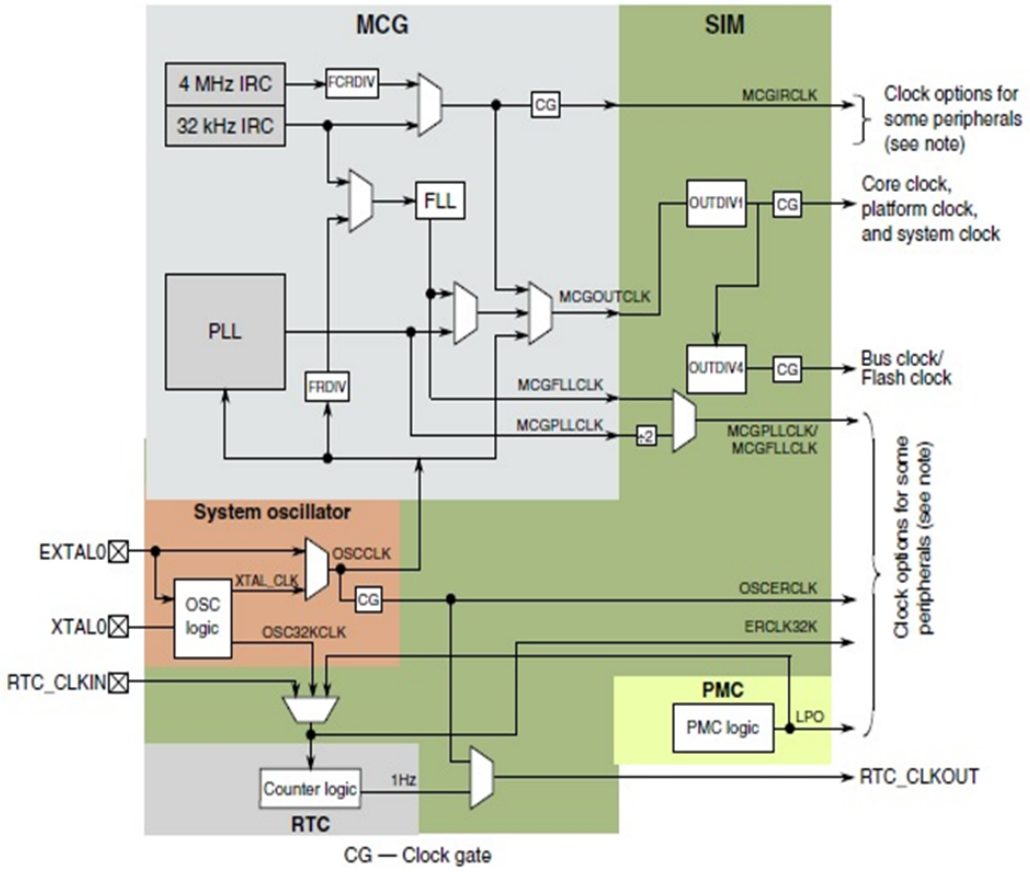

Figure 24: Clock generation system of the main controller [30, p. 116].

oscillator logic block of the MCU consists of a Pierce oscillator and a divider that is used to produce an additional 32 kHz output.

MCGOUTCLK, as shown in the Figure 24, is the main core, system and bus clock. This clock can be produced directly from the internal RC oscillators, the external crystal or oscillator or through the PLL or FLL. USB 2.0 full-speed operation requires a clock signal of 48 MHz. From the figure it can also be seen that either MCGPLLCLK or MCGFLLCLK can be used to produce the clock. If PLL is used, the correct clock frequency setting is 96 MHz because of the divider in the clock path.

For more accurate clocking, external clock sources are used in the design. Using Equation (3), the total load capacitance for the crystal can estimated as 16 pF. An external 32.768 kHz oscillator is used to provide the RTC_CLKIN pin a stable and accurate clock signal. This can be used to power certain peripherals in extremely low-power sleep modes where almost everything is otherwise clocked off. Selection of the correct clock sources must be handled in software by configuring the proper registers. The MCU defaults to using FLL with an internal reference clock.

The main controller provides nine different power modes in addition to a normal run mode. General-purpose I/O pin states are held in each power mode but data

retention and peripheral state retention depend on the power mode used. Low-leakage wake-up unit (LLWU) is used as the primary wake-up source for the lowest power modes. Depending on the power mode, wake-up is performed through either a normal interrupt, an LLWU interrupt or a system reset.

Similar to the radio controller, the debug interface of main controller consists of the programming interface and a UART peripheral for serial debugging. Programming of the main controller is performed through the ARM-specified SWD interface.

3.4.7 Interface between MCUs

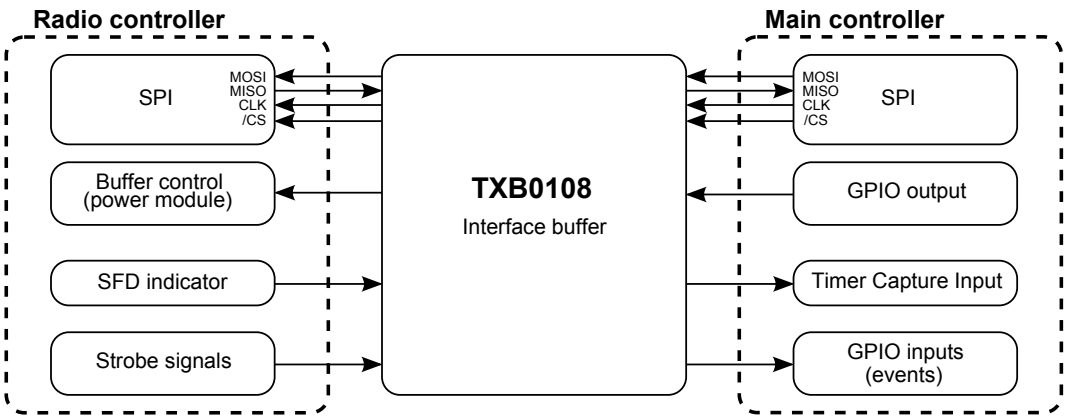

Figure 25: Interface between radio controller and the main controller.

Figure 25 presents the high-speed interface between radio controller and main controller. Data is transferred by using serial peripheral interface (SPI) which is a synchronous serial communication interface. Radio controller uses direct memory access (DMA) controller for the SPI module assigned to the interface. Thus, the data received through the interface is directly transferred to a specific memory address location. Directions in figure are based on the assumption that the main controller is the master of the SPI bus. As a master, it is responsible for generating the clock signal.

In addition to SPI, the interface has the SFD indicator required by the timing management and two strobe signals. The strobe signals are used to indicate various events. For example, radio controller can inform the main controller that is has processed the data that was sent by the main controller and is ready to receive more. These indications can be registered by the event manager, a part of the software that creates and handles various events.

Since both the radio controller and the main controller have access to certain same power module resources, only one of the controllers can be a power module master at a time. One GPIO pin of the main controller is dedicated to controlling state of the power module buffers. An inverted control signal is used to drive main controller side buffers. Radio controller's buffers are enabled by default since it cannot be presumed that the main controller will always be powered. Thus, by default, radio controller is the controller of power module.

The interface buffer is automatically enabled when both radio controller and the main controller is powered. Enable pin of the interface buffer is not controllable. Thus, when entering a low-power mode, software needs to set the interface pins to high-impedance state in order to avoid excessive current consumption due to the internal input/output drivers of the buffer.

3.4.8 Summary of features

Radio controller provides a complete SoC solution by integrating an 8051-based microcontroller and a Bluetooth Low Energy compliant RF transceiver. Main controller is a powerful ARM Cortex-M0+ -based microcontroller that provides increased processing capabilities and extends the available memory resources. This is especially useful for large or complex applications since the compiled code size for 8-bit 8051-based microcontroller can be substantially larger than for microcontrollers using 32-bit architecture, such as the main controller in this case [31]. For example, depending on the configuration, the compiled BLE protocol stack size itself can be up to 128 kB, consuming 50 % of the program memory available for the radio controller.

Since the main controller provides a highly flexible clock generation and distribution system, processing and memory resources can be scaled to meet the requirements of a wide range of applications. These resources can be further extended by designing simple slave modules. Extended abstraction software of the node provides a common middleware for device accessing. Thus, only the device-specific software development is required since the middleware can be reused as it is [9].

Table 5: Interfaces provided by the main module's MCUs.

Interface	Radio controller	Main controller
GPIO	4	12
Analog	0	2
I^2C	1	1
UART	1	2
SPI	1	1
Timer - capture input	1	1
Timer - compare output	1	1
Timer - PWM	2	2

Table 5 provides a list of the interfaces provided by the radio controller and the main controller. These interfaces can be used to connect the slave modules. Interfaces provided by the main controller can be used freely. Radio controller, however, has a limited number of pins and has to use the same connections for the interface between the MCUs and the extension interface. Because of this, available radio controller interfaces must be studied carefully to avoid overlapping before application development.

3.5 Extension module

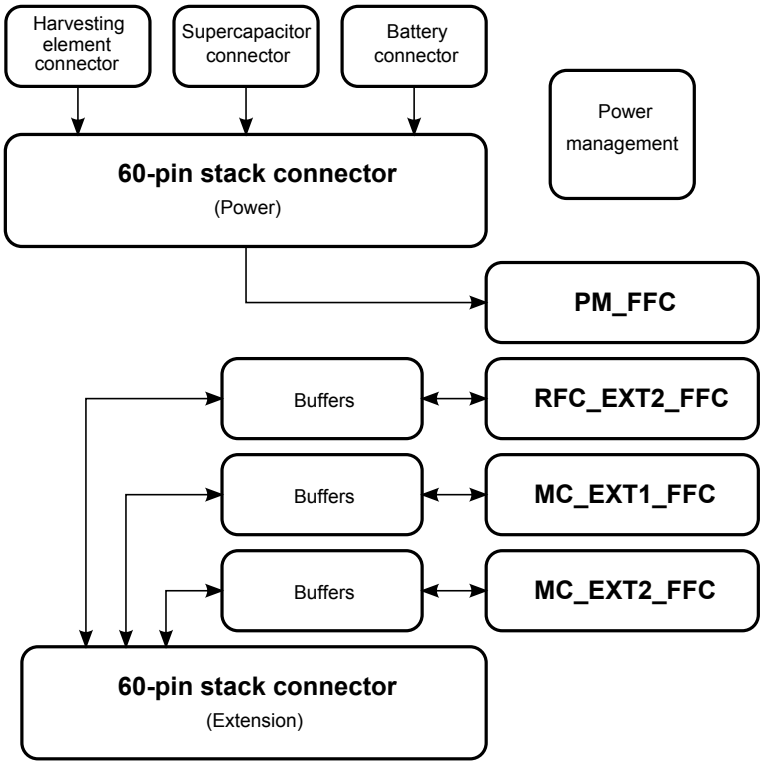

Figure 26: Block diagram of the extension module.

Figure 26 presents block diagram of the extension module. It is the simplest module; only the necessary power supply connectors and the interface buffers and connectors are featured. The same power management subsystem that was introduced in Section 3.4.1 is used to prioritize the 3.3 V supplies provided by power module, main module and debug module.

Since supply voltage of the main module can vary, voltage-level translators, or buffers, are used to ensure safe voltages and signal isolation if required. The buffers are controllable by the main controller. Only the RFC_EXT2 buffer is enabled by default to ensure that it is usable in radio controller only -scenarios. Reference voltage for the buffers on extension module is 3.3 V. Thus, if a 5.0 V supply is used by the slave modules, it is necessary to convert the signals to 3.3 V beforehand.

Extension module is assumed to be the topmost module. Thus, it features the bulky PH-connectors through which a battery, a harvesting element and a supercapacitor are connected. Extension and power connectors are 20-pin FFCs. Slave modules can be supplied and interfaced through these connectors. Designing slave modules that use stacking connectors instead is also allowed. In this case, it is important to remember that voltage-level translations must be done for the used signals.

3.6 Debug module

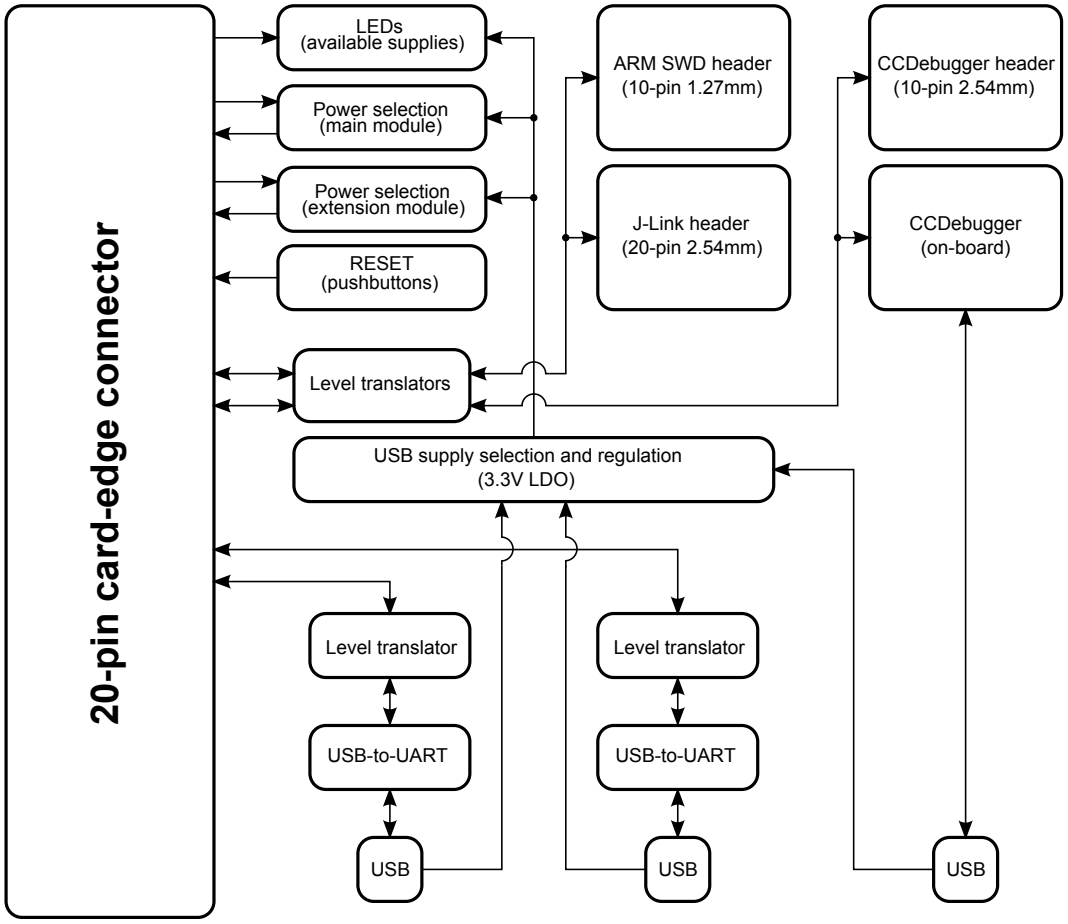

Figure 27: Block diagram of the debug module.

Block diagram of the debug module is presented in Figure 27. Debug module features various options for programming and debugging the node. The main controller can be programmed by using either Segger J-Link JTAG+SWD emulator or with any emulator supporting ARM specified 10-pin 1.27 mm SWD connector. An on-board JTAG/SWD emulator is not provided because an open source binary file to program the emulator is not available.

The radio controller CC2541 can be programmed directly using a Texas Instruments' general programmer, the CCDebugger. CCDebugger features are provided with an on-board emulator. The biggest benefit of the on-board emulator is the possibility to program the device of interest through a standard USB port. It should be noted that, in these cases, the emulator needs to be programmed as well. A specific programming header for the on-board CCDebugger is provided in the design.

Debug module features also possibility for serial port debug output via USB for both MCUs. The USB data is converted to a serial format using USB-to-UART converter ICs. To guarantee safety of the MCUs, voltage-level translators are used to ensure that voltage levels are properly set for the UART signals. Since the debug

module requires power to operate and should not be supplied from the node side, a 3.3 V LDO regulator is included on the debug module. The programmer should use one of the active USB power signals as an input for the LDO. The input is selected with a jumper.

Plugging debug module to the main module disables primary power path on the main module immediately. It is required to provide a proper supply voltage from the debug module. The debug module is designed in such a way that the various power sources of the main module can enabled by jumper selection. This is possible because the primary power paths of the main module are routed to the debug module as well. Debug module simply adds its own supply to the selection.

3.6.1 Programmers

CCDebugger emulator is based on the CC2511 MCU which operates from 48 MHz external crystal which is required to run the USB functionalities. The designed emulator is modified slightly from the original reference design of CCDebugger to reduce the number of required components. Programming signals are buffered to protect the radio controller. RESET signal is both inverted and voltage-level translated through a simple transistor configuration.

In addition to the CCDebugger on-board emulator, debug module provides possibility to program the radio controller with a standalone CCDebugger device. Data, clock and RESET lines are common for both programming methods. Only one of the programmers should be used at a time to avoid possible conflicts due to common lines. SPI debugging and programming is not provided in the design.

There is no on-board JTAG/SWD emulator provided so the main controller has to be programmed using either Segger J-Link or with another device supporting ARM specified 10-pin programming connector. This SWD interface provides all normal JTAG debug and test functionalities. The 10-pin Cortex debug header is a 1.27 mm connector. In the design, an unshrouded version of the connector is used. Because of this, the cable should be connected carefully. There exists no additional protection to prevent possible system damage when the cable is connected improperly. The purpose of the debug header is to provide an alternative way to program the main controller should programming via J-Link fail.

3.6.2 Serial port debugging

Serial port debugging enables monitoring of the node's functions on a PC screen. To provide a useful debugging interface, both software and hardware elements are important. Implementing a working USB connection that is compliant to the standard is a time and resource consuming task and requires a specific USB module to be integrated in the hardware. Instead, a simple serial interface can often be used to provide an option for debugging. In this case, special ICs called USB-to-UART converters can be applied to convert the differential USB signal to a convenient serial format. The serial data can be transferred between the IC and target MCU through a standard UART interface.

The USB data lines are routed as a 90 Ω differential pair. RX and TX lines are buffered to a safe voltage level before routed to the card-edge connector. Driving capabilities of the converters are sufficient to use a TXB series buffer. The I/O threshold voltages of the buffered IC and the buffer itself should always be compared to ensure that voltage levels are interpreted properly.

3.7 PCB design

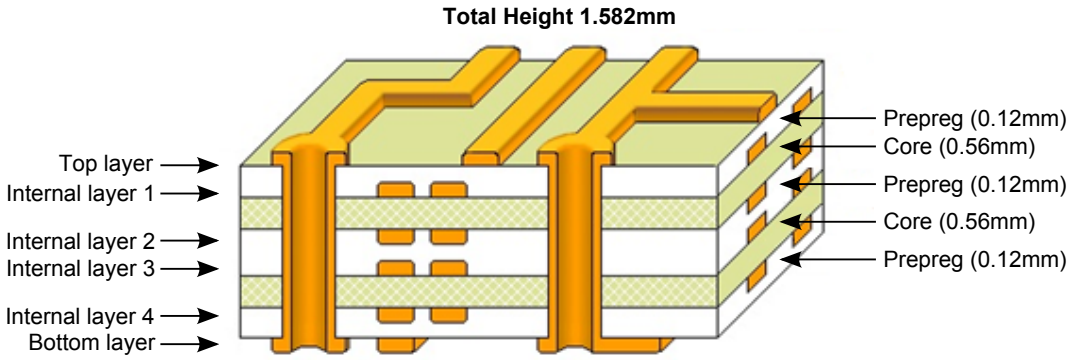

Figure 28: PCB layer stack-up of the node has 6 layers and total height of approximately 1.6 mm.

Figure 28 presents the PCB layer stack-up used in the design. A 6-layer board with 17 μm copper thickness and total height of approximately 1.582 mm is used for each module. Usage of the internal layers differ per module; main module, for example, uses internal layer 2 as the RF ground plane while other modules use it for signal routing. The PCBs are designed with board base dimensions of 35 mm x 40 mm with possible 5 mm extensions on the sides. These extensions are for casing purposes and to provide easier access to the connectors.

Figures 29, 31 and 30 present top views of the designed core modules along with the physical dimensions of the boards. In addition to the three core modules, a small adapter board and a debugging and programming module, the debug module, were designed. These boards, however, take no part in the deployment and thus, have no size or power constraints. First revision of the node hardware implemented male card-edge connector on the main module board. The second revision removed this and instead provided a small adapter board featuring the male card-edge connector. The adapter board can be connected either by an FFC cable or through the stack connector to the main module.

The main module, presented in Figure 31, is more densely populated than the other modules. Thus, special attention on routing and component placement is critical due to the sensitive radio parts. In order to reduce trace width of the 50-Ω transmission line, internal layer 2 is selected as the RF ground plane. This selection gives 0.68 mm as the total thickness of the substrate between the transmission line on the top layer and the RF ground plane. This is the exact value used in the simulations of Section 3.4.5.

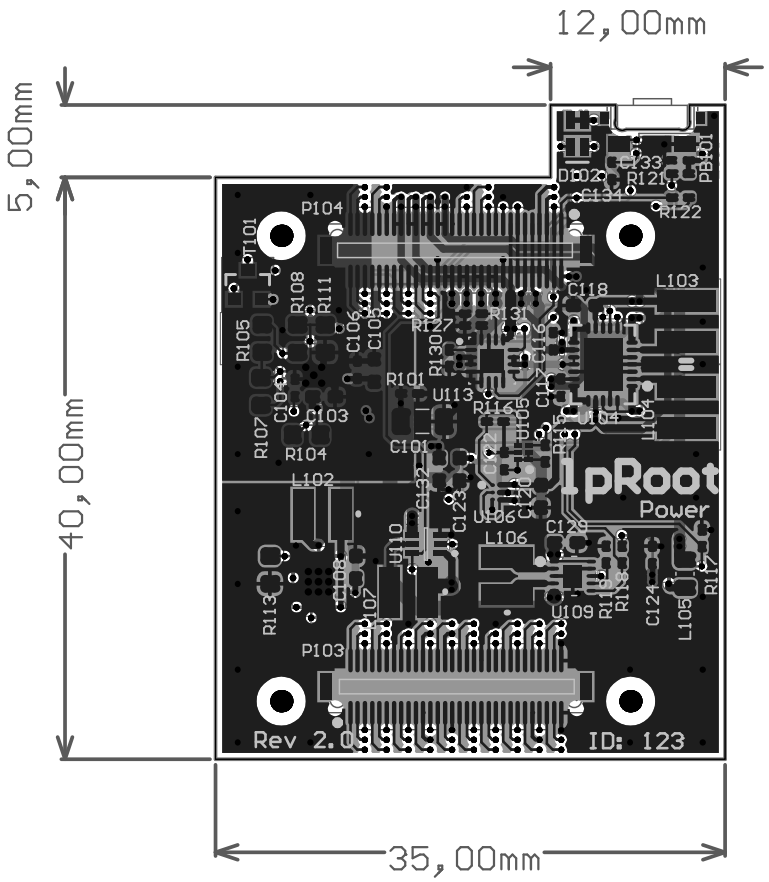

Figure 29: Top view of the power module PCB.

Extension module must be placed as the topmost module since it has the stacking connectors only on the bottom side. Power module and main module can be connected in any order. Mated stacking height of the modules is only 3 mm so component placement is critical. Bulky components, such as the inductors, should be placed in such a way that they face a component-free zone on the opposing module. In the end, a 3D model of the node with different stacking orders was created and used to confirm that the components of the modules do not prevent the stacking.

Some of the power module's functionalities are placed on the extension module instead. The reason for this is that since the power supply connectors are located on the extension module, routing certain blocks can be performed more easily on the extension module. As an example, the bypass circuit presented in Section 3.3.1 requires only connections between the harvesting and storage elements. Thus, the components of this unit can be placed directly between these connectors.

3.8 Estimated power consumption

Power consumption estimations for various blocks of the node while in a low-power state are presented in Table 6. The total power calculated specifies the minimum required power that must be provided by the energy harvester to maintain battery

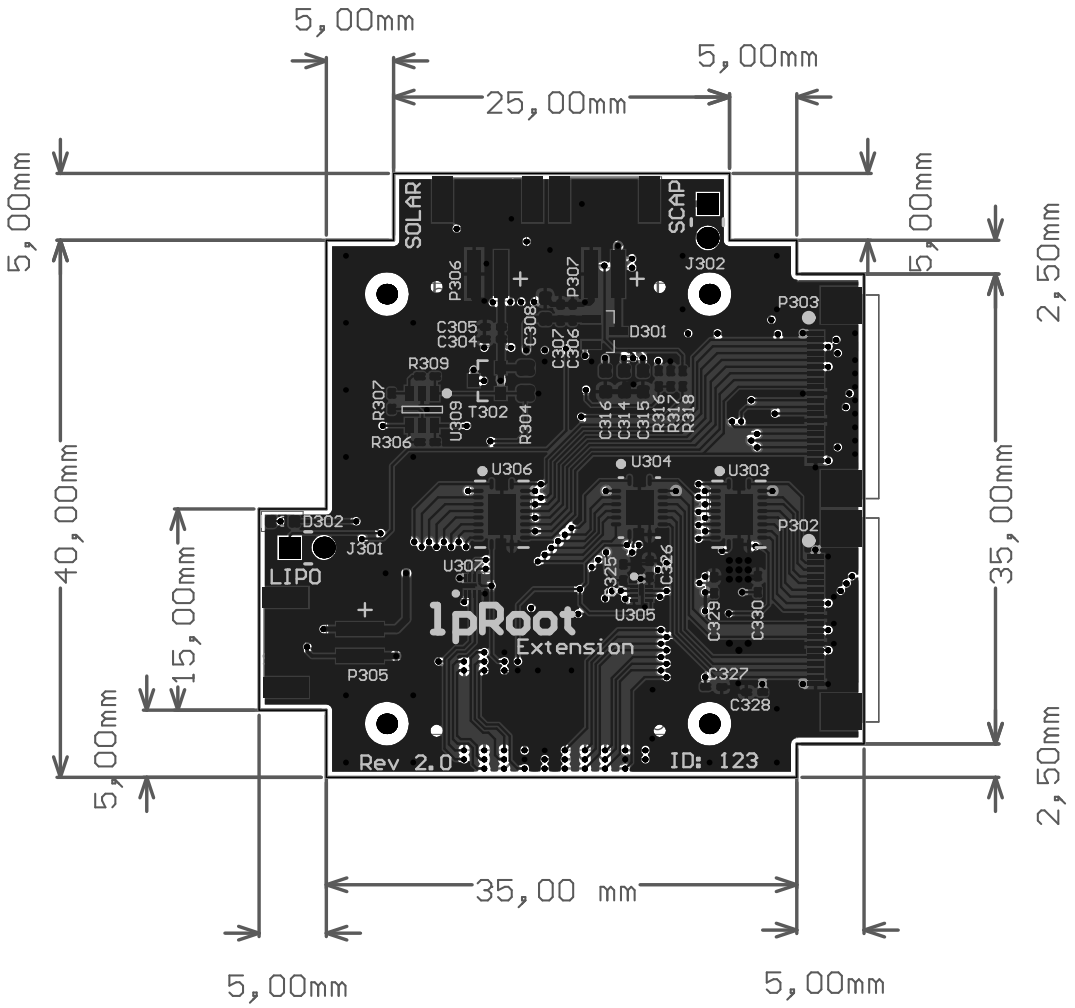

Figure 30: Top view of the extension module PCB.

level while the node is in a low-power mode. Otherwise, the battery level will begin to decrement until the power is cut off completely. As can be observed from the Table, approximately 53 % of the total power is consumed by the power switches of the power path controller and the power management subsystem of main module while the node is in the lowest power state.

- Low power consumption
- Reverse current blocking
- Low losses on the power paths
- Controllable output enable
- Controllable path selection
- Forced default state
- Small size.

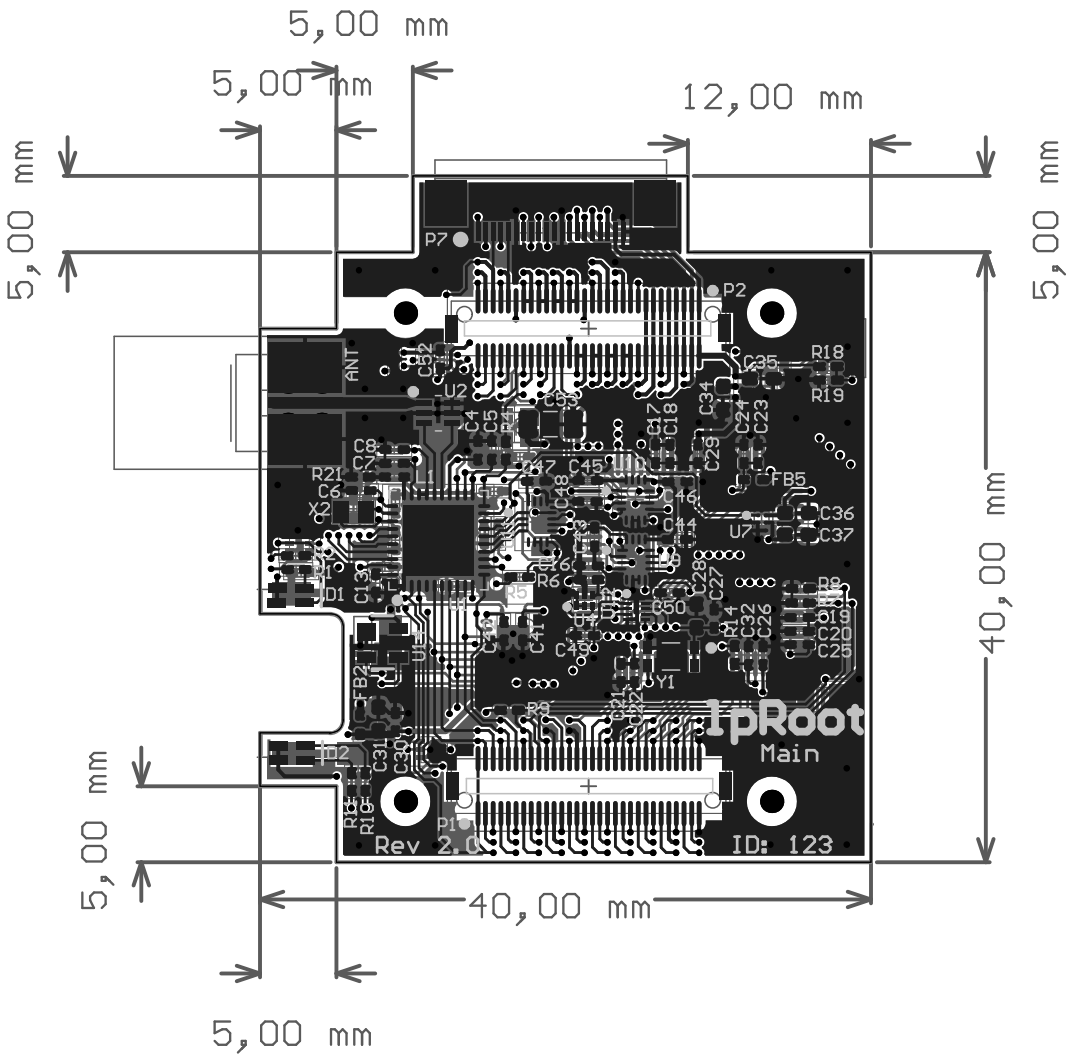

Figure 31: Top view of the main module PCB.

Table 6: Estimated minimum power consumption of the node.

Source	**Current consumption**
Bypass circuit	3.0 μA
Energy harvester	3.0 μA
Pushbutton controller	2.0 μA
Power path controller	15.0 μA
Main regulator (bypass)	0.5 μA
3.3V regulator (disabled)	1.0 μA
Power management (main module)	7.0 μA
MC power control (disabled)	0.5 μA
Radio controller (lowest)	$<$1.0 μA
Main controller (lowest)	$<$1.0 μA
MC-RFC interface	3.5 μA
	Total: 34 μA, 125.8 μW at 3.7 V supply

4 Measurements and results

This section presents measurement results for power consumption of the designed node. The measurements are performed to complete power consumption profiling of the node. For this purpose, the node is configured with different clock and power related settings. Measurements are carried out in such a way that usually one setting, either clock or power mode related, is altered at a time. These various configurations are referred to as power states. However, the results are presented as current values to enable easier comparison to the values listed in the datasheets. Current values can be converted to actual power values by multiplying the results with the input supply voltage of 3.7 V.

4.1 Measurement setup

4.1.1 Equipment

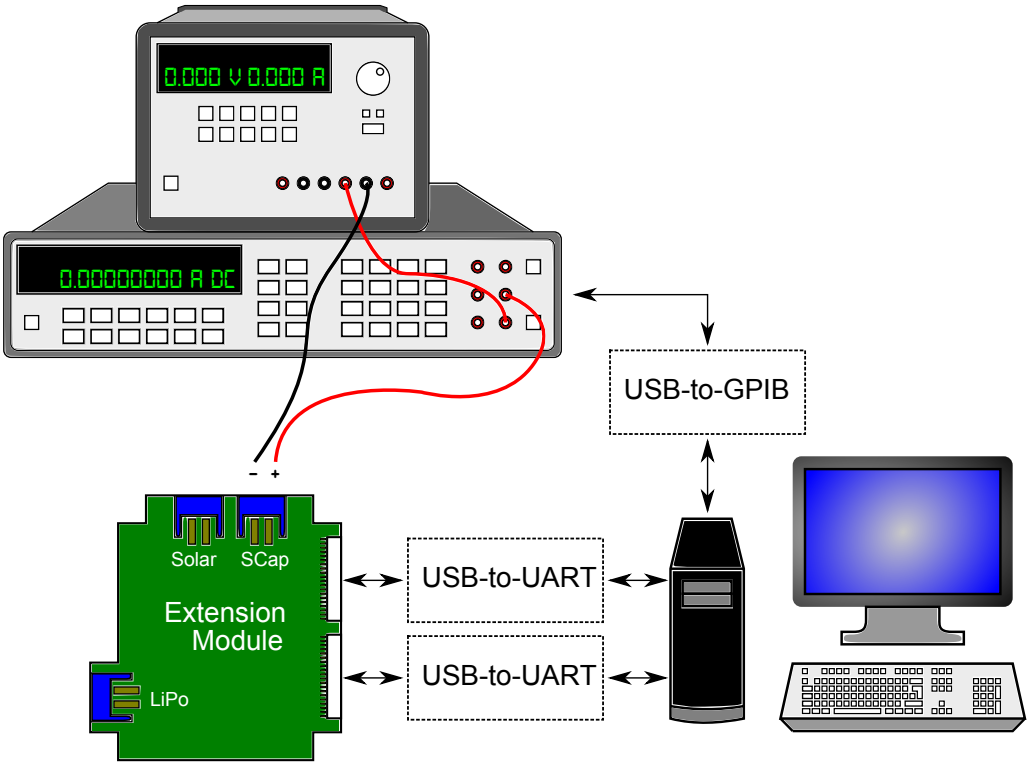

Figure 32: Hardware setup used during the measurements.

Figure 32 presents hardware setup used in the measurements. Digital power supply is connected through a digital multimeter to the node for DC current measurements. The multimeter is connected to PC through a USB-to-GPIB converter. Radio and main controller of the node are connected to the same PC through node's extension connectors using USB-to-Serial converters. Since the cables used for this cause convert data in USB format to RS-232 and vice versa, small adapter boards are used

to match the standard DB9 connector of the cables and to translate voltage levels between node and cables. These adapter boards are supplied from 3.3 V regulator of the power module. This means that the regulator must be turned off during measurements to eliminate effects of adapter boards on the results. Since the 3.3 V regulator is intended to serve as a main supply of external sensor boards, measuring the power consumption of the regulator is essential. One power state is dedicated for running the node with the regulator left enabled. In this case, the power state configuration is programmed directly to the node without connecting the adapter boards.

Voltage that is supplied is set to 3.7 V and is fed from the node's storage element connector. If power is supplied from harvesting element connector instead, a storage element is required to be connected for the node to function. In this case, properties of the used storage element, such as leakage current, generate an unknown offset on the results. In order to take this into account, used element must be completely characterized first to identify magnitude of this offset. While this approach is more realistic, it applies only for the selected storage element. For example, leakage current of a supercapacitor, as discussed earlier in this thesis, stabilizes typically after a certain period of time and also varies between different models. Thus, the measurements are performed by feeding power through the storage element connector to measure power that is required to keep the system operational. Measured power consumption can be used to define minimum requirements for harvesting and storage elements. A harvesting element must be able to provide enough power to match the application's average power consumption, taking into account leakages that might occur due to the selected storage element and possible variations in ambient conditions.

Host PC controls operation of both microcontrollers of the node and the digital multimeter. Because of USB-to-Serial conversion, microcontrollers can be controlled from the PC through virtual COM ports. Microcontrollers must enable correct internal UART interface to become serially accessible. GPIB, or more generally IEEE-488, is an interface standard that is commonly used in measurement equipment for automated operation. GPIB devices can be chained since each such a device has an individual address which can often be altered in the equipment's configuration options. Almost all modern devices use a 24-pin standardized connector that is not available in most PCs. Hence, an adapter is required to operate a GPIB device from PC. Table 7 presents a list of equipment used in the measurements.

Table 7: List of equipment.

`Power supply`	Agilent E3631A
`Digital multimeter`	Agilent 3458A
`USB-to-GPIB converter`	Agilent 82357B
`USB-to-Serial converter`	Belkin F5U257
`Node hardware`	lpRoot Rev 2.0

4.1.2 Software

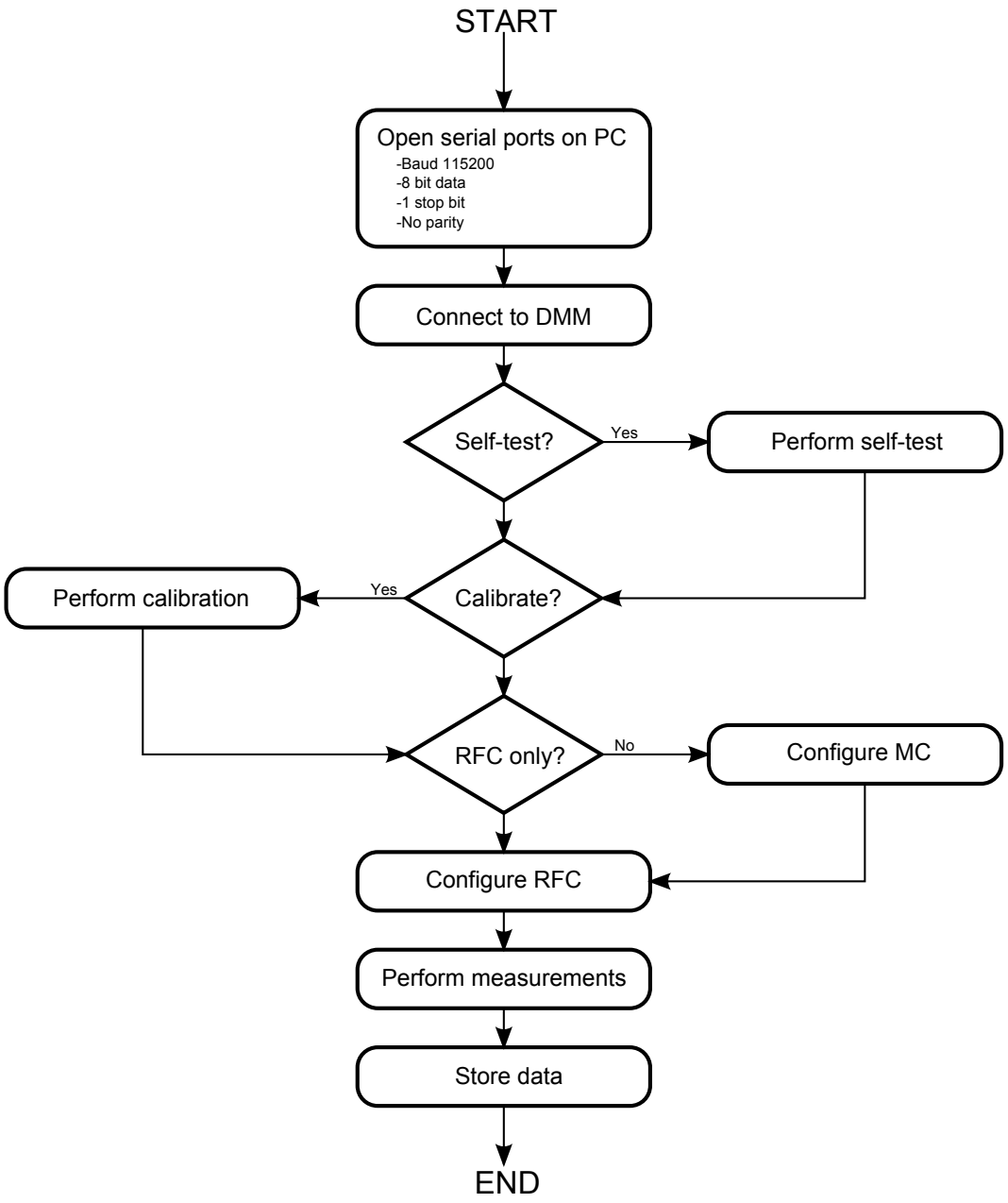

Figure 33: Measurement software flow chart.

Measurements were performed by controlling operation of the digital multimeter from MATLAB. Flow chart of the measurement program is presented in Figure 33. Both self-test and calibration were performed before the first measurement but not afterwards. In radio controller -only modes, the target power state was sent directly to the radio controller through the serial port. Otherwise, the target power state was sent to the main controller which in turn configured the radio controller properly. Measurement time was set to 3 minutes per power state.

4.2 Error estimation

Errors in the results are mainly caused by the digital multimeter. Different error sources are listed in Table 8 along with the estimated values. Accuracy of the multimeter is specific to range that is used and thus, value listed in the table applies only for 100 mA range which was used in the measurements. Ambient temperature was not monitored during the time measurements were performed but can be assumed to be within ±1 °C range. Errors due to used cables are not discussed here since these errors can be estimated to be very small for the current range that was measured.

Table 8: Errors due to the multimeter.

Source	Error type	Value
Accuracy	ppm Reading + ppm Range	25 + 4
Temperature coefficient	(ppm Reading + ppm Range)/°C	2 + 1
RMS noise	ppm Range	1
Additional gain error	ppm Reading	0.1

4.3 Power states

Configurations for the different power states are defined in Table 9. Since the node can be operated with the main controller side completely powered down, it is important to measure the power consumption separately for both operation modes. For the radio controller only -mode, the power consumption is characterized with different clock and low-power mode settings while the main controller is powered down. For the operation mode where both MCUs are powered up, the radio controller is placed in the lowest power consuming mode while similar characterization is performed for the main controller. Power consumption of the node when everything is enabled is also measured. Figure 34 presents a graphical view of the different power states and their corresponding operation modes.

4.4 Radio controller

4.4.1 Clock configurations

During states 1 through 4, the radio controller is configured with different clock-related settings. In states 1 and 3, a 32 MHz XTAL is used as the clock source. Radio controller is programmed to enter idle mode in state 3. In this mode, the core itself is not clocked but the peripherals remain enabled and can cause interrupts to exit from the idle mode. Same configuration is used for states 2 and 4 but a 16 MHz internal RC oscillator of the radio controller is used instead as the clock source.

Measurement results for states 1 to 4 are presented in Figure 35. As expected, entering the idle mode reduces total current consumption. Current savings in this

Table 9: Measured power state configurations.

	POWERED		CORE CLOCK		CLOCK SOURCE		POWER MODE[1]		REGULATORS			
	Radio controller	Main controller	Radio controller	Main controller	Radio controller	Main controller	Radio controller	Main controller	2.1V	3.3V	5.0V	Radio
State 1	Yes	No	32 MHz	-	XTAL	-	Run	-	On	Off	Off	Off
State 2	Yes	No	16 MHz	-	IRC	-	Run	-	On	Off	Off	Off
State 3	Yes	No	32 MHz	-	XTAL	-	Idle	-	On	Off	Off	Off
State 4	Yes	No	16 MHz	-	IRC	-	Idle	-	On	Off	Off	Off
State 5	Yes	No	-	-	-	-	PM1	-	Off	Off	Off	Off
State 6	Yes	No	-	-	-	-	PM2	-	Off	Off	Off	Off
State 7	Yes	No	-	-	-	-	PM3	-	Off	Off	Off	Off
State 8	Yes	No	-	-	-	-	PM3	-	Off	On	Off	Off
State 9	Yes	No	32 MHz	-	XTAL	-	Run	-	On	Off	Off	On
State 10	Yes	No	32 MHz	-	XTAL	-	Run	-	Off	Off	Off	On
State 11	Yes	Yes	-	48 MHz	-	FLL (IRC reference)	PM3	Run	On	Off	Off	Off
State 12	Yes	Yes	-	45.75 MHz	-	FLL (XTAL reference)	PM3	Run	On	Off	Off	Off
State 13	Yes	Yes	-	48 MHz	-	PLL	PM3	Run	On	Off	Off	Off
State 14	Yes	Yes	-	4 MHz	-	IRC	PM3	Run	On	Off	Off	Off
State 15	Yes	Yes	-	8 MHz	-	XTAL	PM3	Run	On	Off	Off	Off
State 16	Yes	Yes	-	4 MHz	-	XTAL (divided by 2)	PM3	VLPR	On	Off	Off	Off
State 17	Yes	Yes	-	-	-	PLL	PM3	WAIT	On	Off	Off	Off
State 18	Yes	Yes	-	-	-	PLL	PM3	PSTOP1	On	Off	Off	Off
State 19	Yes	Yes	-	-	-	PLL	PM3	PSTOP2	On	Off	Off	Off
State 20	Yes	Yes	-	-	-	-	PM3	STOP	Off	Off	Off	Off
State 21	Yes	Yes	-	-	-	-	PM3	LLS	Off	Off	Off	Off
State 22	Yes	Yes	-	-	-	-	PM3	VLLS3	Off	Off	Off	Off
State 23	Yes	Yes	-	-	-	-	PM3	VLLS1	Off	Off	Off	Off
State 24	Yes	Yes	-	-	-	-	PM3	VLLS0	Off	Off	Off	Off
State 25	Yes	Yes	32 MHz	48 MHz	XTAL	PLL	Run	Run	On	On	On	On

[1] As defined in the device's datasheet.

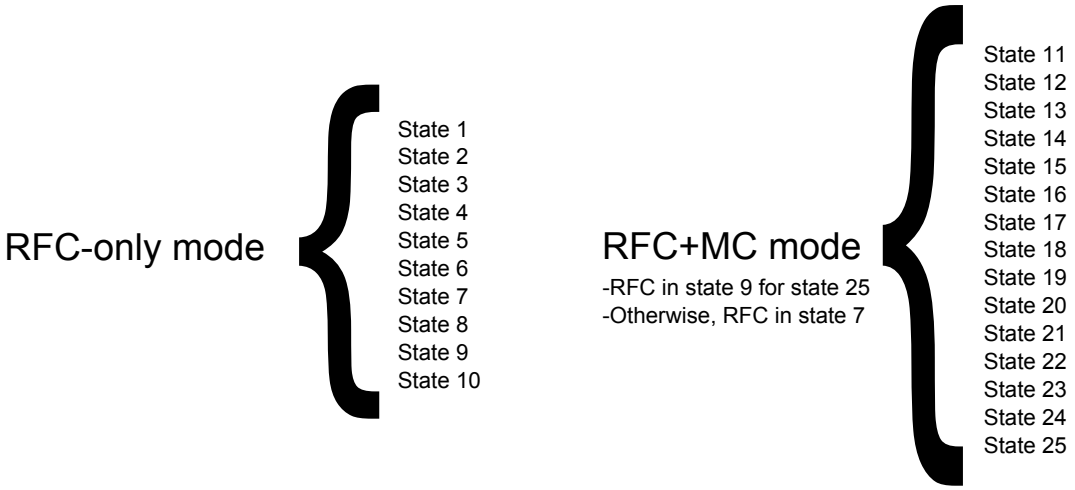

Figure 34: Graphical view of the power states and their relevant operation modes.

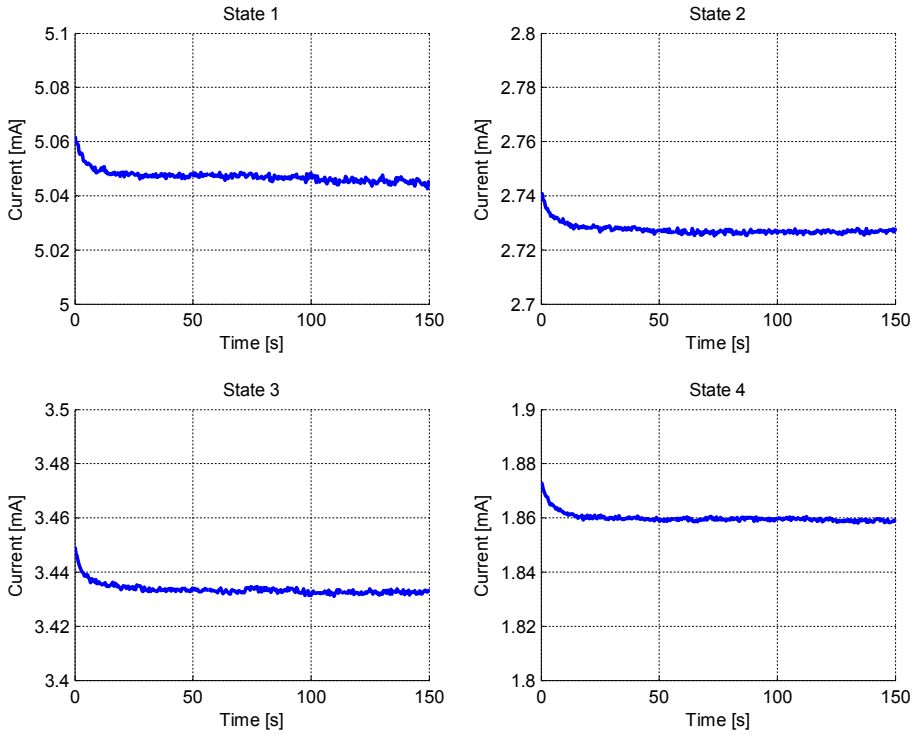

Figure 35: Measurement results for radio controller's clock-related power states.

state are approximately 30 % compared to continuously running operation. Since the power consumption is almost linear with frequency, increasing the clock speed has a significant impact on the total power consumption. This can observed when comparing states 1 and 2 of the Figure 35.

4.4.2 Low-power mode configurations

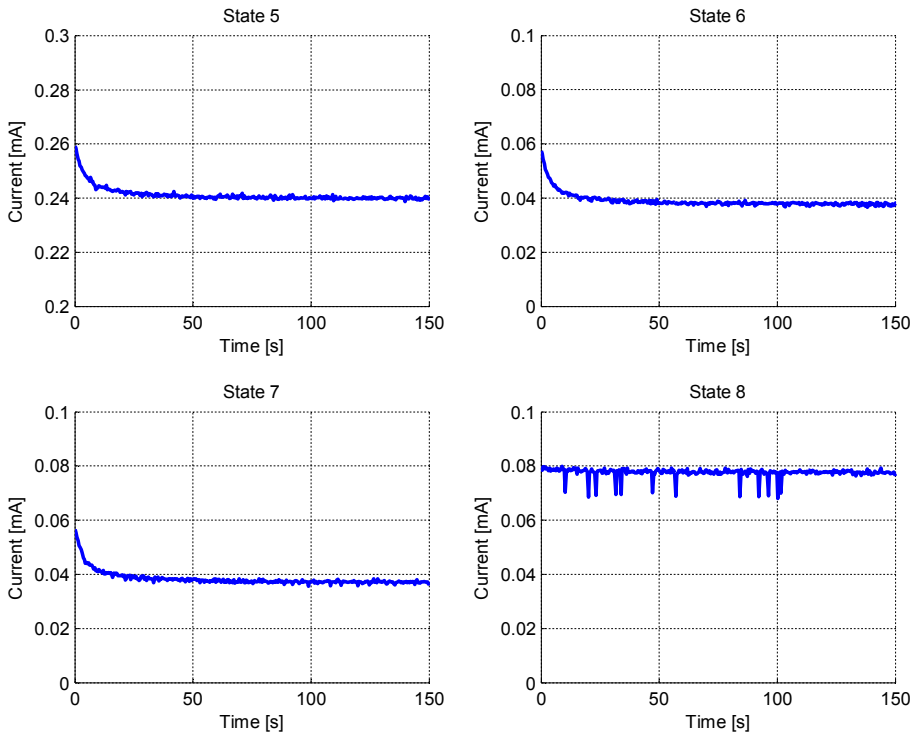

Figure 36: Measurement results for radio controller's low-power mode -related power states.

States 5 through 8 are related to low-power mode settings of the radio controller. In state 5, the controller is programmed to enter fast sleep mode, or PM1 as defined in the datasheet, where the voltage regulator for digital block remains enabled in order to decrease wake-up time. As can be seen from Figure 36, this increases the power consumption drastically compared to other low-power modes. It should be noted that while the high-speed oscillators are disabled, a 32 kHz XTAL or internal RC oscillator is enabled to power up certain peripherals that can cause interrupts to exit from this power mode. Similarly during state 6, radio controller is programmed to enter sleep mode (PM2) which is essentially the same as the fast sleep mode without the regulator.

Radio controller enters an extremely low-power mode, the deep sleep mode (PM3), during state 7. In this mode, almost everything is disabled on-board. Only available wake-up sources from this mode are chip reset and external interrupts. The external interrupts are generated, as the name suggests, by GPIO pins capable of registering rising or falling edges of the signals used to generate the interrupts. In state 8, radio controller is again in the deep sleep mode but the 3.3 V regulator on power module remains enabled in order to provide power for slave modules and voltage-level translators of extension module. Thus, state 8 indicates the minimum power consumption when constant power is required on the connected slave modules.

4.4.3 Radio configurations

Radio power consumption is measured by placing the radio to a specific test mode. In the test mode, radio is set for TX operation with 0 dBm TX power which is the maximum output power of the device. When the test mode is enabled, the radio starts sending a continuous stream of all zeroes at 2.4 GHz frequency.

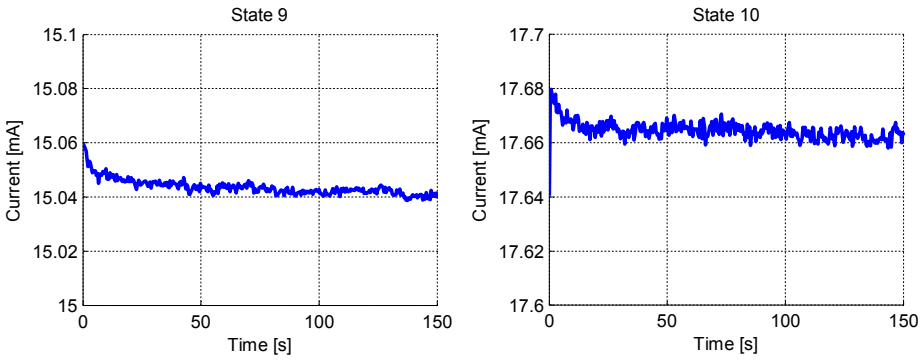

Figure 37: Measurement results for radio operation -related power states.

Figure 37 presents the measurement results for states 9 and 10. In these states, a 32 MHz XTAL is used as the clock source which is a requirement set by the radio. The radio is enabled in a test mode and sends a continuous stream of all-zeroes at 2.4 GHz with 0 dBm TX power. Difference between these two power states is the status of 2.1 V regulator of the power module. The regulator is disabled in state 10. In this case, the supply voltage of the main module is 2.7 V.

Motivation to measure these two states separately was to confirm the promised power savings when using the particular regulator. As can be seen from the Figure, current savings of approximately 15 % are achieved when the regulator is enabled. However, effects of lowering the supply voltage on the radio performance were not measured but should be done in the future when the radio stack is made to work.

4.5 Main controller

4.5.1 FLL/PLL clock sources

Measurement results for main controller's normal clock configurations are presented in Figure 38. In states 11 and 12, clock source of the main controller is the internal FLL unit. Internal 32.768 kHz RC oscillator is used as a reference for FLL in state 11 to produce a 48 MHz output while state 12 uses reference clock derived from an 8 MHz XTAL. Due to the internal clock divider, the actual reference clock frequency in state 12 for the FLL is 31.25 kHz which results in 45.75 MHz output frequency.

In state 13, internal PLL unit is used to generate 48 MHz clock. Only external reference is applicable for PLL. Clock generated by the PLL is more stable and accurate than clock generated by the FLL. As a drawback, PLL consumes more power than FLL. This can be observed from the measurement results. FLL using

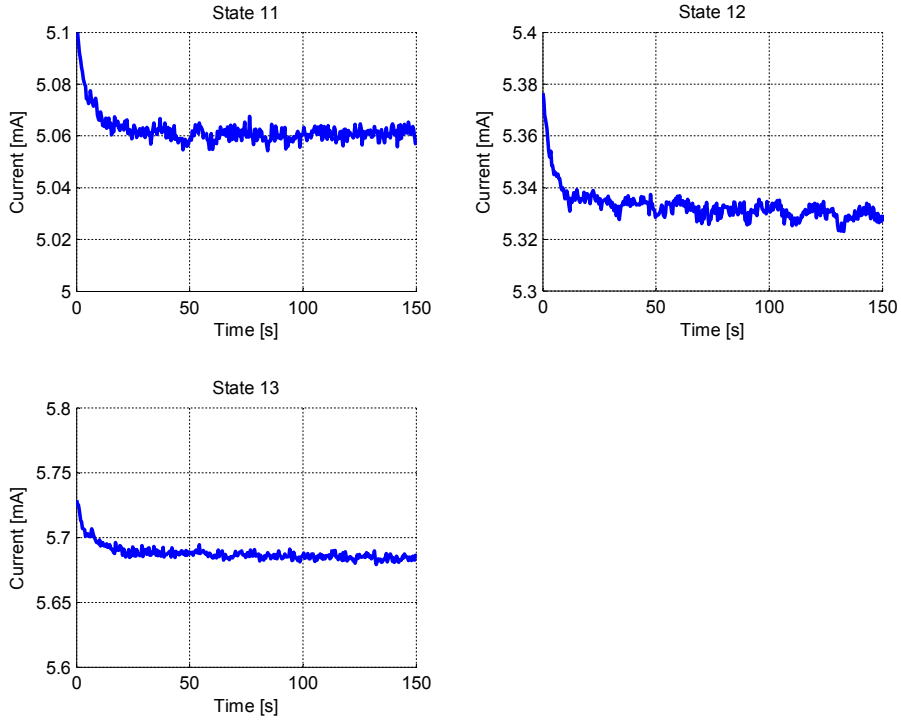

Figure 38: Measurement results for main controller's FLL/PLL clock source configurations.

external reference demands more power than when using the internal reference. This is expected since using an external reference requires powering of additional units such as the internal Pierce oscillator and clock dividers.

4.5.2 XTAL/IRC clock sources

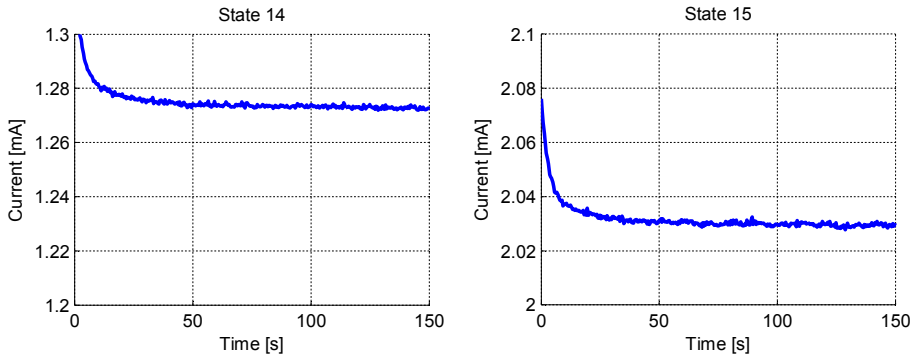

Figure 39: Measurement results for main controller's XTAL/IRC clock source configurations.

In addition to FLL and PLL, the main controller provides options to clock the core and peripherals directly from the internal and external oscillators. An 8 MHz XTAL is used in state 14 to produce the clock while state 15 uses internal 4 MHz RC oscillator. Measurement results for these power states are presented in Figure 39. The linear behaviour of clock frequency versus power consumption can be observed here as well.

States 14 and 15 are referred to as low-power clock sources. FLL and PLL units are disabled to conserve power when either XTAL or IRC is used to generate the clock. Because of this, when transitioning between the various clock sources, it is extremely important to ensure that the selected clock generator has sufficient time to acquire lock on the target frequency and stabilize before enabling the source. Otherwise, unstable clock signal might be provided to the core and peripherals, causing the main controller to enter a fault mode requiring a manual restart.

4.5.3 Low-power run modes

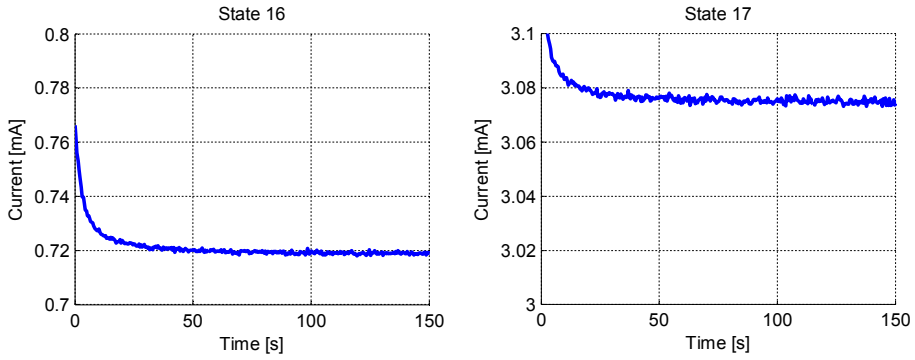

Figure 40: Measurement results for main controller's low-power run modes.

Figure 40 presents the measurement results for low-power run modes of the main controller. In state 16, the main controller is programmed to enter a very-low-power run mode or VLPR as named in the datasheet. This is essentially a power mode that operates the node under reduced processing capabilities in order to conserve power. Clock configuration of either state 14 or state 15 must be used to enter VLPR mode. Maximum core clock during VLPR is 4 MHz and bus clock 1 MHz. The bus clock is used by most peripherals as the input clock source. Since an 8 MHz XTAL is used in the design, it is required to divide the clock down before trying to enter VLPR. Clock dividers are adjusted in such a way that the maximum core and bus clock frequencies are used. Any interrupt can be used to cause transition from VLPR to the normal run mode.

State 17 is very similar than states 3 and 4 for the radio controller. In this run mode, labelled as WAIT mode, the core clock is gated off while rest of the clocks remain enabled. Interrupts can be utilized to wake up the main controller from this mode. WAIT mode is useful when peripherals are operated at high speeds but otherwise power conservation is feasible.

4.5.4 Normal low-power modes

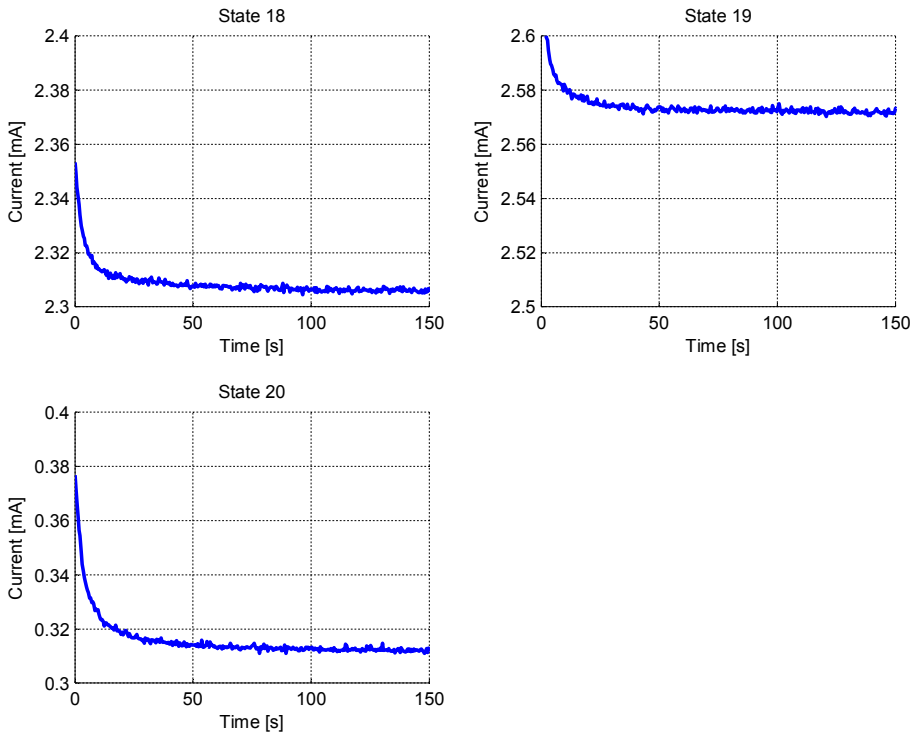

Figure 41: Measurement results for main controller's normal low-power modes.

During state 20, the main controller is programmed to enter normal low-power mode named as STOP mode in the datasheet. The power modes entered in states 18 and 19 are called PSTOP1 and PTOP2, respectively. Differences between the power modes are mainly clock gating -related. In the normal STOP mode of state 20, all normal clock generation methods are disabled. In PSTOP1 power mode of state 18, both the core clock and the bus clock are disabled but the clock generators remain active. In PSTOP2, the core clock is again gated off but the bus clock remains enabled for peripheral usage.

Measurement results for the normal low-power modes are presented in Figure 41. As expected, state 19 consumes most power since it provides clocks that are disabled for other modes. During the normal STOP mode, approximately 300 μA of current is consumed. This is only a portion of the power consumption of other normal low-power modes.

4.5.5 Low-leakage low-power modes

In addition to normal low-power modes, the main controller features a set of low-leakage low-power modes. Wake-up from these power modes is handled by a specific low-leakage wake-up unit. Low-leakage stop (LLS) mode of state 21 is the lowest power consuming mode where a wake-up occurs through a normal interrupt procedure.

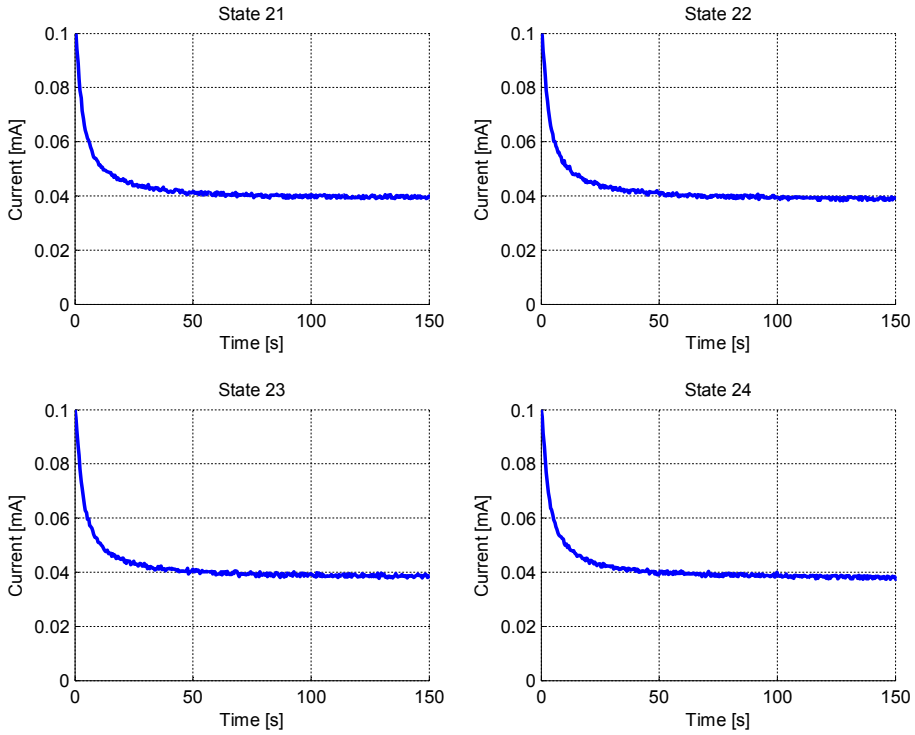

Figure 42: Measurement results for main controller's low-leakage low-power modes.

For VLLS3, VLLS1 and VLLS0 modes of states 22 to 24, the wake-up is performed through a reset routine. GPIO and oscillator are placed on hold state and must be released after reinitialization. Otherwise, using any of the GPIO or oscillator features causes the main controller to enter a fault mode where power cycling is required.

Figure 42 presents the measurement results for the low-leakage low-power modes of the main controller. Current consumption of LLS mode of state 21 is approximately 2 μA higher than for the ultimate power conservation mode VLLS0 of state 24. VLLS3 is the lowest power mode where SRAM contents are retained. In VLLS0 and VLLS1, SRAM contents are no longer retained.

4.6 Maximum power consumption

Maximum current consumption of the node is presented in Figure 43. In state 25, both MCUs are enabled and running with maximum core clock. 32 MHz XTAL source is used as a clock source for the radio controller and 48 MHz PLL for the main controller. Radio and all regulators are enabled. The average current consumption of this state is approximately 23.1 mA. It should be noted that the current consumed by LEDs is not taken into account.

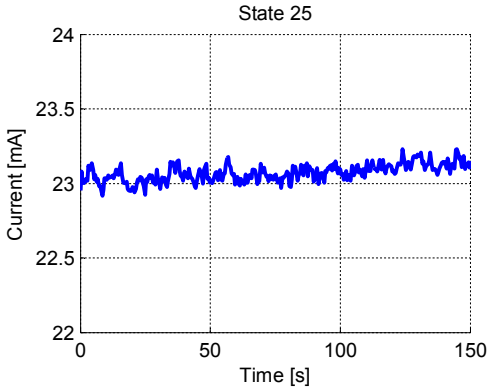

Figure 43: Maximum current consumption of the node.

4.7 Summary of results

Measurement results of the different states are summarized in Table 10. Average current consumptions of the different states are a valuable input when implementing power management algorithm to provide the energy adaptivity. Since hardware of the node already allows software control over the power management resources, it is only a matter of implementing an automated daemon that makes the decisions based on the available energy levels and power consumption of the current state.

State 7 has the lowest achievable power consumption but requires an external interrupt to wake up. This interrupt must be generated outside of the core modules. With 3.7 V input supply voltage, 140.6 μW of power is consumed in this state. In state 24 where both MCUs are enabled, the main controller can utilize it's low-power peripherals to generate the wake-up and signal the radio controller. If the extension module and connected slave modules are required to remain powered while the node itself is in a low-power state, approximately 80 μA of current is required as the result of state 8 shows. Based on the typical harvested energy levels presented in Section 2.3.2, a PV cell of approximately 15 cm^2 is required to maintain the battery level in normal indoor lightning conditions while the node is in state 24. In this case, though, the node will not have sufficient energy to perform any additional operations without depleting the storage element.

Supposing that an application operates at 1 % duty cycle where it shares the time between low-power state 24 and active state 25, the average current consumed is 0.27 mA. This corresponds to 1 mW of average power consumption at 3.7 V input supply as suggested by Equation (1). Thus, a PV cell of size 100 cm^2 is required to maintain the battery level in typical indoor conditions. If the conditions suddenly change drastically and the element is not capable of producing any power, a 1 F supercapacitor charged to 3.7 V would deplete to 2.8 V in approximately an hour based on Equation (2). In an energy adaptive wireless sensor node, the power management software component can detect the diminishing energy level on the storage element and, for example, adjust the duty cycle to conserve energy or change to a finite battery source momentarily to guarantee that the node will not power off.

Table 10: Average current consumption of the different power states.

Power state	$\mathbf{I}_{avg}$	**Configuration**	**Special notes**
State 1	5.047 mA	32 MHz XTAL	-
State 2	2.727 mA	16 MHz IRC	-
State 3	3.434 mA	32 MHz XTAL	Core not clocked
State 4	1.860 mA	16 MHz IRC	Core not clocked
State 5	0.241 mA	PM1	-
State 6	0.039 mA	PM2	-
State 7	0.038 mA	PM3	Lowest power consumption
State 8	0.078 mA	3.3V regulator ON	-
State 9	15.043 mA	Radio enabled	-
State 10	17.665 mA	Radio enabled	2.1V regulator OFF
State 11	5.062 mA	48 MHz FLL	IRC reference
State 12	5.333 mA	45.75 MHz FLL	XTAL reference
State 13	5.679 mA	48 MHz PLL	-
State 14	1.275 mA	4 MHz IRC	-
State 15	2.032 mA	8 MHz XTAL	-
State 16	0.721 mA	VLPR	Lowest power run mode
State 17	3.077 mA	WAIT	Core not clocked
State 18	2.308 mA	PSTOP1	Core and bus clocks disabled
State 19	2.574 mA	PSTOP2	Core clock disabled, bus clock enabled
State 20	0.315 mA	STOP	Clock generators disabled
State 21	0.042 mA	LLS	Lowest power mode with ISR wake-up
State 22	0.042 mA	VLLS3	Exit through reset
State 23	0.042 mA	VLLS1	SRAM not retained; exit through reset
State 24	0.041 mA	VLLS0	SRAM not retained; exit through reset
State 25	23.080 mA	Everything enabled	Maximum power consumption

As a conclusion, the node requires that the harvesting element produces at least 140.6 μW of power in order to keep the system powered in the lowest possible power mode. While the node cannot be used for anything practical with the specified power level, it can serve as a reference value when selecting the element.

5 Conclusion

This thesis presents hardware implementation of an energy adaptive resource-scalable wireless sensor node. The main goal was to design hardware of the node using state-of-the-art commercial off-the-shelf components and identify the limiting factors regarding minimized power consumption. Essentially, the project aimed to investigate how low it is possible to push the power consumption of a complex wireless sensor node design without aid of dedicated integrated circuits. The thesis begins with a brief overview of the fundamental wireless sensor node components and is followed by requirements and benefits of the proposed node architecture. Designed node hardware is then presented and the design choices explained. Finally, power consumption of the designed node is measured in order to create a complete power profile of the device.

An important goal of the thesis was to determine and characterize in what conditions the node is capable of autonomous operation. For this, the power profile of the node was utilized. It became soon apparent that the functional block demanding the most power is the radio itself. Based on the measurement results, radio power consumption dominates even if both of the MCUs are in the highest power consuming active modes. When the MCUs are placed in the lowest power consuming states, power consumed by other components becomes dominant. In these states, over 50 % of the total power is consumed by load switches used for power path control purposes. Energy autonomous operation of the node requires an energy harvesting element that is capable of producing at least 140.6 μW of power to the system. This is the minimum amount of power that is required to keep the node operational in the lowest power consuming state without depleting the storage element. In typical indoor conditions, a PV cell of approximately 14 cm^2 produces the required power.

Many of the commercial components used in the design include features that are unnecessary but yet cannot be completely bypassed. One of the key outcomes of this thesis was to describe operating principles of the critical functional blocks of the node in order to provide sufficient background information for low-power IC and SoC designers in the future. Designed node significantly improves design re-usability since the same hardware can be used for a wide range of applications with different energy, timing and processing power constraints. This is advantage over conventional node implementations. However, the advantage comes at the expense of power consumption and form factor. While traditional wireless sensor nodes can be designed for a very small form factor using only a few necessary components, complexity of the designed node increases the number of required components, power consumption and board area.

The designed node can function as a traditional wireless sensor node that simply transmits gathered information from the sensors wirelessly. In addition, the node can serve as a relay which receives information from other nodes and transmits it further into the network. Finally, the node can operate as a decision-making unit that takes actions based on the received information. Communication part of the software is still under progress. Existing parts of the software providing the operating system and abstraction software must be combined with the available Bluetooth stack.

Future trends show a growing interest in designing low-power RF transceivers and software protocols. While it is already possible to develop low-power radios, an IoT device is most effectively designed by using a well-known protocol. For example, a wireless sensor node using Bluetooth LE radio can be accessed from a smart phone supporting Bluetooth LE, providing gateway to the internet. Also, microprocessor developers are increasingly putting effort into designing processors with lower dynamic and static power consumption. At the end of this project, a new BLE radio built around low-power ARM Cortex-M0 core has been released, featuring less than 10 mA radio peak currents for RX and TX at 0 dBm. Comparing to the state-of-the-art BLE radio at the beginning of the project, the new radio has managed to cut the peak currents by over 30 %. Hence, it is safe to predict that within a couple of years, the limiting factors of energy autonomous wireless sensor networks are reduced to the point where many of the applications impossible with current technology, such as applications requiring high duty-cycle, become a possibility.

Furthermore, it became clear already at an early stage of this project that the design will be very complex. In order to reduce the amount of design errors, a specific design procedure was followed. However, despite initially following the procedure carefully, some design flaws still occurred. The procedure was updated based on these errors and should now provide a clear path for approaching a complex design. This procedure is explained in detail in this thesis and can serve as a guideline when designing complex or otherwise large designs.

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