Department of Electrical Engineering and Automation

Digital Control in Grid Converters: Methods and Comparative Analyses

Ville Pirsto

Aalto University

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Ville Pirsto

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Abstract

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Abstract

Due to the ongoing transition towards fossil-free energy production by means of renewable energy resources, grid converters that act as power-electronic interfaces between the renewable energy sources and the electric grid are deployed in unprecedented numbers. This paradigm change has introduced a host of challenges related to the control of grid converters. The control system is a quintessential part of the grid converter, and in modern converters it is invariably implemented by using a digital processor. This thesis presents a collection of methods and comparative analyses applicable to digital control of grid converters. Throughout the thesis, state-feedback control framework is focused on due to its several desirable properties. The topics of this thesis can be divided into three categories: converter modeling, identification, and control design. Related to converter modeling, an intersample admittance modeling method is presented which takes into account the discrete-time nature of the converter control system. The presented method improves the modeling accuracy over conventional methods and eliminates the need for approximations used in the existing state-of-the-art methods. Regarding identification, focus is on developing computationally efficient methods that can be executed in real time. Two such methods are developed: one for identifying the parameters of an LCL filter and the other for identifying unbalanced grid impedance. These two methods can be embedded to a control system of a pulse-width-modulation-based converter in a plug-in manner. On the topic of control design, comparative analyses of different state-feedback current controllers are carried out to examine their properties as well as reveal connections between the different controllers. In particular, mathematical equivalence of the integrator-based and disturbance-observer-based state-feedback current controllers is shown. Moreover, an enhanced direct pole-placement design for weak-grid tolerant state-feedback positive- and negative-sequence current control is proposed which remains stable in grids ranging from strong to very weak. Related to current limiting in converters operating as voltage sources, a multifunctional cascade control structure is proposed which renders the current reference limiting methods previously restricted to cascade controllers equally available to direct AC-voltage controllers. All the results presented in this thesis are experimentally evaluated using a 12.5-kVA 50-Hz three-phase grid converter system. The results find applications in industry, for example, in wind turbine and solar photovoltaic systems as well as in active front-ends of motor drives.

Keywords Converter output admittance, disturbance feedforward, disturbance observer, double-frequency control, grid converter, grid impedance, integrator, L filter, LC filter, LCL filter, multifunctionality, observer, overcurrent protection, real-time identification, sampled-data systems, state-feedback control, voltage-source converter, weak grid

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Tiivistelmä

Ihmiskunta pyrkii siirtymään fossiilisista polttoaineista riippumattomaan energiantuotantoon uusiutuvien energialähteiden avulla. Tästä johtuen verkkosuuntaajia, jotka toimivat tehoelektronisina rajapintoina uusiutuvien energialähteiden ja sähköverkon välissä, on viime aikoina otettu käyttöön valtavia määriä. Tämä muutos energiantuotannon paradigmassa on tuonut esiin useita haasteita liittyen verkkosuuntaajien säätöön. Säätöjärjestelmä on olennainen osa verkkosuuntajaa, ja nykyaikana se on lähes poikkeuksetta toteutettu digitaalisessa prosessorissa. Tässä työssä esitetään kokoelma menetelmiä ja vertailevia analyysejä, joita voidaan soveltaa verkkosuuntaajan digitaalisessa säädössä. Työhön sisältyvät menetelmät ja vertailut esitetään tilasäädön puitteissa sen useista suotavista ominaisuuksista johtuen. Työn aiheet voidaan jaotella kolmeen osaan: suuntaajan mallinnus, identifiointi ja säätösuunnittelu. Suuntaajan mallinnukseen liittyen työssä esitellään digitaalisesti säädetyn suuntaajan lähtöadmittanssin mallinnusmenetelmä, joka huomioi järjestelmän hybridiluonteen siinä esiintyvien signaalien aikatasojen suhteen. Esitetty menetelmä parantaa mallinnustarkkuutta perinteisiin menetelmiin verrattuna. Tämän lisäksi se poistaa tarpeen approksimaatioille, joita käytetään tämänhetkistä huipputasoa edustavissa menetelmissä. Identifioinnin saralla työssä keskitytään laskennallisesti tehokkaiden menetelmien kehittämiseen, jotta identifointi voitaisiin suorittaa reaaliajassa. Kaksi tälläista menetelmää esitetään: yksi LCL suodattimen parametrien ja toinen epäsymmetrisen verkkoimpedanssin identifiointiin. Nämä menetelmät voidaan sisällyttää pulssinleveysmoduloidun suuntaajan säätöjärjestelmään suoraviivaisesti. Säätösuunnittelun aihepiiriin liittyen työssä tehdään useita vertailevia analyysejä erilaisten tilasäädinten välillä, joissa tarkoituksena on vertailla säädinten ominaisuuksia sekä paljastaa niiden välisiä yhteyksiä. Erityisesti integraattorilla ja häiriöhavaitsijalla toteutettujen tilasäätöön pohjautuvien virtasäädinten matemaattinen ekvivalenssi näytetään. Tämän lisäksi työssä esitetään parannettu suora napojensijoittelu myötä- ja vastakomponentin tilasäätöön pohjautuvalle virtasäätimelle. Ehdotettu napojensijoittelu takaa säätimen stabiilin toiminnan sekä vahvoissa että heikoissa verkoissa. Työssä esitellään myös jännitelähteinä toimivien suuntaajien virranrajoitukseen liittyvä monitoiminnallinen kaskadisäätörakenne. Ehdotettu rakenne mahdollistaa virtareferenssiin perustuvien virranrajoitusmenetelmien, joiden käyttö on aikaisemmin rajoitettu kaskadirakenteisiin säätimiin, käyttämisen AC-jännitettä suoraan säätävissä rakenteissa. Kaikki työn tulokset on arvioitu kokeellisesti käyttäen 12.5-kVA 50-Hz kolmivaiheista verkkosuuntajalaitteistoa. Tuloksia voidaan soveltaa teollisuudessa esimerkiksi tuuliturbiini- ja aurinkosähköjärjestelmissä ja sähkömoottorikäyttöjen aktiivisissa tasasuuntaajissa.

Avainsanat Havaitsija, heikko verkko, häiriöhavaitsija, häiriön myötäkytkentä, integraattori, jännitevälipiirillinen suuntaja, kaksitaajuussäätö, L-suodatin, LC-suodatin, LCL-suodatin, monitoiminnallisuus, näytteistettyjä signaaleja sisältävä järjestelmä, reaaliaikainen identifiointi, suuntaajan lähtöadmittanssi, tilasäätö, verkkoimpedanssi, verkkosuuntaaja, ylivirtasuojaus

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Preface

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Last, but not least, I would like to thank my parents, Juhani and Anita, and my love, Susan, for their endless support and encouragement.

Espoo, August 28, 2022,

Ville Waldemar Pirsto

Contents

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I V. Pirsto, J. Kukkola, M. Hinkkanen, and L. Harnefors. Intersample modeling of the converter output admittance. *IEEE Transactions on Industrial Electronics*, vol. 68, no. 11, pp. 11348–11358, November 2021.

II V. Pirsto, J. Kukkola, F. M. M. Rahman, and M. Hinkkanen. Real-time identification of LCL filters employed with grid converters. *IEEE Transactions on Industrial Applications*, vol. 56, no. 5, pp. 5158–5169, September-October 2020.

III F. M. M. Rahman, V. Pirsto, J. Kukkola, M. Routimo, and M. Hinkkanen. State-space control for LCL filters: Converter versus grid current measurement. *IEEE Transactions on Industry Applications*, vol. 56, no. 6, pp. 6608–6618, November-December 2020.

IV F. M. M. Rahman, V. Pirsto, J. Kukkola, M. Hinkkanen, D. Pérez-Estévez, and J. Doval-Gandoy. Equivalence of the integrator-based and disturbance-observer-based state-space current controllers for grid converters. *IEEE Transactions on Industrial Electronics*, vol. 68, no. 6, pp. 4966–4976, June 2021.

V V. Pirsto, J. Kukkola, and M. Hinkkanen. Multifunctional cascade control of voltage-source converters equipped with an LC filter. *IEEE Transactions on Industrial Electronics*, vol. 69, no. 3, pp. 2610–2620, March 2022.

VI J. Kukkola, V. Pirsto, M. Routimo, and M. Hinkkanen. Estimation of an unbalanced grid impedance using a three-phase power converter. In *Proc. European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Lyon, France, pp. 1–10, September 2020.

VII V. Pirsto, J. Kukkola, and M. Hinkkanen. Comparative analysis of the effects of integral action and disturbance feedforward on current

control of voltage-source converters. In *Proc. European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium, pp. 1–10, September 2021.

VIII V. Pirsto, J. Kukkola, F. M. M. Rahman, and M. Hinkkanen. Weak-grid tolerant positive- and negative-sequence current control of voltage-source converters. In *Proc. IEEE PES Innovative Smart Grid Technologies (ISGT Europe)*, Espoo, Finland, pp. 1–6, October 2021.

Author's Contribution

Publication I: "Intersample modeling of the converter output admittance"

The author wrote the paper under the guidance of Dr. Kukkola and Prof. Hinkkanen. Prof. Harnefors contributed by commenting on the manuscript.

Publication II: "Real-time identification of LCL filters employed with grid converters"

The author wrote the paper under the guidance of Dr. Kukkola and Prof. Hinkkanen. Dr. Rahman contributed by helping with the measurements and commenting on the manuscript.

Publication III: "State-space control for LCL filters: Converter versus grid current measurement"

The author contributed by helping with the experiments and participating in the writing of the manuscript.

Publication IV: "Equivalence of the integrator-based and disturbance-observer-based state-space current controllers for grid converters"

The author contributed to deriving the conditions for the mathematical equivalence of the controllers. The author also helped with the experiments and participated in the writing of the manuscript.

Publication V: "Multifunctional cascade control of voltage-source converters equipped with an LC filter"

The author wrote the paper under the guidance of Dr. Kukkola and Prof. Hinkkanen.

Publication VI: "Estimation of an unbalanced grid impedance using a three-phase power converter"

The author performed the simulations for the estimation of the dq-asymmetric grid impedance in synchronous coordinates, helped with the experiments, and commented on the manuscript.

Publication VII: "Comparative analysis of the effects of integral action and disturbance feedforward on current control of voltage-source converters"

The author wrote the paper under the guidance of Dr. Kukkola and Prof. Hinkkanen.

Publication VIII: "Weak-grid tolerant positive- and negative-sequence current control of voltage-source converters"

The author wrote the paper under the guidance of Dr. Kukkola and Prof. Hinkkanen. Dr. Rahman contributed by helping with the measurements and by commenting on the manuscript.

Abbreviations

2DOF	Two-degrees-of-freedom
A/D	Analog-to-digital
AC	Alternating current
CC	Current controller
DSE	Disturbance-signal estimator
DSRF	Double synchronous reference frame
EMF	Electromotive force
FRT	Fault ride-through
LC	Inductor-capacitor (filter)
LCL	Inductor-capacitor-inductor (filter)
LQR	Linear quadratic regulator
MPC	Model-predictive control
PCC	Point of common coupling
PI	Proportional integral
PLL	Phase-locked loop
PR	Proportional resonant
PWM	Pulse-width modulation
RMS	Root-mean square
SCR	Short-circuit ratio
SFB	State-feedback

SRF	Synchronous reference-frame
VSC	Voltage-source converter
VC	Voltage controller
ZOH	Zero-order hold

Symbols

Vectors and matrices are marked with boldface symbols in lower- and uppercase, respectively. Complex-valued quantities are marked with boldface italic symbols. Space vectors in stationary coordinates are denoted with a superscript s. State and parameter estimates are denoted with a circumflex. Reference values are denoted with a subscript ref, and limited reference values with an overline. Subscripts + and – are used to denote positive- and negative-sequence components, respectively.

$\mathbf{A}, \mathbf{B}_\mathrm{c}, \mathbf{B}_\mathrm{g}$	Continuous-time system matrices
$\boldsymbol{C}$	Feedback controller
C_dc	DC-bus capacitance
C_f	LCL-filter capacitance
$\mathbf{C}_\mathrm{g}, \mathbf{C}_\mathrm{gp}$	Output vectors for the grid current
$d_\mathrm{a}, d_\mathrm{b}, d_\mathrm{c}$	Phase-leg duty ratios
$\boldsymbol{e}_\mathrm{g}$	Grid voltage
$e_\mathrm{ga}, e_\mathrm{gb}, e_\mathrm{gc}$	Grid phase voltages
$\boldsymbol{e}_\mathrm{i}$	Tracking error
$\boldsymbol{e}_\mathrm{o}$	Estimation error
$\boldsymbol{F}$	Reference prefilter
f_s	Sampling frequency
$\boldsymbol{G}_\mathrm{cl}$	Closed-loop reference-tracking transfer function
$\boldsymbol{G}_\mathrm{h}$	Zero-order hold
$\boldsymbol{H}$	Disturbance feedforward filter
$\mathbf{I}$	Identity matrix

$\boldsymbol{i}_\mathrm{c}$	Converter current
$\boldsymbol{i}_\mathrm{c,ref}$	Converter current reference
$i_\mathrm{ca}, i_\mathrm{cb}, i_\mathrm{cc}$	Converter phase currents
$\boldsymbol{i}_\mathrm{g}$	Grid current
$\boldsymbol{i}_\mathrm{g,ref}$	Grid current reference
j	Imaginary unit
$\boldsymbol{k}_\mathrm{c+}, \boldsymbol{k}_\mathrm{c-}$	Reference cross-coupling gains
$\boldsymbol{k}_\mathrm{f}, \boldsymbol{k}_\mathrm{t}$	Reference feedforward gains
$\mathbf{K}_\mathrm{fd}, \mathbf{K}_\mathrm{fi}$	State-feedback gain vectors
$\boldsymbol{k}_\mathrm{i}, k_\mathrm{i}$	Integral gain
$\mathbf{K}_\mathrm{o}$	Observer gain vector
k_p	Proportional gain
$\boldsymbol{k}_\mathrm{w}$	Observer gain for the disturbance state
L_fc	Converter-side inductance of an LCL filter
L_fg	Grid-side inductance of an LCL filter
$q_\mathrm{a}, q_\mathrm{b}, q_\mathrm{c}$	Phase-leg gate signals
$\boldsymbol{r}, \mathbf{r}$	Disturbance model state vectors
s	Laplace variable
$\boldsymbol{u}_\mathrm{c}$	Converter voltage
$\boldsymbol{u}_\mathrm{c,ref}$	Converter voltage reference
u_dc	DC-bus voltage
$\boldsymbol{u}_\mathrm{f}$	Filter capacitor voltage
$\boldsymbol{u}_\mathrm{ff}$	Filtered disturbance feedforward
$\boldsymbol{u}_\mathrm{f,ref}$	Capacitor voltage reference
$\boldsymbol{u}_\mathrm{g}$	PCC-voltage
$\boldsymbol{u}_\mathrm{i}$	Integral state
$\boldsymbol{w}$	Output vector for the disturbance model
$\mathbf{x}, \mathbf{x}_\mathrm{r}, \mathbf{x}_\mathrm{p}$	State vectors

$\boldsymbol{Y}_\mathrm{c}, \boldsymbol{Y}_\mathrm{g}$	Open-loop admittances including the delay
$\boldsymbol{Y}_\mathrm{cd}, \boldsymbol{Y}_\mathrm{cp}, \boldsymbol{Y}_\mathrm{gd}, \boldsymbol{Y}_\mathrm{gp}$	Open-loop admittances excluding the delay
$\boldsymbol{Y}_\mathrm{oa}$	Intersample converter admittance
$\boldsymbol{Y}_\mathrm{oa,c}$	Continuous-time converter admittance
$\boldsymbol{Y}_\mathrm{oa,d}$	Discrete-time converter admittance
$\boldsymbol{Y}_\mathrm{oa,h}$	Single-frequency converter admittance
z	Z-transform variable
$\boldsymbol{Z}_\mathrm{g}$	Grid impedance
$\boldsymbol{Z}_\mathrm{o}$	Converter output impedance
$\boldsymbol{Z}_\mathrm{vi}$	Virtual impedance
α_f	Low-pass filter bandwidth
$\boldsymbol{\Gamma}_\mathrm{c}, \boldsymbol{\Gamma}_\mathrm{g}, \boldsymbol{\Phi}$	Discrete-time system matrices including the delay
$\boldsymbol{\Gamma}_\mathrm{cp}, \boldsymbol{\Gamma}_\mathrm{gp}, \boldsymbol{\Phi}_\mathrm{p}$	Discrete-time system matrices excluding the delay
$\vartheta_\mathrm{g}, \vartheta_\mathrm{g0}$	PCC-voltage angle
ω_ar	Filter angular antiresonance frequency
ω_g	Grid angular frequency
ω_r	Filter angular resonance frequency
ω_s	Sampling angular frequency

1. Introduction

1.1 Background

During the last decade, the share of renewable energy generation used in energy production has increased in strides to combat the environmental detriment caused by the use of fossilized fuels. Consequently, voltage-source converters (VSCs) that act as interfaces between the renewable energy source and the electric grid have likewise been deployed in unprecedented numbers. VSCs that are used to interface various systems including the aforementioned renewable energy sources to the electric grid are referred to as grid converters.

The use of renewable energy resources, such as solar and wind, has opened up new alternatives to implementing energy production. For example, renewable energy production can be distributed throughout the grid instead of solely having centralized energy production facilities, as in the conventional power system. Alternatively, a large monolithic installation of renewable energy sources can be connected to the electric grid for bulk power provision, in which case, the grid converter typically has current source characteristics. Furthermore, a single production facility can behave as a standalone voltage source for provisioning of its local loads to replace or complement previously used diesel generator systems (Teodorescu et al., 2011). As a result of this revolutionary paradigm change in energy production, new challenges related to the integration and stability of grid converters have been observed as demonstrated in (Enslin and Heskes, 2004; Liserre et al., 2006b; Agorreta et al., 2011).

Being able to accurately analyze and predict converter–grid interconnection stability is of great importance. Two methods in particular have been extensively used for such an analysis (Wang and Blaabjerg, 2019). These methods are the state-space model-based eigenvalue analysis presented, for example, in (Kundur, 1994), and the impedance-based stability analysis presented for grid converter systems by Sun (2011). Of these two

methods, of particular interest is the impedance-based stability analysis in which the converter–grid interconnection stability is determined based on the models of the externally observable behavior of both the grid and the converter, that is, the converter output admittance and the grid impedance. While the eigenvalue analysis approach provides more detailed information about the analyzed system, the modularity achieved by the use of subsystem-level behavior in the impedance-based stability analysis is a desirable quality. The converter output admittance and grid impedance characteristics can either be modeled or estimated by means of measurements. Considering the converter output admittance, an abundance of literature can be found related to its modeling, such as (Harnefors et al., 2016; Wen et al., 2016; Harnefors et al., 2017; Wang et al., 2018; Freijedo et al., 2019). Moreover, several methods have also been developed for its identification, including (Francis et al., 2011; Shen et al., 2013a; Liao and Wang, 2020). In the majority of the model-based analyses, the admittance modeling is completely carried out in the continuous-time domain. However, the control algorithms of modern VSCs are invariably implemented on digital processors that execute difference equations in the discrete-time domain. Consequently, the converter system is actually a hybrid in which both continuous- and discrete-time signals exist. Due to this discrepancy between the assumptions and reality, inaccurate results may ensue as a result of using purely continuous-time models (Pirsto, 2019). Therefore, taking into account the hybrid nature of the converter system would be beneficial for the accuracy of the interconnection stability analysis.

The increasingly distributed nature of energy production exposes the grid converters to a wider variety of operating conditions, including weak grids in which the grid impedance seen by the converter can be exceptionally high (Liserre et al., 2006b). This high grid impedance may cause detrimental interactions between the converter and the grid impedance which results in an instability that can be predicted, for example, by using the above-mentioned impedance-based stability analysis. Alas, the grid impedance is typically unknown due to its time- and frequency-varying nature (Knop and Fuchs, 2009; Shuai et al., 2014; Zhang et al., 2014; Jessen et al., 2015). To prevent instability due to the converter–grid interaction caused by a weak grid, weak-grid tolerant control methods are required. Alternatively, the control tuning of the converter could be adjusted based on the real-time estimate of the grid impedance.

VSCs are sources of high-frequency harmonics due to the switching behavior of the semiconductor bridge in the converter system. International standards, such as IEEE 519-2014 (2014), set limits on the permissible harmonic levels a VSC can inject into the grid. To comply with these requirements, a low-pass filter is placed between the semiconductor bridge and the point of common coupling (PCC) to attenuate the harmonics generated by the semiconductor bridge. Various different filters of different

orders are used, but the most commonly used ones are the L filter, LC filter, and LCL filter. The L and LCL filters are typically used in converters with current source characteristics. Out of these two filters, the L filter provides moderate damping with simple control requirements. On the other hand, the switching harmonic attenuation of the LCL filter is superior as compared to the L filter of equal magnetic volume (Liserre et al., 2005; Jalili and Bernet, 2009). However, the LCL filter is a resonant filter that imposes additional requirements on the converter system design. For applications in which the converter behaves as a voltage source, the resonant LC and LCL filters are favored. There are several methods to dampen the filter resonance and they can be divided into two categories: passive and active damping. In passive damping, the filter is equipped with additional resistive components that naturally dampen the filter resonance without any additional control effort (Peña-Alzola et al., 2013). However, while simple to implement, this approach reduces the overall efficiency of the converter system. In active damping methods, the control system is designed to dampen the resonance without any additional losses. A multitude of different methods for implementing active damping exist, such as (Twining and Holmes, 2003; Dannehl et al., 2010a; Parker et al., 2014; Xu et al., 2014).

Implementing active damping methods whilst effectively controlling the current or voltage is a challenging task. Considering three-phase systems, a popular approach has been to employ controllers operating on space vectors. The celebrated proportional integral (PI) and proportional resonant (PR) controllers, while simple in their implementation and proven effective for the control of L filters, face severe limitations when considering the control of LC and LCL filters. As mentioned above, practical control algorithms of modern converter systems are implemented on a digital processor. The finite computational resources of the processor (Franklin et al., 1998) and modulation (Ma et al., 2018) introduce additional delay to the system. The interaction of this delay together with the resonant characteristics of the filter imposes several restrictions on the tuning of the control system (Dannehl et al., 2009; Parker et al., 2014; Zou et al., 2014; Wang et al., 2016a; Liao et al., 2020). Consequently, additional functionality is often embedded in the aforementioned controllers to implement active damping of the filter resonance, such as in (Twining and Holmes, 2003; Dannehl et al., 2009, 2011; He and Li, 2012; Xu et al., 2014; Wang et al., 2017).

On the contrary, discrete-time state-feedback control is not hindered in a similar manner by the interaction of the delay and the filter resonance, as shown for a state-feedback-based current controller in (Pérez-Estévez et al., 2017). Similar conclusions can be drawn for state-feedback-based AC-voltage control. State-feedback control framework offers a flexible and effective approach to dealing with filter resonance and simultaneously setting the dominant dynamics of the resulting closed-loop system. In

essence, state-feedback control builds upon the feedback of weighted sum of the system states. The states can either be measured as in (Wu and Lehn, 2006; Kim et al., 2019) or estimated by means of an observer (Kukkola et al., 2015; García-Fernández et al., 2021). Especially for the control of a three-phase LCL filter, the use of an observer can be of significant benefit. Fewer sensors are required in the system, resulting in reduced system cost while simultaneously improving its reliability. A manifold of methods exist for determining the feedback gains for the state-feedback controller. For example, one can determine the weights based on the desired closed-loop poles either analytically (Kukkola et al., 2015; Kim et al., 2019) or numerically (Pérez-Estévez et al., 2017). Another possible approach is to indirectly solve the gains through optimization, for example, to obtain fast reference tracking (Wu and Lehn, 2006) or robustness to grid parameter variations (Lai and Kim, 2018). Nevertheless, irrespective of the tuning method, discrepancies between the system model used in the control design and the actual system model will translate into discrepancies between the desired closed-loop pole placement and the actual closed-loop pole placement.

As briefly mentioned above, grid converters interfacing a renewable energy source can also be operated as standalone voltage sources to provide electricity to local loads in remote locations. For such systems, the overcurrent protection of the converter hardware is an important, yet often overlooked aspect of the control system. There are two dominating approaches to implementing overcurrent protection of VSCs operated as voltage sources. The first one is current reference limiting that requires a cascade control structure comprising an outer voltage loop and an inner current loop (Bottrell and Green, 2014; Sadeghkhani et al., 2017). The second method is to use adaptive virtual impedance, which essentially reduces the converter voltage reference during fault situations in proportion to the output current (Paquette and Divan, 2015; Lu et al., 2018). Other proprietary methods also exist, such as (Moon and Johnson, 1999), in which the converter voltage reference is reduced in proportion to the load current by using a lookup table, but the majority of them lack general applicability and efficiency. The virtual admittance methods are not capable of regulating the current during fault situations. Consequently, these approaches are found to be lacking in light of recent grid code revisions, such as the German VDE-AR-N 4110 (2018) and IEEE 1547-2018 (2018), in which dynamic voltage support is required during fault conditions. On the other hand, the methods based on current reference limiting are capable of regulating the currents during fault conditions. Unfortunately, controllers without a cascade control structure, such as state-feedback-based controllers, are not capable of utilizing current reference limiting methods due to the lack of inner current loop. It would be beneficial to develop an overcurrent protection method with the properties of current

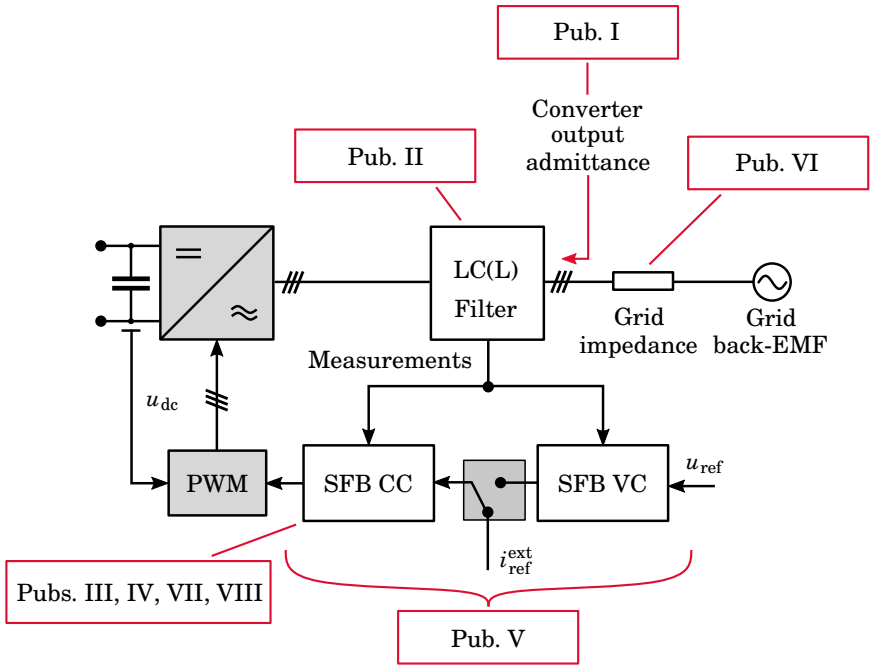

Figure 1.1. Graphical summary of the focus of each publication included in the thesis. EMF stands for electromotive force, SFB for state-feedback, CC for current controller, and VC for voltage controller.

reference limiting methods for such controllers.

1.2 Objective and Outline of the Thesis

The high-level objective of this thesis is to develop methods applicable in digital control of grid converters. State-feedback control will receive special attention due to its desirable properties, as discussed in the previous section. More specifically, the objectives of this thesis are:

- To analyze and unify state-of-the-art state-feedback current control methods
- To develop an efficient and flexible current-limiting method for state-feedback AC-voltage control
- To develop a modeling method for the output admittance of a grid converter, which takes into account the hybrid nature of the converter system

This thesis consists of an overview and eight publications. A graphical summary of the main focus of each publication contained in this thesis is given in Fig. 1.1. The overview is organized as follows. Chapter 2 presents preliminaries for the content of this thesis. Single- and double-frequency

current control literature is reviewed in Chapter 3, which also presents the state-feedback current control framework, including its augmentation with an integrator and a disturbance observer. The relations of these two implementations are then considered. Chapter 4 includes a review of current-limiting methods for voltage-source operation of VSCs, and provides an introduction to multifunctional cascade control structure. The structure allows for augmenting direct AC-voltage controllers, such as the state-feedback AC-voltage controller, with overcurrent protection methods previously restricted to cascade voltage controllers. Chapter 5 gives a review of the applications of converter admittance modeling, followed by a presentation of the intersample admittance model through an example. After that, the intersample model is compared with state-of-the-art modeling methods, as well as more conventional approaches to admittance modeling. Chapter 6 contains an overview of the experimental setup used in the publications of this thesis. The contributions as well as the summaries of the publications are outlined in Chapter 7. Finally, this thesis concludes with Chapter 8.

2. Preliminaries

In this chapter, space vectors are introduced and an overview of a grid converter equipped with an LCL filter is given. Additionally, discrete-time modeling of the computational delay is presented. This chapter concludes with a discussion on the modeling of the electric grid.

2.1 Space Vectors

This thesis deals with three-phase systems without a neutral wire. In such systems, the sum of instantaneous phase currents and voltages is equal to zero, and three-phase quantities can be represented more compactly using Clarke transform (Akagi et al., 2017). Clarke transform can either be defined as a complex- or vector-valued function that maps the three-phase quantities into a space vector in stationary coordinates. In grid converters, complex-valued representation of space vectors is favored for symmetric systems. For asymmetric systems, real-valued vector representation is typically applied, although a slightly more involved complex-valued representation can also be used (Harnefors, 2007; Harnefors et al., 2020). For the sake of simplicity, symmetric systems are assumed in this overview. For application of real-valued space vectors, see Publication I. Space vectors are marked with boldface italic symbols, and a superscript s is used to denote vectors in stationary coordinates. As an example, the Clarke transform of the converter current, defined as $\boldsymbol{i}_{\mathrm{c}}^{\mathrm{s}} = i_{\mathrm{c}\alpha} + \mathrm{j} i_{\mathrm{c}\beta}$, is given by

$$\boldsymbol{i}_{\mathrm{c}}^{\mathrm{s}} = \frac{2}{3}\left(i_{\mathrm{ca}} + \mathrm{e}^{\mathrm{j}\frac{2\pi}{3}} i_{\mathrm{cb}} + \mathrm{e}^{\mathrm{j}\frac{4\pi}{3}} i_{\mathrm{cc}}\right) \tag{2.1}$$

where $i_{\mathrm{ca}}, i_{\mathrm{cb}}$, and i_{cc} are the instantaneous converter phase currents. The amplitude-invariant scaling of the space vector is used throughout the thesis.

The vector given by the Clarke transform rotates at the angular frequency of the three-phase signal in the complex plane. If the coordinate system is rotated in synchronism with the space vector, the space vector appears as a constant quantity in steady state. This is typically considered to be

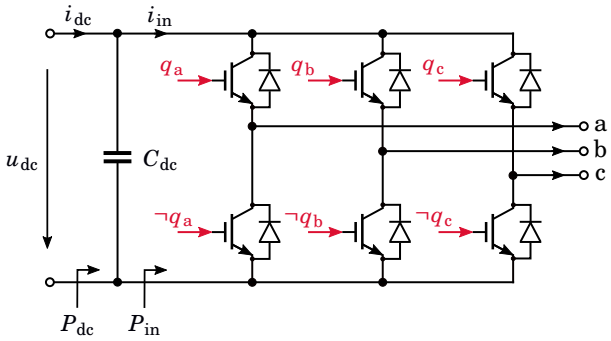

Figure 2.1. Three-phase two-level semiconductor bridge comprising insulated-gate bipolar transistors, together with a DC-bus capacitor.

desirable from the control design perspective. The rotation of the coordinate system, yielding the space vector in synchronous coordinates, is called the Park transform. As an example, the Park transform of the converter current is given by

$$\boldsymbol{i}_c = \mathrm{e}^{-\mathrm{j}\vartheta_g} \boldsymbol{i}_c^s \tag{2.2}$$

where ϑ_g is the instantaneous angle of the coordinate system, given by the integral of the grid angular frequency ω_g over the elapsed time

$$\vartheta_g = \int \omega_g(\tau)\mathrm{d}\tau + \vartheta_{g0} \tag{2.3}$$

where ϑ_{g0} is the initial value for the angle. In this thesis, the estimation of the grid-voltage angle ϑ_g for establishing a grid-voltage-oriented synchronous reference frame (SRF) is carried out using a phase-locked loop (PLL) in current-control applications (Kaura and Blasko, 1997). In Publication V, which deals with voltage-source operation of VSCs, the angle is internally generated in the control system for the sake of simplicity.

2.2 Grid Converter

A circuit diagram of a three-phase two-level semiconductor bridge, based on insulated-gate bipolar transistors, together with the DC-bus of the converter is shown in Fig. 2.1. The AC-bus voltage of the converter is realized using pulse-width modulation (PWM). During each sampling period T_s, the control system computes a set of upper-leg duty ratios $0 \le d_x \le 1$, $x \in \{a,b,c\}$, that express the relative conduction time of the upper semiconductor in phase leg x over the sampling period. These duty ratios are then compared to a carrier signal, resulting in a set of gate signals $q_x \in \{0,1\}$, $x \in \{a,b,c\}$, which determine whether the corresponding upper (1) or lower (0) semiconductor in phase leg x is conducting. To exemplify the process of PWM and the piecewise constant nature of the duty ratio

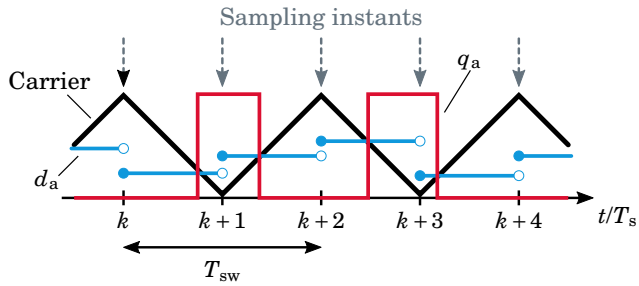

Figure 2.2. Pictorial presentation of the double-update PWM method for a single phase-leg of a three-phase semiconductor bridge.

signals for each phase, a graphical example is shown in Fig. 2.2 depicting the double-update PWM method.

For the purposes of dynamic analysis and control design, detailed modeling of switching events may be omitted without a significant loss of accuracy. Consequently, switching-cycle-averaged models can be used (Yazdani and Iravani, 2010). The average converter voltage vector in stationary coordinates can be directly obtained from the product of duty ratio signals and the DC-bus voltage u_{dc} as

$$\boldsymbol{u}_c^s = \frac{2}{3} u_{dc}(d_a + e^{j\frac{2\pi}{3}} d_b + e^{j\frac{4\pi}{3}} d_c). \tag{2.4}$$

Fig. 2.1 also includes an ideal DC-bus capacitor C_{dc}. The source current is defined as i_{dc} and the current to the semiconductor bridge as i_{in}. The dynamics of the DC bus are dictated by the capacitor voltage equation

$$C_{dc}\frac{du_{dc}}{dt} = i_{dc} - i_{in}. \tag{2.5}$$

or, equivalently, the DC-bus dynamics can also be represented using the power-balance approach as

$$\frac{dW_{dc}}{dt} = P_{dc} - P_{in} \tag{2.6}$$

where $W_{dc} = C_{dc}u_{dc}^2/2$ is the capacitor energy, $P_{dc} = u_{dc}i_{dc}$ is the power fed to the dc bus, and $P_{in} = u_{dc}i_{in}$ is the power flowing to the semiconductor bridge. The power-balance model (2.6) can be found to be useful in the design of the DC-bus voltage controller (Hur et al., 2001; Harnefors et al., 2007). However, the outer control loops related to ancillary services such as the DC-bus voltage control are not within the scope of this thesis, and consequently, are not discussed any further in this overview.

LCL Filter

Various different filters are considered in the publications of this thesis. An L filter is considered in Publications VII and VIII, an LC filter is considered in Publication V, and an LCL filter in Publications I-IV, and VI. Here, the

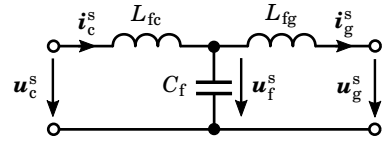

Figure 2.3. Space-vector circuit model of an ideal LCL filter, presented in stationary coordinates.

modeling of LCL filter is briefly covered. For the modeling of L and LC filters, the interested reader is referred to the corresponding publications.

An ideal LCL filter in stationary coordinates is shown in Fig. 2.3. The converter-side filter inductance is L_{fc}, the filter capacitance C_{f}, and the grid-side filter inductance is L_{fg}. Furthermore, $\boldsymbol{u}_{\mathrm{f}}^{\mathrm{s}}$ is the voltage over the filter capacitor, $\boldsymbol{i}_{\mathrm{g}}^{\mathrm{s}}$ is the grid current, and $\boldsymbol{u}_{\mathrm{g}}^{\mathrm{s}}$ is the voltage at the PCC. By employing the state-space modeling framework, the dynamic model of the LCL filter in synchronous coordinates rotating at the angular frequency ω_{g} can be expressed as

$$\frac{\mathrm{d}\mathbf{x}_{\mathrm{p}}}{\mathrm{d}t} = \underbrace{\begin{bmatrix} -\mathrm{j}\omega_{\mathrm{g}} & -\frac{1}{L_{\mathrm{fc}}} & 0 \\ \frac{1}{C_{\mathrm{f}}} & -\mathrm{j}\omega_{\mathrm{g}} & -\frac{1}{C_{\mathrm{f}}} \\ 0 & \frac{1}{L_{\mathrm{fg}}} & -\mathrm{j}\omega_{\mathrm{g}} \end{bmatrix}}_{\mathbf{A}} \mathbf{x}_{\mathrm{p}} + \underbrace{\begin{bmatrix} \frac{1}{L_{\mathrm{fc}}} \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{B}_{\mathrm{c}}} \boldsymbol{u}_{\mathrm{c}} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_{\mathrm{fg}}} \end{bmatrix}}_{\mathbf{B}_{\mathrm{g}}} \boldsymbol{u}_{\mathrm{g}} \tag{2.7}$$

where $\mathbf{x}_{\mathrm{p}} = [\boldsymbol{i}_{\mathrm{c}}, \boldsymbol{u}_{\mathrm{f}}, \boldsymbol{i}_{\mathrm{g}}]^{\mathrm{T}}$ is the state vector. The value of the grid current $\boldsymbol{i}_{\mathrm{g}}$ can be extracted from the model as

$$\boldsymbol{i}_{\mathrm{g}} = \underbrace{\begin{bmatrix} 0 & 0 & 1 \end{bmatrix}}_{\mathbf{C}_{\mathrm{gp}}} \mathbf{x}_{\mathrm{p}}. \tag{2.8}$$

Other state variables can be extracted from the model in an analogous manner. The open-loop dynamic behavior of the LCL filter can be evaluated by computing the transfer functions of interest from the continuous-time model of the filter (2.7) and (2.8). For example, the transfer function from the PCC voltage $\boldsymbol{u}_{\mathrm{g}}$ to the grid current $-\boldsymbol{i}_{\mathrm{g}}$ and from the converter voltage $\boldsymbol{u}_{\mathrm{c}}$ to the grid current $\boldsymbol{i}_{\mathrm{g}}$, respectively, are obtained as

$$\boldsymbol{Y}_{\mathrm{gp}}(s) = -\frac{\boldsymbol{i}_{\mathrm{g}}(s)}{\boldsymbol{u}_{\mathrm{g}}(s)} = -\mathbf{C}_{\mathrm{gp}}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_{\mathrm{g}} = -\frac{1}{L_{\mathrm{fg}}} \frac{(s + \mathrm{j}\omega_{\mathrm{g}})^2 + \omega_{\mathrm{ar}}^2}{(s + \mathrm{j}\omega_{\mathrm{g}})\left[(s + \mathrm{j}\omega_{\mathrm{g}})^2 + \omega_{\mathrm{r}}^2\right]} \tag{2.9}$$

$$\boldsymbol{Y}_{\mathrm{cp}}(s) = \frac{\boldsymbol{i}_{\mathrm{g}}(s)}{\boldsymbol{u}_{\mathrm{c}}(s)} = \mathbf{C}_{\mathrm{gp}}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_{\mathrm{c}} = \frac{1}{C_{\mathrm{f}}L_{\mathrm{fc}}L_{\mathrm{fg}}} \frac{1}{(s + \mathrm{j}\omega_{\mathrm{g}})\left[(s + \mathrm{j}\omega_{\mathrm{g}})^2 + \omega_{\mathrm{r}}^2\right]} \tag{2.10}$$

where s is the Laplace variable, $\mathbf{I}$ is an identity matrix, and where the resonance and anti-resonance frequencies of the filter, ω_{r} and ω_{ar}, respectively,

are

$$\omega_{\mathrm{r}} = \sqrt{\frac{L_{\mathrm{fc}} + L_{\mathrm{fg}}}{L_{\mathrm{fc}} C_{\mathrm{f}} L_{\mathrm{fg}}}} \tag{2.11}$$

$$\omega_{\mathrm{ar}} = \sqrt{\frac{1}{C_{\mathrm{f}} L_{\mathrm{fc}}}}. \tag{2.12}$$

The transfer functions $\boldsymbol{Y}_{\mathrm{gp}}$ and $\boldsymbol{Y}_{\mathrm{cp}}$ are referred to as the open-loop admittances of the LCL filter, and they are quintessential building blocks of the closed-loop output admittance of the converter system further discussed in Chapter 5.

A hold-equivalent discrete-time model of the LCL filter is considered in Publications I-IV. In discretization of the dynamic model (2.7), the following assumptions formulated by Kukkola et al. (2015) are made:

1. Sampling of the measurements is synchronized with the PWM.
2. PWM is modeled as a zero-order hold (ZOH) in stationary coordinates, which means that the converter voltage vector $\boldsymbol{u}_{\mathrm{c}}^{\mathrm{s}}$ remains constant between two consecutive sampling instants.
3. System parameters and the grid angular frequency ω_{g} are assumed constant over T_{s}.
4. The disturbance input is assumed constant over T_{s} in synchronous coordinates.

Under these assumptions, the hold-equivalent model of the LCL filter in synchronous coordinates rotating at ω_{g} becomes

$$\mathbf{x}_{\mathrm{p}}(k+1) = \boldsymbol{\Phi}_{\mathrm{p}} \mathbf{x}_{\mathrm{p}}(k) + \boldsymbol{\Gamma}_{\mathrm{cp}} \boldsymbol{u}_{\mathrm{c}}(k) + \boldsymbol{\Gamma}_{\mathrm{gp}} \boldsymbol{u}_{\mathrm{g}}(k) \tag{2.13}$$

where the system matrices are obtained by solving (Kukkola et al., 2015)

$$\boldsymbol{\Phi}_{\mathrm{p}} = \mathrm{e}^{\mathbf{A} T_{\mathrm{s}}}, \qquad \boldsymbol{\Gamma}_{\mathrm{cp}} = \int_0^{T_{\mathrm{s}}} \mathrm{e}^{\mathbf{A}\tau} \mathrm{e}^{-\mathrm{j}\omega_{\mathrm{g}}(T_{\mathrm{s}}-\tau)} \mathrm{d}\tau \cdot \mathbf{B}_{\mathrm{c}}, \qquad \boldsymbol{\Gamma}_{\mathrm{gp}} = \int_0^{T_{\mathrm{s}}} \mathrm{e}^{\mathbf{A}\tau} \mathrm{d}\tau \cdot \mathbf{B}_{\mathrm{g}}. \tag{2.14}$$

2.3 Control-Hardware-Induced Delay

In addition to the delay caused by the PWM, the finite computational resources of the processor executing the control algorithms implemented on a converter incur additional delay in the system. A computational delay equal to one sampling period is typically used (Wu and Lehn, 2006; Kukkola et al., 2015). In the discrete-time domain, this delay can be simply modeled as

$$\text{Stationary coordinates:} \quad \boldsymbol{u}_{\mathrm{c}}^{\mathrm{s}}(k+1) = \boldsymbol{u}_{\mathrm{c,ref}}^{\mathrm{s}}(k) \tag{2.15}$$

$$\text{Synchronous coordinates:} \quad \boldsymbol{u}_{\mathrm{c}}(k+1) = \boldsymbol{\gamma} \boldsymbol{u}_{\mathrm{c,ref}}(k) \tag{2.16}$$

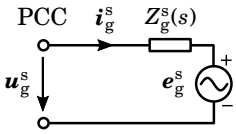

Figure 2.4. Equivalent circuit model of an electric grid, presented in stationary coordinates.

where the rotation factor is $\boldsymbol{\gamma} = \mathrm{e}^{-\mathrm{j}\omega_\mathrm{g} T_\mathrm{s}}$. The rotation factor is not unique, and may take different values depending if reference frame angle prediction is used and on the order in which the reference frame angle update and the inverse Park transformation are carried out. Augmenting the computational delay into the hold-equivalent LCL filter model (2.13), one obtains

$$\underbrace{\begin{bmatrix}\mathbf{x}_\mathrm{p}\\ \boldsymbol{u}_\mathrm{c}\end{bmatrix}}_{\mathbf{x}}(k+1) = \underbrace{\begin{bmatrix}\boldsymbol{\Phi}_\mathrm{p} & \boldsymbol{\Gamma}_\mathrm{cp}\\ \mathbf{0} & 0\end{bmatrix}}_{\boldsymbol{\Phi}}\mathbf{x}(k) + \underbrace{\begin{bmatrix}0\\ \boldsymbol{\gamma}\end{bmatrix}}_{\boldsymbol{\Gamma}_\mathrm{c}}\boldsymbol{u}_{\mathrm{c,ref}}(k) + \underbrace{\begin{bmatrix}\boldsymbol{\Gamma}_\mathrm{gp}\\ 0\end{bmatrix}}_{\boldsymbol{\Gamma}_\mathrm{g}}\boldsymbol{u}_\mathrm{g}(k). \tag{2.17}$$

As a consequence of augmenting the LCL filter model with a computational delay, its order increases by one. Analogously to the continuous-time state-space model, the grid current can be extracted from the model as

$$\boldsymbol{i}_\mathrm{g}(k) = \underbrace{\begin{bmatrix}0 & 0 & 1 & 0\end{bmatrix}}_{\mathbf{C}_\mathrm{g}}\mathbf{x}(k). \tag{2.18}$$

Now, the discrete-time open-loop admittances of the LCL filter, including the delay, can be expressed using the state-space model (2.17) and (2.18) as

$$\boldsymbol{Y}_\mathrm{g}(z) = -\frac{\boldsymbol{i}_\mathrm{g}(z)}{\boldsymbol{u}_\mathrm{g}(z)} = -\mathbf{C}_\mathrm{g}(z\mathbf{I} - \boldsymbol{\Phi})^{-1}\boldsymbol{\Gamma}_\mathrm{g} \tag{2.19}$$

$$\boldsymbol{Y}_\mathrm{c}(z) = \frac{\boldsymbol{i}_\mathrm{g}(z)}{\boldsymbol{u}_{\mathrm{c,ref}}(z)} = \mathbf{C}_\mathrm{g}(z\mathbf{I} - \boldsymbol{\Phi})^{-1}\boldsymbol{\Gamma}_\mathrm{c} \tag{2.20}$$

where z is the Z-transform variable.

2.4 Grid

An equivalent circuit model of the electric grid in stationary coordinates is shown in Fig. 2.4, where Z_g^s is the grid impedance and $\boldsymbol{e}_\mathrm{g}^\mathrm{s}$ is the grid back-EMF. A converter is connected to the PCC terminals, forming the converter–grid interconnection. In this thesis, an ideal grid is assumed in the control design stage, i.e., $Z_\mathrm{g}^\mathrm{s}(s) = 0$, unless otherwise stated. The characteristic of the grid impedance is typically unknown due to its highly dependent behavior on both frequency and time (Knop and Fuchs, 2009;

Shuai et al., 2014; Zhang et al., 2014; Jessen et al., 2015), complicating the exact modeling of the grid impedance. Consequently, simplifying assumptions are typically made when considering the effect of grid impedance on the control behavior. In the control-loop bandwidth of the converter, the grid impedance typically appears as inductive-resistive; thus, it is modeled as a series connection of an inductive and resistive elements. In literature related to control design, a popular approach has been to omit the resistive characteristic of the impedance, resulting in a purely inductive impedance. This same approach is adopted in the control-design related publications of this thesis. For purely inductive grids, the short-circuit ratio (SCR) of the grid can be defined as the inverse of the per-unit inductance as seen from the PCC, that is, as

$$\mathrm{SCR} = \frac{1}{L_\mathrm{g}\,[\mathrm{p.u.}]}. \tag{2.21}$$

Alternatively, the series inductance of the converter filter can also be included in the definition of the SCR, as is done in Publication VIII. The grid is referred to as strong if $\mathrm{SCR} > 3$, weak if $2 \leq \mathrm{SCR} \leq 3$, and very weak if $\mathrm{SCR} < 2$ (IEEE 1204-1997, 1997). On the other hand, for validation of the real-time identification methods presented in Publications II and VI, grid impedances including the effect of additional converters connected to the same PCC (Agorreta et al., 2011) and resonant modes (Papathanassiou and Papadopoulos, 2006) are also considered in addition to a purely inductive-resistive impedance.

The phase voltages of the grid are defined as

$$\begin{aligned} e_\mathrm{ga} &= E_\mathrm{ga}\cos\left(\omega_\mathrm{g} t + \varphi_\mathrm{ga}\right) \\ e_\mathrm{gb} &= E_\mathrm{gb}\cos\left(\omega_\mathrm{g} t + \varphi_\mathrm{gb} - \frac{2\pi}{3}\right) \\ e_\mathrm{gc} &= E_\mathrm{gc}\cos\left(\omega_\mathrm{g} t + \varphi_\mathrm{gc} + \frac{2\pi}{3}\right) \end{aligned} \tag{2.22}$$

where $E_\mathrm{ga}, E_\mathrm{gb}$, and E_gc are the phase-voltage peak-amplitudes and $\varphi_\mathrm{ga}, \varphi_\mathrm{gb}$, and φ_gc are the phase-voltage shifts. In the case of balanced operation, the peak amplitudes and shifts are equal, i.e., $E_\mathrm{ga} = E_\mathrm{gb} = E_\mathrm{gc}$ and $\varphi_\mathrm{ga} = \varphi_\mathrm{gb} = \varphi_\mathrm{gc}$, and the locus of the grid-voltage vector $\boldsymbol{e}_\mathrm{g}^\mathrm{s}$ traces a circle in the complex plane. However, practical electric grids are typically unbalanced to some extent. Unbalance is induced by uneven loading of the phases and various faults in the grid, and it can be modeled by superimposing a negative-sequence component with the fundamental-frequency component. Considering space vectors, the negative-sequence components rotates at an angular frequency equal to the fundamental-frequency component, but in the opposite direction. Therefore, the locus of an unbalanced grid-voltage vector is an ellipsoid. Moreover, real grid voltages are typically polluted with varying degrees of harmonics that are integer multiples of the

fundamental frequency (IEEE 519-2014, 2014). Analogously to modeling the effect of unbalanced grid voltages, additional harmonic components can be modeled through the principle of superposition.

3. Single- and Double-Frequency Current Control

This chapter deals with current control of grid converters by first briefly introducing the topic. After this introduction, state-feedback current control of a grid converter equipped with an LCL filter is focused on. Only one of the states of the filter, meaning, either the converter current or the grid current, is assumed to be measured, and the rest of the states are estimated using an observer. Two different implementations for integral action are presented, state augmentation with an integrator and observer augmentation with a disturbance-signal estimator, followed by a discussion on their relations. This chapter is concluded by an overview of aspects related to control design and tuning.

3.1 Introduction to Current Control

Current control methods for grid converters have been intensely researched for several decades due to the growing utilization of converters in various grid applications. During this time, vast amounts of different control methods and analyses have been produced. From the perspective of this chapter, the current control methods suitable for the control of converters equipped with an LCL filter are of particular interest. A block diagram of an example current-controlled grid converter equipped with an LCL filter is shown in Fig. 3.1, in which either the converter or the grid current is measured for the control system. In the case of converter current measurement, converter overcurrent protection is inherently achieved. For grid current measurement, this is not the case. However, for example, the methods discussed in subsection 4.4 can be applied. For the rest of this section, grid current feedback is assumed. The control system operates in grid-voltage-oriented SRF, which is established using a PLL (Kaura and Blasko, 1997).

The body of literature on the current control methods suitable for converters equipped with LCL filters encompasses SRF PI controllers (Blasko and Kaura, 1997; Twining and Holmes, 2003; Malinowski and Bernet,

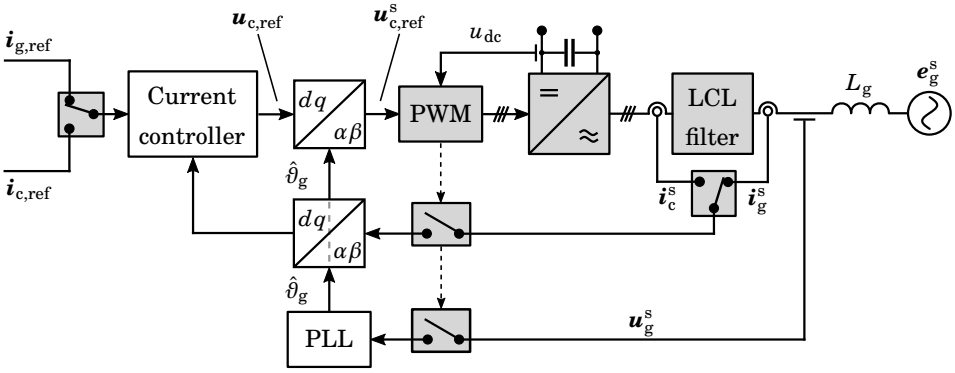

Figure 3.1. Grid converter system equipped with an LCL filter, connected to an inductive grid.

2008; Dannehl et al., 2009, 2010a; Parker et al., 2014; Miskovic et al., 2014; Xu et al., 2014), PR controllers (Zmood et al., 2001; Zmood and Holmes, 2003; Twining and Holmes, 2003; Hwang et al., 2010; Wang et al., 2016b; Zhao et al., 2022), state-feedback controllers (Wu and Lehn, 2006; Dannehl et al., 2010b; Xue et al., 2012; Kukkola et al., 2015; Rahman et al., 2018; Rodríguez-Cabero et al., 2019; Su et al., 2019), predictive controllers (Mariethoz and Morari, 2009; Zhang et al., 2016; Rodriguez et al., 2013), and various nonlinear controllers (Serpa et al., 2007; Suul et al., 2011; Hao et al., 2013), to name a few. Each of these control methods have their own advantages and disadvantages, and the choice of control method highly depends on the requirements imposed on the converter system. In this thesis, linear current controllers, in particular state-feedback controllers, are focused on due to their numerous desirable characteristics, including reproducibility, ease of analysis, flexibility of design, and good performance.

3.2 State-Feedback Current Control

As the research on the current control methods of converters matured, several interesting links between the different linear control methods were uncovered. The SRF PI controller was found to be equivalent to the PR controller operating in stationary coordinates (Zmood et al., 2001; Zmood and Holmes, 2003; Hwang et al., 2010). Furthermore, the SRF PI controller was shown to be a special case of the state-feedback controller (Kukkola and Hinkkanen, 2014). Consequently, both the SRF PI and the PR controllers can be considered as special cases of state-feedback control. This structural hierarchy implies that the SRF PI and PR controllers are simpler in both structure and design, but inevitably lack in flexibility as compared to the full-fledged state-feedback control.

Indeed, the stability of SRF PI and PR controllers is severely limited

by a specific ratio of sampling frequency and resonance frequency (Zou et al., 2014; Parker et al., 2014; Wang et al., 2016a), a limitation which does not apply to state-feedback controllers (Pérez-Estévez et al., 2017). Moreover, state-feedback control allows for setting the closed-loop dynamics arbitrarily (Franklin et al., 1998). This flexibility is a double-edged sword since the complexity of the pole-placement problem increases steeply as the order of the controlled system increases. Thankfully, a manifold of potential solutions for placing the system poles have been devised. The different pole-placement methods can be roughly divided into direct and indirect approaches. In the direct approach, the control designer explicitly defines the desired pole locations, and solves the controller gains based on these pole locations and system parameters either analytically (Wu and Lehn, 2006; Dannehl et al., 2010b; Kukkola et al., 2015) or numerically (Xue et al., 2012; Pérez-Estévez et al., 2017, 2018). The benefit of direct pole placement is that the desired control performance can be defined in terms of typical control-theoretic quantities, such as bandwidth and overshoot. In the indirect approach, the controller gains are obtained by solving an optimization problem, for example, to maximize robustness against grid impedance variations. Indirect pole placement methods include those based on linear quadratic regulator (LQR) theory (Wu and Lehn, 2006; Busada et al., 2015; Huerta et al., 2018; Khajehoddin et al., 2018; Tran et al., 2018; Rodríguez-Cabero et al., 2019; Su et al., 2019; Xie et al., 2020), $\mathscr{H}_\infty$ methods (Maccari et al., 2012; Koch et al., 2019), linear matrix inequality (LMI) methods (Maccari et al., 2014; Lai and Kim, 2018), particle swarm optimization (PSO) methods (Borin et al., 2020), and hybrid solutions (Bimarta and Kim, 2020; Koch et al., 2020). These methods are found to be particularly useful for systems with high order, in which the solution space of the pole placement problem, and thus the complexity, increases steeply. An example of such a system is a converter equipped with a multi-frequency current controller (Xie et al., 2020).

The state-feedback controller can be augmented with various auxiliary components, such as the reference feedforward for enhancing reference-tracking dynamics (Kukkola et al., 2015), disturbance feedforward for improving disturbance rejection performance (Xue et al., 2012), and integral action for removing any steady-state errors in the controlled signal (Wu and Lehn, 2006). While the inclusion of disturbance feedforward typically reduces the steady-state error of the system, it does not completely eliminate it as integral action does. Moreover, the differences between the effect of the disturbance feedforward and integral action are not explicit for all grid converter systems, and they can be designed to very similarly affect the reference-tracking and disturbance-rejection behavior of the system, as elucidated in Publication VII. The augmentation of a state-feedback controller with integral action can be implemented by using either an integral state in the controller or by equipping the state observer with a

disturbance-signal estimator (Franklin et al., 1998).

3.3 Positive- and Negative-Sequence State-Feedback Current Control

In its simplest form, integral action eliminates the steady-state error from the DC component of the controlled current. In synchronous coordinates, this corresponds to the fundamental-frequency positive-sequence component. As discussed in Section 2.4, grid unbalance induced by either asymmetrical grid impedance or voltage causes a fundamental-frequency negative-sequence component to appear in the system. A simple integrator is unable to eliminate this negative-sequence component, and steady-state oscillations will ensue in the controlled signal. To achieve error-free steady-state reference tracking in the unbalanced case, double-frequency control is required. In the existing literature, double-frequency current control in synchronous coordinates is conventionally implemented using double synchronous reference frame (DSRF) control (Song and Nam, 1999; Suh and Lipo, 2006; Reyes et al., 2012). The DSRF controller essentially comprises two parallel SRF PI controllers; one operates in positive-sequence synchronous coordinates and the other one in negative-sequence synchronous coordinates. Other implementations also exist, such as one based on LQR controllers proposed by Alepuz et al. (2009). The DSRF controller requires maintenance of two synchronous reference frames, and four separate PI controllers with decoupled d- and q-axes, resulting in a complex structure. Another implementation by employing generalized integrators is introduced in Busada et al. (2012), in which the integrators for different frequency components are implemented in a single reference frame. The resonators in PR controllers can be implemented using two generalized integrators (Liserre et al., 2006a; Busada et al., 2012).

In view of state-feedback-based implementation, the integral action for the negative-sequence component can be implemented either through addition of a generalized integrator or by modifying the disturbance model in the disturbance-signal estimator. In fact, integral action can be implemented for an arbitrary number of frequencies by using a superposition of separate generalized integrators (Busada et al., 2015) or modification of the disturbance-signal estimator (Pérez-Estévez et al., 2018). In addition to the two single-frequency implementations of integral action for state-feedback controllers, this chapter also includes their corresponding double-frequency variants. These two approaches to implementing integral action can also be considered to follow the principle of an internal model (Fukuda and Yoda, 2001), according to which the controller needs to include a model for the disturbance to eliminate the steady-state error caused by it. The internal models for a constant-amplitude disturbance of

a specific frequency are the generalized integrator and the disturbance-signal observer in the integrator-based and the disturbance-observer-based implementations, respectively.

As already briefly mentioned in the previous section, for high-order systems, such as the multi-frequency current controllers, it may become unnecessarily arduous to study the various possible direct pole placements, in which case the use of indirect pole placement methods becomes favorable. However, for the special case of double-frequency control, direct pole-placement methods have been used with satisfactory results (Pérez-Estévez et al., 2017), although the robustness to grid inductance variations does not match those of the indirect methods nor the single-frequency controller case. Upon examining the collection of pole placements obtained using the existing robust indirect methods, a bigger picture can be perceived; the closed-loop integrator poles tend to be located near their open-loop locations. This is realized by low controller gains, which can be interpreted as maintaining a low control effort (Franklin et al., 2015). Additionally, low controller gains are tied to enhancing the system robustness to uncertainty (Goodwin et al., 2001).

This observation is applied in Publication VIII, in which an enhanced direct pole-placement design is presented for positive- and negative-sequence current control of grid converters. In the presented design, a closed-loop pole is located in the vicinity of the negative-sequence integrator open-loop pole. This results in a considerable improvement in the robustness of the system to variations in the grid inductance as compared to a recently proposed direct pole-placement design by Pérez-Estévez et al. (2017), in which the corresponding pole is placed on the positive real axis. The design presented in Publication VIII is shown to operate stably in grids ranging from strong to very weak, essentially matching in robustness with state-of-the-art indirect pole-placement methods. Furthermore, good dynamic performance is obtained in the whole range of examined grid inductances with the presented design. The results of this publication demonstrate that while indirect pole-placement methods involving potentially complex optimization problems are powerful tools, the control designer can use the results obtained from the existing indirect methods to synthesize a direct pole-placement design that closely matches the performance of these methods. This can greatly simplify the controller design process without compromising control performance as the explicitly parameterized pole locations can be used to either analytically or numerically solve the controller gains in a straightforward manner, thus avoiding use of any complex optimization routines.

3.4 State Observers

State-feedback controllers rely on the availability of each state in the control law. All the states can be measured for the controller, as is done in (Wu and Lehn, 2006; Dannehl et al., 2010b; Rodríguez-Cabero et al., 2019; Xie et al., 2020). For applications such as current control of a three-phase converter equipped with an LCL filter, the cost of including three sets of sensors can become economically unfeasible. Thankfully, one set of current measurement sensors suffices when an observer is used to estimate the unknown states (Franklin et al., 1998). The use of an observer increases the complexity of the controller while simultaneously increasing the system reliability due to fewer components. However, the separation principle (Franklin et al., 1998) enables isolated design of the observer and the control law, thus alleviating the increase in the overall controller complexity.

There is a wide variety of different observer structures and implementations from which one can choose. Implementations have been proposed in the existing literature based on full-order observers (Kukkola and Hinkkanen, 2014; Miskovic et al., 2014; Kukkola et al., 2015; Lai and Kim, 2018; Tran et al., 2018), reduced-order observers (Pérez-Estévez et al., 2017; Rahman et al., 2018; Su et al., 2019), and Kalman filters (Ahmed et al., 2009; Huerta et al., 2012; Xue et al., 2012). The full-order observer reconstructs the whole state vector, including both the unknown and measured states, whereas the reduced-order observer only reconstructs the unknown states. The Kalman filter is an adaptive-gain observer suitable for noisy environments, and it carries a structural resemblance to the full-order observer. In fact, its steady-state implementation is identical to a full-order observer (Huerta et al., 2012). The full-order observer can be implemented in discrete-time either as a current type (Tran et al., 2018) or as a prediction type (Miskovic et al., 2014; Kukkola et al., 2015; Lai and Kim, 2018). The difference between these two implementations lies in the measurement used to compute the prediction error (Franklin et al., 1998). In the current-type observer, the prediction error at time instant k is based on the measurement at the same time instant, whereas for the prediction-type observer the prediction error is computed based on the measurement from the previous sampling instant. In the work by Rahman et al. (2020), the reduced-order observer is shown to be a special case of the current-type full-order observer. Furthermore, an observer can be augmented with additional adaptation laws for estimating grid parameters, such as impedance (Kukkola et al., 2019), frequency (Kukkola and Hinkkanen, 2016), and voltage (Ahmed et al., 2009; Kukkola and Hinkkanen, 2016), based on the estimation error of the observer.

While the combination of state-feedback control and an observer can yield great flexibility in setting the dynamic of the resulting closed-loop system

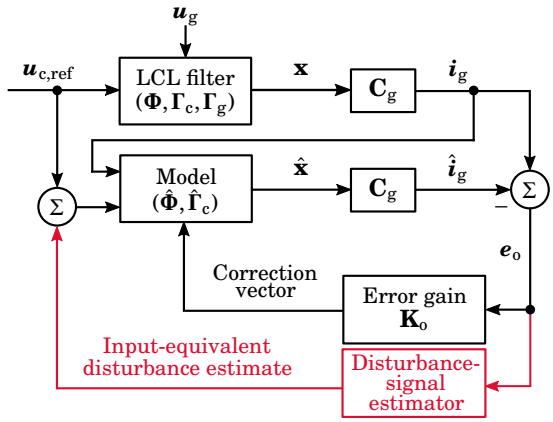

Figure 3.2. Block diagram of the system model, cf. (2.17) and (2.18), and a reduced-order observer used to estimate the unknown states of the system. The input-equivalent disturbance-signal estimator highlighted in red is used only in the disturbance-observer-based design of Publication IV.

even when only a single state is measured, similar results can also be obtained by means of polynomial-based design (Turner et al., 2011; Pérez-Estévez et al., 2018). However, in comparison to the polynomial-based designs, the modularity of the state-feedback control in combination with an observer results in a less abstract structure and simplifies the design procedure due to the celebrated separation principle. Moreover, contrary to state-feedback control, implementing anti-windup is not feasible in polynomial-based designs. The lack of an anti-windup mechanism has a significant adverse impact on the system behavior when the converter voltage reference is saturated.

In Publications I-III, the observer design is based on the state-space model (2.13). On the other hand, in Publication IV, the computational delay is included in the observer, and consequently, the converter voltage is included as a state in the observer model together with the converter current and capacitor voltage; in other words, the state-space model (2.17) is used in the observer design. In the controller designs covered in this chapter, a reduced-order observer, shown in Fig. 3.2, is considered. For further details of the observer, the reader is referred to Publication IV.

3.5 Disturbance-Observer-Based Design

The integral action can be implemented using a disturbance-signal estimator depicted as an auxiliary component of the observer in Fig. 3.2. In fact, the disturbance-signal estimator is a more general concept that can be used to compensate for various grid voltage components. It is based on assuming the nature of the disturbance signal in an explicit form, after which a state-space representation for the signal is formulated. The plant

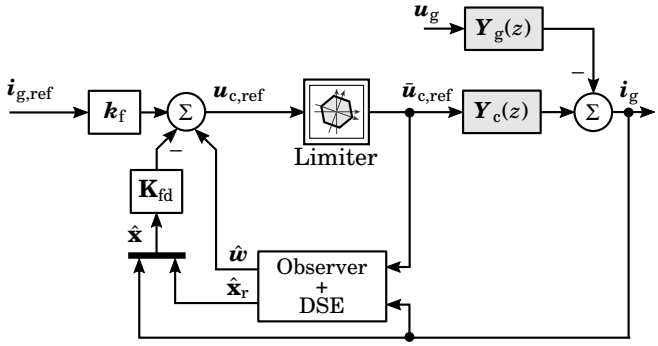

Figure 3.3. Disturbance-estimator-based state-feedback current controller. DSE stands for disturbance-signal estimator. In linear modulation range, the limiter does not have an effect on the converter voltage reference, meaning $\boldsymbol{u}_\mathrm{c,ref} = \bar{\boldsymbol{u}}_\mathrm{c,ref}$.

model used in the observer design is then augmented with the state-space representation of the disturbance model. The discrete-time model of a constant-amplitude fundamental-frequency disturbance in synchronous coordinates, which corresponds to a DC quantity, can be written as

$$\boldsymbol{r}(k+1) = \boldsymbol{r}(k) \tag{3.1}$$

$$\boldsymbol{w}(k) = \boldsymbol{r}(k) \tag{3.2}$$

where $\boldsymbol{r}$ is the state of the disturbance model, and $\boldsymbol{w}$ is its output. A disturbance-observer-based design of the state-feedback current controller is shown in Fig. 3.3. In the figure, $\boldsymbol{Y}_\mathrm{g}$ and $\boldsymbol{Y}_\mathrm{c}$ are the hold-equivalent open-loop admittances of the LCL filter, cf. (2.19) and (2.20). In addition to augmenting the system model with the disturbance state, the inclusion of the disturbance-signal estimator to the observer requires that the input-equivalent disturbance is superimposed with the converter voltage reference signal in the observer model (2.17), cf. Fig. 3.2. The input-equivalent disturbance state in the observer can be expressed as

$$\hat{\boldsymbol{w}}(k+1) = \hat{\boldsymbol{w}}(k) - \boldsymbol{k}_\mathrm{w}\boldsymbol{e}_\mathrm{o}(k) \tag{3.3}$$

where $\boldsymbol{k}_\mathrm{w}$ is the observer gain for the state and $\boldsymbol{e}_\mathrm{o} = \boldsymbol{i}_\mathrm{g} - \hat{\boldsymbol{i}}_\mathrm{g}$ is the estimation error. Symbols equipped with a circumflex refer to estimated quantities. This state is then augmented to the control law, yielding

$$\boldsymbol{u}_\mathrm{c,ref}(k) = \boldsymbol{k}_\mathrm{f}\boldsymbol{i}_\mathrm{g,ref}(k) - \mathbf{K}_\mathrm{fd}\hat{\mathbf{x}}(k) + \hat{\boldsymbol{w}}(k) \tag{3.4}$$

where $\boldsymbol{k}_\mathrm{f}$ is the reference feedforward gain, $\mathbf{K}_\mathrm{fd}$ is the state-feedback gain vector, and $\hat{\mathbf{x}} = [\boldsymbol{i}_\mathrm{g}, \hat{\mathbf{x}}_\mathrm{r}]^\mathrm{T} = [\boldsymbol{i}_\mathrm{g}, \hat{\boldsymbol{u}}_\mathrm{f}, \hat{\boldsymbol{i}}_\mathrm{c}, \hat{\boldsymbol{u}}_\mathrm{c}]^\mathrm{T}$.

In case a negative-sequence disturbance component is also to be estimated, the disturbance-signal estimator can be modified by including an additional state corresponding to the negative-sequence signal. In fact, one can include an arbitrary number of disturbance components in

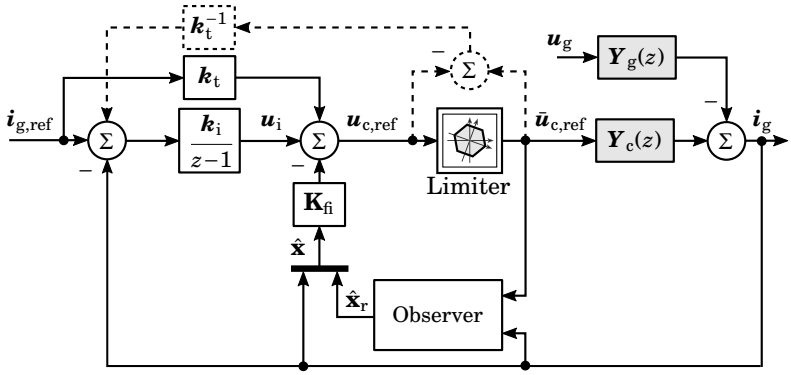

Figure 3.4. Single-frequency integrator-based state-feedback current controller. In linear modulation range, the limiter does not have an effect on the converter voltage reference, meaning $\boldsymbol{u}_{\mathrm{c,ref}} = \bar{\boldsymbol{u}}_{\mathrm{c,ref}}$. The anti-windup scheme of the integrator is marked with dashed lines.

the disturbance-signal estimator. The fundamental-frequency disturbance model comprising (3.1) and (3.2) can be extended to accommodate constant-amplitude negative-sequence disturbance estimation, which appears to be rotating at $2\omega_{\mathrm{g}}$ to the clockwise direction in synchronous coordinates, as

$$\mathbf{r}(k+1) = \begin{bmatrix} 1 & 0 \\ 0 & \mathrm{e}^{-2\mathrm{j}\omega_{\mathrm{g}}T_{\mathrm{s}}} \end{bmatrix} \mathbf{r}(k) \tag{3.5}$$

$$\boldsymbol{w}(k) = \begin{bmatrix} 1 & 1 \end{bmatrix} \mathbf{r}(k). \tag{3.6}$$

The control law is identical to the single-frequency case, since the negative-sequence component can be succinctly superimposed with the positive-sequence component in the output $\boldsymbol{w}$. One of the benefits of using disturbance-observer-based implementation is that the observer inherently provides anti-windup mechanism for the integral action in the event of converter voltage reference saturation (Franklin et al., 1998), since the limited converter voltage reference $\bar{\boldsymbol{u}}_{\mathrm{c,ref}}$ is used as the input to the observer, cf. Fig. 3.3.

3.6 Integrator-Based Design

Another alternative to implementing integral action is to augment the controller with an integrator. A block diagram of the integrator-based design is shown in Fig. 3.4. The integral state $\boldsymbol{u}_{\mathrm{i}}$ is defined as

$$\boldsymbol{u}_{\mathrm{i}}(k+1) = \boldsymbol{u}_{\mathrm{i}}(k) + \boldsymbol{k}_{\mathrm{i}}\boldsymbol{e}_{\mathrm{i}}(k) \tag{3.7}$$

where $\boldsymbol{e}_{\mathrm{i}}(k) = \boldsymbol{i}_{\mathrm{g,ref}}(k) - \boldsymbol{i}_{\mathrm{g}}(k)$ is the tracking error and $\boldsymbol{k}_{\mathrm{i}}$ is the integral gain. The control law of a state-feedback current controller augmented with an

integrator can be written as

$$\boldsymbol{u}_{\mathrm{c,ref}}(k) = \boldsymbol{k}_{\mathrm{t}}\boldsymbol{i}_{\mathrm{g,ref}}(k) - \mathbf{K}_{\mathrm{fi}}\hat{\mathbf{x}}(k) + \boldsymbol{u}_{\mathrm{i}}(k) \tag{3.8}$$

where $\boldsymbol{k}_{\mathrm{t}}$ is the reference feedforward gain and $\mathbf{K}_{\mathrm{fi}}$ is the state-feedback gain vector.

The integrator concept can be extended to double-frequency control in order to eliminate undesired negative-sequence component from the controlled signal by simply adding another appropriately designed integrating state to the controller. However, these integrators are coupled by default, resulting in a deterioration of performance as compared to the corresponding double-frequency disturbance-signal estimator. To match the performance of these two double-frequency integral action implementations, decoupling of the two integrators is required. In Publication IV, the decoupling is achieved by introducing additional cross-coupling of the reference inputs to the integrators. Consequently, the decoupled integrators are defined as

$$\boldsymbol{u}_{\mathrm{i}+}(k+1) = \boldsymbol{u}_{\mathrm{i}+}(k) + \boldsymbol{k}_{\mathrm{i}+}\left[\boldsymbol{i}_{\mathrm{g,ref}+}(k) - \boldsymbol{i}_{\mathrm{g}}(k) + \boldsymbol{k}_{\mathrm{c}-}\boldsymbol{i}_{\mathrm{g,ref}-}(k)\right] \tag{3.9}$$

$$\boldsymbol{u}_{\mathrm{i}-}(k+1) = \boldsymbol{\phi}\boldsymbol{u}_{\mathrm{i}-}(k) + \boldsymbol{k}_{\mathrm{i}-}\left[\boldsymbol{i}_{\mathrm{g,ref}-}(k) - \boldsymbol{i}_{\mathrm{g}}(k) + \boldsymbol{k}_{\mathrm{c}+}\boldsymbol{i}_{\mathrm{g,ref}+}(k)\right] \tag{3.10}$$

where $\boldsymbol{\phi} = \mathrm{e}^{-\mathrm{j}2\omega_{\mathrm{g}}T_{\mathrm{s}}}$, $\boldsymbol{k}_{\mathrm{i}-}$ and $\boldsymbol{k}_{\mathrm{i}+}$ are the integrator gains, and $\boldsymbol{k}_{\mathrm{c}+}$ and $\boldsymbol{k}_{\mathrm{c}-}$ are the cross-coupling gains. These integrators are graphically depicted in Fig. 3.5. The reference cross-coupling paths in the state equations (3.9) and (3.10) create additional zeros to the reference-tracking transfer functions $\boldsymbol{i}_{\mathrm{g}}(z)/\boldsymbol{i}_{\mathrm{g,ref}+}(z)$ and $\boldsymbol{i}_{\mathrm{g}}(z)/\boldsymbol{i}_{\mathrm{g,ref}-}(z)$. The location of these zeros can be adjusted through the gains $\boldsymbol{k}_{\mathrm{c}+}$ and $\boldsymbol{k}_{\mathrm{c}-}$, and the zeros can be used to cancel out the effect of the other integrator. By augmenting the state-feedback control law with these integrators, one obtains

$$\boldsymbol{u}_{\mathrm{c,ref}}(k) = \boldsymbol{k}_{\mathrm{t}+}\boldsymbol{i}_{\mathrm{g,ref}+}(k) + \boldsymbol{k}_{\mathrm{t}-}\boldsymbol{i}_{\mathrm{g,ref}-}(k) - \mathbf{K}_{\mathrm{fi}}\mathbf{x}(k) + \boldsymbol{u}_{\mathrm{i}+}(k) + \boldsymbol{u}_{\mathrm{i}-}(k). \tag{3.11}$$

Unlike for the disturbance-observer-based implementation, in which anti-windup was inherently included in the observer structure, additional measures are required in the integrator-based implementation. If an anti-windup mechanism is not implemented, the system becomes prone to overshoots during actuator saturation, as elucidated in (Åström and Wittenmark, 1997). In the relevant publications of this thesis, the realizable reference anti-windup method presented in (Peng et al., 1996) is employed, which is shown by the dashed lines in Figs. 3.4 and 3.5. An advantage of the integrator-based implementation is that the negative-sequence current component can be controlled to a nonzero value in steady state due to the existence of $\boldsymbol{i}_{\mathrm{g,ref}-}$. This can be useful, for example, for implementing unbalance compensation or dynamic voltage support.

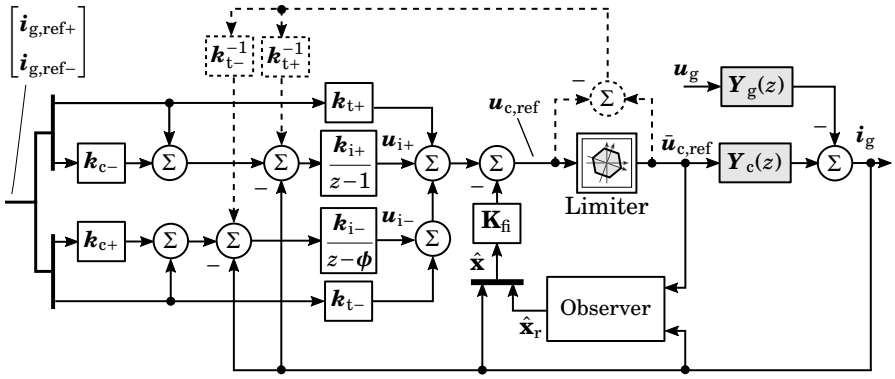

Figure 3.5. Double-frequency integrator-based state-feedback current controller. In linear modulation range, the limiter does not have an effect on the converter voltage reference, meaning $\boldsymbol{u}_{\mathrm{c,ref}} = \bar{\boldsymbol{u}}_{\mathrm{c,ref}}$. The anti-windup scheme of the integrator is marked with dashed lines.

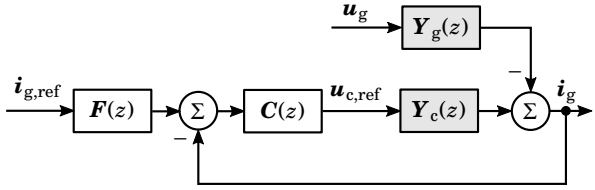

Figure 3.6. Double-frequency integrator-based state-feedback current controller.

3.7 On the Equivalence of Designs

In Publication IV, the two controllers introduced above in Figs. 3.3 and 3.4 are found to be mathematically equivalent under a set of conditions related to their tuning. Prior to this publication, the links between these two controller structures had not been well understood in the literature. To show the equivalence, the two controllers are formulated in the two-degree-of-freedom (2DOF) framework presented, for example, in (Skogestad and Postlethwaite, 1996). A block diagram of the system model in the 2DOF framework is presented in Fig. 3.6. The framework comprises two controller transfer functions, the prefilter $\boldsymbol{F}$ and the feedback controller $\boldsymbol{C}$. The LCL filter is modeled by its open-loop admittances $\boldsymbol{Y}_{\mathrm{g}}$ and $\boldsymbol{Y}_{\mathrm{c}}$ found in (2.19) and (2.20), respectively. The closed-loop system in Fig. 3.6 can be written as

$$\boldsymbol{i}_{\mathrm{g}}(z) = \underbrace{\frac{\boldsymbol{F}(z)\boldsymbol{C}(z)\boldsymbol{Y}_{\mathrm{c}}(z)}{1+\boldsymbol{C}(z)\boldsymbol{Y}_{\mathrm{c}}(z)}}_{\boldsymbol{G}_{\mathrm{cl}}(z)} \boldsymbol{i}_{\mathrm{g,ref}}(z) - \underbrace{\frac{\boldsymbol{Y}_{\mathrm{g}}(z)}{1+\boldsymbol{C}(z)\boldsymbol{Y}_{\mathrm{c}}(z)}}_{\boldsymbol{Y}_{\mathrm{oa,d}}(z)} \boldsymbol{u}_{\mathrm{g}}(z) \tag{3.12}$$

where $\boldsymbol{G}_{\mathrm{cl}}$ is the reference-tracking transfer function and $\boldsymbol{Y}_{\mathrm{oa,d}}$ is the converter output admittance.

Since the open-loop admittances $\boldsymbol{Y}_{\mathrm{g}}$ and $\boldsymbol{Y}_{\mathrm{c}}$ are defined by the physical filter, they are immutable assuming that the same filter is used for both controllers. Therefore, to show that the two closed-loop systems are equiv-

alent, it remains to be shown that the two controller transfer functions, $\boldsymbol{F}$ and $\boldsymbol{C}$ are equal in both controller designs. The conditions for their equivalence are derived in Publication IV by comparing the closed-loop systems (3.12) and, in essence, they can be stated for the single-frequency case as

1. The reference feedforward gains $\boldsymbol{k}_\mathrm{t}$ and $\boldsymbol{k}_\mathrm{f}$ in (3.8) and (3.4), respectively, are set equal.
2. The feedforward zero of the integrator-based design is used to achieve pole-zero cancellation of the pole corresponding to the integral action.
3. The desired characteristic polynomials of the closed-loop systems are set equal.

Analogous conditions can be written for the equivalence of the corresponding double-frequency controllers. Despite these results being presented for systems using grid current as feedback, they also apply to systems employing converter current feedback. Furthermore, even though a reduced-order observer is assumed, the results extend to full-order observers.

3.8 Control Tuning

A flowchart describing a tuning procedure for the state-feedback current controllers employed in Publications I-IV and VI is shown in Fig. 3.7. Structurally similar flowcharts can be formulated for the state-feedback controllers in Publications V,VII, and VIII. Often the nominal parameters of the LCL filter, that is, the converter- and grid-side inductances and the filter capacitance, are known in advance. However, in the case there is uncertainty regarding the parameter values, one can estimate them using the real-time identification method presented in Publication II. The presented method can also be used to track the degradation of the filter capacitor, which manifests as a decrease of the filter capacitance (Soliman et al., 2016).

As mentioned in Section 2.4, the grid impedance is a time- and frequency-varying entity. Due to the uncertainty regarding the grid impedance, it is typically assumed to be zero during the control tuning phase. This assumption was also followed in the publications of this thesis. The only exception was in Publication III, in which a tuning based on the assumption of a very weak inductive grid was also considered. It was observed that the combination of high bandwidth design target and high inductance of the controlled system was found to lead to high control gains, and consequently, less robust system that is also more prone to actuator saturation. Therefore, lowered bandwidth targets need to be used in practice when designing the controller under the assumption of a weak grid.

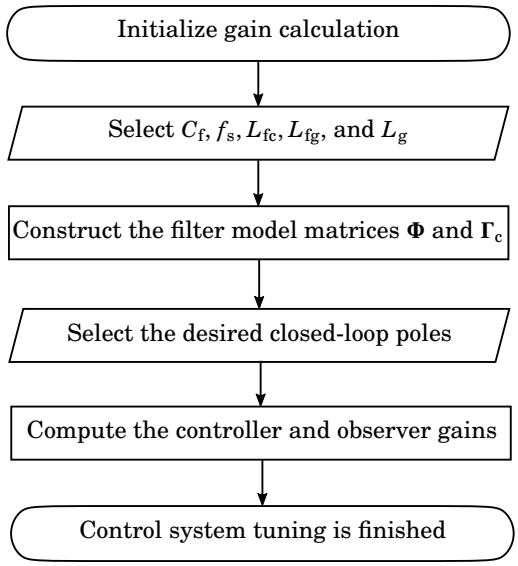

Figure 3.7. Flowchart of the control system tuning procedure.

In addition to the parameters C_f, L_{fc}, L_{fg}, and L_g, one needs to select the sampling frequency f_s of the converter system. The effect of sampling frequency on the stability of the converter system for controllers based on either converter or grid current measurement was comprehensively studied in Publication III. It was found that the state-feedback-based current controller is free of the inherent limitations regarding the ratio of the filter resonance frequency to the sampling frequency found in PI and PR controllers (Parker et al., 2014), irrespective of the choice of current measurement. Furthermore, the assumption of grid strength in controller tuning was found to significantly affect the result of comparison between the measurement options. These results were found to apply to a wide variety of different LCL filters, and not exclusively for the LCL filter studied in Publication III.

After choosing the parameter values used in the design, the state matrix $\mathbf{\Phi}$ and the input vector $\mathbf{\Gamma}_c$ of the state-space model (2.17) are constructed. These two parts are used to compute the state-feedback and observer gains together with the desired closed-loop pole locations. In all of the publications dealing with resonant filters, the resonant poles of the system are damped using radial projection method (Franklin et al., 1998). As explained in various textbooks, such as (Goodwin et al., 2001) and (Franklin et al., 2015), the choice of pole locations always comes down to finding a suitable balance between dynamic performance and robustness to parameter variations. The pole parameterizations used for both the state-feedback and observer in Publications III and IV yield good dynamic performance while retaining stable operation for grid strengths ranging from strong to very weak. However, in the natural extension of these aforementioned

designs to positive- and negative-sequence current control presented in (Pérez-Estévez et al., 2017), the system becomes significantly more sensitive to grid inductance variations and does not tolerate very weak grids, as shown in Publication VIII. This problem could be alleviated by estimating the prevailing grid conditions, for example, by using the real-time grid impedance estimation method presented in Publication VI, and adjusting the control tuning by applying the estimated the grid inductance value. On the other hand, the enhanced direct pole-placement design for positive- and negative-sequence current control presented in Publication VIII offers a solution without the need for adaptive controller gains.

4. Current-Limiting Methods in Voltage-Source Operation of Converters

This chapter delves into the topic of current-limiting methods in voltage-source operation of VSCs. First, a brief introduction to AC-voltage control methods resulting in the voltage-source operation of VSCs is given. In its wake, the most common current-limiting structures used in linear voltage controllers are presented: current limitation by means of current reference saturation and virtual-impedance-based current limiting. Furthermore, other current limiting methods that do not fall into either of these categories are also briefly discussed. Lastly, the multifunctional cascade control structure presented in Publication V is broached.

4.1 Introduction to Voltage-Source Operation

The fundamental goal of converters operated as voltage sources is to regulate the AC-side output voltage of the converter. Consequently, the converter behaves as a regulated voltage source behind an impedance, meaning that the converter system can be modeled as a Thevenin equivalent circuit. AC-voltage control, henceforth referred to as voltage control, methods find a multitude of different applications in power converters. For example, they are used in interfacing renewable energy generation to the electric grid (Quan et al., 2018; Huang et al., 2019; Chen et al., 2020; Pérez-Estévez et al., 2020), VSC-based high-voltage DC transmission systems (Guan et al., 2015), dynamic voltage restorers (Vilathgamuwa et al., 2002), uninterruptible power supplies (Mattavelli, 2005), grid emulators (Averous et al., 2015; Steurer et al., 2010), and various power supplies (Jensen et al., 2000; Mattavelli, 2001; Li et al., 2010).

Akin to current control methods of converters, a bountiful collection of various methods and analyses to tackle the problem of voltage control have been produced during the last decades. This chapter focuses on linear voltage controllers. However, highly-performant nonlinear voltage control methods have also been developed (Cortés et al., 2009; Do et al., 2013; Zheng et al., 2020). From the perspective of current limiting in voltage-

controlled converters, solutions based on model-predictive control (MPC), such as that presented by Cortés et al. (2009), deserve a special mention due to the possibility of integrating current limiting directly to the optimized cost function without having to alter the structure of the controller (Rodriguez and Cortes, 2011). The majority of linear voltage control methods available in the literature can be roughly divided into

- direct, or single-loop, voltage controllers (Mattavelli, 2005; Li et al., 2010; Kim et al., 2015; Wang et al., 2017; Geng et al., 2018; Quan et al., 2018; Kim et al., 2019; Pérez-Estévez et al., 2020; García-Fernández et al., 2021) and
- cascade, or double-loop, voltage controllers (Ito and Kawauchi, 1995; Tzou, 1995; Loh et al., 2003; Loh and Holmes, 2005; Turner et al., 2011; Averous et al., 2015; de Bosio et al., 2016).

The direct voltage controller, shown in Fig. 4.1(a), can be considered as a coherent entity that generates the converter voltage reference based on the input reference and a set of measurements. To further elaborate, direct controllers comprise both those solely based on voltage feedback as well as those employing additional feedback signals, for example, to implement active damping or state-feedback control. The cascade controllers, shown in Fig. 4.1(b), have a clear hierarchical structure with the outer voltage controller providing the current controller a reference signal. In this chapter, the cascade controller is assumed to consist of an outer capacitor voltage loop and an inner converter current loop. The division between these two categories is not explicit as often times cascade voltage controllers can be represented as an equivalent direct voltage controller (He and Li, 2012; Geng et al., 2018). Due to the blurred line between these two conventional controller structures, the categorization of controllers in literature is typically based on the design methodology. Whereas the direct controllers are designed as a whole, the cascade controller design typically starts with the design of the current loop, followed by the design of the voltage loop.

Certain trade-offs exist in choosing between direct and cascade control structures for voltage control. Direct controllers can typically achieve higher bandwidths as compared to cascade controllers containing dynamics in the current controller. This is due to the dynamic coupling between the two control loops of a cascade controller, which imposes restrictions on the achievable bandwidth of the outer voltage control loop. Typically the bandwidth of the voltage control loop is to be selected several times lower in comparison to the current control loop (Jensen et al., 2000). Similar guidelines can also be found for cascade control structures in general (Harnefors et al., 2007). On the other hand, in the case of converter current being the controlled variable in the inner current control loop, the cascade controller structure offers inherent overcurrent protection through limitation of the inner current reference as depicted in Fig. 4.1(b). Another alternative is to

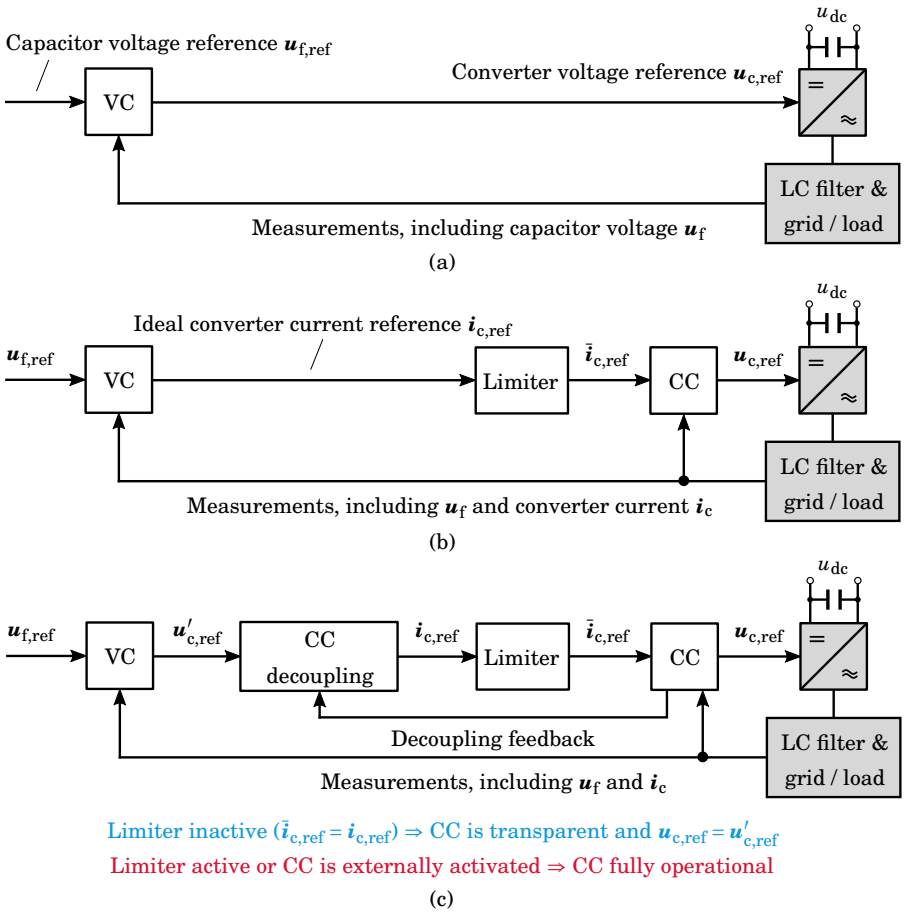

Figure 4.1. Different voltage controller structures: (a) direct, (b) cascade, and (c) presented multifunctional cascade control structure. VC stands for voltage controller and CC for current controller.

use capacitor current as the controlled variable. This improves the dynamic performance of the controller at the cost of lacking inherent overcurrent protection (Loh et al., 2003).

Overcurrent protection is an important, yet typically overlooked, aspect in the design of a voltage controller. The fault current levels of VSCs are restricted by the low thermal inertia of the semiconductor switches in the converter. Consequently, fast-acting overcurrent protection schemes are mandatory in practical converter systems. From the hardware point of view, tolerance to fault currents can be enhanced by overdimensioning the semiconductor switches and minimizing the saturation of filter inductors under high currents (Nuutinen et al., 2013). However, these approaches are often economically infeasible. While the simplest approach of dealing with overcurrent protection is to trip the converter upon overload detection (Nuutinen et al., 2013; Pérez-Estévez et al., 2020), standards and require-

ments in various different applications demand that the converter remains operational for short-lived faults. An example application that has gained large traction in the recent years is renewable energy production.

For grid converters, modern grid codes, such as the German VDE-AR-N-4110, require fault ride-through (FRT) capability of the converter (VDE-AR-N 4110, 2018). Thankfully, a rich collection of different overcurrent protection methods that keep the converter operational during overloading has developed during the recent decades. These methods can either be based on hardware (Chokhawala et al., 1995; Lu and Sharma, 2009; Nuutinen et al., 2013), software (Paquette and Divan, 2015; Bottrell and Green, 2014; Etemadi and Iravani, 2013), or their combination (Pei and Kang, 2012; Chen et al., 2018). In this chapter, software-based current-limiting methods are focused on due to their flexibility, economy, and efficiency. The majority of these methods can be categorized into current reference saturation methods and virtual-impedance-based methods.

4.2 Virtual-Impedance-Based Current Limiting

In essence, virtual impedance concept encompasses the manipulation of a controller voltage reference based on the measured current. Virtual impedance can be used to enhance several aspects related to control of converters. For example, it can be used to improve load sharing between converters (Guerrero et al., 2005), decrease the coupling between the control of active and reactive power (He and Li, 2011), improve disturbance rejection and system stability (Wang et al., 2015), and last, but not least, provide overcurrent protection (Paquette and Divan, 2015). As elaborated by Wang et al. (2015), several different control configurations exist for using a virtual impedance. Typically, the virtual impedance used for current limiting is implemented to adjust the capacitor voltage reference, that is, the voltage controller input reference, based on the measured load current, as shown in Fig. 4.2. The capacitor voltage reference could be a user-defined constant or determined, for example, by outer control loops. For an overview of various virtual impedance control configurations, the interested reader is referred to (Wang et al., 2015) and the references cited therein. The effect of adding a virtual impedance in accordance to Fig. 4.2 can be equivalently modeled by adding an additional impedance in series with the Thevenin equivalent circuit of the converter system, as shown in Fig. 4.3. In the figure, $\boldsymbol{G}_{\mathrm{cl}}$ is the reference-tracking transfer function from $\boldsymbol{u}_{\mathrm{f,ref}}$ to $\boldsymbol{u}_{\mathrm{f}}$, and $\boldsymbol{Z}_{\mathrm{o}}$ is the output impedance of the converter system, excluding the virtual impedance. The additional impedance, highlighted in red, depends on both the virtual impedance, as well as on the reference-tracking transfer function $\boldsymbol{G}_{\mathrm{cl}}$ (Wang et al., 2015).

While the concept of virtual impedance has existed for several decades al-

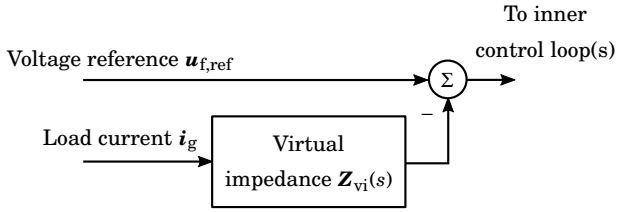

Figure 4.2. Inclusion of virtual impedance in the controller is realized through modification of the voltage reference $\boldsymbol{u}_{\mathrm{f,ref}}$ based on the measured load current $\boldsymbol{i}_{\mathrm{g}}$.

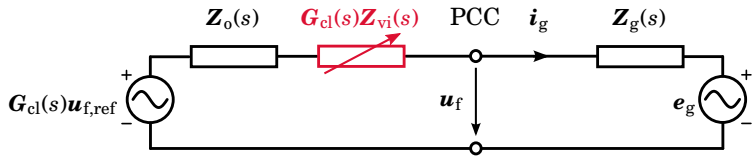

Figure 4.3. Equivalent circuit model of a grid-forming converter connected to an electric grid, where both the converter and the grid are represented by their Thevenin equivalent circuits.

ready, with one of the earliest applications in implementing active damping for the resonance of an LC filter (Middlebrook, 1987), one of the pioneering examples of using virtual impedance for current limiting is by Vilathgamuwa et al. (2006), in which an inductive-resistive virtual impedance was developed for a series-connected converter to limit the current between a microgrid and the utility grid. Since then, virtual impedance has been further developed and extensively used for overcurrent protection in converters (Salha et al., 2010; He and Li, 2011; Gkountaras et al., 2015; Paquette and Divan, 2015; Wang et al., 2015; Lu et al., 2018; Zarei et al., 2019; Qoria et al., 2020; Li et al., 2021; Zubiaga et al., 2021).

The prevailing approach of using virtual impedance for current limiting is based on activating the current-limiting virtual impedance only upon exceeding a predefined current threshold. This way it does not interfere with the normal operation of the converter and degrade its performance, since a constant voltage drop caused by additional impedance tends to significantly affect the reactive power sharing of parallel converters (Paquette and Divan, 2015). Typically, an inductive-resistive virtual impedance is used, and its design is a two-step process. The constant part that is used to enhance system characteristics, such as those mentioned at the beginning of the section, is designed first. Afterwards, the adaptive part of the impedance is designed according to the system properties and desired fault current levels.

The key advantages of virtual-impedance-based current limiting methods are their wide applicability, simplicity, and effectiveness under suitable conditions. As only the voltage reference input to the voltage controller is manipulated, the methods can easily be embedded into various different controllers, both of direct and cascade structures. The concept of virtual

impedance is especially enticing for VSCs operated as voltage sources, since it is desirable to maintain voltage-source behavior even during faults, which is enabled through the use of virtual impedance.

Alas, virtual-impedance-based current limiting methods are sensitive to the operating conditions (Nuutinen et al., 2013). In ideal conditions, the tuning of the virtual impedance should be based on the impedance seen by the converter during the fault (Vilathgamuwa et al., 2006). The tuning procedure by Paquette and Divan (2015) assumes a negligible impedance seen by the converter during faults, which can result in an overly conservative limiting behavior, leaving a part of the converter capacity unused during faults in which the impedance is non-negligible. Similarly, Lu et al. (2018) tunes the virtual impedance based on assumptions regarding the magnitude and angle of the impedance during faults. The full potential of the converter will remain unused if these assumptions are not valid. For more accurate tuning, an estimate of the impedance is desired, which increases the complexity of the approach. For example, the real-time grid impedance estimation method presented in Publication VI could be used. In addition, the response of the virtual impedance also depends on the dynamics of the inner control loops as observed from Fig. 4.3. This fact has been recognized in (Zarei et al., 2019), in which the overcurrent protection method is a combination of virtual impedance and current-reference limiting. Current-reference limiting is the first line of defense in the event of a fault due to its fast response. The virtual impedance, having a slower response, follows. A similar approach of combining virtual admittance and current reference limiting is presented by Plet and Green (2011) and Lin et al. (2019), in which the virtual admittance is used used to reduce distortion caused by unbalanced faults. Finally, a severe shortcoming of the virtual impedance concept is the lack of controllability of the currents during faults. Several of the modern grid codes require that the converters offer grid support, such as dynamic voltage support, during faults. Examples of such standards include VDE-AR-N 4110 (2018). Discussion related to provision of dynamic voltage support during faults can also be found from the recently revised IEEE 1547-2018 (2018) despite not being stated as being mandatory.

4.3 Current Reference Limiting

The concept of current reference limiting in voltage-controlled converters relies on the existence of a current control loop, since the fundamental idea is to limit the current reference to maintain the current levels within specified limits. Consequently, this method requires the controller to have a cascade structure shown in Fig. 4.1(b), in which the current reference limiter can be seen between the voltage and current controllers. There are two approaches for implementing current reference limiting, either

by using instantaneous saturation limit or latched limit (Bottrell and Green, 2014). In the instantaneous saturation limiter, the magnitude of the input reference is scaled down to remain within the hardware limits of the converter. In the latched limiter, the current reference is replaced with a predefined reference on detecting a fault that results in an overcurrent. Latched limit is especially useful in those cases in which the desired fault current differs from the regular supplied current. An example of this is the provision of grid support during faults in compliance with grid codes. The fault inception and clearance detection can be based on, for example, a combination of converter current reference and PCC voltage measurement (Bottrell and Green, 2014). As compared to the instantaneous saturation limiting, the inclusion of the fault detector in the latched limiter brings forth additional complexity and possible additional delay to the system. Moreover, latch-up can occur in latched limiting, during which the controller remains in limiting mode after the fault has been cleared due to the unsuccessful detection of fault clearance (Bottrell and Green, 2014). Comprehensive comparisons of the various different current reference limiters are presented by Bottrell and Green (2014) and Sadeghkhani et al. (2017).

An additional degree of freedom to the design of the current reference limiters is brought about by the choice of reference frame in which the limiting is carried out. The limiting can be carried out either in the natural (abc) (Plet et al., 2011; Mahamedi et al., 2020; Rosso et al., 2021), stationary ($\alpha\beta$) (Wei et al., 2019; Taul et al., 2020a), or synchronous (dq) (Brucoli et al., 2007; Plet et al., 2011; Gkountaras et al., 2015; Huang et al., 2019) reference frame. Furthermore, limiters based on positive- and negative-sequence component decomposition have also been employed (Taul et al., 2020b; Rosso et al., 2021). In the majority of existing literature, the same reference frame is used for the current reference limiter and the rest of the controller. Diverging from this majority, the current-limiting method presented by Zarei et al. (2019) uses a current reference limiter implemented in natural reference frame, while the rest of the controller operates in synchronous reference frame. Limiters operating in natural reference frame have the benefit of being inherently capable of properly limiting faults during both balanced and unbalanced faults. Consequently, excessive voltages are avoided in the unhealthy phases during unbalanced faults due to the individual limitation of each phase current. Additional measures have to be adopted in case of stationary and synchronous reference frame limiters to achieve matching performance under unbalanced faults, as demonstrated in (Rizo et al., 2015).

The reference signals in both natural and stationary reference frames are sinusoid by nature, and consequently, RMS-value based limiters are typically used to prevent signal clipping which occurs if the instantaneous value is limited instead. However, RMS-value based limiters introduce

additional complexity and delay to the system (Bottrell and Green, 2014; Sadeghkhani et al., 2017; Zarei et al., 2019). While fast RMS-value estimators exist, such as that used by Mahamedi et al. (2020), they are inherently more sensitive to noise as compared to the conventional quarter-cycle or half-cycle estimators due to their unfiltered derivative action. The synchronous reference frame limiters are free of RMS-value computation delay due to the fundamental-frequency positive-sequence signals being DC quantities in steady state.

Amongst the benefits of current reference limiting, one can appreciate the possibility of controlling the currents during times of overcurrent, which allows compliance with dynamic voltage support requirements of various grid codes. The current reference limiters are also efficient and simple in their implementation. Unlike the virtual impedance, current reference limiting does not require implementation of adaptive gains or load current measurement, and the current-limiting behavior does not significantly depend on the fault scenario.

On the other hand, as explicated in (Paquette and Divan, 2015; Huang et al., 2016; Xin et al., 2016), there are some issues related to current reference limiting, especially in VSCs operated as voltage sources in which the synchronization is based on the flow of active power. During faults, the voltage control loop and any additional outer control loops are fundamentally open. This can aggravate instability, especially in the synchronization loop. Since the discovery of these issues, remedies have been devised, such as those presented by Taul et al. (2020a) and Chen et al. (2020). In these methods, the outer loop references are modified during faults to prevent transient instability. Furthermore, the integrating states of the outer loop controllers can wind up during faults unless preventive actions are adopted. One could use various anti-windup mechanisms, such as those presented by Peng et al. (1996), or freeze the integrating states during faults to prevent the wind-up phenomenon.

4.4 Other Current-Limiting Methods

A host of other current-limiting methods have also emerged that do not clearly fall into the two abovementioned categories. One typical method is to alter the control structure upon fault detection to enable current-limiting capability (Nuutinen et al., 2013; Dong et al., 2016; Shuai et al., 2017; Piya et al., 2018). In (Nuutinen et al., 2013; Shuai et al., 2017), the whole voltage controller is replaced by a separate current controller. The challenges of such implementations lie in ensuring smooth transitions between the controllers as well as ensuring the stability of both controllers. Moreover, the need for detection mechanisms for the inception and clearance of the fault increase the overall complexity of the control system. In contrast, the

methods in (Dong et al., 2016; Piya et al., 2018) propose additions to the controller structure during faults to ensure proper limiting of the current. Another typical approach, especially suitable for direct voltage controllers, is to manipulate the converter voltage reference to limit the converter currents (Moon and Johnson, 1999; Etemadi and Iravani, 2013; Kim et al., 2019). In (Moon and Johnson, 1999), the converter voltage reference is reduced by using an additional coefficient which is obtained from a lookup table based on the converter current. In (Etemadi and Iravani, 2013; Kim et al., 2019), the converter current is predicted based on the model of the filter inductor, and limited accordingly. Hybrid hardware- and software-based limiting methods also exist, such as (Pei and Kang, 2012; Chen et al., 2018). In these methods, the initial overcurrent is reined in by using a hardware-based hysteresis controller that directly manipulates the gate driver signals output by the control algorithm. After the initial transient, the voltage controller is swapped to a current controller to yield less distorted current waveforms for the duration of the fault. Last, but not least, the designer has always the choice of forcing the converter to cease operation upon detecting a fault (Nuutinen et al., 2013; Pérez-Estévez et al., 2020).

4.5 Multifunctional Cascade Control Structure

The multifunctional cascade controller structure presented in Publication V renders the current reference limiting methods previously restricted to cascade controllers equally available to direct voltage controllers. The multifunctional cascade controller resembles the conventional cascade controller in structure. However, it contains a decoupling loop between the outer voltage and inner current loops, as shown in Fig. 4.1(c). Due to the existence of voltage and current control loops, operation in either voltage or current control mode is possible. In essence, the decoupling loop can be designed to render the current controller completely transparent to the voltage controller during operation in normal conditions. On the other hand, under fault conditions when the current needs to be limited, the current controller activates and takes over. The consequences of this result are twofold.

First, the presented structure enables overcurrent protection by seamless transition to current control mode in the event of a fault. Consequently, the presented structure allows for the integration of overcurrent protection methods based on current reference limiting, discussed in Section 4.3, to direct voltage control methods. This significantly expands the pool of overcurrent protection methods available for direct voltage controllers. The mode changes between voltage and current control mode can also be triggered by using an external signal.

Secondly, since the current controller does not affect the system dynamics under normal operation in voltage control mode, and vice versa, the design of voltage and current controllers can be done separately. As compared to conventional cascade controllers, in which the control loops are coupled by default, the proposed structure does not compromise in the performance of either control mode; for instance, both the voltage and current controller can be based on state-feedback control with comparable bandwidths as demonstrated in Publication V.

The combination of seamless transitions between control modes and decoupled design of the voltage and current controllers indicates that the presented structure could also find use in applications in which operation in both control modes is required. A timely example of such an application is that of the flexible inverter-interfaced generation required to be able to operate in both grid-connected and standalone mode (Teodorescu et al., 2004; Arafat et al., 2012; Dong et al., 2012; Liu et al., 2014; Kulkarni et al., 2017). Whilst the main challenges of enabling multifunctional operation of such converters lie elsewhere, such as, in ensuring transient-free reconnection to the grid (Ochs et al., 2014), the elimination of transient due to the controller alteration could be achieved by employing the presented multifunctional cascade control structure.

The restrictions imposed by the presented structure are few. The main requirement is related to the form of the current controller. Its open-loop transfer function from the current reference to the current controller output should be proper, but not strictly proper. This corresponds to the open-loop current controller transfer function including a static reference feedforward path. As with conventional cascade controller structures equipped with current reference limiting, one ought to avoid aggressive derivative action of the load current feedforward in the outer voltage loop, since this will induce significant chatter at the threshold of the current limit during overcurrent faults.

Approaches similar to the multifunctional cascade control structure have been adopted in (Mattavelli, 2005; Zhang et al., 2010; Harnefors et al., 2021). In these works, the inner current loop of a cascade controller is rendered transparent during normal operation. However, a static inner current loop is assumed, which greatly simplifies the task of rendering the current controller transparent. Furthermore, while the change of synchronization method upon mode changing was not addressed in Publication V, one could apply the approach, for example, as done in (Zhang et al., 2010) and change to a PLL on entering current control mode. Alternatively, as recently discussed in (Harnefors et al., 2021), a hybrid synchronization approach could be adopted, in which more than one synchronization method is implemented in parallel to establish the controller synchronous reference frame. While the detailed description of the presented multifunctional cascade control structure is found in Publication V, it is showcased below

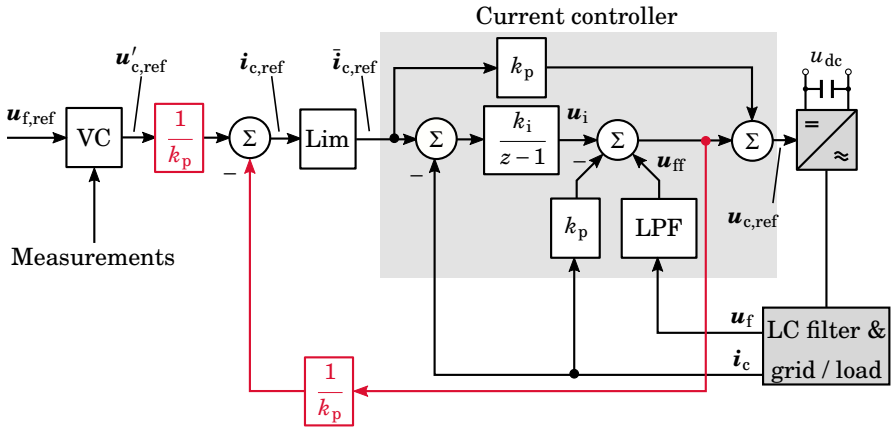

Figure 4.4. Block diagram of the example scenario in which a direct voltage controller is augmented with overcurrent protection by employing multifunctional cascade control structure. The current controller consists of a PI controller and a low-pass filtered capacitor voltage feedforward. LPF stands for low-pass filter and VC for voltage controller.

through an example.

Example Application of the Multifunctional Cascade Control Structure
In this section, a brief example of applying the multifunctional cascade controller structure on a direct voltage control scheme is presented. The focus is on providing overcurrent protection capability; thus, externally commanded control mode transitions are not considered. The control system is assumed to operate in synchronous reference frame, but the synchronization mechanism is omitted for simplicity. The voltage controller is not explicitly defined, but it could be, for example, the synchronverter presented by Zhong and Weiss (2011) or the state-feedback controller presented by Pérez-Estévez et al. (2020). A PI-type current controller with low-pass filtered capacitor voltage feedforward is selected as the current controller to provide overcurrent protection, which is defined by the control law

$$\boldsymbol{u}_{c,ref}(k) = k_p \bar{\boldsymbol{i}}_{c,ref}(k) - k_p \boldsymbol{i}_c(k) + \boldsymbol{u}_i(k) + \boldsymbol{u}_{ff}(k) \tag{4.1}$$

$$\boldsymbol{u}_i(k+1) = \boldsymbol{u}_i(k) + k_i \left(\bar{\boldsymbol{i}}_{c,ref}(k) - \boldsymbol{i}_c(k) \right) \tag{4.2}$$

$$\boldsymbol{u}_{ff}(k+1) = \mathrm{e}^{-\alpha_f T_s} \boldsymbol{u}_{ff}(k) + (1 - \mathrm{e}^{-\alpha_f T_s}) \boldsymbol{u}_f(k) \tag{4.3}$$

where $\bar{\boldsymbol{i}}_{c,ref}$ is the limited converter current reference, k_p is the proportional gain, k_i is the integral gain, and α_f is the bandwidth of the low-pass filter. Due to the presence of a proportional part of the error term in the controller, the requirement related to the existence of a static reference feedforward is satisfied.

In accordance with the results of Publication V, a block diagram of the control system is presented in Fig. 4.4. To render the current controller

transparent to the voltage controller during normal operation, the last three terms on the right-hand side of (4.1) are fed back to the input of the limiter through a decoupling gain, which is equal to the inverse of the static reference feedforward gain of the current controller. Similarly, the output of the voltage controller, $\boldsymbol{u}'_{\mathrm{c,ref}}$, is multiplied by the decoupling gain. In the following, the limiter is assumed to be inactive, that is, the ideal reference $\boldsymbol{i}_{\mathrm{c,ref}}$ equals the limited reference $\bar{\boldsymbol{i}}_{\mathrm{c,ref}}$. The equation for the converter voltage reference $\boldsymbol{u}_{\mathrm{c,ref}}$ can be written as

$$\boldsymbol{u}_{\mathrm{c,ref}}(k) = k_{\mathrm{p}}\boldsymbol{i}_{\mathrm{c,ref}}(k) - k_{\mathrm{p}}\boldsymbol{i}_{\mathrm{c}}(k) + \boldsymbol{u}_{\mathrm{i}}(k) + \boldsymbol{u}_{\mathrm{ff}}(k). \tag{4.4}$$

The current reference signal can then be expressed in accordance with Fig. 4.4 as

$$\boldsymbol{i}_{\mathrm{c,ref}}(k) = \frac{1}{k_{\mathrm{p}}}\left(\boldsymbol{u}'_{\mathrm{c,ref}}(k) - \boldsymbol{u}_{\mathrm{i}}(k) - \boldsymbol{u}_{\mathrm{ff}}(k)\right) + \boldsymbol{i}_{\mathrm{c}}(k). \tag{4.5}$$

Placing this into (4.4) yields

$$\begin{aligned}\boldsymbol{u}_{\mathrm{c,ref}}(k) &= k_{\mathrm{p}}\left[\frac{1}{k_{\mathrm{p}}}\left(\boldsymbol{u}'_{\mathrm{c,ref}}(k) - \boldsymbol{u}_{\mathrm{i}}(k) - \boldsymbol{u}_{\mathrm{ff}}(k)\right) + \boldsymbol{i}_{\mathrm{c}}(k)\right] - k_{\mathrm{p}}\boldsymbol{i}_{\mathrm{c}}(k) + \boldsymbol{u}_{\mathrm{i}}(k) + \boldsymbol{u}_{\mathrm{ff}}(k)\\ &= \boldsymbol{u}'_{\mathrm{c,ref}}(k).\end{aligned} \tag{4.6}$$

As can be seen from (4.6), the converter voltage reference $\boldsymbol{u}_{\mathrm{c,ref}}$ becomes equal to the voltage controller output $\boldsymbol{u}'_{\mathrm{c,ref}}$. Therefore, the current controller appears to be completely transparent during normal operation when the limiter is not active. On the contrary, if the current reference is limited, the transparency does not hold and the current controller takes over. Since the output of the voltage controller is scaled by the decoupling gain, the possible anti-windup mechanisms associated with the current reference limiter must be scaled analogously to compensate for the decoupling gain. However, no further alterations to the voltage controller are required.

5. Admittance Modeling

This chapter discusses admittance and impedance modeling methods for grid converters. First, a brief introduction to the applications of converter output admittance models is provided as motivation. Secondly, an introduction to the intersample admittance modeling method presented in Publication I is given. Lastly, its connections to the existing admittance modeling methods found in the literature are discussed. Since the admittance can also be represented as the inverse of the impedance, the results of this chapter naturally extend to the output impedance modeling of the converter.

5.1 Introduction to Converter Output Admittance

Converter output admittance, henceforth referred to as converter admittance, characterizes the behavior of the converter system as observed externally from the terminals of the converter. It has two primary areas of application: stability analysis and control design for stability enhancement.

The converter admittance can be used in stability analysis of the converter–grid interconnection together with the grid impedance, as eloquently presented by Sun (2011). This impedance-based stability analysis is based on formulating an equivalent circuit of the converter–grid system, as shown in Fig. 5.1, in which a partitioning into converter and grid subsystems is made. The converter is modeled as an ideal current source in parallel with its output admittance and the grid is modeled as an ideal voltage source in series with the grid impedance. The stability of such systems can then be analyzed by applying the Nyquist stability criterion presented, for example, in (Harnefors, 2007), or its generalized variant applicable to asymmetrical systems (MacFarlane and Postlethwaite, 1977).

The use of succinct representations for the externally observable behavior of these subsystems is beneficial. The foremost benefit is that detailed information regarding the converter or the grid is not necessarily required, since the grid impedance and converter admittance can be extracted from the

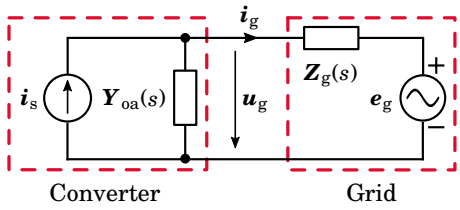

Figure 5.1. Linearized model of a three-phase grid-converter system connected to a grid. The converter is modeled as an ideal current source $\boldsymbol{i}_s$ in parallel with the output admittance $\boldsymbol{Y}_{oa}$ of the converter. The grid is modeled as an impedance $\boldsymbol{Z}_g$ in series with an ideal voltage source $\boldsymbol{e}_g$.

system by means of simulations or measurements. For example, the grid impedance could be estimated using the real-time identification method presented in Publication VI and the converter admittance could be estimated using the approach presented by Francis et al. (2011), as is done in Publication I. To avoid the practical challenges related to converter admittance measurement in synchronous reference frame, as elucidated in (Shen et al., 2013b; Gong et al., 2019a,b), one could also carry out the measurement in the stationary reference frame as in (Liao and Wang, 2020). Alternative methods to grid impedance and converter admittance estimation can be found in various works, such as, from (Cobreces et al., 2009; Roinila et al., 2014; Alves et al., 2019) and (Shen et al., 2013a; Fan and Miao, 2021), respectively. Moreover, as presented by Luhtala et al. (2018), one can even carry out the stability analysis in real time. One of the benefits of the impedance-based approach to stability analysis is that it provides information about the frequency region in which the potential stability problems lie, providing guidelines as to how one could reshape the admittance of the converter to achieve stability or to provide a sufficient stability margin.

An alternative approach to interconnection stability analysis is to formulate a state-space model of the whole system, and then analyze its eigenvalues. This approach yields more information as compared to the impedance-based analysis, as the sensitive modes in the system can be identified by using participation factor analysis (Verghese et al., 1982) and the dynamic behavior of the full system can be analyzed. However, the eigenvalue-based approach requires detailed information regarding both the grid and the converter. This is typically unrealistic due to the time- and frequency-varying nature of the grid impedance, as well as due to the strictly safeguarded control algorithms of commercial converters. Moreover, the whole system must be remodeled in the event of structural changes occuring in it, which is an arduous process. To alleviate this challenge, component connection method has been developed in which the system model is essentially created based on partitioning the system and formulating its model using the resulting subsystem models (Gaba et al., 1988). For

further comparison of the impedance- and eigenvalue-based methods to converter–grid interconnection stability analysis, the interested reader is referred to (Wang and Blaabjerg, 2019) among others.

Furthermore, the converter admittance may be used as one of the criteria in control design, which is typically referred to as admittance shaping (Harnefors et al., 2007; Wang et al., 2015; Harnefors et al., 2015; Pérez et al., 2017). In these approaches, the controller is designed to fulfill certain criteria related to the converter admittance based on the equivalent system model in Fig. 5.1. The ultimate of goal in such designs is to achieve passivity of the converter system, which imposes a specific set of conditions on the converter admittance that must be fulfilled (Brogliato et al., 2007). These conditions can be stated as follows: for a stable linear time-invariant system with a rational transfer function $\boldsymbol{Y}_{\mathrm{oa}}(s)$, the system is passive if the real part of $\boldsymbol{Y}_{\mathrm{oa}}(\mathrm{j}\omega)$ is nonnegative for all $\omega \in [-\infty, \infty]$, i.e., $\mathrm{Re}\{\boldsymbol{Y}_{\mathrm{oa}}(\mathrm{j}\omega)\} \geq 0 \ \forall \omega \in [-\infty, \infty]$. However, such complete passivity of a converter system is often difficult to achieve and compromises are required. If the converter system is passive, its feedback interconnection with another passive system will result in a passive system. Such interconnection appears in the equivalent system in Fig. 5.1.

In modeling the converter admittance, one needs to consider the domain of modeling. In the majority of cases, the modeling is carried out in either space vector or phase domain (Shah and Parsa, 2017). Moreover, the choice of reference frame for space vectors has a significant impact on the complexity of the resulting model if the converter system is asymmetrical in at least one of the reference frames (Harnefors, 2007). Asymmetrical systems cannot be represented using a single complex transfer function, but require either two complex transfer functions or a transfer function matrix (Harnefors, 2007; Harnefors et al., 2020). Asymmetry is introduced to the converter system, for example, by outer loop controllers such as the PLL and DC-bus voltage controller (Harnefors et al., 2016; Wang et al., 2018).

As mentioned in the introduction, the control algorithms of a modern converter system are implemented on a digital processor that executes difference equations in the discrete-time domain. On the other hand, the rest of the system operates in the continuous-time domain, resulting in a hybrid system. The interfaces between the two time domains are the sampler and hold as shown in Fig. 5.2 in which the sampler is depicted by a switch. The sampler is known to cause aliasing due to the frequency folding effect (Franklin et al., 1998). The hold circuit models the effects of realizing the converter voltage from its reference through PWM, which has also been shown to cause aliasing (Verghese and Thottuvelil, 1999), on top of emitting various frequency components in addition to the fundamental component (Holmes and Lipo, 2003). In the majority of admittance modeling methods, the nonlinear nature of the PWM is omitted from the model through

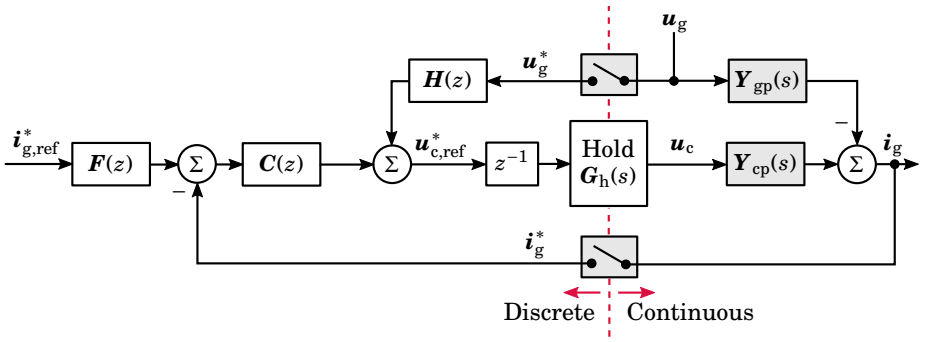

Figure 5.2. Block diagram of an example current-controlled system used to present the various admittance models appearing in this chapter.

the use of a switching-cycle-average model of the system (Yazdani and Iravani, 2010). However, detailed modeling of PWM behavior has also been considered, e.g., in (Holmes and Lipo, 2003; Mouton and Putzeys, 2012; du Toit Mouton et al., 2014; Liu et al., 2022).

5.2 Interface Models

To present both the interface models and the various admittance modeling methods introduced in the following sections, the current-controlled grid converter system shown in Fig. 5.2 is used as an example. In the figure, $\boldsymbol{F}$ is the reference prefilter, $\boldsymbol{C}$ is the feedback controller, $\boldsymbol{H}$ is the disturbance feedforward filter, and z^{-1} models the one-sample computational delay discussed in Section 2.3. The transfer function $\boldsymbol{G}_\mathrm{h}$ models the PWM process, and is further discussed below. The transfer functions $\boldsymbol{Y}_\mathrm{gp}$ and $\boldsymbol{Y}_\mathrm{cp}$ are the open-loop admittances of the filter that could be, for example, an L filter or an LCL filter. This particular system structure corresponds to the disturbance-feedfoward-based current controller presented in Publication VII and the small-signal model of the current control system including a PLL that was experimentally verified in Publication I. Nonetheless, before delving into the admittance models, the modeling of sampling and hold is briefly introduced.

Sampling

Practical sampling is implemented using analog-to-digital (A/D) converters that takes a continuous-time signal as an input and outputs a sequence of discrete pulses whose envelope is the input function, cf. Fig. 5.3. As the number of bits in an A/D converter is finite, a discrepancy between the input and the output value arises. This inaccuracy caused by the A/D conversion is often called the quantization error (Franklin et al., 1998). In this thesis, the number of bits used in the A/D conversion is assumed to be

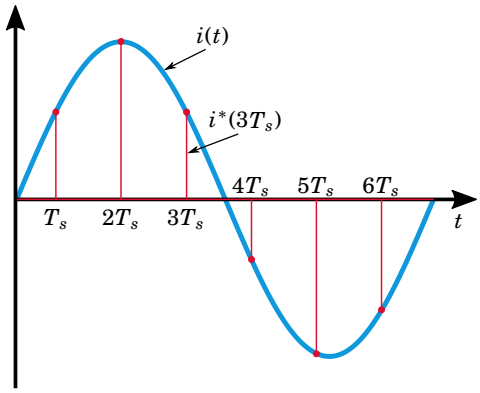

Figure 5.3. Visualization of the sampling operation. The blue line represents the input signal to the sampler, and the red line represents the sampled signal, modeled as a continuous-time signal comprising pulses at sampling instants enveloped by the input signal.

sufficiently high for the quantization error to be negligible. Under these assumptions, the output signal from the sampler is discrete in the time domain and it can obtain a continuous range of values. Such signals are referred to as sampled-data signals (Ogata, 1995).

In lieu of using sequences to represent the discrete-time signals, it is preferred to have a continuous-time function representation of the sampled signal for ease of continuous-time analysis. Consequently, the process of sampling is typically modeled as amplitude modulation of a carrier signal consisting of an infinite series of impulse functions, that is, Dirac delta functions δ, by the sampled signal. As a result, assuming a constant sampling period T_s, a sampled continuous-time signal $i(t)$ can be represented in the continuous-time domain as (Franklin et al., 1998)

$$i^*(t) = T_\mathrm{s} \sum_{k=0}^{\infty} i(t)\delta(t - kT_\mathrm{s}) \tag{5.1}$$

where the sampled nature of the signal is emphasized by the use of an asterisk in the superscript. This notation also applies to transfer functions. Scaling by T_s is done to match the unit of the sampled signal with the original signal. Furthermore, negative values of k are not considered since the signal $i(t)$ is assumed to vanish for negative t.

Application of the Laplace transform $\mathscr{L}\{\cdot\}$ on the sampled signal $i^*(t)$ yields the starred transform of the signal $i(t)$, that is, the frequency characteristics of the sampled version of the signal, as

$$i^*(s) = \mathscr{L}\{i^*(t)\} = T_\mathrm{s} \sum_{k=0}^{\infty} i(kT_\mathrm{s})\mathrm{e}^{-skT_\mathrm{s}}. \tag{5.2}$$

The above equation can be recognized as the one-sided Z-transform of the signal $i(t)$ with a change of variables $z = \exp(sT_\mathrm{s})$, which is scaled

by the sampling period T_s. Consequently, a relation between the starred transform and Z-transform is obtained as (Ragazzini and Zadeh, 1952)

$$i^*(s) = i(z)\big|_{z=\exp(sT_s)}. \tag{5.3}$$

An equivalent alternative representation of the starred transform (5.2) can be obtained by using the Poisson summation rule (Ragazzini and Zadeh, 1952), which yields

$$i^*(s) = \sum_{k=-\infty}^{\infty} i(s + jk\omega_s) \tag{5.4}$$

where $\omega_s = 2\pi/T_s$ is the sampling angular frequency. While the above derivation of the starred transform (5.4) relied on the concept of impulse modulation, one can arrive at the result without the use of impulse functions as in (Phillips et al., 1968).

The form (5.4) lends insight to the effects of sampling: the spectrum of the sampled signal becomes periodic with period equal to ω_s, i.e., $i^*(s) = i^*(s + \mathrm{j}k\omega_s)$ for every integer k. Consequently, a sampled version of a single-frequency input signal appears to have an infinite number of frequency components equally spaced by ω_s in the frequency spectrum. These new frequency components in the output signal are referred to as images of the original input frequency. If the newly-created images overlap with the frequency content of the input signal to the sampler, aliasing is said to occur since the frequency components become indistinguishable from one another based on the result (5.4). Consequently, one can observe that two single-frequency sinusoids cannot be distinguished from one another after sampling due to aliasing if their frequencies are separated by the multiple of ω_s. This is detrimental from control perspective, since high-frequency components such as noise can be aliased to the control bandwidth of the converter. To prevent this, low-pass filtering is typically implemented in conjunction with sampling. The additional filtering can be modeled as an additional transfer function in the measurement feedback path. Measurement filtering is considered in Publication I, but omitted here for the sake of simplicity.

Hold

The converter voltage reference fed to the PWM of the converter is typically maintained constant and equal to its value during the last update instant of the control algorithm in order to construct a continuous-time signal, cf. Fig. 5.4. If one assumes that the modulator can perfectly realize its input reference and that the harmonics injected by the modulator are disregarded, the effect of modulation can be neglected. Under these assumptions, the transformation from the converter voltage reference output by the controller to the realized converter voltage can be modeled by using

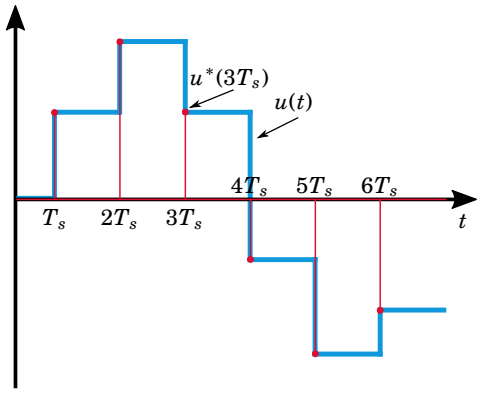

Figure 5.4. Visualization of the hold operation. The blue line represents the output signal from the hold, and the red line represents the sampled signal output by the controller, modeled as a continuous-time signal comprising pulses at the sampling instants.

the ZOH (Buso and Mattavelli, 2006)

$$\boldsymbol{G}_{\mathrm{h}}(s) = \frac{1 - \mathrm{e}^{-sT_{\mathrm{s}}}}{sT_{\mathrm{s}}} \tag{5.5}$$

Above, PWM nonlinearities such as minimum- and maximum-pulse limits and sidebands due to modulation were omitted for the sake of simplicity. Such effects can have a detrimental effect on the accuracy of the obtained admittance model, especially at higher frequencies. The accuracy of modeling PWM as ZOH has been studied in (Ma et al., 2018; Hans et al., 2019) with proposals to enhance the modeling accuracy. More accurate models for PWM have been devised, such as in de Sype et al. (2004) and Van de Sype et al. (2006). Even the effect of modulation sidebands has been augmented into the PWM model of a VSC in (San et al., 2020), which is supported by similar results previously obtained for DC-DC converters in (Li et al., 2018). Even though the aforementioned models that capture the PWM characteristics in a more detailed manner can be included in the presented intersample model by modifying $\boldsymbol{G}_{\mathrm{h}}$ to improve its accuracy, they are out of the scope of this thesis.

From the point of view of the intersample admittance modeling method presented in Publication I and exemplified below, it is relevant to examine the starred transform of the combination of hold $\boldsymbol{G}_{\mathrm{h}}$ and the open-loop admittance $\boldsymbol{Y}_{\mathrm{cp}}$ found in series in the example system of Fig. 5.2. The starred transform has such a property that components of the transformed function that are already periodic with ω_{s} can be factored out of the transformation. Thus, we can write the starred transform of $\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s)$ as

$$\left[\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s)\right]^* = (1 - \mathrm{e}^{-sT_{\mathrm{s}}}) \left[\frac{\boldsymbol{Y}_{\mathrm{cp}}(s)}{sT_{\mathrm{s}}}\right]^* \tag{5.6}$$

where $\left[\boldsymbol{Y}_{\mathrm{cp}}(s)/sT_{\mathrm{s}}\right]^*$ can be considered to be samples obtained from the unit step response of $\boldsymbol{Y}_{\mathrm{cp}}(s)/T_{\mathrm{s}}$. By applying the definition (5.2) together

with the change of variables (5.3), the result becomes equivalent to the step-invariant Z-transform of $\boldsymbol{Y}_{\mathrm{cp}}(s)$

$$\left[\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s)\right]^{*} = \boldsymbol{Y}_{\mathrm{cd}}(z) = (1-z^{-1})\mathcal{Z}\left\{\mathscr{L}^{-1}\left\{\frac{\boldsymbol{Y}_{\mathrm{cp}}(s)}{s}\right\}\Bigg|_{t=kT_{\mathrm{s}}}\right\} \tag{5.7}$$

where $\mathcal{Z}$ is the Z-transform and $\mathscr{L}^{-1}$ is the inverse Laplace transform.

5.3 Intersample Admittance Model

This section introduces the intersample modeling method presented in Publication I through derivation of the intersample admittance expression for the system in Fig. 5.2. The presented method is applicable for small-signal analysis, and consequently, the results should be interpreted in a small-signal sense. In accordance with Fig. 5.2, we can write

$$\boldsymbol{u}_{\mathrm{c}}(s) = \boldsymbol{G}_{\mathrm{h}}(s)z^{-1}\left[\boldsymbol{C}(z)\boldsymbol{F}(z)\boldsymbol{i}^{*}_{\mathrm{g,ref}}(s) - \boldsymbol{C}(z)\boldsymbol{i}^{*}_{\mathrm{g}}(s) + \boldsymbol{H}(z)\boldsymbol{u}^{*}_{\mathrm{g}}(s)\right] \tag{5.8}$$

$$\boldsymbol{i}_{\mathrm{g}}(s) = \boldsymbol{Y}_{\mathrm{cp}}(s)\boldsymbol{u}_{\mathrm{c}}(s) - \boldsymbol{Y}_{\mathrm{gp}}(s)\boldsymbol{u}_{\mathrm{g}}(s) \tag{5.9}$$

where the relation $z = \exp(sT_{\mathrm{s}})$ introduced in (5.3) is used to map the controller pulse-transfer functions into the Laplace domain. Defining the loop gain as

$$\boldsymbol{L}(s) = \boldsymbol{C}(z)z^{-1}\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s) \tag{5.10}$$

and placing (5.8) into (5.9) results in

$$\boldsymbol{i}_{\mathrm{g}}(s) = \boldsymbol{L}(s)\left[\boldsymbol{F}(z)\boldsymbol{i}^{*}_{\mathrm{g,ref}}(s) - \boldsymbol{i}^{*}_{\mathrm{g}}(s)\right] + \boldsymbol{Y}_{\mathrm{cp}}(s)\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{H}(z)z^{-1}\boldsymbol{u}^{*}_{\mathrm{g}}(s) - \boldsymbol{Y}_{\mathrm{gp}}(s)\boldsymbol{u}_{\mathrm{g}}(s) \tag{5.11}$$

where the current $\boldsymbol{i}_{\mathrm{g}}$ and the PCC voltage $\boldsymbol{u}_{\mathrm{g}}$ appear both in continuous and sampled form. The next step is to obtain an expression for $\boldsymbol{i}^{*}_{\mathrm{g}}$ by applying the starred transform on both sides of (5.11), which yields

$$\boldsymbol{i}^{*}_{\mathrm{g}}(s) = \frac{\boldsymbol{F}(z)\boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)\boldsymbol{i}^{*}_{\mathrm{g,ref}}(s) + \boldsymbol{H}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)\boldsymbol{u}^{*}_{\mathrm{g}}(s) - \left[\boldsymbol{Y}_{\mathrm{gp}}(s)\boldsymbol{u}_{\mathrm{g}}(s)\right]^{*}}{1 + \boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)} \tag{5.12}$$

that can be described as the closed-loop system seen by the digital controller. Placing (5.12) into (5.11) yields

$$\begin{aligned}\boldsymbol{i}_{\mathrm{g}}(s) = {} & \frac{\boldsymbol{F}(z)\boldsymbol{L}(s)}{1 + \boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)}\boldsymbol{i}^{*}_{\mathrm{g,ref}}(s) + \frac{\boldsymbol{H}(z)z^{-1}\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s)}{1 + \boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)}\boldsymbol{u}^{*}_{\mathrm{g}}(s) \\ & - \boldsymbol{Y}_{\mathrm{gp}}(s)\boldsymbol{u}_{\mathrm{g}}(s) + \frac{\boldsymbol{L}(s)}{1 + \boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)}\left[\boldsymbol{Y}_{\mathrm{gp}}(s)\boldsymbol{u}_{\mathrm{g}}(s)\right]^{*}.\end{aligned} \tag{5.13}$$

The last term on the right-hand side reveals an interesting property of the analyzed system. Since both $\boldsymbol{u}_{\mathrm{g}}$ and $\boldsymbol{Y}_{\mathrm{g}}$ are continuous by nature, neither of them can be factored out of the starred transform to simplify the expression. Consequently, this entanglement of the input signal and

system dynamic results in the system becoming time-variant (Franklin et al., 1998). For the purpose of solely examining the response excited by a single input frequency, this does not pose a problem. The identity (5.4) is then applied on the sampled PCC voltages on the right-hand side of the above equation (5.13), and the $k = 0$ components are separated from the rest of the sum. This results in

$$\begin{aligned}\boldsymbol{i}_{\mathrm{g}}(s) = {} & \frac{\boldsymbol{F}(z)\boldsymbol{L}(s)}{1+\boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)}\boldsymbol{i}^{*}_{\mathrm{g,ref}}(s) \\ & \underbrace{-\left[\boldsymbol{Y}_{\mathrm{gp}}(s) - \frac{\boldsymbol{H}(z)z^{-1}\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s) + \boldsymbol{L}(s)\boldsymbol{Y}_{\mathrm{gp}}(s)}{1+\boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)}\right]}_{\text{Output admittance } \boldsymbol{Y}_{\mathrm{oa}}(s)} \boldsymbol{u}_{\mathrm{g}}(s) \\ & \underbrace{+ \frac{\boldsymbol{H}(z)z^{-1}\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s)}{1+\boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)} \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} \boldsymbol{u}_{\mathrm{g}}(s+\mathrm{j}k\omega_{\mathrm{s}})}_{\text{Current component due to sampling nonlinearity}} \\ & \underbrace{+ \frac{\boldsymbol{L}(s)}{1+\boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)} \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} \boldsymbol{Y}_{\mathrm{gp}}(s+\mathrm{j}k\omega_{\mathrm{s}})\boldsymbol{u}_{\mathrm{g}}(s+\mathrm{j}k\omega_{\mathrm{s}})}_{\text{Current component due to sampling nonlinearity}}.\end{aligned} \tag{5.14}$$

The two infinite sums in (5.14) depict the effect of images created by sampling. The intersample output admittance $\boldsymbol{Y}_{\mathrm{oa}}(s)$ which describes the system dynamics from the PCC voltage $\boldsymbol{u}_{\mathrm{g}}$ to the grid current $\boldsymbol{i}_{\mathrm{g}}$ can then be obtained from the above equation as

$$\boldsymbol{Y}_{\mathrm{oa}}(s) = -\frac{\boldsymbol{i}_{\mathrm{g}}(s)}{\boldsymbol{u}_{\mathrm{g}}(s)} = \boldsymbol{Y}_{\mathrm{gp}}(s) - \frac{\boldsymbol{H}(z)z^{-1}\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s) + \boldsymbol{L}(s)\boldsymbol{Y}_{\mathrm{gp}}(s)}{1+\boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)} \tag{5.15}$$

in which one can observe the effect of the open-loop admittance in the first term. The second term describes the admittance-shaping effect of the control system, including the feedforward from the measured PCC voltage. Furthermore, one can use (5.14) to analyze the admittance of different images by examining individual terms of the sums that correspond to the image frequency of interest.

An equivalent form of (5.15) is presented in (Harnefors et al., 2017). Differing from the presented intersample model, the transfer function $\boldsymbol{Y}_{\mathrm{cd}}$ is represented by an infinite sum in the denominator of (5.15). The practical implementation of this infinite sum is not elaborated in (Harnefors et al., 2017). Nonetheless, one can surmise that the sum is approximated by truncating it to a set of low-order terms, for example, from −3 to 3, which has been a common approach in related works, such as (Linvill, 1951) and (Freijedo et al., 2019). In the intersample model, this sum is recognized as the step-invariant Z-transform of $\boldsymbol{Y}_{\mathrm{cp}}$ under the assumption of PWM being modeled as ZOH. Consequently, an exact and compact representation

for the denominator is obtained without the need for an approximation. Moreover, this result is not limited by the use of ZOH to model PWM, since a compact and exact representation for the starred transform of the product of $\boldsymbol{G}_{\mathrm{h}}$ and $\boldsymbol{Y}_{\mathrm{cp}}$ can also be obtained for other PWM models by using the Z-transform relation shown in (5.2) and (5.3).

A multiple-frequency admittance matrix model is presented in (Freijedo et al., 2019) that accounts for the nonlinearity of sampling. The modeling method yields an infinite-dimensional admittance matrix, which resembles a harmonic transfer function (Mollerstedt and Bernhardsson, 2000). Due to the practical challenges of implementing infinite dimensional matrices, the result is truncated to finite size. From the truncated representation, one can extract the output admittance as well as various admittances between the different coupled frequencies. However, due to diverging assumptions made during the modeling, this approach does not yield a model equivalent with the presented intersample admittance model. Nevertheless, one can formulate a harmonic transfer function in a similar manner to (Freijedo et al., 2019) which contains an equivalent model of the admittance (5.15).

Furthermore, a similar result is obtained in (Brown and Middlebrook, 1981) in which detailed modeling of switching behavior in converters was considered through the use of state-space modeling and under the assumption of constant-gain state-feedback control. Additionally, in contrast to the assumptions in the presented intersample admittance model, analog implementation of the control algorithm is assumed. On a related note, recent work focusing on the small-signal modeling of PWM can be found in (Yue et al., 2016; Yang et al., 2018; Tao et al., 2020; San et al., 2020). For example, a multi-frequency model for PWM is derived in (San et al., 2020). The model derivation is based on modeling duty cycle perturbations using Dirac delta functions. Consequently, the resulting structure of the small-signal PWM model strongly resembles the structure of the intersample admittance model (5.15). Similar multi-frequency matrix models of converters relying on the use of impulse modulation, that is, infinite series of Dirac delta functions, can be found in (Yue et al., 2016; Yang et al., 2018; Tao et al., 2020).

When dealing with models that are more complex as compared to their conventionally used counterparts, it is natural to wonder when do the benefits brought about by the more detailed model outweigh the additional labor required due to the increased complexity. To summarize the findings of Publication I, the difference between $\boldsymbol{Y}_{\mathrm{cp}}(s)\boldsymbol{G}_{\mathrm{h}}(s)$ and its starred transform largely dictates the effect of images. In essence, if the damping for frequencies approaching the Nyquist frequency, that is, one-half of the sampling frequency, and above it is low, significant aliasing can occur. This aliasing is not captured by the conventional models, deteriorating their accuracy. Further insight is offered by Braslavsky (1995), Remarks 5.2.2 and 5.2.3, in which a quantity is defined for evaluating the intersample activity

of the system. Analogously to the findings of Publication I, this measure of intersample activity only depends on the potential measurement filter, plant, and hold. In fact, a similar quantity is defined in (Goodwin and Salgado, 1994) for evaluating the relation of discrete-time complementary sensitivity function and its sampled-data equivalent, termed the reference gain function. An example of a system design for which the intersample modeling approach yields significant accuracy improvement can be found in (Tang et al., 2016), as elucidated in Publication I. Furthermore, another example of additional accuracy provided by the intersample model as compared to a discrete-time model is found in Publication VII.

5.4 Comparison with Conventional Admittance Models

Various conventional models typically found in the related literature can be extracted from the presentation of the intersample admittance modeling method, revealing the fundamental differences between the intersample model and the conventional models.

Single-Frequency Hybrid Admittance Model
A close approximation of the presented intersample model is obtained by disregarding the nonlinearity of sampling, that is, assuming that it does not generate any images. Consequently, $\boldsymbol{i}_{\mathrm{g}}^{*}(s) = \boldsymbol{i}_{\mathrm{g}}(s)$ and $\boldsymbol{u}_{\mathrm{g}}^{*}(s) = \boldsymbol{u}_{\mathrm{g}}(s)$ in Fig. 5.2. The resulting admittance model was coined the single-frequency model by Harnefors et al. (2017), and it can be expressed for the system of Fig. 5.2 as

$$\boldsymbol{Y}_{\mathrm{oa,h}}(s) = -\frac{\boldsymbol{i}_{\mathrm{g}}(s)}{\boldsymbol{u}_{\mathrm{g}}(s)} = \frac{\boldsymbol{Y}_{\mathrm{gp}}(s) - \boldsymbol{H}(z)z^{-1}\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s)}{1 + \boldsymbol{C}(z)z^{-1}\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s)} \tag{5.16}$$

where the change of variables $z = \exp(sT_{\mathrm{s}})$ introduced in (5.3) is employed. This model has been employed, for example, in (Kato et al., 2017) and (Awal et al., 2020).

Continuous-Time Admittance Model
The continuous-time admittance modeling approach is typically employed in conjunction with the design of $\boldsymbol{F}$, $\boldsymbol{C}$, and $\boldsymbol{H}$ carried out in the continuous-time Laplace domain with rational functions, that is, the discrete nature of the controller is disregarded. In such cases, the nonlinearity of sampling is invariably omitted and the hold interface may also appear as crudely approximated. Consequently, the one-sample computational delay z^{-1} in Fig. 5.2 is expressed using a transfer function $\boldsymbol{G}_{\mathrm{d}}$ that could either be the equivalent Laplace domain expression of the delay [cf. (5.3)] or an approximation thereof, for example, the Padé approximation (Buso and Mattavelli, 2006). Consequently, the continuous-time admittance model of

the system in Fig. 5.1 is given by

$$\boldsymbol{Y}_{\mathrm{oa,c}}(s) = -\frac{\boldsymbol{i}_{\mathrm{g}}(s)}{\boldsymbol{u}_{\mathrm{g}}(s)} = \frac{\boldsymbol{Y}_{\mathrm{gp}}(s) - \boldsymbol{H}(s)\boldsymbol{G}_{\mathrm{d}}(s)\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s)}{1 + \boldsymbol{C}(s)\boldsymbol{G}_{\mathrm{d}}(s)\boldsymbol{G}_{\mathrm{h}}(s)\boldsymbol{Y}_{\mathrm{cp}}(s)} \tag{5.17}$$

The abovementioned assumptions limit the general applicability of continuous-time models to the control bandwidth of the system, and thus, the main applications for such models are those of control design, such as in the passivity-based designs in (Harnefors et al., 2007, 2016). Other applications of the continuous-time model can be found, for example, in (Wang et al., 2014; Wen et al., 2016; Wang et al., 2018).

Discrete-Time Admittance Model

Another alternative to the continuous-time model is to model the physical plant as a discrete-time system, similarly to when the control design is carried out directly in the discrete-time domain, such as in (Kukkola et al., 2015). Consequently, all the inputs to the system are considered as discrete-time signals, including the PCC voltage $\boldsymbol{u}_{\mathrm{g}}$. As a result, the PCC voltage can be factored out from $\left[\boldsymbol{Y}_{\mathrm{gp}}(s)\boldsymbol{u}_{\mathrm{g}}(s)\right]^*$ which results in the traditional discrete-time pulse transfer function model. Consequently, the discrete-time output admittance of the converter can be obtained from (5.12) as

$$\boldsymbol{Y}_{\mathrm{oa,d}}(z) = -\frac{\boldsymbol{i}_{\mathrm{g}}(z)}{\boldsymbol{u}_{\mathrm{g}}(z)} = \frac{\boldsymbol{Y}_{\mathrm{gd}}(z) - \boldsymbol{H}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)}{1 + \boldsymbol{C}(z)z^{-1}\boldsymbol{Y}_{\mathrm{cd}}(z)} \tag{5.18}$$

where $\boldsymbol{Y}_{\mathrm{cd}}$ is the hold-equivalent discrete-time model of the open-loop admittance $\boldsymbol{Y}_{\mathrm{cp}}$ together with the one-sample computational delay, cf. (2.20). $\boldsymbol{Y}_{\mathrm{gd}}$ is a discretized model of the open-loop admittance $\boldsymbol{Y}_{\mathrm{gp}}$. The discrete-time admittance model describes the externally observed behavior of the converter as seen by the sampled voltage and current signals with sampling period T_{s}. Due to the loss of information arising from sampling in accordance with the sampling theorem (Proakis and Manolakis, 2006), the response observed by the converter does not coincide with the true response. Discrete-time admittance models are applied, for example, in (Wagner et al., 2014; Kukkola et al., 2015; Rodriguez-Diaz et al., 2019; Rahman et al., 2020).

Another alternative discrete-time method to evaluate the intersample behavior of the converter admittance is to employ the modified Z-transform (Franklin et al., 1998). In essence, the modified Z-transform can be used to obtain the system response based on samples obtained at time instants $kT_{\mathrm{s}} + mT_{\mathrm{s}}$, where k is an integer and $0 \leq m < 1$ is a constant. However, this approach is arduous to use due to the need to compute the system response for various values of m to obtain a comprehensive intersample response.

Summary

Having introduced the intersample model presented in Publication I and relating it to the existing state-of-the-art admittance models as well as

the conventional admittance models, a brief summary is in place. The intersample admittance modeling method provides means to accurately model the converter output admittance, including the hybrid nature of the converter system. In particular, the effect of sampling is included in detail. As compared to the closely related state-of-the-art admittance models proposed by Harnefors et al. (2017) and Freijedo et al. (2019), the intersample model offers a more compact, yet exact, representation without the use of approximations. Furthermore, the accuracy of the intersample model is higher than that of the conventionally used single-frequency, continuous-time, and discrete-time admittance models. In addition to its primary application of stability analysis, the intersample admittance model can also be used as a reference model for evaluating the accuracy of simulated or experimentally measured converter admittances as well as the conventional admittances that were shown to be approximations of the intersample admittance model.

6. Experimental Setup

This chapter provides a description of the experimental test setup used in the publications of this thesis. Furthermore, the implementation of the control algorithms on a dSPACE processor board is briefly discussed.

6.1 Setup Overview

Fig. 6.1 presents a block diagram of the experimental setup used to validate the results presented in the publications of this dissertation. The setup comprises two 12.5-kVA three-phase converters (ABB ACSM1) connected in a back-to-back configuration. Regarding the choice of filter, an LCL filter is used in Publications I-IV and VI, an LC filter is used in Publication V, and an L filter in Publications VII and VIII. The converter under test in the experimental setup can be connected to either a 400-V, 50-Hz grid, a 50-

Table 6.1. Nominal parameters of the 12.5-kVA converter system and the grid.

Parameter	Value	Value (p.u.)
Converter		
Rated current (peak)	$\sqrt{2} \cdot 18.3$ A	1
DC-link voltage	650 V	2
LCL filter		
Converter-side inductance	3.3 mH	0.082
Grid-side inductance	3.0 mH	0.075
Capacitance	8.8 µF	0.035
LC filter		
Inductance	2.8 mH	0.070
Capacitance	15 µF	0.060
L filter		
Inductance	5 mH	0.125
Grid		
Angular frequency	$2\pi \cdot 50$ rad/s	1
Voltage (phase-neutral, peak)	$\sqrt{2/3} \cdot 400$ V	1

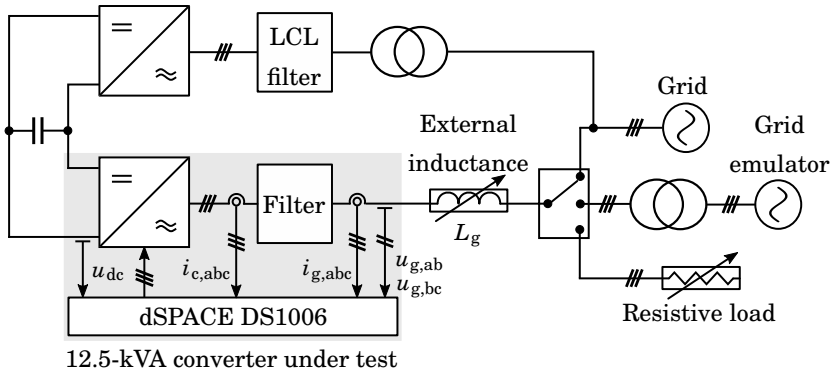

Figure 6.1. Block diagram presentation of the experimental setup. The available measurements are depicted in the figure, although not all of them are used at all times.

kVA four-quadrant three-phase grid emulator (Regatron TopCon TC.ACS), or to a passive resistive load. External inductors can be connected between the converter under test and the load at will. The load converter in the back-to-back configuration is used to regulate the voltage of the DC-bus. The parameters of the system are provided in Table 6.1. Photographs of the experimental setup are shown in Fig. 6.2.

6.2 Controller Implementation

The methods presented and employed in all of the publications were implemented using Matlab software, followed by a direct compilation into code compatible with dSPACE DS1006 processor board, and finally uploaded into the processor board. A proprietary interface board was used for passing the duty ratio signals from the dSPACE to the converter under test. The interface board also provides protective features, such as overvoltage and overcurrent protection. In addition, a deadtime of 2 µs is implemented in the interface board. Voltages and currents were measured using external closed-loop Hall-effect transducers by LEM. LEM LA 55-P were used as the current transducers, LEM LV 25-800 as the AC-voltage transducers, and LEM LV 25-1000 as the DC-voltage transducer. The transducers were mounted on proprietary measurement boards. Sampling and PWM were programmed to operate in synchronism.

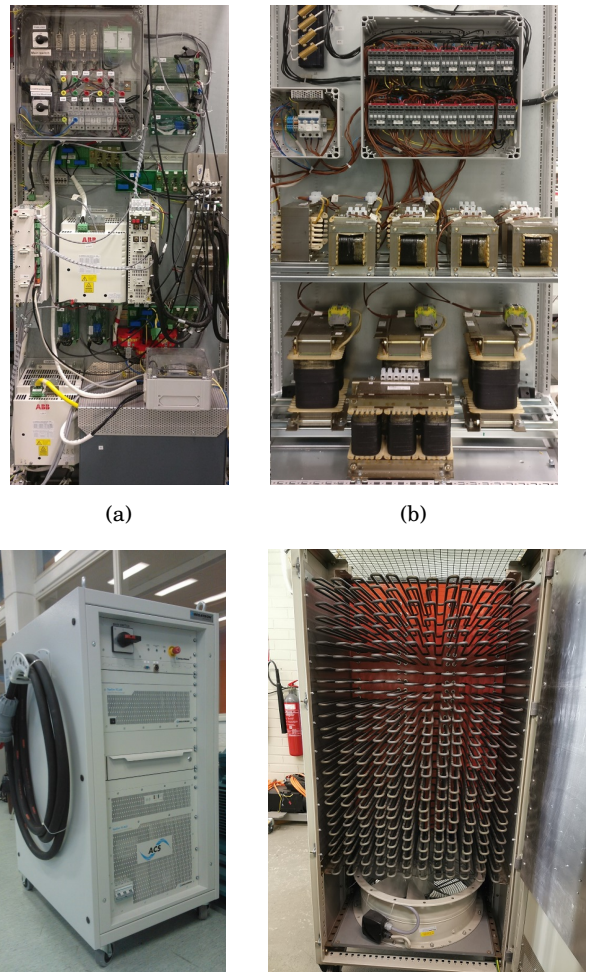

Figure 6.2. Photograph of (a) back-to-back converter setup with measurements; (b) external inductors for emulating different grid conditions; (c) grid emulator; and (d) resistive load used in Publication V.

7. Summaries of Publications

This chapter presents the abstracts of the publications and the scientific contributions of this thesis.

7.1 Abstracts

The abstracts of the publications are provided in this section.

Publication I

The stability of the converter-grid interconnection can be studied by analyzing the product of the converter output admittance and the grid impedance. For reliable stability analysis, it has been of interest to obtain accurate converter output admittance models for a wide range of frequencies, ideally also around and above the Nyquist frequency of the converter system. This article presents a modeling method for the output admittance of power converters defined in the Laplace domain that takes into account the discrete nature of the control system. The modeling method is based on analyzing the intersample behavior of sampled-data systems, a class of systems that includes the modern digitally controlled power converters. The proposed method is compared to conventional admittance modeling methods, and its accuracy is validated by means of simulations and experiments.

Publication II

This article presents a real-time identification method for LCL filters used with three-phase grid converters. The method can be applied to identify both the inductance and capacitance values of the filter and the series resistance seen by the converter. As a side-product, an estimate of the grid inductance seen from the point of connection is also obtained. A wideband excitation signal is added to the converter voltage reference. During the excitation, converter current and converter voltage reference samples

are used for identification. The samples are preprocessed in real time by removing DC biases and significant grid-frequency harmonics. Parameters of two discrete-time models are estimated at each sampling instant with a recursive estimation algorithm. Depending on the estimated model, the model parameter estimates are translated to either the resistance or the inductance and capacitance values of the system. The method can be embedded to a control system of pulsewidth-modulation-based converters in a plug-in manner. Only the DC-link voltage and converter currents need to be measured. Simulation and experimental results are presented for a 12.5-kVA grid converter system to evaluate the proposed method.

Publication III

This article deals with discrete-time state-space current control of three-phase converters equipped with an LCL filter. Either the converter or grid current is measured and the unknown states are estimated using a reduced-order observer. The stability and dynamic performance of the control designs based on these two current measurement options are compared by means of analysis and experiments at different sampling frequencies and under varying grid conditions, ranging from strong to very weak. Equal reference-tracking performance under nominal conditions is used as a basis for comparison between these two options. If a strong grid is assumed in the control tuning, the controller based on the grid current measurement (GCM) is found to be more robust against varying grid conditions in a wide range of sampling frequencies than the controller based on the converter current measurement (CCM). The CCM leads to better dynamic performance as compared to the GCM if the resonance frequency of the system falls below the critical resonance frequency.

Publication IV

This article deals with discrete-time state-space current controllers for three-phase grid converters equipped with an LCL filter. The integral action in the controller can be implemented either using an integrator or a disturbance observer. The results show that the disturbance-observer-based and integrator-based controllers become mathematically equal if the feedforward gains are selected to be equal, the feedforward zero is placed to cancel the pole originating from the integral action, and the closed-loop poles are placed identically. The equivalent performance in both designs is verified by means of analyses and experiments. The equivalence is also shown for double-frequency current controllers.

Publication V

This article proposes a multifunctional cascade controller structure for voltage-source converters. The proposed structure contains a decoupling loop between the outer voltage control loop and the inner current control loop, and operation in either voltage or current control mode is possible. In voltage control mode, the current controller can be made completely transparent. In the case of faults, the proposed structure enables inherent overcurrent protection by a seamless transition from voltage to current control mode, wherein the current controller is fully operational. Seamless transitions between the control modes can also be triggered with an external signal to adapt the converter to different operating conditions. The proposed structure allows for integration of simple, accurate, and flexible overcurrent protection to state-of-the-art single-loop voltage controllers without affecting voltage control properties under normal operation. The properties of the proposed controller structure are validated experimentally on a 10-kVA converter system.

Publication VI

This paper proposes a real-time method for estimating an unbalanced grid impedance using a three-phase converter. In the method, a periodic single-frequency or multi-frequency excitation signal is added to the converter voltage reference. The converter measures currents and voltages at the point of common coupling. The impedance estimate is obtained from the measurements using sliding discrete Fourier transform (SDFT). The method is experimentally validated.

Publication VII

This paper presents a comparison between integral action and disturbance feedforward in current control of grid converters. The current controllers are designed directly in the discrete-time domain with the objective of similar reference-tracking and disturbance-rejection performance under nominal conditions. Partial compensation of time delays is included in the controller designs. The analytically and experimentally compared properties, in addition to reference tracking and disturbance rejection, are noise sensitivity and robustness to grid impedance variations. The controllers are found to have comparable dynamic performance, although the realized disturbance-rejection performance of the integrator-based controller is slightly better. The disturbance-feedforward-based controller is found to be less susceptible to current measurement noise at the cost of having an additional entry point for noise through the voltage measurement. The integrator-based controller is found more robust to grid impedance

variations.

Publication VIII

This paper deals with positive- and negative-sequence current control of voltage-source converters. An enhanced weak-grid tolerant state-feedback controller design based on direct pole placement approach is proposed. The controller is synthesized from a body of literature on multi-frequency current control of grid converters. The resulting design yields consistent dynamic performance for varying grid strengths, and remains stable even under very weak grids. Due to the explicit parameterization of the pole locations, complex optimization methods often associated with robust control designs are avoided, which simplifies the controller design process.

7.2 Scientific Contributions

The main scientific contributions of this doctoral thesis are summarized as follows:

- Publication I proposes an intersample admittance modeling method which takes into account the hybrid nature of the converter system. The presented method improves the modeling accuracy of digitally controlled grid converters as compared to conventional modeling methods. Furthermore, the presented modeling method improves over the existing state-of-the-art methods by disposing of any infinite sums or infinite-dimensional matrices that need to be approximated in practice, replacing them with exact and compact representations.
- A multifunctional cascade control structure is presented in Publication V. The structure allows the embedding of a normally transparent inner current loop to direct AC-voltage controllers. Upon overcurrent fault conditions, the current loop activates and takes over, limiting the converter current. Furthermore, the proposed structure allows operation in both voltage and current control modes with seamless mode transitions as well as enables decoupled design of the voltage and current controllers.
- Mathematical equivalence of the integrator-based and disturbance-observer-based state-feedback current controllers is shown in Publication IV for grid converters. The equivalence is shown to also hold for the corresponding double-frequency controllers.
- Weak-grid tolerant state-feedback current control is advanced in Publications III and VIII. A thorough comparison of converter and grid current measurement options at different sampling frequencies

and varying grid strengths, ranging from strong to very weak, is given in Publication III for observer-based state-feedback current control of grid converters. A weak-grid tolerant direct pole-placement design is proposed in Publication VIII for positive- and negative-sequence state-feedback current control of grid converters, which tolerates a wide range of different grid strengths from strong to very weak.

- Real-time estimation methods for the filter and grid are formulated in Publications II and VI. The method in Publication II estimates the inductance and capacitance values of the LC or LCL filter elements, as well as the series resistance seen by the converter. The method in Publication VI estimates the elements of the grid impedance transfer function matrix. Both methods are embedded in the control system of the grid converter, and real-time execution is made feasible through the use of computationally efficient recursive methods.

8. Conclusions

The control system is a quintessential part of any VSC, including grid converters serving as power-electronic interfaces to several systems such as renewable energy sources. Modern VSCs are invariably equipped with digital processors that are responsible for executing the algorithms and functionalities to realize the desired behavior of the converter system. This thesis presented a wide-ranging array of methods related to the digital control of grid converters. The methods contained in this thesis can be roughly divided into three categories: control design, converter modeling, and identification. In all of these categories, the discrete-time nature of the control platform is taken into account. Furthermore, another unifying factor is the use of discrete-time state-feedback control methods. Such methods are based on the model of the controlled system, and consequently, knowledge of the model parameters is required. Typically, the nominal parameters of the filter in the converter system are known. However, in the case of an LC or LCL filter they could also be identified in real time by employing the method presented in Publication II. The presented method can also be used for condition monitoring of the filter.

Publications III, IV, VII, and VIII deal with current control of grid converters. In these methods, direct pole-placement approach to control design was employed. In the current control of LCL filters, either the converter or grid current can be used as the measured variable, and the rest of the filter states can be estimated using an observer, resulting in increased reliability of the system. In Publication III, a thorough comparison was carried out between the use of converter and grid current measurement in state-feedback current control of LCL filter for different sampling frequencies and grid strengths from the perspective of stability and dynamic performance. It was found that the grid current measurement tolerates weaker grids as compared to the converter current measurement under the assumption of a strong grid in control tuning. However, the dynamic performance obtained by using the converter current measurement is better than that obtained with the grid current measurement.

In Publication IV, two state-feedback current controllers with different

integral action implementations were compared. The first implementation is based on the use of an integrator and the second implementation on the use of a disturbance-signal estimator. Despite these two controllers displaying a seemingly different structure, a comparison of their closed-loop models reveals conditions under which the two systems become mathematically equivalent. The obtained result is also extended for the corresponding double-frequency current controllers. In general, the integrator-based implementation is more flexible due to the freedom of choosing the location of one of the reference-tracking zeros by suitable choice of the reference feedforward gain. On the other hand, the disturbance-observer-based design inherently includes an anti-windup mechanism, making it structurally simpler.

Similar to Publication IV, a comparison of low-pass filtered disturbance feedforward and integral action by means of an integrator was carried out for discrete-time current control of an L filter in Publication VII. Despite integral action being typically associated with error-free steady-state reference tracking and disturbance-feedforward with improving disturbance-rejection capabilities, these two controllers can be designed to yield nearly identical reference-tracking and disturbance-rejection properties. This result is in line with previous research related to similar continuous-time systems. However, the noise sensitivities of these two controllers are different and the realized disturbance rejection of the integrator-based design is found to be slightly better.

An enhanced weak-grid tolerant direct-pole placement design was presented in Publication VIII for positive- and negative-sequence current control of grid converters. The design was synthesized based on the existing body of literature on weak-grid tolerant pole placement designs obtained using indirect pole placement approaches, in which the controllers gains are obtained through optimization. The resulting pole-placement design avoids the use of any optimization methods and yields guaranteed stability in grids ranging from strong to very weak while simultaneously exhibiting good dynamic performance.

Having designed a control system for the grid converter, it is of significant interest to examine the interactions between the converter system and the grid. For this, one can apply the impedance-based stability analysis that requires knowledge of the converter output admittance. The control platforms of modern VSCs, that is, digital processors, execute difference equations in the discrete-time domain whilst the rest of the converter system operates in the continuous-time domain. Therefore, contrary to the popular approach of considering the converter system to completely operate in either the continuous- or the discrete-time domain, the converter system is actually a hybrid. A converter output admittance modeling method was presented in Publication I that includes this hybrid characteristic of the converter system. In particular, the focus was on integrating the

effects of sampling into the output admittance. The presented modeling method improves over the existing state-of-the-art models by disposing of the any infinite sums or infinite-dimensional matrices, replacing them with an exact and compact representation. Furthermore, an analysis of the system characteristics for which the intersample modeling methods can yield a considerable increase in accuracy was provided. In addition to the converter output admittance, the impedance-based converter–grid stability analysis requires knowledge of the grid impedance. Whilst the grid impedance is typically time- and frequency-varying by nature, it can be identified in real-time with the method presented in Publication VI.

A multifunctional cascade control structure was presented in Publication V. The structure renders the current reference limiting methods previously limited to cascade controllers equally available to direct AC-voltage controllers. An example of such a controller is the state-feedback AC-voltage controller recently studied in several publications. In essence, the multifunctional cascade control structure enables the addition of a normally transparent inner current loop to the controller. In the event of faults during which the current reference to the inner current loop exceeds its threshold value, the inner current loop loses its transparency and activates, seamlessly taking over to limit the converter current. The presented structure can also be used to manually transition between voltage and current control modes in a seamless manner, which can be used in converter systems that are required to flexibly operate as either voltage source or possess current source characteristics. In addition, the presented structure enables decoupled design of the current and voltage controllers.

The multifunctional cascade controller structure was presented in the framework of standalone voltage-source converter systems. However, its applicability is not limited to such systems. For instance, the multifunctional cascade control structure could be applied in the control of grid-forming converters that have been under intense research during the last years. Grid-forming converters include outer control loops, such as P-f and Q-V droops. These additional outer control loops need to be taken into account in order to prevent instability, for example, during fault scenarios where the multifunctional cascade controller transitions into current control mode. Furthermore, use of several synchronisation methods was not considered in presenting the proposed method. Especially from the point of view of grid-code compliance in grid-connected operation mode, it is of paramount importance to be able to provide dynamic support in the form of reactive power during faults. This task is simplified greatly by the use of an appropriate synchronisation method that decouples the control of active and reactive power. The challenges in implementing several synchronisation methods lie in proper implementation of synchronisation changeover during operating mode transitions. Therefore, an interesting avenue of research could be to examine the additional requirements for implementing

a switch of synchronisation method together with the presented structure. Moreover, the introduction of another synchronisation method, such as a PLL or P-f droop, brings a host of challenges related to system behavior and stability. Lastly, majority of faults in practical electric grids are not symmetrical by nature. In its current state, the multifunctional cascade control structure is not equipped to deal with asymmetrical faults. However, as mentioned in subsection 4.5, the limitations related to the choice of controllers are few. For instance, either of the double-frequency current controllers introduced in Chapter 3 could be employed in the multifunctional cascade control structure. Then, the extension of the control structure for double-frequency control schemes would entail the modification of the current reference limiter. Another future topic could be the addition of an observer to the weak-grid tolerant positive- and negative-sequence current controller presented in Publication VIII to reduce the number of sensors required to implement the design in converters equipped with LCL filters.

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Errata

Publication I

The open-loop admittances Y_{d} in (27) and (29) are missing a minus sign in both of their rational expressions.

The closed-loop admittance Y_{oa} in (18) is missing a minus sign in the rational expression $\frac{i_{\mathrm{o}}}{u_{\mathrm{g}}}$.

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