Publication [P6]

A 12-bit Ratio-Independent Algorithmic A/D Converter for a Capacitive Sensor Interface

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***Abstract*—This paper describes a ratio-independent algorithmic A/D converter architecture that is insensitive to capacitance ratio, amplifier offset voltage, amplifier input parasitics, and flicker noise. It requires only one differential amplifier, a dynamic latch, six capacitors, 36 switches, and some digital logic. The prototype 12-bit, 40-kS/s A/D converter with an active die area of 0.041 mm^2 is implemented in a 0.13-μm CMOS. The power dissipation is minimized using a dynamically biased operational amplifier. With a 68.4-μW power dissipation, the A/D converter achieves 80.2 dB spurious-free dynamic range (SFDR) and 63.3 dB signal-to-noise and distortion ratio (SNDR).**

***Index Terms*—Algorithmic A/D converter, ratio-independent, low-power, accelerometer, sensor.**

I. Introduction

With modern deep sub-micron CMOS processes, the cost-effective integration of a whole system-on-a-chip (SoC) has become feasible. The key requirements for battery-powered integrated sensor systems are extremely low power dissipation and material costs. Hence, for long stand-alone operation and cost-effective realization, minimizing power dissipation and silicon area are the main design targets.

A/D converters targeted for these kinds of applications with a medium resolution (8–12 bits) at sample rates up to hundreds of kilosamples per second have received attention recently [1], [2]. Such A/D converters can be used in applications that require a small die area and low power dissipation at the cost of reduced accuracy. Possible applications are, for example, sensors, toys, and different measurement and control systems.

Successive-approximation register (SAR) A/D converters are popular in low-power sensor systems [1], [2]. However, to keep the capacitor ratios accurate under process variations, the capacitors should be realized using unit capacitors [3]. The capacitor matching depends on their area [4]. Therefore, for accurate matching, the size of a unit capacitor cannot be small, resulting in a large silicon area. Also, at the system level, the preceding circuit stage and the voltage references have to be capable of driving the large capacitive load, resulting in increased power dissipation. To meet the stringent requirements for power dissipation and silicon area, an algorithmic A/D converter is an attractive choice. The benefits of algorithmic A/D converters at the system level are the low loading of the driving stage and the voltage references. Furthermore, if a capacitance ratio-independent algorithmic A/D converter is used [5], the matching requirements for the capacitors are relaxed, resulting in an even smaller capacitance area.

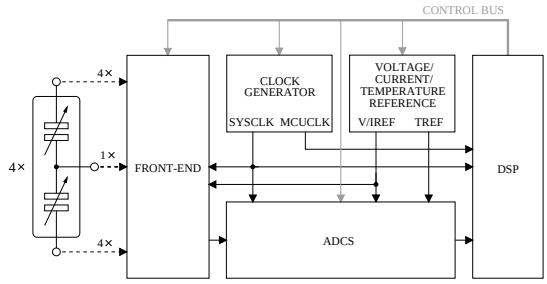

Fig. 1. Block diagram of a low-power interface for a three-axis capacitive microaccelerometer.

This paper presents an improved ratio-independent algorithm that eliminates the comparator required in [6], resulting in more area-efficient and robust implementation. The designed A/D converter [7] requires only one differential amplifier, a dynamic latch, six capacitors, 36 switches, and some digital logic. The A/D converter is integrated to a low-power interface for the three-axis capacitive microaccelerometer shown in Fig. 1 [8], [9]. The front-end converts the capacitive acceleration information to a voltage. Two A/D converters (ADCs) identical to the one considered in this paper convert the acceleration and temperature information to the digital domain. The clock generator provides the required clock signals (2 MHz SYSCLK, 1–50 MHz MCUCLK). The bandgap-based voltage, current, and temperature reference (V/I/TREF) provides all reference voltages and currents and temperature information. The off-chip digital signal processor (DSP) performs signal processing in the digital domain and controls the functioning of all the other parts of the system. Since the measured acceleration signals are at a very low frequency, or at dc, reducing offset voltage and flicker noise is critical. Hence, auto-zeroing techniques [10] are used in the designed A/D converter to remove offset voltage and flicker

Manuscript received October 15, 2007; revised December 1, 2007.

This work was supported by Nokia Research Center, VTI Technologies, and the Finnish Funding Agency for Technology and Innovation (TEKES).

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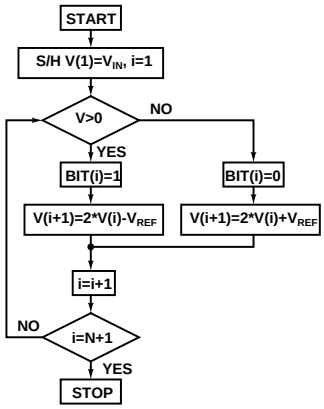

Fig. 2. Algorithmic A/D conversion principle.

noise.

The organization of the paper is as follows: Section II gives a short introduction to properties of algorithmic A/D converters. Section III gives an overview of the ratio-independent operation and circuits published in the literature. Section IV describes the designed ratio-independent operation. Section V describes the limitations and challenges in accurate A/D converter realization. Section VI describes the circuit implementation. The measurement results are presented in Section VII, and finally, conclusions are drawn in Section VIII.

II. Algorithmic A/D Converters

An algorithmic A/D converter uses the same hardware to perform the A/D conversion in successive cycles. Hence, it requires very little silicon area and is a suitable candidate for low-cost sensor applications. Furthermore, the algorithmic architecture makes it possible to use a variable sampling rate and resolution together with time-multiplexed sampling, and leads to low loading for the driving stage and voltage reference. The programmable duty cycle of the A/D converter and the voltage references allow the current consumption to be controlled more flexibly.

The algorithmic A/D converter is based on a binary search algorithm, which determines the closest digital word to match an input signal. The basic conversion flow of an algorithmic A/D converter is shown in Fig. 2. In every cycle, the signal is doubled and a positive or negative reference voltage is added according to (1).

$$V(i) = 2V(i-1) + (-1)^{BIT(i-1)}V_{REF}, \qquad (1)$$

where the number of cycle $i \in [2 \dots N]$, N is the resolution of the A/D conversion, $V(i)$ the signal on the ith cycle, $V(1) = V_{IN}$, V_{IN} the input signal, $BIT(i-1)$ the bit resolved on the previous cycle, and V_{REF} the reference voltage. The minimum conversion time for an algorithmic A/D converter is N cycles, where N is the resolution of the A/D converter. However, more than one clock phase is typically required to resolve one bit.

The most important factors limiting the accuracy of a switched-capacitor (SC) algorithmic A/D converter are noise, operational amplifier gain and bandwidth, switch nonidealities, and capacitor matching. In a straightforward implementation of an SC algorithmic A/D converter [11], the multiply-by-two operation depends on the capacitor ratios. Since the matching of on-chip elements is about 0.1% at best, the achievable accuracy is limited by the capacitor matching to 10 bits [4]. However, the accuracy can be improved by using a capacitance ratio-independent technique [5], which will be discussed next.

III. Ratio-Independent Operation

The operation of an algorithmic A/D converter requires a multiply-by-two operation. To relax the matching requirements, it is possible to implement an algorithmic A/D converter using a capacitance ratio-independent technique first proposed by Li et al. [5]. This technique makes the algorithmic A/D conversion independent of the capacitance ratios, which reduces the silicon area and makes it possible to implement an A/D converter of more than 10 bits without digital calibration. The total operation in [5] takes 6 clock phases to resolve one bit, two for sample-and-hold and four for ratio-independent multiply-by-two switching, and requires two amplifiers and a comparator.

Improvements to the traditional ratio-independent operation, such as reducing the required number of clock steps, relaxing the operational amplifier gain requirements, and increasing the accuracy have been proposed [12]–[18]. The designs presented in [12]–[16] all require two operational amplifiers and a comparator. The ratio-independent operation presented in [17] is suitable only for pipeline A/D converters and cannot be used as it is for algorithmic operation. The A/D converter presented in [18] uses pseudo-differential operation and requires two single-ended amplifiers, eight capacitors, and a comparator. The designed A/D converter presented here is fully differential and requires only one differential amplifier, a dynamic latch, six capacitors, 36 switches, and some digital logic.

IV. Implemented Ratio-Independent Operation

The operating phases of the implemented A/D converter are shown in Fig. 3. One-bit polarity is resolved in four clock steps. Thus, the total conversion time is $4{\cdot}N = 48$ clock steps, where the number of bits $N = 12$. Next, each phase of the operation is explained. Phases 1°– 4° constitute the most significant bit (MSB) cycle, and Phases 5°– 8° are recycled to resolve the rest of the bits.

In Phase 1°, the input signal V_{IN} is sampled and concurrently the amplifier offset voltage V_{OFF} is stored in capacitors C_1 and C_2, resulting in charges

$$Q^{1^\circ}_{C_1} = C_1(V_{OFF} - V_{IN}) \qquad (2)$$

and

$$Q^{1^\circ}_{C_2} = C_2 V_{OFF} \qquad (3)$$

in the respective capacitors. Thus, the total charge in Phase 1° is

$$Q^{1^\circ}_{tot} = C_1(V_{OFF} - V_{IN}) + C_2 V_{OFF}. \qquad (4)$$

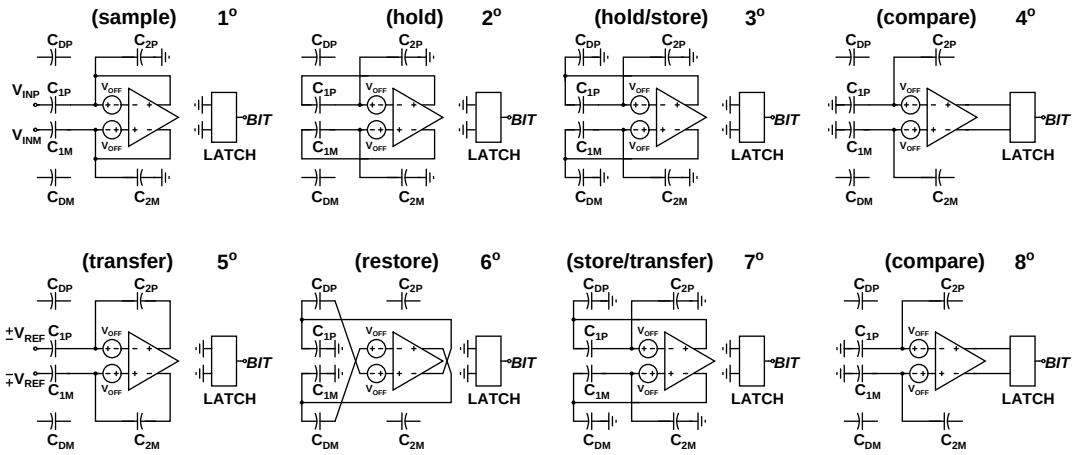

Fig. 3. A/D converter operating phases.

In the second phase, the amplifier is in hold mode. The total charge $Q_{tot}^{2^\circ}$ is

$$Q_{tot}^{2^\circ} = C_1(V_{OFF} - V_{OUT}) + C_2 V_{OFF}. \quad (5)$$

As a result of the charge conservation $Q_{tot}^{1^\circ} = Q_{tot}^{2^\circ}$, the resulting output voltage is

$$V_{OUT}^{2^\circ} = V_{IN}. \quad (6)$$

Hence, the amplifier offset voltage is canceled.

In Phase 3°, the amplifier is still in hold mode. The amplifier output voltage is now stored in capacitor C_D for the next cycle. The charge in capacitor C_D is

$$Q_{C_D}^{3^\circ} = -C_D V_{IN}. \quad (7)$$

Phase 3° could also have been combined with Phase 2°. The benefit of this would have been a marginal reduction of the conversion time. The drawback of the combination would have been much more complicated clocking. So, in order to keep the MSB cycle as similar as possible to the following cycles, four phases are used in the MSB cycle.

In Phase 4°, the amplifier is in open-loop configuration, and is used as a preamplifier to attenuate the kick-back transients from the following dynamic latch [19]. The bottom plate of capacitor C_2 is floating, so that the capacitor does not load the amplifier input. Capacitor C_D floats, and thus holds the sampled input signal. In Phase 4°, the charge in C_1 is

$$Q_{C_1}^{4^\circ} = C_1 V_X, \quad (8)$$

where V_X is the voltage on the top plate of capacitor C_1. Again, $Q_{C_1}^{1^\circ} = Q_{C_1}^{4^\circ}$, resulting in

$$V_X^{4^\circ} = V_{OFF} - V_{IN}. \quad (9)$$

It follows that the input voltage seen by the amplifier is

$$V_{INPUT}^{4^\circ} = V_X^{4^\circ} - V_{OFF}. \quad (10)$$

From (9) and (10), the amplifier input voltage is

$$V_{INPUT}^{4^\circ} = -V_{IN}. \quad (11)$$

From (11) it can be seen that the offset voltage at the amplifier input is canceled. In Phase 4°, the polarity of the sampled input voltage is resolved. The dynamic latch is connected to the amplifier output and the amplifier magnifies the differential input voltage so that it is larger than the dynamic latch offset voltage.

If there is parasitic capacitance C_P at the amplifier input, some of the charge stored in capacitor C_1 is transferred to this parasitic capacitance, reducing the amplifier input voltage by a factor of $C_1/(C_1 + C_P)$. The amplifier offset voltage is canceled since it is stored in capacitors C_1 and C_P in the previous phases. The reduction of the input voltage is not a problem if the amplifier is capable of resolving the input voltage difference correctly, since, in the following phase, the charge transferred to capacitor C_2 remains independent of the input parasitic capacitance of the amplifier. Hence, the noise level at the amplifier input has to be lower than the minimum resolved signal in order to make a correct decision.

Next, the operating phases 5°– 8° are described. These phases are recycled $(N-1)$ times for N-bit resolution. First, in Phase 5°, the charge in capacitor C_1 is

$$Q_{C_1}^{5^\circ} = C_1[V_{OFF} - (-1)^{BIT(i-1)}(-V_{REF})], \quad (12)$$

where $BIT(i-1)$ is the bit from the previous cycle and V_{REF} is the reference voltage. Since $Q_{C_1}^{1^\circ} + Q_{C_2}^{1^\circ} = Q_{C_1}^{5^\circ} + Q_{C_2}^{5^\circ}$, the charge $Q_{C_2}^{5^\circ}$ transferred to capacitor C_2 is

$$Q_{C_2}^{5^\circ} = C_2\{V_{OFF} - k[V_{IN} + (-1)^{BIT(i-1)}V_{REF}]\}, \quad (13)$$

where $k = C_1/C_2$. Now the amplifier output voltage is

$$V_{OUT}^{5^\circ} = V_{OFF} - Q_{C_2}^{5^\circ}/C_2 = k[V_{IN} + (-1)^{BIT(i-1)}V_{REF}]. \quad (14)$$

It should be noted that in this phase, the desired output voltage is still distorted by the factor k.

In Phase 6°, charge $Q_{C_1}^{1^\circ}$ is restored in capacitor C_1. This is accomplished using offset polarity reversing [17], [20]. The polarity of the offset voltage is changed by cross-connecting

the differential amplifier inputs and outputs during this step. In Phase 6°, the charge in capacitor C_D is

$$Q^{6^\circ}_{C_D} = C_D(-V_{OFF} - V^{6^\circ}_{OUT}). \tag{15}$$

The charges from (7) and (15) are equal ($Q^{3^\circ}_{C_D} = Q^{6^\circ}_{C_D}$), and the amplifier output voltage is

$$V^{6^\circ}_{OUT} = V_{IN} - V_{OFF}, \tag{16}$$

and the charge

$$Q^{6^\circ}_{C_1} = C_1(-V^{6^\circ}_{OUT}) = C_1(V_{OFF} - V_{IN}) = Q^{1^\circ}_{C_1}. \tag{17}$$

Thus, the charge $Q^{1^\circ}_{C_1}$ is restored in capacitor C_1. The capacitor C_2 floats, and hence $Q^{6^\circ}_{C_2} = Q^{5^\circ}_{C_2}$.

Phase 7° is identical to Phase 3°. In Phase 7°, the charge $Q^{5^\circ}_{C_2} = Q^{6^\circ}_{C_2}$ from (13) is transferred back from capacitor C_2 to capacitor C_1. In Phase 7°, the charge in capacitor C_2 is

$$Q^{7^\circ}_{C_2} = C_2 V_{OFF}. \tag{18}$$

As a result of the charge conservation $Q^{6^\circ}_{C_1} + Q^{6^\circ}_{C_2} = Q^{7^\circ}_{C_1} + Q^{7^\circ}_{C_2}$, it follows that

$$Q^{7^\circ}_{C_1} = C_1(V_{OFF} - V_{IN}) - C_1[V_{IN} + (-1)^{BIT(i-1)}V_{REF}], \tag{19}$$

resulting in an output voltage of

$$V^{7^\circ}_{OUT} = V_{OFF} - Q^{7^\circ}_{C_1}/C_1 = 2V_{IN} + (-1)^{BIT(i-1)}V_{REF}. \tag{20}$$

Thus, the output voltage is independent of the capacitance ratio k and amplifier offset voltage V_{OFF}, and is equal to the ideal output shown in (1). As a consequence, the operation is also independent of amplifier input parasitic capacitances and flicker noise. Finally, the output voltage $V^{7^\circ}_{OUT}$ is stored in capacitor C_D for the next cycle.

Phase 8° is identical to Phase 4°. In Phase 8°, the polarity of the output voltage $V^{7^\circ}_{OUT}$ is resolved for the next cycle. Phases 5°– 8° are then recycled to resolve the desired number of bits.

V. Error Sources in A/D Converter Operation

In the previous discussion of ratio-independent operation, the only non-idealities taken into account are capacitance mismatch and the operational amplifier input-referred offset voltage. However, in the practical implementation of an A/D converter, the following error sources also have to be considered:

1) Operational amplifier finite gain and settling accuracy.
2) Signal-dependent charge injection from MOS switches.
3) Signal-dependent MOS switch on-resistance.
4) Thermal and flicker noise

Next, the effects of these error sources are discussed.

A. Operational Amplifier Gain and Settling Requirements

Since the algorithmic A/D converter operates in consecutive cycles, in which the output depends on the output of the previous cycle, the conversion errors caused by finite operational amplifier gain and incomplete settling cumulate during the conversion and determine the achievable conversion

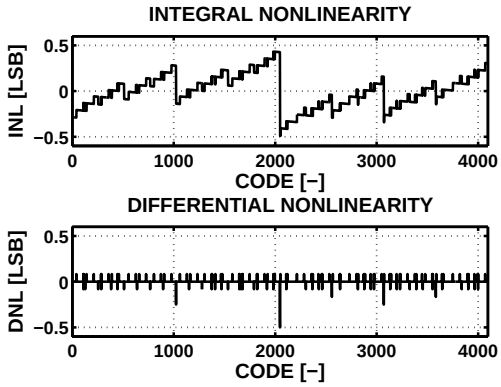

Fig. 4. MATLAB simulation of INL and DNL using 12-bit accuracy. k=2, V_{OFF}=100 mV, and A=80 dB.

accuracy. Next, the accuracy of ratio-independent operation shown in Fig. 3, with finite operational amplifier gain and settling taken into account, is discussed. The accuracy of the MSB cycle is determined by the output voltage in Phase 3°. The output voltage of the first cycle, taking into account the finite operational amplifier gain A, is

$$V(1) = \frac{1}{1 + \frac{1}{A} + \frac{1}{kA}} V_{IN} + \frac{\frac{k+1}{A+1}}{\frac{A+1}{A}k + \frac{1}{A}} V_{OFF}, \tag{21}$$

where $k = C_1/C_2$ is the capacitor ratio. When $A \to \infty$, the output voltage $V(1) = V_{IN}$.

The accuracy of the following cycles (2-N) is determined by the output voltage in Phase 7°. Neglecting the higher-order terms $(1/A)^2$, the resulting output voltage can be expressed as

$$V(i) \approx \frac{\left(2k + \frac{k^2}{A} + \frac{4k}{A} + \frac{1}{A}\right) V(i-1)}{k + \frac{k^2}{A} + \frac{3k}{A} + \frac{1}{A}} + \frac{\left(k + \frac{2k}{A}\right)(-1)^{BIT(i-1)} V_{REF} + \frac{k}{A} V_{OFF}}{k + \frac{k^2}{A} + \frac{3k}{A} + \frac{1}{A}}. \tag{22}$$

When $A \to \infty$, the output voltage is equal to the ideal output shown in (1).

Assuming that the operational amplifier settling accuracy is limited by dc gain, to keep the calculated integral nonlinearity (INL) and differential nonlinearity (DNL) below $\pm 1/2$ least significant bit (LSB), the required dc gains for 10- and 12-bit accuracies are 68 dB and 80 dB, respectively. With these gains, the error remains within $\pm 1/2$ LSB up to capacitor ratios of $k = 2$ and an amplifier offset voltage V_{OFF} of hundreds of millivolts, as shown for 12-bit accuracy in Fig. 4. The gain requirement does not decrease significantly even with smaller values of k or V_{OFF}. Transistor-level simulations give similar results. It should be noted that the requirements for settling accuracy are equal to the gain requirements.

Even though the operation is insensitive to capacitance mismatches, large mismatches between differential branches give rise to harmonic distortion. Fortunately, the matching of differential branches is not critical and drawing the layout for

the differential capacitors in common-centroid ensures that the impact of harmonic distortion on the overall performance as a result of the mismatches is negligible.

B. Signal-Dependent Charge Injection

MOS switch transistors have a significant non-ideality called charge injection [21]. When a MOS switch transistor is turned off, unwanted charges are injected into the circuit. The charge injection is mainly caused by the charge stored in the channel region flowing out to the source and drain areas. For an n-channel MOS transistor operating in the linear region, the channel charge is given by

$$Q_{ch} = -WLC_{ox}(V_{GS} - V_{tn}), \tag{23}$$

where C_{ox} is the transistor gate oxide capacitance, V_{GS} is the transistor gate-source voltage, V_{tn} is the n-channel MOS transistor threshold voltage and W and L are the transistor gate width and length, respectively. As can be seen from (23), the channel charge depends on the signal through the voltage V_{GS}. In order to keep the charge signal-independent, V_{GS} should be kept constant.

The charge injection can be either canceled or made signal-independent by using several well-known techniques. Charge injection can be canceled by using half-sized dummy switches with their drain and source terminals short-circuited and clocked at the opposite clock phase compared to the sampling switch. A similar effect happens when using CMOS switches, where the charges from equally sized n-channel MOS (NMOS) and p-channel MOS (PMOS) switch transistors cancel each other. The drawback of both of these methods is that they both rely on the matching of different transistor parameters and on the accurate timing of the gate control clock edges.

An efficient way to make the charge injection signal-independent is bottom plate sampling [19], where switches connected to ground or virtual ground are opened first. The charge injection caused by these switches is constant, since the switches are always connected to a fixed voltage. The resulting constant charge injection can be made common-mode by using differential structures and suppressed by the common-mode rejection of the operational amplifier.

C. Signal-Dependent On-Resistance

The NMOS transistor on-resistance operating in the linear region is given by

$$R_{ON} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})}, \tag{24}$$

where μ_n is the NMOS transistor carrier mobility. As can be seen from (24), the MOS switch on-resistance depends on the signal through the voltage V_{GS}, which causes harmonic distortion when tracking continuous time signals. Fortunately, the signal dependency can be relaxed to meet the requirements for 12-bit accuracy by using a CMOS switch that consists of parallel NMOS and PMOS transistors. Therefore, all switches handling full-scale signals are implemented as CMOS switches.

D. Thermal and Flicker Noise in Algorithmic A/D Converters

The sampling in SC circuits generates noise, which degrades the performance. There are two important noise sources: thermal and flicker noise. The effect of flicker noise can be reduced by increasing the area of the MOS transistor and, for example, by using auto-zeroing, chopper stabilization or correlated double-sampling techniques [10]. In this design, the flicker noise is reduced to a negligible level by using a ratio-independent structure that utilizes auto-zeroing, and therefore this noise analysis concentrates on the effect of thermal noise and how it should be taken into account in device sizing. Since an algorithmic A/D converter operates in consecutive cycles, each cycle increases the total noise contribution. Fortunately, the signal is doubled in every cycle, so the input-referred rms noise voltage resulting from each cycle decreases as $2^{-(i-1)}$, where i is the number of the cycle. The analysis presented here uses the principles described in [22].

There are two thermal noise sources in SC circuits: noise from the switches and the operational amplifier noise. In this analysis, it is assumed that a single-stage operational amplifier is used and that the settling time is limited by the operational amplifier, not by the sampling switches, resulting in the condition $R_{ON} \ll 1/g_m$, where the resistance R_{ON} models the finite on-resistance of the MOS switch transistor, as defined in (24), and g_m is the transconductance of the single-stage operational amplifier. Thus, the noise bandwidth is always determined by the operational amplifier, and it therefore dominates the thermal noise contribution in each phase. The noise contribution of analog ground or reference voltages is assumed to be negligible. All capacitor values are assumed to be equal, which is the case in the designed A/D converter. The capacitor value is denoted with C in the following equations. These calculations are carried out for a single-ended circuit. For a differential circuit, the noise contribution should be doubled.

In Phase 1°, the operational amplifier is connected to the top plates of the capacitors C_1 and C_2. The thermal noise sampled to capacitors C_1 and C_2 in Phase 1° is given by

$$\overline{v^2_{1^\circ,C_{1,2}}} = \frac{16kT/3g_m}{4 \cdot 2C/g_m} = \frac{2}{3}\frac{kT}{C}, \tag{25}$$

where k is the Boltzmann constant and T is the absolute temperature.

In Phase 2°, the thermal noise sampled to capacitor C_2 in Phase 1° is now transferred to capacitor C_1. Because the noise in both capacitors originates from the same source, they are fully correlated. Therefore, their amplitudes are summed, and the resulting thermal noise in capacitor C_1 is

$$\overline{v^2_{2^\circ,C_1}} = \left(\sqrt{\overline{v^2_{1^\circ,C_1}}} + \sqrt{\overline{v^2_{1^\circ,C_2}}}\right)^2 = \frac{8}{3}\frac{kT}{C}. \tag{26}$$

In Phase 3°, the equivalent load capacitance seen by the amplifier is $3C$. Thus, the thermal noise sampled into capacitors C_1 and C_2 is

$$\overline{v^2_{3^\circ,C_{1,2}}} = \frac{16kT/3g_m}{4 \cdot 3C/g_m} = \frac{4}{9}\frac{kT}{C}. \tag{27}$$

In C_1, this noise is added to the noise already sampled into the capacitor in Phase 2°.

In Phase 4°, no noise is sampled to capacitor C_1, since the only low impedance node is the ground node. However, the input-referred noise of the operational amplifier working as a preamplifier can cause an additional error when resolving the bit polarity. In the present implementation, this error source can be neglected.

The total noise contribution of the MSB cycle in capacitor C_1 is therefore

$$\begin{aligned}\overline{v_{MSB,C_1}^2} &= \overline{v_{2^\circ,C_1}^2} + \overline{v_{3^\circ,C_1}^2} \\ &= \frac{8}{3}\frac{kT}{C} + \frac{4}{9}\frac{kT}{C} = \frac{28}{9}\frac{kT}{C}.\end{aligned} \tag{28}$$

Next, the thermal noise contribution of the following cycles is discussed. The thermal noise sampled to capacitors C_1 and C_2 in Phase 5° is equal to

$$\overline{v_{5^\circ,C_{1,2}}^2} = \frac{16kT/3g_m}{4 \cdot C/g_m} = \frac{4}{3}\frac{kT}{C}. \tag{29}$$

In Phase 6°, the thermal noise sampled to capacitor C_1 is given by

$$\overline{v_{6^\circ,C_1}^2} = \frac{16kT/3g_m}{4 \cdot C/g_m} = \frac{4}{3}\frac{kT}{C}. \tag{30}$$

The thermal noise in Phase 7° is equal to that in Phase 3°, and is given by

$$\overline{v_{7^\circ,C_{1,2}}^2} = \frac{16kT/3g_m}{4 \cdot 3C/g_m} = \frac{4}{9}\frac{kT}{C}. \tag{31}$$

As discussed above for Phase 4°, no thermal noise is sampled in Phase 8°, either. The total noise contribution of the cycles 2-N to capacitor C_1 is given by

$$\begin{aligned}\overline{v_{2-N,C_1}^2} &= \overline{v_{5^\circ,C_1}^2} + \overline{v_{6^\circ,C_1}^2} + \overline{v_{7^\circ,C_1}^2} \\ &= \frac{4}{3}\frac{kT}{C} + \frac{4}{3}\frac{kT}{C} + \frac{4}{9}\frac{kT}{C} = \frac{28}{9}\frac{kT}{C}.\end{aligned} \tag{32}$$

The total thermal noise contribution through a whole conversion can be calculated by summing the squares of the input-referred noise voltages. This results in

$$\overline{v_{tot}^2} = \overline{v_{MSB,C_1}^2} + \left(\frac{\overline{v_{2-N,C_1}}}{2}\right)^2 + \left(\frac{\overline{v_{2-N,C_1}}}{2^2}\right)^2 + \cdots. \tag{33}$$

Hence, the total thermal noise contribution is

$$\overline{v_{tot}^2} = \frac{37.333}{9}\frac{kT}{C} \approx 4.15 \cdot \frac{kT}{C}. \tag{34}$$

For a differential circuit, the thermal noise power given in (34) is doubled, and the achievable signal-to-noise ratio with a 2.2 $V_{pp,diff}$ full-scale input signal, differential reference voltages of ± 0.55 V, and 2 pF capacitors is 75.5 dB, taking into account only the thermal noise. When the quantization noise power for 12 bits is summed with the thermal noise power, the achievable accuracy is 71.7 dB, resulting in an effective number of bits (ENOB) of ~ 11.6 bits.

VI. Circuit Implementation

The schematic of the designed A/D converter and the clock phases that drive the switches are shown in Fig. 5. The A/D converter requires four non-overlapping clock phases. In addition, there is a clock signal that indicates whether the current cycle is the first cycle (MSB) or one of the following cycles (2-N). These clock signals can be combined to achieve the desired clock signals using simple digital logic. The switches are minimum-length switches in order to minimize charge injection. Furthermore, the switches connected to the amplifier inputs are opened first in order to make the charge injection signal-independent, as discussed earlier. All the switches connected to the amplifier inputs or to ground are implemented as NMOS switches. Switches connected to amplifier outputs are implemented as CMOS switches. All six capacitors are metal-insulator-metal (MIM) capacitors, 2 pF each.

A. Operational Amplifier

The operational amplifier (opamp) accounts for a major part of the total current consumption of the A/D converter. Therefore, its power dissipation has to be minimized, but at the same time, care must be taken that the performance is not compromised. In SC circuits, opamps are used to transfer charges between capacitors within a clock cycle. The accuracy of the charge transfer is defined as the settling accuracy S, which is the relative error of the output voltage V_{out} at the end of the settling period compared to the ideal output voltage $V_{out,ideal}$, or

$$S = \left|\frac{V_{out}(T_s) - V_{out,ideal}}{V_{out,ideal}}\right|, \tag{35}$$

where T_s denotes the length of the settling period. The settling accuracy is often given in bits b, in which case $S = 2^{-b}$. For example, for 12-bit accuracy, $S = 2^{-12} \approx 244 \cdot 10^{-6}$. Both the dc gain A and the gain-bandwidth product GBW (defined as $GBW = A \cdot p_1$, where p_1 is the dominant pole frequency) of an opamp affect the achievable settling accuracy, in such a way that A defines the maximum accuracy than can be reached when $t \to \infty$ and GBW defines the settling speed. Additionally, if the maximum achievable accuracy $1/A$ is close to the target accuracy S, then the dc gain also affects the settling speed. However, the difference between $1/A$ and S has to be very small to have any significant effect. For example, when $A = 3 \cdot S^{-1}$ (giving a margin of approximately 10 dB), the settling to a given accuracy is less than 3% longer than in the ideal case. Thus, this effect can be disregarded in a practical case. If the opamp is modeled as a single-pole system, the required GBW for a given settling accuracy S is given by

$$GBW = -\frac{\ln S}{\beta T_s}, \tag{36}$$

where β is the feedback factor of the closed-loop system.

If the opamp is modeled with a more accurate two-pole model, the fastest possible settling without overshoot or ringing can be obtained when the system is critically damped. In

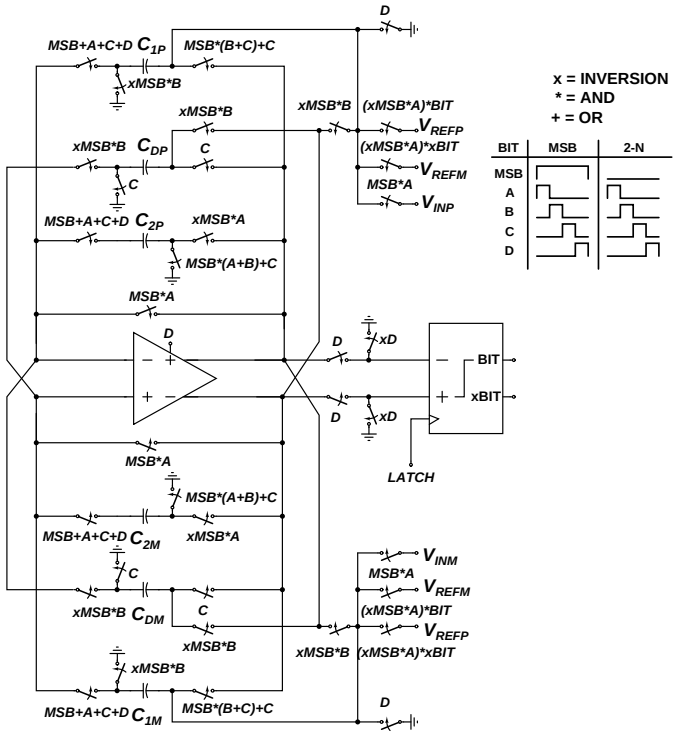

Fig. 5. Schematic of the A/D converter.

this case, the nondominant pole frequency p_2 is four times the GBW multiplied by the feedback factor β, that is,

$$p_2 = 4 \cdot \beta \cdot GBW = 4 \cdot \beta \cdot A \cdot p_1, \tag{37}$$

Under this condition, the phase margin of the amplifier is 76.0°.

The s-domain transfer function of a critically-damped second-order system is

$$H(s) = \frac{G\omega_n^2}{s^2 + 2\omega_n s + \omega_n^2}, \tag{38}$$

where G is the low-frequency gain and ω_n the critical (cut-off) frequency. By now taking an inverse Laplace transformation of this, the relative settling error in a critically damped system can be written as

$$e^{-\omega_n t} + \omega_n t e^{-\omega_n t}, \tag{39}$$

with ω_n defined as [23]

$$\omega_n = \sqrt{p_1 p_2 (1 + \beta A)}. \tag{40}$$

Using (37), ω_n can be written as

$$\omega_n = \sqrt{p_1 \cdot 4 \cdot \beta \cdot A \cdot p_1 (1 + \beta A)} \approx 2 \cdot \beta \cdot GBW, \tag{41}$$

with $\beta A \gg 1$.

If the required settling accuracy is S and the settling time is T_s, the minimum GBW requirement can now be solved from

$$e^{-2 \cdot \beta \cdot GBW \cdot T_s} + 2 \cdot \beta \cdot GBW \cdot T_s \cdot e^{-2 \cdot \beta \cdot GBW \cdot T_s} = S. \tag{42}$$

This equation cannot be solved for GBW in a closed form. However, the required GBW as a function of β, S, and T_s can be calculated using numerical methods. If a settling accuracy of $b = 13.3$ is required (corresponding to the 80-dB requirement derived earlier), then a relationship $\beta \cdot GBW \cdot T_s = 5.883$ can be achieved. By observing Fig. 3, the minimum β during the operation can be found to be equal to 0.5. If T_s is taken to be 0.5 μs, then the GBW has to be at least 3.7 MHz to achieve the aforementioned settling accuracy. Thus, the GBW is approximately 1.9 times the clock frequency. For comparison, if single-pole settling is assumed, then the GBW requirement is equal to 5.9 MHz (from (36)), which is 1.6 times more than that achieved assuming two-pole settling.

Unfortunately, with traditional opamp design where amplifying stages are biased with a constant current (the so-called Class A biasing), the limited maximum slew rate of one of the stages (typically the first stage in a multistage opamp) creates a more stringent requirement for the GBW. As a general rule of thumb, the GBW is set to be approximately seven times the clock frequency. This means that the actual GBW in the example case is approximately four times the optimum GBW, leading to an increased current consumption.

The current consumption of an opamp can be considerably lowered if the slew rate limitation can be overcome. This leads to the so-called dynamically biased (Class AB biased) opamps. In dynamic biasing, the biasing current of the opamp is controlled on the basis of the differential input signal.

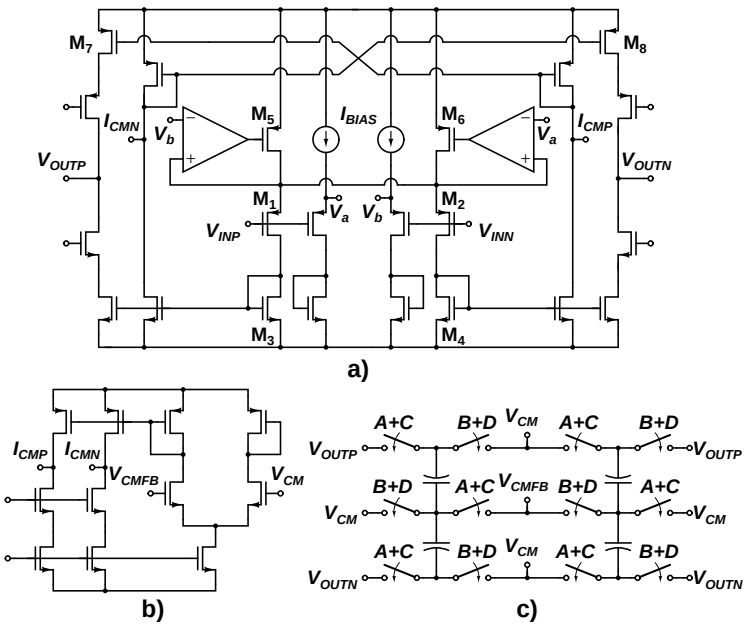

Fig. 6. Schematic of the tail-current boosted Class AB operational amplifier. a) Opamp, b) CMFB buffer, c) SC CMFB circuit.

When there is a large differential input signal present, the current is increased to speed up the settling. Hence, no slew rate limitation occurs, and the GBW requirement is relaxed. As the settling proceeds, the input voltage decreases and the biasing current is reduced. The biasing current needs only to be kept at a level that provides enough GBW for an adequate small-signal performance. In addition to the relaxed GBW requirement, the decreased static biasing current makes the design for a high dc gain easier, which is an important factor in algorithmic A/D converters.

For the reasons mentioned above, a tail-current boosted Class AB operational amplifier, shown in Fig. 6 [24], is used in the design. The original design is improved to a fully differential form with a double-sampling SC common-mode feedback (CMFB) circuit. An inverting CMFB buffer is designed to control low-impedance diode branches. This way, the dc gain is not degraded. A constant bias current I_{bias} is used to bias the replica of the input pair, which generates reference voltages for the internal amplifiers. Unlike the original design, in order to reduce static current consumption and to increase the dc gain, the current I_{bias} is bypassed to a dummy diode load. To maximize the current efficiency g_m/I_D, the differential input pair M_1–M_2 is operated in weak inversion. The internal single-ended amplifiers are implemented using a basic differential pair with a current-mirror load. Cascode transistors are added to the output stage to further increase gain. With a 1.8-V supply, the amplifier differential peak-to-peak output voltage swing is over 2.2 V. When the amplifier is used as a comparator in Phases 4° and 8° in Fig. 3, tail-current boosting is disabled by replacing the dynamically controlled current sources M_5–M_6 with a static current source.

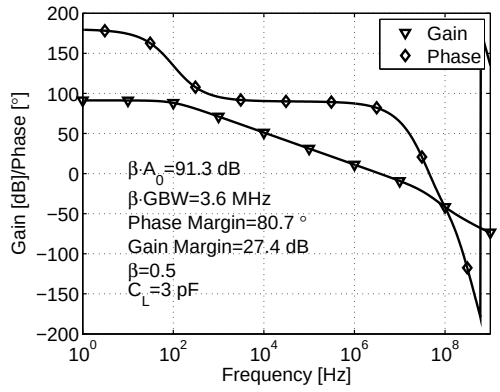

Fig. 7. Simulated small-signal performance (gain and phase) of the opamp.

The simulated small-signal performance of the opamp is shown in Fig. 7. The simulation is performed under the worst-case loading condition (Phases 3° and 7° in Fig. 3), using the configuration shown in Fig. 8. This configuration takes the GBW and A reduction resulting from β into account and accurately shows the gain and phase response of the whole feedback loop. The simulated input-referred noise of the opamp in the same configuration is shown in Fig. 9.

Fig. 10 shows the simulated transient response of the amplifier. It represents the operation in Phases 5°– 7°, when the differential voltage in C_{1P} and C_{1M} (and also in C_{DP} and C_{DM}) at the end of the previous cycle is -0.2 V. This is

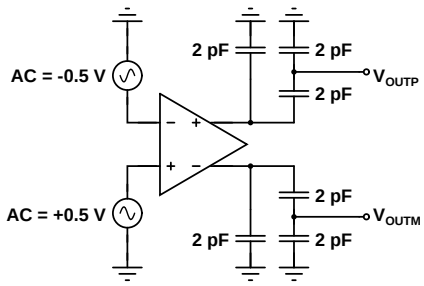

Fig. 8. Schematic of the configuration used in the simulation of the small-signal performance.

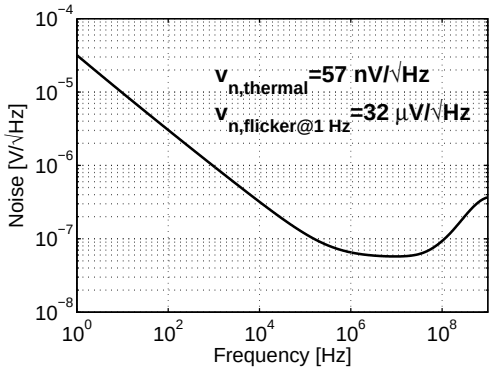

Fig. 9. Simulated input-referred noise of the opamp.

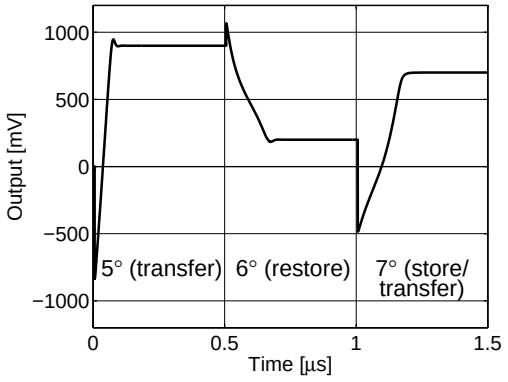

Fig. 10. Simulated transient response of the opamp.

multiplied by two and a differential reference voltage of 1.1 V is added to it. The resulting output voltage of $+0.7$ V is stored into the capacitors at the end of Phase 7°. From the figure, the operation of the dynamic biasing can be clearly seen. The Phase 7° can also be identified to represent the worst-case loading condition, as the settling is slowest.

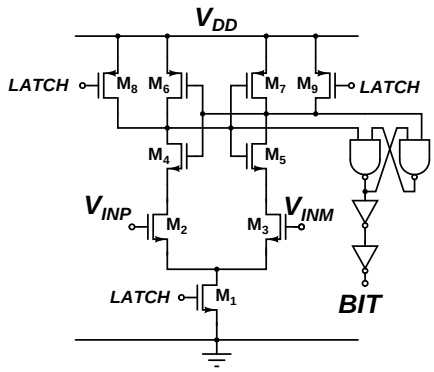

Fig. 11. Schematic of the dynamic latch.

B. Dynamic Latch

The designed dynamic latched comparator shown in Fig. 11 does not consume any static power and thus is well suited to low-power applications [25]. The area of the input transistors M_2–M_3 is large $(160\ \mu m/1\ \mu m)$ in order to reduce the dynamic latch offset resulting from the V_t mismatch below 1 mV [26]. Furthermore, the large gate capacitances of the input transistors are exploited in the compensation of the common-mode feedback loop of the amplifier in Phases 4° and 8°.

In the reset phase, the PMOS switch transistors M_8 and M_9 pull the comparator outputs to the supply voltage. The current through the NMOS input pair M_2–M_3 is prevented with the NMOS switch transistor M_1. When the comparator is latched, the two back-to-back inverters formed by the transistors M_4–M_7 rapidly generate full-scale digital levels at the outputs. After the regeneration phase, the positive and negative outputs are at the supply voltages and no static current flow occurs. Hence, the power efficiency is maximized. However, the drawback of the dynamic latched comparator is a large kick-back noise. This results from the fact that when the comparator is latched, the drain voltages of M_2–M_3 vary between supply voltages and the large transients are coupled to the input through the gate-drain capacitances. In addition, the input transistors change the operating region from the cut-off to the active region when the comparator is latched. There are different techniques to reduce the effect of the kick-back noise. The most popular one is to use a preamplifier which attenuates the kick-back transients entering the driving circuitry [19]. The preamplifier with offset voltage cancellation is used in this design. However, it should be noted that preamplification with offset voltage cancellation requires no additional hardware, only one extra clock step.

VII. Measurement Results

The prototype A/D converter is fabricated in a 0.13-μm CMOS technology. Fig. 12 shows a microphotograph of the A/D converter and the location of different blocks. The active chip area is 0.041 mm^2 and it draws 38 μA at 40 kS/s from a 1.8-V supply. To characterize only the A/D converter

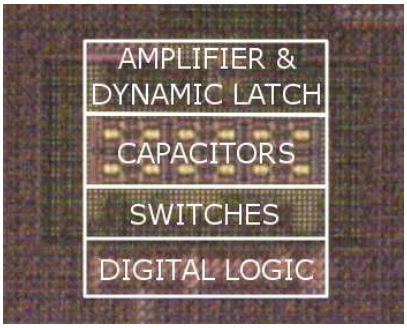

Fig. 12. A/D converter microphotograph.

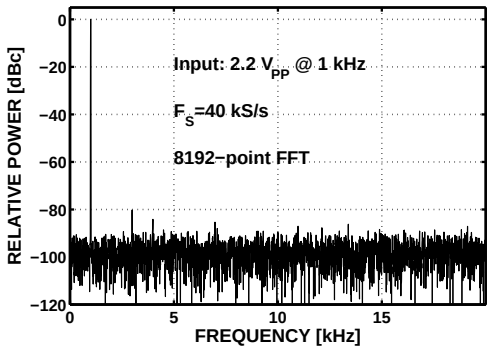

Fig. 13. Measured output spectrum.

performance, the measurements were made using an external clock signal, external reference voltages, and external bias current. The performance of the whole system has been published in [8], [9]. Fig. 13 shows the measured 8192-point FFT plot for a full-scale 1-kHz sinusoidal input signal. The measured SNDR=63.3 dB and SFDR=80.2 dB. Fig. 14 shows the measured performance over the signal bandwidth.

The measured INL and DNL are shown in Fig. 15. The INL is better than 1.8 LSB and the DNL shows two missing codes. The performance is degraded by a systematic error when resolving the sixth bit (N=6). When the sixth bit is resolved as zero, the output voltage is reduced by approximately 0.75 LSB. On the other hand, when the sixth bit is resolved as one, approximately 0.75 LSB is added to the output voltage. This phenomenon is seen as a sawing effect in the INL plot, and the cause is still unknown to the authors. The overall performance is summarized in Table I.

VIII. Conclusion

In this paper, a 12-bit ratio-independent algorithmic A/D converter for a capacitive sensor interface has been presented. The implemented ratio-independent architecture is insensitive to capacitance ratios, amplifier offset voltage, input parasitics, and flicker noise. With a power dissipation of 68.4-μW and an active area of 0.041-mm^2, the A/D converter is very suitable for low-power sensor applications.

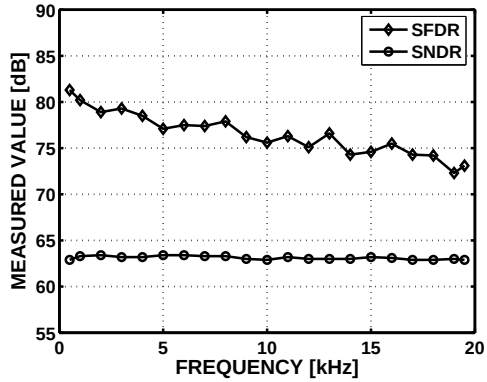

Fig. 14. Measured performance over the signal bandwidth.

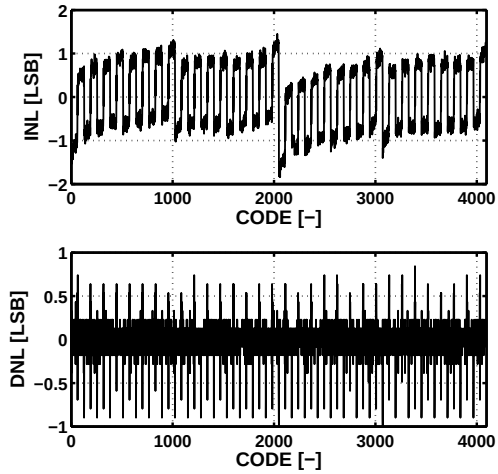

Fig. 15. Measured integral and differential nonlinearity.

TABLE I
Performance Summary

Resolution	12 bits
Conversion rate	40 kS/s
Process	0.13-μm CMOS
Active area	0.041 mm^2
SNDR / SFDR	63.3 dB / 80.2 dB
ENOB	10.2
Maximum INL	+1.4 / -1.8 LSB
Maximum DNL	+0.8 / -1.0 LSB
Full scale input signal range	2.2 $V_{\mathrm{pp,diff}}$
Supply voltage	1.8 V
Current consumption	38 μA
Power dissipation	68.4 μW
Power FOM	1.45 pJ/conv

Acknowledgments

The authors wish to thank M. Paavola, M. Kämäräinen, and M. Laiho for co-operation with the system-level implementation. M. Paavola and M. Kämäräinen are also acknowledged for the measurement setup design and their efforts in the system-level verification.

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