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Direct-Conversion Receiver for Ubiquitous Communications

J. Kaukovuori, J. A. M. Järvinen, J. Ryynänen, J. Jussila[1], K. Kivekäs[1], K. A. I. Halonen

Electronic Circuit Design Laboratory, Helsinki University of Technology
P.O. Box 3000, FIN-02015 HUT, Finland. [1)] Nokia Research Center, Helsinki, Finland.
Phone: +358 9 451 2988, Fax: +358 9 451 2269, E-mail: jouni.kaukovuori@ecdl.hut.fi

Abstract — **A direct-conversion receiver for a 2.4-GHz sensor network is described. The receiver is designed to operate in a Bluetooth system where slight changes are made in the radio parameters to meet the low power requirement. The receiver includes an LNA, downconversion mixers, a 90-degree phase shift circuit, analog filters, a 1-bit analog-to-digital converter, and a received signal strength indicator (RSSI). The receiver consumes 4.1 mA from a 1.2-V power supply and it achieves 43-dB voltage gain, 25-dB noise figure, -22-dBm IIP3, and +11-dBm IIP2.**

Index Terms — **CMOS, receiver, sensor networks.**

I. Introduction

The microsensors must operate autonomously for several years to minimize the maintenance cost and effort. To achieve the required power consumption, the sensors are at the sleep mode for most of the time, with duty cycle in the order of 0.1 to 1 percent [1]. In addition, the wake-up time should be minimized. Typically, the transceiver parameters are traded for operating range. Due to the unique nature of sensor networks new circuit and system solutions are presented recently [1-3].

In typical radios, the current consumption increases along with the operational frequency. For that reason, operating at the sub-1-GHz frequency ISM band [1,4,5] would be beneficial to reach the minimal power consumption. However, the current mobile terminals usually have Bluetooth (BT) as the short-range wireless connection. Thus, to avoid the need for yet another radio, utilizing BT for sensor networks is preferred. In addition, to meet the power requirements, slight changes in the BT radio parameters are proposed for sensor systems [6].

In this paper, the design of a direct-conversion receiver (RX) and its measurement results are presented. The RX is part of a single-chip transceiver circuit fabricated in a 0.13-µm CMOS process. The RX block diagram is presented in Fig. 1. The RX has a shared RF i/o port with the transmitter (TX) and both use the same VCO for the local oscillator (LO) signal generation. Compared to the previous prototype [7], the separate LNA and mixers are used and 90-degree phase shift circuit is added. In addition, the RX includes two baseband channels with improved selectivity. The wake-up logic and RSSI are added and limiters are fully differential. Biasing is implemented by using an on-chip current reference (I_{ref}). As a result, a receiver with a complete functionality and improved performance is achieved.

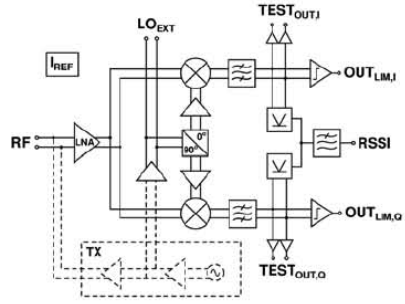

Fig. 1. Block diagram of the fabricated receiver (RX). Part of the transmitter (TX) and the RX/TX interface are shown with a dashed line.

II. RF Front-End

A. Low-Noise Amplifier

The low-noise amplifier (LNA) shown in Fig. 2a uses a common-gate (CG) topology with a cascode stage. The input transistors are biased into subthreshold region to maximize the transconductance versus drain current ratio. The LNA uses an LC-resonator tuned at 2.45-GHz center frequency as a load. The RX shares the same time-divided RF input-output port with the TX. The CG input allows high impedance path towards RX in the transmit mode. Thus, a proper matching performance is achieved without using the switches in the signal path.

In the previous published prototype receiver, the front-end and the baseband interface consisted of four stacked transistors [7]. As a result, the drain-to-source voltage V_{ds} of the LNA was susceptible to the supply voltage V_{dd}. The deviation from the nominal V_{dd} changed the LNA drain current, which altered the bias condition of the mixers and the baseband interface. With separate LNA and mixer, the performance dependence from the supply voltage is reduced. In addition, the input transistors of a separate LNA have a higher V_{ds}, which improves the gain and noise performance. However, with separate LNA and mixer, the whole receiver consumes more current compared to [7]. In this design, the LNA consumes approximately 2.3 mA including biasing, which is half of the total receiver current.

B. Downconversion Mixer

The mixer schematic is shown in Fig. 2b. The mixer does not have a typical common source (CS) input stage due to

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the strict current budget. The simulated current consumption of the whole mixer is 410 µA, which is 10% of the RX total current. With such a small current a CS amplifier realized with deep sub-micron CMOS transistors would not improve the gain or the noise performance. Hence, the LNA output signal is fed directly on the sources of the switch transistors to maximize the linearity. The switches are designed with minimum transistor length to minimize the load of the LO buffers [5].

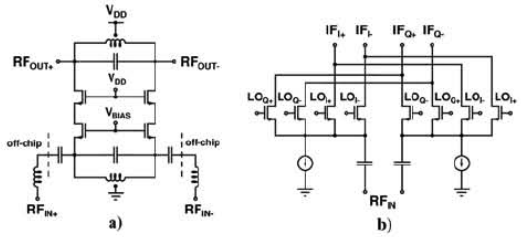

Fig. 2. a) LNA b) Mixer.

C. Quadrature LO Signal Generation

The quadrature LO signal generation circuit is shown in Fig. 3. When the transceiver operates normally, the LO signal is generated on-chip (LO_{VCO}) and it is fed into the first buffer. However, in the receiver measurements the VCO is shut down to be able to measure the receiver performance only. Thus, an external LO signal (LO_{EXT}) is required. It is fed to the output of the first LO buffer. The first buffer uses an LC-resonator as a load for better LO swing, but the buffers driving the mixers do not include inductors to save the silicon area.

The 90-degree phase shifting is realized with a single-stage polyphase filter (SPF). While the amplitude balance of the SPF is poor and susceptible to process variations, it was chosen to minimize the LO signal loss and hence the power consumption. According to the simulations, the loss due to the SPF was 5 dB in this design. The target current consumption for the LO buffers was approximately 1 mA only. Thus, the compensation of the LO signal loss caused by two or more filter stages would increase the current of LO buffers to an unacceptable level. The first buffer consumes approximately 0.46 mA and one second-stage buffer 0.33 mA supply current.

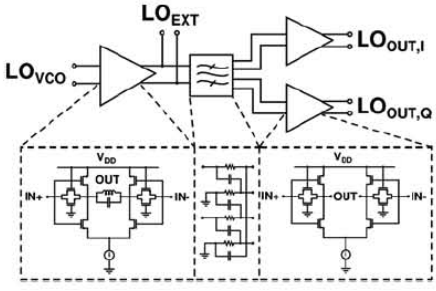

Fig. 3. Schematic of the LO buffers and 90-degree phase shifter.

III. Baseband

A. Mixer-Baseband Interface and Channel-Select Filter

The channel-select filter is a fourth-order all-CMOS filter with a –3-dB corner frequency of 600 kHz. Fig. 4 shows one half of the filter. The simulated current consumption including bias circuit is 40 µA. The selectivity of the filter is improved from [7] by adding a 2nd real pole. Furthermore, the value of the servo capacitor M_{FB} was halved to decrease silicon area. Since the DC gain of the servo loop was also halved with a constant current source M_1, the –3-dB frequency of the resulting highpass filter is unchanged.

The wake-up time of the filter depends on the –3-dB corner frequency of the servo loop. To decrease the wake-up time, the servo loop is bypassed during wake-up. Hence, the charging of the feedback capacitor M_{FB} is speeded up by shifting the –3-dB corner frequency of the servo loop from a nominal 60 kHz to a higher frequency. As a result, the wake-up time of the filter is reduced to one fifth compared to the solution without the wake-up logic.

The –3dB-corner frequency of the channel-select filter deviates due to process and temperature variations. The deviation is limited to ±10% with a current reference. The reference is a constant-g_m circuit where the resistor, which defines the value of g_m, is replaced with a switched NMOS capacitor equivalent. Because clock signal has an accurate frequency, the g_m of a filter transconductor is inversely proportional to the capacitance of an NMOS capacitor and the variation of the filter time constants is compensated. However, mismatches and the limited accuracy of MOSFET current mirrors determine the accuracy of compensation.

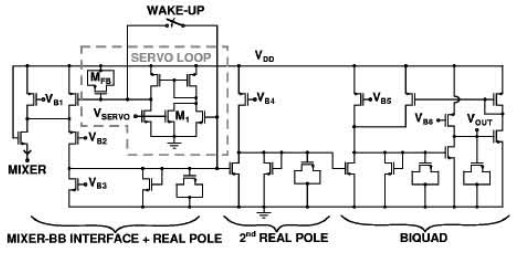

Fig. 4. Mixer-baseband interface and a channel-select filter (one half).

B. Limiting Amplifier

The 1-bit A/D conversion is realized with a limiter, which together with a large modulation index makes the receiver insensitive to strong reception signals [6]. The limiter block diagram is shown in Fig. 5. It consists of an unity gain input stage, four cascaded amplifiers with a total small signal gain of 47 dB, a balun, and a flip-flop that samples the output signal. A differential common-source input stage with cross-coupled PMOS current mirrors and diode-connected NMOS loads buffers the filter output and has common mode rejection. The limiter amplifier is a differential pair with PMOS input devices and cross-coupled NMOS devices in parallel with diode-connected NMOS transistors to increase the load impedance and thus the gain of the amplifier.

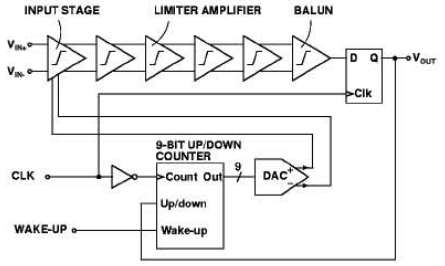

Fig. 5. Limiter architecture.

A DC feedback loop is required to reduce the limiter input-referred DC offset. To achieve a large time constant without large resistors and capacitors, the DC feedback loop is implemented by using digital circuitry. The DC feedback loop consists of a digital 9-bit up/down counter and a 9-bit current-steering DAC to filter out the DC offsets [8]. The –3-dB frequency of the resulting highpass filter is inversely proportional to the signal power. Since each highpass filter in the signal path decreases the signal quality, the maximum –3-dB frequency of the highpass filter was set to 40 kHz. The wake-up time of the limiter is reduced to one fourth by switching the counter to a wake-up mode where the six most significant bits of the original counter are used. The simulated limiter current consumption of one channel is 30 μA.

C. Received Signal Strength Indicator

The designed received signal strength indicator (RSSI) is shown in Fig. 6. The RSSI has separate full-wave rectifiers for I- and Q-branches (only one shown in Fig. 6), but the following two-stage filter and the latched comparator are common. The full-wave rectifier is designed to eliminate common-mode components at the input of the RSSI. For this purpose, a common-mode feedforward technique is utilized [9]. The average I_{cm} of the two input currents I_p and I_m is mirrored to the outputs of the rectifier. As a result, the common-mode component is cancelled from the both input currents. The signal currents I_{om} and I_{op} from the both branches are combined in a diode-connected NMOS-load M_1. The ripple of the rectified signal is attenuated by using a two stage low-pass filter formed by transistors $M_1 - M_4$. With a target –60-dBm input signal level the remaining error compared to the reference level V_{REF} is smaller than 0.1 dB with the nominal parameters. The simulated current consumption of the whole RSSI including biasing is 7 μA.

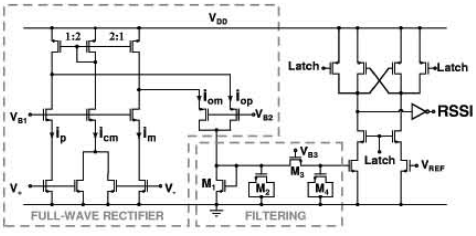

Fig. 6. Received signal strength indicator (RSSI).

IV. Experimental Results

The chip was fabricated with a 0.13-μm CMOS process. The active area of the RX is approximately 1.0 mm^2. The chips were directly bonded on a printed circuit board (PCB) made of FR-4 substrate. Measurements were performed both from the analog test output of the baseband circuit and from the limiter output. The performance was characterized by using the on-chip current reference. According to the measurements from several samples, the noise figure (NF) in the Q-channel was approximately 3 dB higher than in the I-channel. In addition, the IIP2 result of the Q-channel was degraded compared to the I-channel. The imbalance and the noise leakage are probably due to a systematic error in the layout. Thus, the NF and IIP2 performance of the receiver are determined according to the I-channel measurement results only. For the other measured parameters such significant performance difference between the I- and Q-branches was not observed.

The maximum voltage gain of 43 dB is achieved at 2.45 GHz. The NF measured from the analog test output is 25 dB. The measured voltage gain and NF versus the supply voltage are presented in Fig. 7, which shows that the receiver operates down to one-volt supply voltage. The mixer and the interface with the baseband set the limit because of four stacked transistors. The measured voltage gain is lower than simulated. Since the circuit model from the latest TX output was not available, the resulting input matching (S11) of the RX was inadequate. Thus, the S11 of the RX was improved by adding series inductances on PCB. As a result, S11 better than -10 dB is achieved between 2.05-2.55 GHz. However, the input matching circuit and RX/TX interface suffers from the parasitic capacitances, which cause signal loss and most of the gain degradation. The parasitic capacitance also increases the NF, because the gain is lacking before the mixers, which have the largest effect on the total output noise.

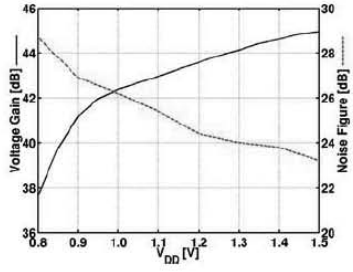

Fig. 7. Measured voltage gain and NF versus supply voltage.

The measured IIP3 of the receiver is –22 dBm with the test tones at 3-MHz and 5.8-MHz offsets from the LO. Because the linearity is dominated by the mixer-baseband interface, the measured IIP3 is 3 dB higher than simulated due to the lower gain at RF. The IIP2 was measured with 5.8-MHz and 6-MHz test signals. The IIP2 result varied between +11…+21 dBm in the I-channel. The Q-channel IIP2 was approximately 0 dBm.

The simulated and measured frequency responses (three samples, six channels) of the channel-select filter are shown in Fig. 8. In Figure 8, the measured and simulated maximum voltage gains are scaled to 0 dB for the purpose of comparison. The measured –3dB-corner frequency variations are within the specified ±10%.

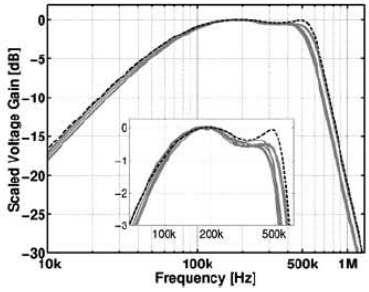

Fig. 8. Measured and simulated channel-select filter responses.

The measured wake-up times of the whole receiver with and without the wake-up logic were 15 µs and 80 µs, respectively. The measured RSSI threshold varied between –59…–55 dBm. The threshold is larger than the designed value due to the lower voltage gain of the front-end. The limiter was characterized by measuring the duty cycle with input signal frequencies from 100 kHz to 600 kHz, and input signal levels from –77 dBm to –27 dBm. In all cases, the duty-cycle variation was between ±1% from the nominal value of 50%. The measured limiter group delay at 200 kHz input signal frequency was 82 ns.

The measured current consumption of the whole receiver was 4.1 mA. Although the RX was measured alone, the whole transceiver couldn't be completely shut down due to the TX on the same chip. Thus, the measured stand-by current consumption of 440 µA is arbitrarily high compared to the simulated value of 20 µA, which include the measured current consumption of the on-chip bias generator (6.2 µA). The measured receiver performance is collated in Table I. The chip microphotograph is shown in Fig. 9.

TABLE I

THE MEASURED RECEIVER PERFORMANCE

Supply Voltage	V	1.2
Supply Current (active)	mA	4.1
Supply Current (stand-by)	µA	440
Voltage Gain	dB	43
NF	dB	25
Out-of-channel IIP3	dBm	-22
Out-of-channel IIP2	dBm	+11
ICP	dBm	-35
S11	dB	< -10
Filter high-pass –3-dB frequency	kHz	66
Filter low-pass –3-dB frequency	kHz	546
Wake-up time	µs	15
Limiter duty cycle	%	49
Limiter group delay @ 200kHz	ns	82
RSSI Threshold	dBm	-55

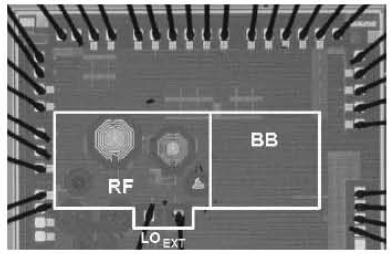

Fig. 9. Chip microphotograph.

V. CONCLUSIONS

A direct-conversion receiver operating in a 2.4-GHz sensor network is presented. The receiver uses modified Bluetooth as a radio connection and consumes 4.3 mA from a 1.2-V supply. Even though the receiver consumes more current compared to the previous prototype design [7], several blocks are added while the active silicon area is not increased. In addition, improvement in the overall performance is achieved. Approximately 90% of the total power is consumed in the RF front-end. Thus, to minimize the power consumption, the optimization should be concentrated on the blocks and elements operating at the radio frequency. In addition, low power consumption is achieved with the trade-offs in the hardware performance and optimization in radio parameters.

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