Zn diffusion doping of III-V semiconductors for new optoelectronics applications

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ABSTRACT OF THE
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Modern high-power light-emitting diodes (LEDs) employ nanoscale structures composed of multiple layers of different III-V compound semiconductors. The same basic types of double heterojunctions (DHJs) have been used in high-efficiency LEDs for decades, and these structure have enabled LEDs to reach higher luminous efficacies than any competing lighting technology. However, issues with current crowding are limiting further improvements in efficiency. One novel method of current injection that could solve some of these problems is diffusion-driven current transport (DDCT), which involves using diffusion currents to drive charge carriers into the active area of the LED.

This thesis aims to investigate the viability of Zn diffusion doping as a fabrication technique for realizing GaAs-based DDCT LED structures. A spin-on glass process for Zn diffusion doping is developed and samples are fabricated using this method. An alternative contact scheme involving metal contacts directly deposited on the sample with no diffusion doped areas is also tested. Characterization of the fabricated samples is performed using current-voltage (IV), capacitance-voltage (CV) and Hall effect measurements. Visual inspections of surface and coating quality were performed using scanning electron microscopy (SEM). Light emission from the samples was observed using an infrared microscope camera system.

Successful p-type doping of intrinsic GaAs samples was achieved, but attempts to convert n-type samples into p-type were unsuccessful due to insufficient density of diffused dopants. Light emission from the alternative contact structure was observed, which indicates successful hole injection. This suggests that direct deposition of metal contacts could be a viable option for realizing the first DDCT devices.

Keywords: LED, GaAs, III-V, semiconductor, spin-on glass, SOG, DILED, DDCT, diffusion, doping

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Nykyaikaisissa hohtodiodeissa (LED, engl. light emitting diode) käytetään useista eri III-V -puolijohteista koostuvia nanomittakaavan kerrosrakenteita, joilla pyritään kasvattamaan niiden hyötysuhdetta. Korkean hyötysuhteen LEDien pohjana on jo vuosikymmenien ajan ollut samantyyppinen kaksoisheterorakenne, ja sillä on saavutettu merkittävästi muita valaistustekniikoita korkeampia hyötysuhteita. Virransyötön ongelmat rajoittavat kuitenkin nykyisillä rakenteilla saavutettavaa suorituskykyä. Näiden ongelmien ratkaisemiseksi on esitetty uudenlaista, diffuusiovirtoja hyödyntävää virransyöttömenetelmää (DDCT, engl. diffusion driven current transport) LEDeihin.
Tämän diplomityön tavoite on tutkia mahdollisuutta käyttää sinkkidiffuusioseostusta galliumarsenidiin (GaAs) pohjautuvien DDCT LED -rakenteiden valmistuksessa. Tätä tarkoitusta varten työn osana kehitettiin näytteen pinnalle levitettävään piidioksidikerrokseen perustuva seostusmenetelmä. Tällä menetelmällä valmistettiin diffuusioseostettuja näytteitä. Lisäksi tehtiin näytteitä, joihin ei valmistettu diffuusioseostettuja alueita, vaan metallikontaktit höyrystettiin suoraan n-tyypin näytteen pinnalle. Näiden näytteiden tarkoitus oli tutkia vaihtoehtoista aukkojen syöttötapaa rakenteeseen. Näytteitä karakterisoitiin virta–jännite- (IV), kapasitanssi–jännite- (CV) sekä Hall-mittauksilla. Lisäksi näytteitä tarkasteltiin pyyhkäisyelektronimikroskoopilla (SEM, engl. scanning electron microscope) pinnan laadun havainnoimiseksi. Valon emissiota havainnoitiin infrapunakameralla.
Työn menetelmällä onnistuttiin seostamaan intrisiikkisten GaAs-näytteiden pintaan p-tyypin johtava kerros. Yritykset muuttaa n-tyypin näytteen pinta p-tyypin puolijohteeksi sen sijaan eivät onnistuneet, sillä seostustiheys oli liian matala. Vaihtoehtoisesta metallikontaktirakenteesta havaittiin valon emissiota, mikä osoittaa aukkojen injektoinnin rakenteeseen onnistuneen. Näin ollen suorat metallikontaktit voisivat olla lupaava tapa toteuttaa ensimmäiset DDCT-laitteet.

Avainsanat: hohtodiodi, valodiodi, LED, DDCT, diffuusio, seostus, diffuusioseostus, puolijohde, III-V, optoelektroniikka

Preface

The work presented in this thesis was carried out at the Department of Electronics and Nanoengineering at Aalto University. I would like to thank Sami Suihkonen and my supervisor, Professor Markku Sopanen for the opportunity to work in the Optoelectronics group and contribute to research in such a fascinating field. I would also like to thank my advisor, Jani Oksanen, for sharing his knowledge and generous guidance throughout the process of working on this thesis. I would also like to thank my colleagues, especially Toufik Sadi and Ivan Radevici, for all of their helpful advice and interesting discussions along the way.

I want to express my gratitude to my friends for helping make these years of studying some of the best ones in my life so far. I would also like to thank my family for supporting me in everything I've decided I want to do, for sparking my interest in science, encouraging me to pursue my dreams, and for putting up with my occasional habit of dismantling household appliances. Finally, I would especially like to thank Riina, for all of her love, support and patience.

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Contents

Abstract ii

Abstract (in Finnish) iii

Preface iv

Contents v

Symbols and abbreviations vii

1 Introduction 1

2 Theoretical background 3
2.1 Crystal structure . . . 3
2.2 Electronic band structure . . . 4
2.3 Doping in semiconductors . . . 6
2.4 Diffusion mechanisms in semiconductors . . . 7
2.4.1 Zn diffusion in GaAs . . . 9
2.4.2 Zn diffusion in other III-V semiconductors . . . 13
2.5 Characterization of doping . . . 16
2.6 p-n junctions . . . 17
2.7 Metal-semiconductor junctions . . . 20

3 LED structures 23
3.1 DHJ LEDs . . . 23
3.2 DDCT LEDs . . . 25

4 Fabrication and characterization methods 28
4.1 Spin-on glass preparation . . . 28
4.2 Spin coating and diffusion anneal . . . 29
4.3 Contact metallization . . . 30
4.4 Electrical characterization . . . 30
4.4.1 IV measurement . . . 30
4.4.2 Hall effect . . . 32
4.4.3 CV measurement . . . 35

5 Results and discussion 38
5.1 Samples . . . 38
5.2 Spin-on glass coating . . . 38
5.3 Diffusion annealing . . . 42
5.4 Diffusion doping on undoped substrate . . . 43
5.4.1 IV measurement results . . . 43
5.4.2 Hall effect measurement results . . . 44
5.5 Diffusion doping on n-type substrate . . . 46
5.5.1 IV measurement results . . . 46

5.5.2 CV measurement results 47
5.5.3 Hall effect measurement results 48
5.6 ZnAu contacts on n-type substrate 49
5.6.1 IV measurement results 49
5.6.2 Light emission 50

6 Summary **52**

Symbols and abbreviations

Symbols

C	Concentration
D	diffusivity
E_C	conduction band energy
E_F	Fermi level
E_V	valence band energy
I	electric current
T	temperature
V	voltage
h	Planck constant (4.135667×10^{-15} eV $\cdot$ s)
k	Boltzmann constant (8.61733×10^{-5} eV/K)
q	elementary charge (1.602×10^{-19} C)
ΔE	activation energy
ϵ_0	vacuum permittivity
ϵ_r	dielectric constant
Φ_B	Schottky barrier
Φ_{metal}	metal work function
χ	electron affinity

Abbreviations

AZO	Aluminum doped zinc oxide
CV	capacitance-voltage
DDCT	diffusion-driven current transport
DHJ	double heterojunction
DILED	diffusion injected light emitting diode
EL	electroluminescence
HF	hydrofluoric acid
IR	infrared
ITO	indium tin oxide
IV	current-voltage
LED	Light-emitting diode
MQW	multi-quantum well
PV	photovoltaic
SEM	scanning electron microscope
SIMS	secondary ion mass spectrometry
SOG	spin-on glass
SQW	single quantum well
TPX	thermophotonics
UV	ultraviolet

1 Introduction

The importance of energy efficiency as a design consideration in the development of new technologies has been continually growing in recent decades, as everything from cars and power plants to computers and phones become more efficient at generating or using energy with each new generation. There are multiple drivers for this development: natural resources getting less abundant and more expensive, growing consumer demand for phone batteries that last longer and appliances with lower operating costs, and most significantly, growing awareness of the environmental effects of unsustainable energy consumption and pollution. All of these factors are driving consumers, corporations and governments increasingly towards more efficient technologies.

One of the most important technologies in this context is the light-emitting diode (LED). Since the invention of the blue LED in 1994 made it possible to make white LEDs, LED technology has increasingly supplanted incandescent and fluorescent bulbs in general lighting applications, and for good reasons. LED bulbs already have a longer lifetime and greater efficiency than any incandescent or fluorescent bulb of similar output on the market, and the amount of research and development put into LED technology continues to see their efficiency improve exponentially. The International Energy Agency (IEA) has estimated the share of lighting to be 19% of total electricity consumption globally, and the adoption of more efficient lighting technology, such as LEDs, has been estimated to reduce this to less than half. [1]

LEDs also show promise in reducing energy consumption and waste in applications beyond just lighting. Specifically, a phenomenon called electroluminescent (EL) cooling could be used to turn the LED into a heat pump. EL cooling is a phenomenon that has been theoretically well understood for decades, [2, 3] but there has been relatively little research into its practical applications. Essentially, EL cooling entails using heat from the environment to provide part of the energy required to operate the LED, cooling the surroundings of the LED while it produces light. [4–6] This effect could be utilized in a thermophotonic (TPX) system to generate energy from waste heat or solar energy, by collecting heat energy to help drive an LED and collecting the emitted light in a photovoltaic (PV) cell. [7] A powerful EL cooling system with high enough efficiency could also be used in refrigeration and heat pump systems, [8] which would reduce the amount of power used globally for cooling and heating – an even more significant portion of total global energy consumption than lighting. [9]

Highly efficient LED structures are required to achieve these goals of reducing energy consumption. Most commercial high-power LEDs have utilized nanometer-scale layered semiconductor structures called double heterojunctions (DHJ) for this purpose. The efficiency that can be achieved with this type of structure is high enough to make LEDs suitable for general lighting purposes. However, some issues inherent to the DHJ LED structure limit further improvements. One such issue is that the relatively low mobility of charge carriers in the semiconductor layers cause an issue known as current crowding, which causes the current density to concentrate near the electrical contacts. This limits the efficiency and lifetime of LEDs, as the areas near the contacts heat up due to the high current density, while the areas

farther away from the contacts get less current density than required to achieve optimal light emission efficiency.

Our group has been developing an alternative current injection scheme called diffusion-driven current transport (DDCT), which utilizes diffusion currents to inject carriers into the active area. This could alleviate some of these problems inherent in DHJ LEDs, such as the current crowding issue described above, while also providing the possibility to develop new applications enabled by the ability to excite active layers on device surfaces. [10] The purpose of this work is to explore some such structures and possible methods for fabricating them. In particular, using Zn diffusion to dope (*i.e.*, introduce electrically active impurities into) GaAs-based semiconductors is explored, as this could be a useful method for fabricating LED structures based on lateral pn-junctions. Utilizing this kind of structure together with diffusion-driven current transport (DDCT) could enable efficient current injection into large-area LEDs, which are challenging structures to inject current into by conventional means. These types of structures could be a promising candidate for EL cooling as well, as simulations predict the efficiency of such structures could be very high. [11]

The goal of this work is to explore the fabrication of the types of structures described above by developing a repeatable process for Zn diffusion doping in GaAs-based semiconductors. The necessary theoretical background to understand selected properties of semiconductors, doping, and diffusion mechanisms are discussed in chapter 2, along with some basic types of semiconductor structures and common characterization methods. The third chapter describes the common DHJ LED and some experimental DDCT LED structures in detail. Chapter 4 explains the experimental methods employed to fabricate and characterize the Zn-doped samples studied in this work. Results obtained from these samples are presented and discussed in detail in chapter 5. Finally, a summary of the work is given in chapter 6.

2 Theoretical background

This section reviews the theoretical background required for understanding the operation of the device structures studied in this work, as well as the fabrication and characterization methods discussed in the subsequent chapters. First, the basic properties of III-V semiconductors that are relevant to diffusion doping and the operation of LEDs are discussed. The topic of diffusion doping is discussed in detail in section 2.4, first in a general manner and then more specifically in the case of Zn diffusion in GaAs, AlGaAs and InGaP. After this, some methods commonly used to characterize doping densities and profiles are broadly outlined (the specific methods used in this work are described in more detail later, in chapter 4). Finally, the physics of two important types of basic semiconductor structures, p-n junctions and metal-semiconductor junctions, are discussed.

2.1 Crystal structure

III-V semiconductors, such as GaAs, are compound semiconductors that consist of a combination of group III elements (*e.g.*, Al, Ga, In) and group V elements (*e.g.*, N, P, As, Sb). These atoms form an organized, periodic structure known as a crystal lattice.

The structure of an ideal crystal lattice is described completely by its smallest repeating group of particles, called the unit cell. This means that the entire lattice can be constructed by repetitive translation of this unit cell along its principal axes. Figure 1 shows unit cells of some common crystal structures. [12]

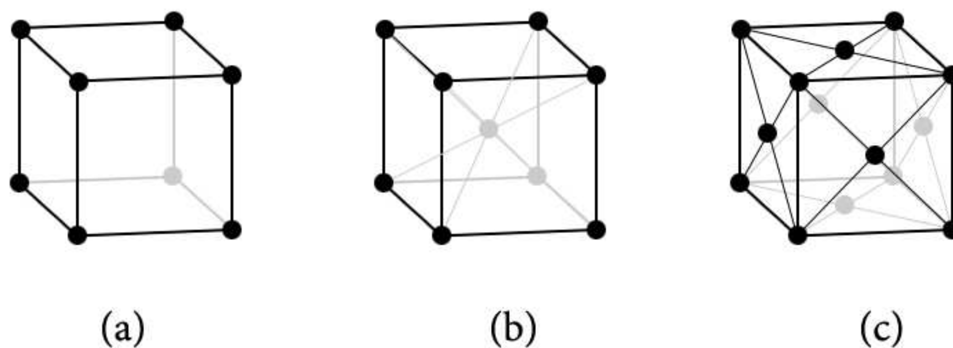

Figure 1: Three primitive lattices in the cubic crystal system: (a) simple cubic, with a particle at each corner; (b) body-centered cubic, with a particle at each corner and in the middle of the cube; (c) face-centered cubic, with a particle at each corner and the middle of each face.

The crystal structure that a given material or material combination adopts

depends on the size of the atoms involved and the details of the bonding between them. GaAs and other III-V semiconductors with a cubic crystal structure, such as GaP and InP, adopt the zincblende crystal structure, which can be thought as two overlapping face-centered cubic lattices, displaced by 1/4 the width of the unit cell in each dimension. One of the lattices has Ga atoms populating its lattice sites, while the other has As atoms. The zincblende crystal structure is illustrated in Figure 2. [13]

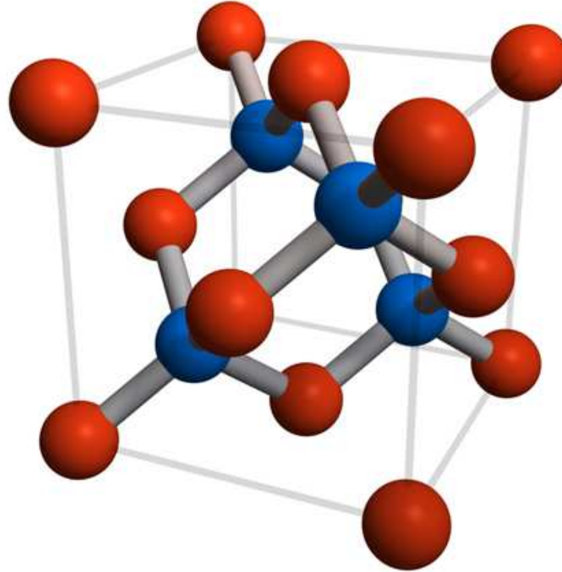

Figure 2: Stick-and-ball model of the zincblende crystal structure. The red and blue spheres represent different atoms, *e.g.*, Ga and As in the case of GaAs.

2.2 Electronic band structure

When atoms bond together to form a crystal lattice, their electron orbitals begin to overlap, forming energy states that are spread over the whole volume of the crystal. Due to the very large number of atoms, and thus energy states, in a typical crystal lattice, the states form several quasi-continuous bands of allowed energy states. These bands may be separated by gaps, where there are no available energy states. This gives rise to the electronic band structure of solid state materials, illustrated for GaAs in Figure 3. [14]

Though there are a large number of bands and gaps in any given solid-state material, the most important ones for the purposes of electronics and optoelectronics are those near the Fermi level, which refers to the level below which all the energy states are filled with electrons at 0 K at equilibrium. Bands far below the Fermi level are always completely filled and, therefore, cannot conduct electricity. Bands far above the Fermi level, on the other hand, are so high in energy that they are typically completely empty in equilibrium conditions. [15]

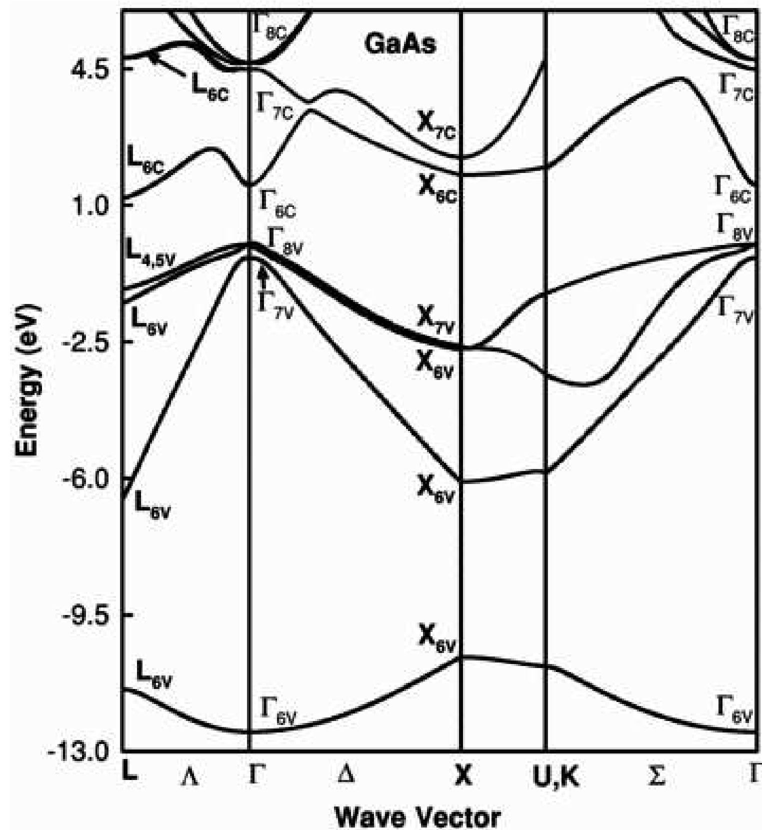

Figure 3: Electronic band structure plot of GaAs. Energy scale is shown relative to the Fermi energy. [14]

The electronic band structure and the Fermi level play an important role in the classification of materials. In metals, the Fermi level resides within at least one energy band. Thus, there are a great number of free energy states near the Fermi level available for electrons to populate – this is the reason that metals are very good at conducting electricity.

If the Fermi level of an ideal crystalline material resides within a band gap, the material is an insulator or a semiconductor. In this context, the gap in which the Fermi level resides is termed simply *the* bandgap, and its magnitude the bandgap energy, E_G. If the bandgap is very large, the band below it (called the valence band) is completely filled and the material does not conduct electricity. Such materials are electrical insulators.

If the bandgap energy is low enough that, at around room temperature, a significant number of electrons can get thermally excited to the energy band above the gap, called the conduction band, the material is called a semiconductor. The difference between insulators and semiconductors (especially wide-bandgap semiconductors) is somewhat ambiguous, as an insulator can also be made conductive by sufficient heating and there is no clearly defined value of E_G that makes a material an insulator. [15]

An important advantage of III-V semiconductors over traditional elemental semi-

conductors, such as Si or Ge, is the possibility to tune the bandgap energy and type (direct or indirect) over a fairly wide range by making ternary or quaternary compounds with the various elements of the III-V material system. This is known as bandgap engineering. This is highly advantageous for optoelectronics, where a direct bandgap with a particular energy enables, for instance, the fabrication of LEDs with a fine degree of control over the color of the emitted light. This will be discussed in more detail in section 2.6. Bandgap engineering is not unique to the III-V material system, but most other material combinations produce bandgaps that are either indirect or are not in the energy range required for optoelectronics. III-V materials also typically offer higher carrier mobilities than other semiconductors, making them more suited to high-speed electronics applications. [13, 16]

This thesis focuses mainly on GaAs and AlGaAs. GaAs has a direct bandgap of 1.4 eV, meaning it emits light in the infrared (IR) range. One ternary compound can be made by combining GaAs and AlAs to form AlGaAs. By varying the respective material fractions of Al and Ga, the bandgap of this compound can be tuned between 1.4 eV (GaAs) and 2.16 eV (AlAs). However, as the bandgap of AlAs is indirect, the bandgap of AlGaAs is also indirect when the Al fraction is greater than 0.4. [16]

2.3 Doping in semiconductors

There is one significant practical difference between insulators and semiconductors: the conductivity of most semiconductors can be tuned by the addition of suitable impurity atoms into the lattice. This process is known as doping, and it is one of the main reasons why semiconductors are such important materials in modern electronics. Without doping, after all, they would simply be materials that neither insulate nor conduct electricity very well.

Replacing an atom in a crystal lattice with one that has fewer valence electrons introduces electron vacancies, called holes, into the material. These form acceptor states close to the valence band edge, so that electrons from the valence band can easily be thermally excited into these states. This leaves excess holes in the valence band, and these act as mobile charge carriers. Materials doped in this way are called p-type materials.

Replacing an atom in the lattice with one that has excess valence electrons produces an n-type material. In this type of material, there are electron donor states near the top of the bandgap, where electrons are easily excited to the conduction band. This leads to the Fermi level moving closer to the conduction band, and an excess of electrons carrying charge in the conduction band.

Doping can be achieved in many different ways. When producing bulk wafers, the donor or acceptor impurities can be added to the melt from which the crystal is pulled. This produces wafers with a uniform dopant distribution across the whole bulk of the wafer. Dopants can also be incorporated during epitaxial crystal growth. In metalorganic vapor-phase epitaxy (MOVPE), which is a commonly used method for growing III-V semiconductor films, this is done by adding a metalorganic precursor gas containing the desired impurity into the reaction during growth. This is the most common method employed today for producing doped III-V thin films, as it offers a

fine degree of control over the doping density and profile. [13]

In addition to the *in-situ* methods presented above, there are techniques that can be used to introduce dopants to crystals after crystal growth. The most common ways of achieving this are ion implantation and diffusion doping. In ion implantation, ions of the desired impurity are accelerated in an electric field and fired at high energy into the substrate. The ions penetrate into the semiconductor crystal, gradually losing their kinetic energy and coming to a halt inside the crystal. After implanting the desired amount of impurities, the sample is annealed to repair the damage caused to the crystal lattice by the ions penetrating through it. The advantage of this method is that it allows fine control of the amount of dopants and the diffusion depth. The depth profile can also be tuned to some extent by doing several implantations at different ion energies. [17]

Diffusion doping involves introducing dopant atoms into the lattice by exposing it to a high concentration of the desired impurity under controlled heating. The diffusion source is often a film or paste containing the dopant that is deposited directly onto the sample. The sample is then heated, facilitating the diffusion of dopants from the higher-concentration region in the film to the lower-concentration region in the substrate. Diffusion may also be achieved from the vapor phase, by sealing the substrate into a container with an elemental or alloyed dopant source and applying heat. This method can be used to achieve high doping concentrations with a relatively simple, fast and inexpensive process. By employing diffusion masks or standard patterning techniques to remove parts of the diffusant film, patterned doping can be achieved. [18]

It is this last method of doping that this thesis focuses on. Diffusion doping was used in the first LEDs and still sees widespread use in fabricating certain types of transistors. [18] However, the technique is rarely used in modern optoelectronics devices, as the thin-film structures employed in them require a higher level of control over the doping profile than can be achieved using diffusion doping. [16] However, the technique could be essential for fabricating some of the experimental LED structures which are presented in section 3.2.

2.4 Diffusion mechanisms in semiconductors

Diffusion refers to a phenomenon where atoms or other particles tend to spread from an area of high concentration to an area of low concentration. No external force or pressure is involved in diffusion – instead, the net movement of the atoms is caused simply by the random thermal motion of the particles, which naturally tends to even out any concentration gradients and maximize entropy. As the concentration difference gets smaller, diffusion slows down. A schematic illustration of diffusion can be seen in Figure 4.

In crystalline solids, diffusion can happen by two general mechanisms: substitutional and interstitial. In substitutional diffusion, the impurity atoms diffuse through the lattice by substituting an atom in the crystal lattice. In general, this sort of process is mediated by a point vacancy in the lattice, *i.e.*, an empty lattice site, as seen in Figure 5. The impurity atom can move within the lattice by moving into an

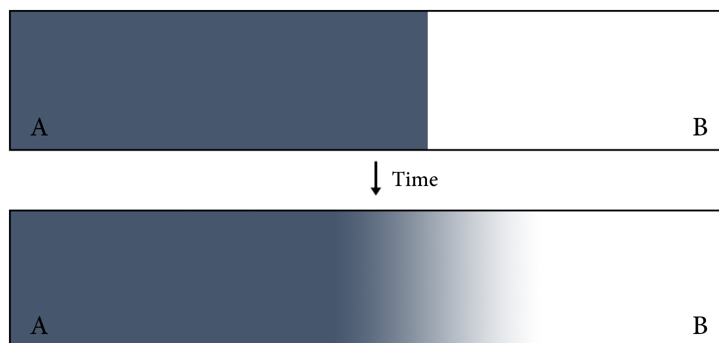

Figure 4: Diffusion between two ideal gas-like substances. Top: two substances, A and B, are separated by a sharp boundary at t = 0. Bottom: after some time, the substances diffuse into each other due to random thermal motion of the atoms. Given infinite time, the concentations of both would be uniform across the whole area.

adjacent vacancy. The vacancy left behind by the impurity atom can then be filled by an atom from one of the lattice sites adjacent to it, and thus, another vacancy gets formed at another lattice site. This is the basic mechanism by which impurity atoms can propagate through the lattice substitutionally.

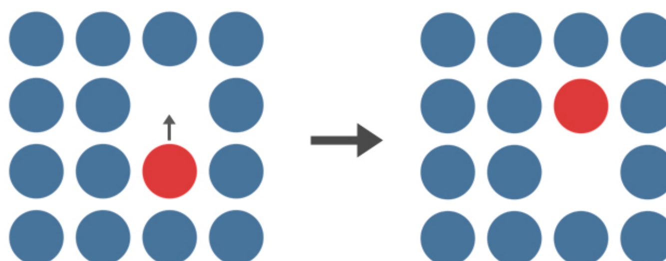

Figure 5: Schematic representation of substitutional diffusion at the atomic level. The red impurity atom moves into a point vacancy in the lattice, leaving another vacancy behind.

Interstitials are impurity atoms that do not occupy lattice sites, instead residing in the spaces between occupied lattice sites. In interstitial diffusion, the dopant atom moves through the material by weaving between the atoms in the lattice, instead of replacing them. Direct interstitial diffusion like this is only possible if the dopant atoms are very small, as they need to be able to travel directly between interstitial sites. [19]

Combinations of these diffusion mecahnisms also occur, and they are referred to as substitutional-interstitial mechanisms. One such mechanism, illustrated in Figure 6, is the so-called ”kick-out” mechanism, which involves an interstitial replacing an atom in the lattice, displacing it into an interstitial position.

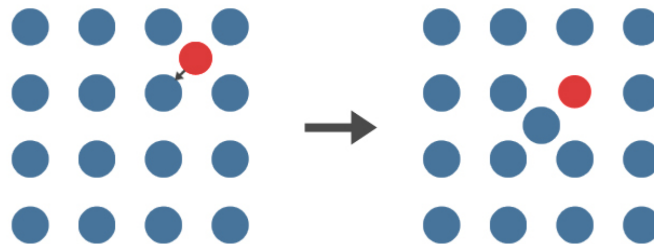

Figure 6: Schematic representation the kick-out mechanism at the atomic level. The red impurity atom replaces an atom in the lattice, pushing it into an interstitial site.

Another mechanism that involves interstitials moving to occupy a lattice site is the Frank-Turnbull, or dissociative, mechanism, where an interstitial impurity gets captured by a vacancy in the lattice, instead of dislodging an atom in the lattice to take its place. This is similar to the substitutional process (depicted in Figure 5), except in this case, the impurity moves into the vacancy from an interstitial site, not a lattice site. [20]

In both of these cases of substitutional-interstitial diffusion, the movement of the impurity atom can involve both direct interstitial jumps and some slower, substitutional mechanisms. The resulting diffusion process must thus be understood as a combination of these interstitial and substitutional components.

Diffusion of dopants is also be affected by defects in the crystal lattice. The presence of a large number of point defects, like interstitials and vacancies, can accelerate or hinder diffusion of impurity atoms through the lattice. Threading dislocations have also been observed to lead to higher diffusivity of dopants. [21]

2.4.1 Zn diffusion in GaAs

Zn is the most widely used p-type dopant in GaAs, so the diffusion characteristics of this pair of materials are relatively well understood. The process is a substitutional-interstitial one, with both dissociative and kick-out mechanisms responsible for the main features in the diffusion curve. Which mechanism dominates depends on the growth conditions and crystal quality of the GaAs sample.

Two distinct types of diffusion profile are identified in the literature for Zn in GaAs: box profile and kink-and-tail profile. Both of these can be seen in Figure 7, which shows two Zn-doped samples, one doped with a Zn-Ga alloy with 3 wt% Zn and one with pure Zn. Diffusion times were the same (2 h) in both cases. Lines of best fit are also plotted.

The sample doped with pure Zn exhibits a kink-and-tail profile, with double diffusion fronts. The high temperature causes Ga atoms to escape the lattice, leaving a high number of vacancies in the surface region. The diffusing Zn atoms can readily

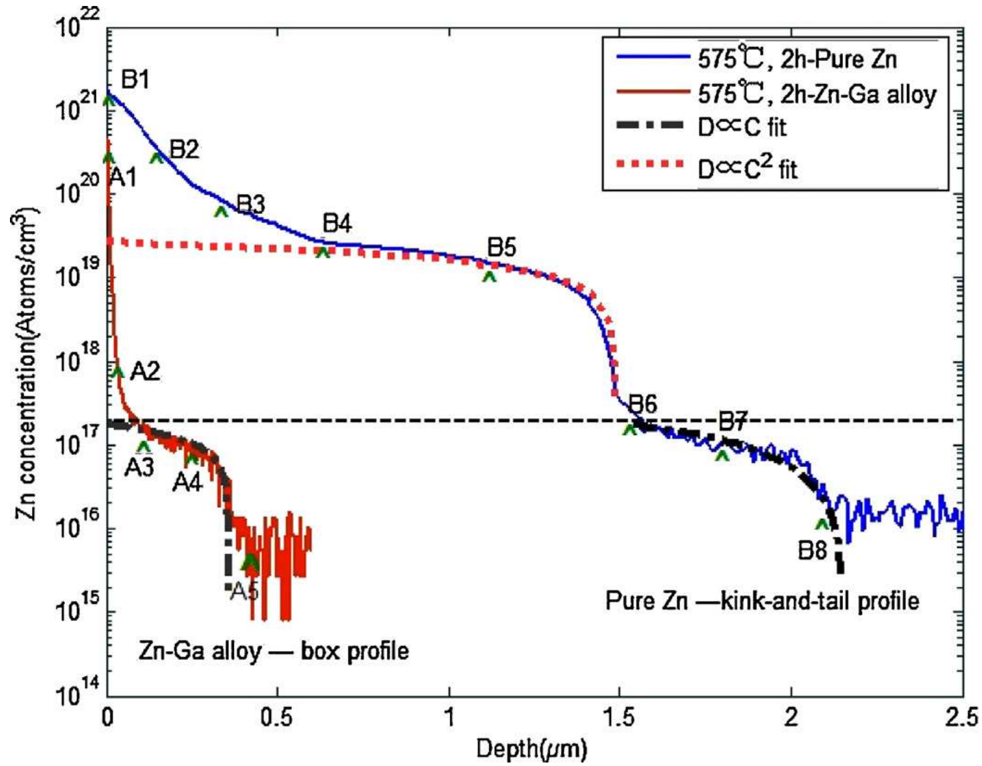

Figure 7: Example diffusion profiles for Zn in GaAs, with simulated fits. A $D \propto C^2$ fit (red dashed line) is fitted to the top region of the kink-and-tail profile, while the tail of the kink-and-tail profile and the box profile are modeled with a $D \propto C$ fit (black dash-dot line). [22]

occupy these vacancies, so Zn concentration is high near the surface. This forms the first diffusion front in which $D \propto C^2$, where D is the diffusivity and C is the Zn concentration. The tail part of the kink-and-tail profile is the second diffusion front. There are few Ga vacancies for the Zn atoms to occupy, so they must diffuse through the lattice interstitially and displace Ga atoms in the lattice in order to be electrically active. The kick-out mechanism is thus dominant at this depth.

The sample exhibiting a box profile was doped with a Zn-Ga alloy. The Ga-rich conditions prevent Ga atoms near the surface from escaping, as the Ga atoms in the alloy fill any vacancies in the lattice. Therefore, the only way Zn atoms can diffuse through the lattice is via the kick-out mechanism. This process is slower than the dissociative mechanism, and thus the diffusion depth is lower than in the pure Zn case. The profile has a similar shape to the tail region of the pure Zn-doped sample. The diffusivity is proportional to the Zn concentration in this region, *i.e.*, $D \propto C$. [22]

From the above, it can be concluded that the diffusivity of Zn in GaAs depends on the annealing temperature, surface Zn concentration and sample properties, such as defects and prior doping. The specific diffusion method and Zn source used also affect diffusivity, as these can have an effect on, *e.g.*, the kinetics of Ga vacancy formation. There is some variation, therefore, in the diffusivity values reported in

the literature. Effective diffusivity is usually reported in the Arrhenius form

$$D_{\mathrm{Zn}}^{\mathrm{eff}} = D_0 e^{-\frac{\Delta E}{kT}}, \tag{1}$$

where D_0 is the diffusion constant (also sometimes called temperature-independent diffusivity), ΔE is the activation energy, k is Boltzmann's constant and T is temperature. Some values found in literature for D_0 and ΔE in the case of an As-rich or pure Zn diffusion source are listed in Table 1.

Table 1: Diffusion constants D_0 and activation energies ΔE for different diffusion sources and setups without a Ga-rich atmosphere.

D_0 (cm^2/s)	ΔE (eV)	Technique	Diffusion source	Reference
26	2.47	sealed ampoule	$ZnAs_2$	23
14	2.38	sealed ampoule	$ZnAs_2$	24
2.05	2.28	sealed ampoule	$ZnAs_2$	25
42	2.42	leaky tube	$ZnAs_2$	26
181	2.33	semi-closed box	pure Zn	22

The variation in the values seen in these is largely due to differences in the diffusion sources and techniques used. The sealed ampoule method, which is commonly used in the literature, consists of placing the sample and the diffusion source into a quartz tube, evacuating the tube and sealing it with a butane-oxygen torch. This is done to ensure saturated vapor pressure inside the ampoule during diffusion, which reduces surface damage and also ensures that the Zn concentration remains uniform and constant during diffusion. The diffusion source can be a Zn-As alloy, as in the examples in Table 1, or pure Zn deposited on the sample surface along with a source of elemental As sealed in the ampoule to provide As overpressure. [27] This method yields very uniform and repeatable results, but is quite time- and labor-intensive.

Several variations of open-tube methods also exist, and these use some form of semi-sealed container filled with an inert gas to form a protective layer and prevent surface damage. Table 1 has two examples. The 'leaky tube' experiment utilized a specialized diffusion furnace, with a semi-sealed liner in an open reaction tube, to achieve a stagnant inert ambient around the wafers. In the 'semi-closed box' experiment, the sample and the diffusion source were placed inside a graphite box, which was closed with screws and filled with an H_2 (3 %)/Ar (97 %) protective gas ambient. Some open-tube methods involve depositing the diffusion source, composed of, *e.g.*, a Zn-doped SiO_2 film on the sample surface. A protective layer of, *e.g.*, phosphosilicate glass (PSG) may then be deposited on top to protect the sample from surface damage during annealing. The additional protective layer may be omitted if an inert gas ambient is used during the anneal. [28]

The differences between the sealed ampoule diffusions listed in Table 1 are fairly minimal, as very similar methods were used in all cases. The differences seen are likely caused by differences in the volume of the ampoule and amount of $ZnAs_2$ source, as these affect the amount of As overpressure in the sealed container. Higher

As overpressure is known to reduce diffusivity of Zn in GaAs, so higher amounts of source material cause lower diffusivity.

The last two cases in Table 1 were not processed in a sealed ampoule, and they exhibit higher diffusivity due to the lower As overpressure and the large number of vacancies caused by escaping Ga atoms. [22, 25] The As overpressure is the lowest in the pure Zn case, and it also exhibits the highest diffusivity.

In order to make it easier to compare diffusivity numbers between experiments with differing Zn concentrations and As pressures, reduced diffusivity is used. This involves a transformation into electrically intrinsic conditions ($p = n = n_i$) and standard As pressure ($\mathrm{P_{As_4}} = 10^5$ Pa or 1 atm) using the following formula:

$$D^{\mathrm{eff}}_{\mathrm{Zn,r}} = D^{\mathrm{eff}}_{\mathrm{Zn}} \left(\frac{n_i}{C^{\mathrm{eq}}_{\mathrm{Zn}}}\right)^2 \left(\frac{P_{\mathrm{As_4}}}{10^5\ \mathrm{Pa}}\right)^{\frac{1}{4}}, \tag{2}$$

where $C^{\mathrm{eq}}_{\mathrm{Zn}}$ is the surface Zn concentration and $P_{\mathrm{As_4}}$ is the As pressure. Complete ionization of the acceptors ($p = C^{\mathrm{eq}}_{\mathrm{Zn}}$) is assumed. [29, 30] In some cases, only the transformation into intrinsic conditions is done, without the adjustment for $P_{\mathrm{As_4}}$, in which case the value is usually quoted as the intrinsic diffusivity. [31]

In the reduced form, the effective diffusivities reported in literature are bounded by

$$D^{\mathrm{eff}}_{\mathrm{Zn,r}}(n_i, 1\ atm) = 1.6 \times 10^{-2}\ e^{-\frac{2.98\ eV}{kT}}\ \mathrm{cm^2s^{-1}} \tag{3}$$

from above and

$$D^{\mathrm{eff}}_{\mathrm{Zn,r}}(n_i, 1\ atm) = 96.8\ e^{-\frac{4.07\ eV}{kT}}\ \mathrm{cm^2s^{-1}} \tag{4}$$

from below. A similar estimation can be derived for Ga-rich conditions by setting P_{As_4} to be along the Ga-rich solidus of the Ga-As system. The effective diffusivities in this case are bounded by

$$D^{\mathrm{eff}}_{\mathrm{Zn,r}}(n_i, \text{Ga-rich}) = 1.18 \times 10^{-6}\ e^{-\frac{1.64\ eV}{kT}}\ \mathrm{cm^2s^{-1}} \tag{5}$$

from above and

$$D^{\mathrm{eff}}_{\mathrm{Zn,r}}(n_i, \text{Ga-rich}) = 7.14 \times 10^{-3}\ e^{-\frac{2.73\ eV}{kT}}\ \mathrm{cm^2s^{-1}} \tag{6}$$

from below. [30] These are plotted in Figure 8 as a function of inverse temperature.

To use the reduced values plotted in Figure 8 to calculate diffusion depth, the effective diffusivity needs to be calculated from Equation 2 for the Zn concentration of the diffusion source and the As overpressure present during diffusion. The diffusion depth L_D can then be estimated as

$$L_D = \sqrt{D^{\mathrm{eff}}_{\mathrm{Zn}} t}, \tag{7}$$

where t is the diffusion time. In this work, this was used together with the diffusivity values reported above to predict diffusion depth in experimental samples. Doping density could then be estimated based on the measured electrical characteristics and the estimated diffusion depth.

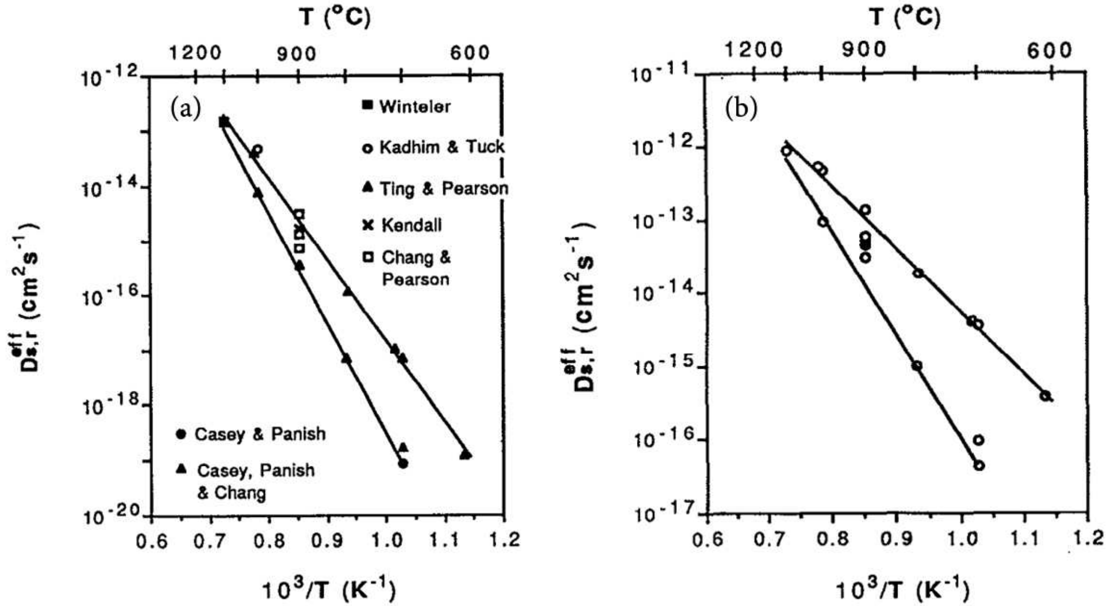

Figure 8: Reported range of the reduced diffusivity values plotted as a function of inverse temperature, with bounding fitted lines. Data reduced to conditions (a) $p = n_i$ and $P_{\mathrm{As}_4} = 1$ atm and (b) $p = n_i$ and P_{As_4} equal to that at the Ga-rich solidus of the Ga-As system. [30]

Doping profiles from the experiment in Ref. [22] can be seen in Figure 9. For the pure Zn case depicted in 9b, the diffusivity values listed in Table 1 apply to the top region of the kink and tail profile, the diffusivity for the tail is $1.47 \times 10^4 \times e^{2.84/kT}$.

2.4.2 Zn diffusion in other III-V semiconductors

Zn diffusion into other compound semiconductors is also of technological interest, as most practical optoelectronics devices are composed of a material system of at least two different materials. In the case of the GaAs-based structures investigated in this thesis, some materials that could be of interest are different compositions of AlGaAs and InGaP.

Results in the literature suggest that in the case of $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$, the diffusivity of Zn increases with increasing Al fraction. There are some conflicts in the reported results when it comes to the exact nature of the diffusion profile, however. Some sources report monotonically or almost monotonically increasing diffusivity as a function of Al fraction. [32, 33] Other sources suggest that some local maxima and minima exist in the diffusion depth as a function of Al fraction. [26] These conflicting results are most likely explained by differences in the diffusion conditions established in each experiment. As an example, Figure 10 shows diffusion results from two different experiments as a function of Al fraction. [23]

The figure indicates significantly higher diffusivity for the leaky-tube samples, regardless of Al fraction. This is related to the low As overpressure associated with such open-tube methods – as discussed in the previous section, low As overpressure

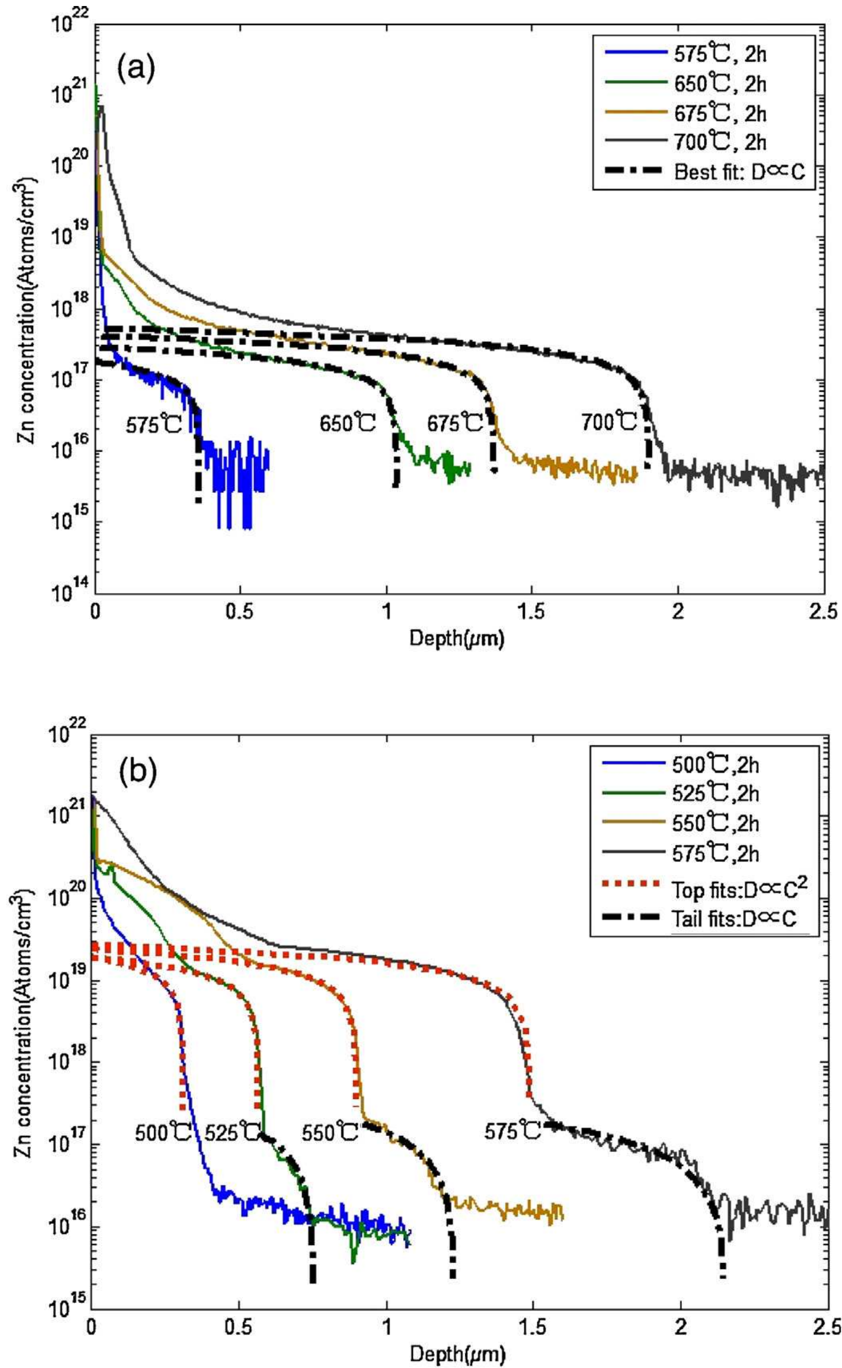

Figure 9: Zn diffusion profiles in GaAs at different temperatures for (a) Ga-rich conditions and (b) pure Zn source. [22]

generally leads to high diffusivity. The leaky-tube diffusion depth profile also differs in other ways from the sealed ampoule experiment. A slight dip around $x = 0.20$ can be seen in the sealed ampoule data, but the reduction is far less dramatic than that observed in the leaky-tube experiment. The initial reduction in diffusivity at low Al fractions is also not observed in the sealed ampoule experiment.

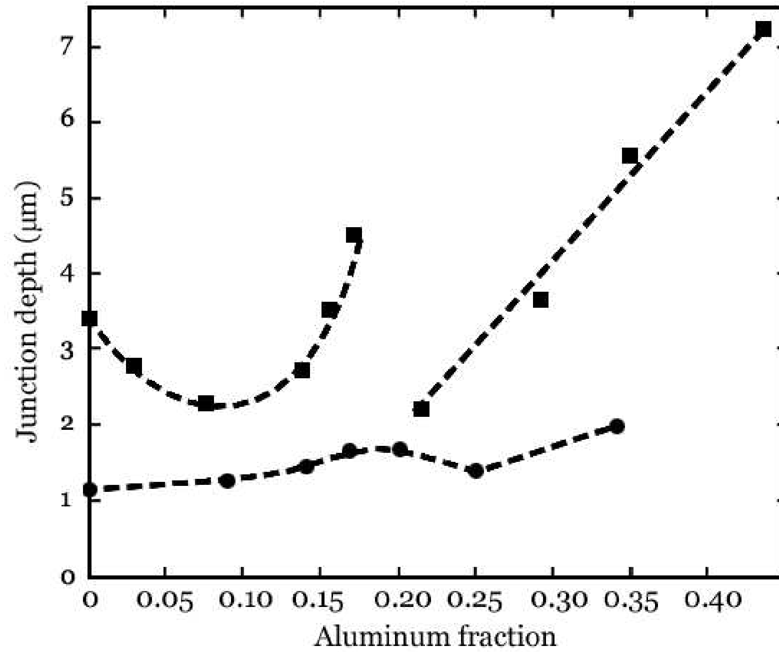

Figure 10: Zn diffusion depths as a function of Al fraction for AlGaAs samples annealed at 650 °C for one hour. The squares represent data from an open-tube diffusion experiment. [26] The circles represent data from a sealed ampoule experiment. [23]

The anomalous diffusion behaviour near $x = 0.20$ has been hypothesized to be caused by deep level defects known as DX centers, as these trap states have also been observed to begin forming when the Al fraction grows greater than 0.20. Possible mechanisms by which the DX centers themselves could affect Zn diffusion are electrostatic repulsion or strain fields in the material. It is also possible that the same underlying factors that cause DX centers to form also hinder Zn diffusion. [26]

One other material of interest for device applications is $In_{1-x}Ga_xP$. This compound has been studied less thoroughly than GaAs and AlGaAs, but some experimental results are available in the literature. These sources indicate that diffusivity of Zn into $In_{1-x}Ga_xP$ depends in an approximately linear fashion on x, such that diffusivity decreases with increasing Ga fraction. This is depicted in Figure 11. [34]

The basic mechanism for diffusion in both AlGaAs and InGaP is similar to that in GaAs, proceeding according to the substitutional-interstitial model. The reason that the diffusivity depends on material composition is that the different group III atoms have a different energy required to replace them by a Zn atom in the lattice. This leads to an effective activation energy that is dependent on the composition, and at a given temperature the composition with a lower activation energy for Zn diffusion exhibits higher diffusivity. [23, 34]

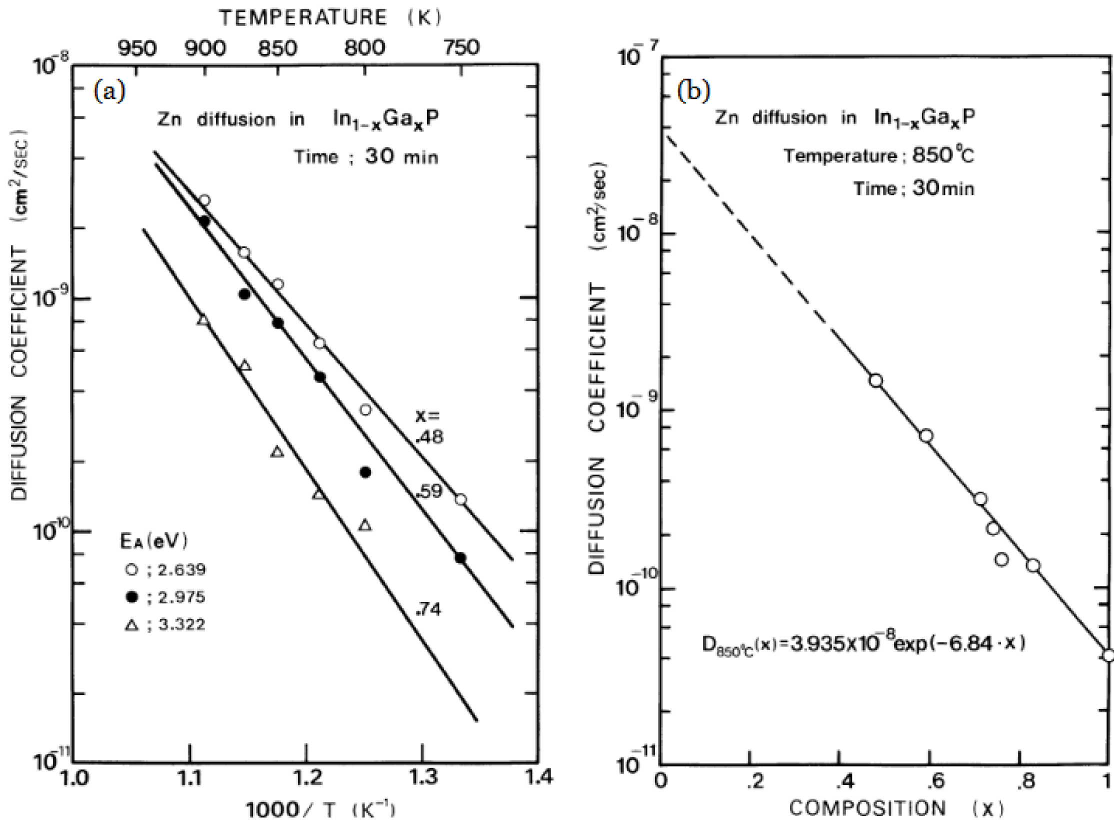

Figure 11: Zn diffusivity in $In_{1-x}Ga_xP$ as a function of (a) inverse temperature and (b) material composition. [34]

2.5 Characterization of doping

There are many methods available for characterizing impurity density and doping profiles in semiconductors. Most characterization techniques involve characterizing the electrical behaviour of the sample and using this data to calculate doping density. For a crude estimate of the doping density, a simple current-voltage measurement can be used to calculate the sheet resistance of the sample. This can then be used in conjunction with an estimated or measured diffusion depth to calculate the resistivity of the sample, which can in turn be used to obtain a rough estimate of the doping level of the sample. This method does not, however, give any information about doping type or diffusion profile.

A more sophisticated method for electrical characterization is the Hall effect method. This involves the same procedure as above for determining the sample resistivity, but measurements are also done in an applied magnetic field to obtain additional information about the charge carriers. As holes and electrons are deflected by the magnetic field, a voltage is induced in the direction perpendicular to the current. The polarity of this voltage depends on the carrier type, so this method also gives information about the type of doping (p-type or n-type) present, in addition to the doping density. Carrier mobility is also measured. [35]

The diffusion depth profile can be simply characterized by capacitance-voltage (CV) profiling. This type of measurement requires a depletion region to be present, so there must be a p-n junction or Schottky contact at the surface. The measurement involves varying the voltage across the junction while measuring the capacitance. The width of the depletion region varies as a function of the bias voltage, so this method allows one to obtain a depth profile of the dopant density in the sample. A variant of this method is electrochemical CV (ECV) profiling, where an electrolyte solution is used to form the Schottky contact at the surface. The bias voltage is kept constant and low, and depth profiling is instead achieved by electrolytic etching of the sample between measurements. The key advantage of this method is unlimited profile depth – in conventional CV, the maximum profile depth is limited by the electrical breakdown voltage of the material. In heavily doped materials, this can make conventional CV profiling impossible. [36]

Instead of using indirect electrical characterization methods, secondary ion mass spectrometer (SIMS) can be used to directly measure the dopant concentration of the sample. SIMS involves using an ion beam to sputter away atoms from the sample surface at a constant known rate and collecting the secondary ions into a mass spectrometer, where the atoms are separated based on mass and electric charge. By analyzing the amounts of different atoms recorded as a function of time, a depth profile of the material composition can be made. SIMS can be very precise, but calibration using well-characterized standards must be done for each sample in order to get good quantitative data. This makes the method slow and labour-intensive compared to the electrical methods. [36, 37]

In the literature, doping profiles in GaAs and other III-V semiconductors are most commonly measured using the SIMS [22, 25, 29, 38, 39] and ECV [26, 29, 40, 41] methods. There are also some examples where repeated Hall effect measurements with etching steps in between are used to obtain a doping depth profile. [41, 42]

2.6 p-n junctions

Combining p-type and n-type semiconductors results in one of the most fundamental structures in semiconductor technology: the p-n junction. This type of junction is a fundamental building block for devices such as solar cells, diodes, LEDs and transistors.

The basic structure of a p-n junction is very simple, consisting of a p-type semiconductor in contact with an n-type semiconductor. This is illustrated in Figure 12. Both sides of the junction may be made of the same material with different doping, or the materials on either side of the the junction may be different semiconductor materials entirely. In the former case, the junction is called a homojunction, and in the latter, a heterojunction. Typically, p-n junctions are formed by either selectively doping a bulk semiconductor (for example, diffusing a p-doped layer on an n-doped substrate) or epitaxially growing an n-doped layer on top a p-doped layer (or vice versa).

A schematic illustration and band diagram of a p-n junction can be seen in Figure 12. Upon the formation of the junction, electrons diffuse from the n-type side to the

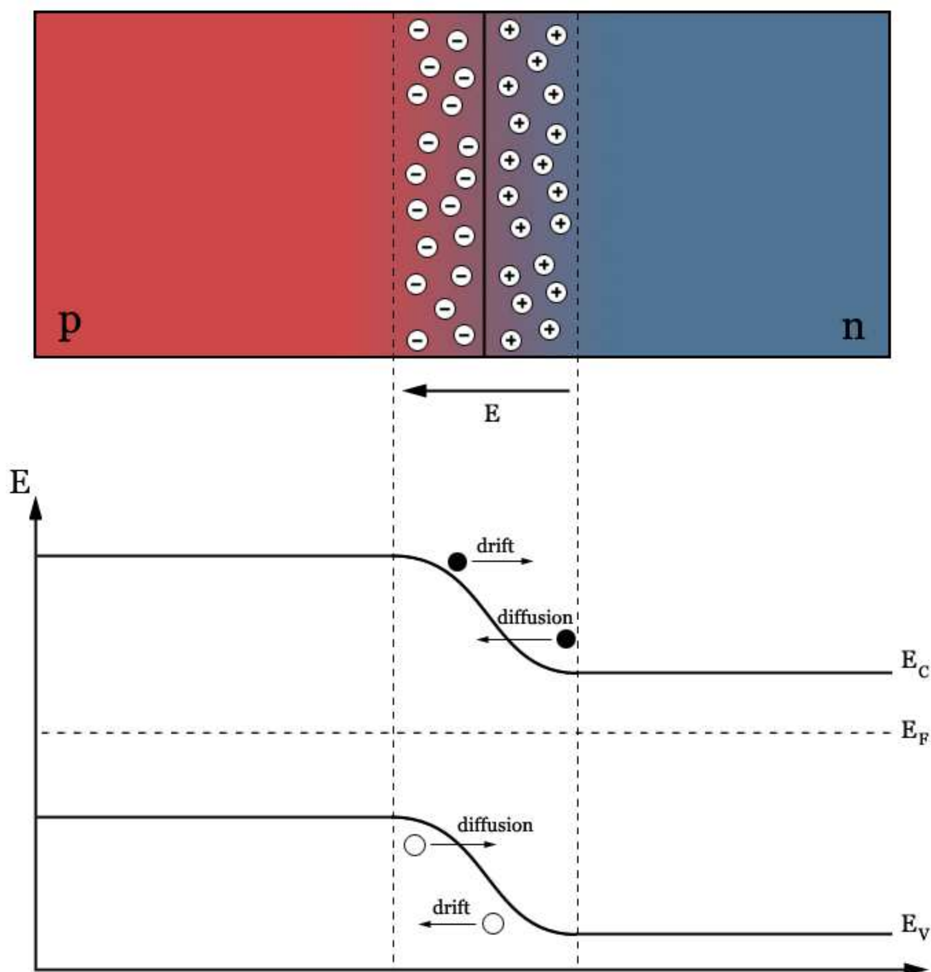

Figure 12: Schematic illustration of a p-n junction at thermal equilibrium. Diffusion and drift of carriers balance each other out, and a depletion layer with a built-in electric field (E) is formed.

p-type side, while holes diffuse in the opposite direction. This process leaves the dopant atoms on each side with no charge carriers to balance their charges, so an electric field forms at the junction. As the n-type side becomes negatively charged and the p-type side positively charged, the direction of the electric field is such that it exerts a force on the charge carriers in a direction opposite to the diffusion direction. At equilibrium, the carrier movement caused by the carrier concentration gradient and the opposing force caused by the the electric field at the junction cancel each other out.

At thermal equilibrium, there are no mobile charge carriers in the immediate vicinity of the p-n junction, which forms a so-called depletion region. As described above, the imbalance of charges cause an electric field to form in the depletion region,

and the potential difference associated with this field is called the built-in voltage.

If a voltage is applied such that the p-type side is at a higher potential, the p-n junction is said to be forward biased. In this arrangement, the applied voltage pushes the majority carriers on each side towards the junction, moving the charge-neutral area closer to the p-n interface and reducing the width of the depletion region. With a large enough forward bias, the potential barrier caused by the depletion region is small enough that it no longer effectively impedes the flow of majority carriers across the junction. The charge carriers that cross the p-n junction are typically eliminated by various recombination processes, where an electron in the conduction band transitions across the bandgap to fill a hole in the valence band. Even though the charge carriers are eliminated soon after crossing the junction to the side where they are minority carriers, current still flows through the structure. This happens because there is a flow of majority carriers towards the junction on both sides, and even though the carriers are moving in opposite directions, their charges having opposite signs means that a net current flows through the structure.

When the applied voltage is reversed such that the n-type side of the junction is at a higher potential, the applied voltage pulls majority carriers away from the interface. This results in the depletion region getting wider and the voltage across the junction getting higher. In this case, the junction is said to be reverse-biased, and only a small amount of current flows. This small current is called the leakage current, and is caused by thermally excited carriers in the depletion region. When the reverse bias grows large enough, electrical breakdown occurs, causing a large reverse current to flow. This happens when the electric field at the junction is large enough to either accelerate electrons to energies sufficient to generate additional mobile charge carriers via collisions with bound electrons (avalanche breakdown), or cause significant tunneling of electrons from the valence band to the conduction band (the Zener mechanism).

As charge carriers cross the p-n interface and recombine, an amount of energy corresponding to the bandgap energy must be dissipated as the electrons transition from a higher energy level to a lower one. In ordinary p-n junction diodes this energy is released as heat, but if the bandgap energy of the material is in the appropriate range, the excess energy can also be released by the emission of a photon of IR, ultraviolet (UV) or visible light. In this case, the p-n junction can act as an LED. However, this also requires that the bandgap of the material is direct, meaning that the minimum energy of the conduction band occurs at the same value of k (crystal momentum) as the maximum energy of the valence band. This makes radiative recombination, where the emission of a photon facilitates the transition between energy bands, more likely to occur. If the bandgap is indirect, radiative recombination can only happen if a phonon (a quantum of crystal vibration) is emitted or absorbed in the process to equalize the momentum of the hole and the electron before recombination. The fact that a phonon is required means that radiative recombination is unlikely in indirect bandgap materials, and the majority of recombinations occur through non-radiative processes, for example via defect states caused by grain boundaries or other crystal defects. This means that indirect bandgap materials make highly inefficient LEDs in most cases.

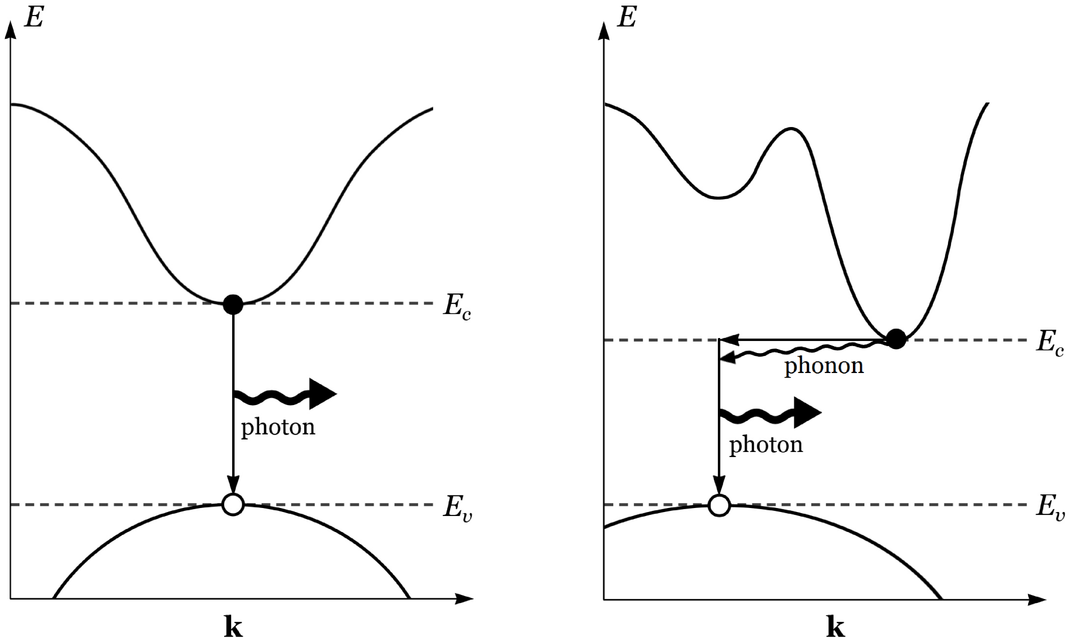

Figure 13: Schematic illustration of radiative recombination in materials with a direct (left) and an indirect (right) bandgap. If the bandgap is indirect, a transfer of crystal momentum, mediated by a phonon, is required in order to facilitate the emission of a photon.

2.7 Metal-semiconductor junctions

In order to make practical devices and characterize doped semiconductor samples, electrical contacts are usually needed, and these typically consist of one or several metal layers deposited on the semiconductor surface. At the metal-semiconductor junction, a potential barrier, called the Schottky barrier, is formed as charges move across the junction and the Fermi levels of the metal and the semiconductor line up. This is illustrated in Figure 14 for n-type semiconductor materials.

Naively, the Schottky barrier height can be predicted by the Schottky-Mott rule

$$\Phi_{\mathrm{B}} = \Phi_{\mathrm{metal}} - \chi_{\mathrm{semi}}, \tag{8}$$

where Φ_B is the Schottky barrier height, Φ_{metal} is the work function of the metal and χ_{semi} the electron affinity of the semiconductor. This formulation applies to n-type materials, and describes the difference between the edge of the conduction band and the Fermi level of the metal. Correspondingly, the Schottky barrier for p-type materials refers to the difference between the Fermi level of the metal and the edge of the valence band.

In practice, however, this idealized model rarely succeeds in accurately predicting the barrier height, as any pre-existing surface states on the semiconductor surface, or gap states induced by the bonding between the metal and the semiconductor, can have a greater effect on the barrier height than the metal's work function does. The

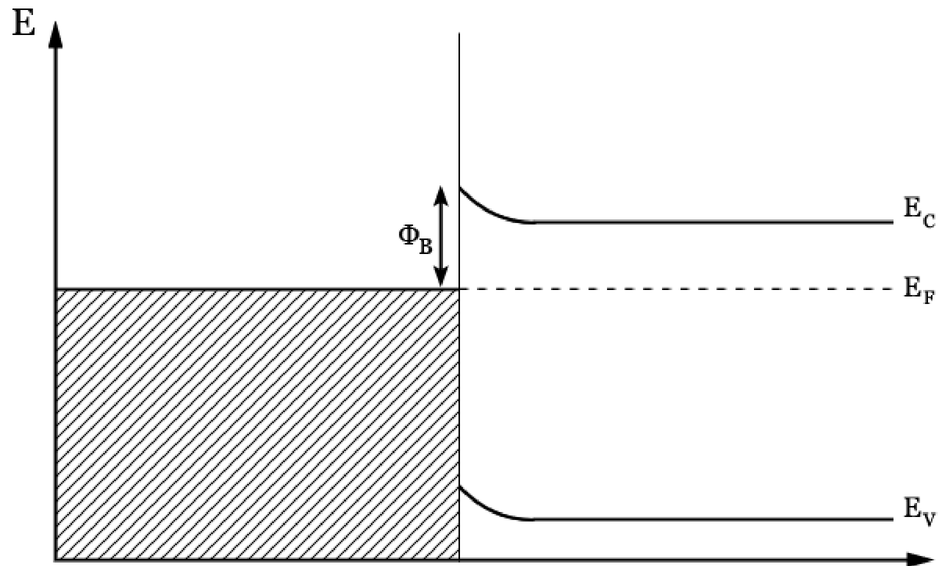

Figure 14: Band diagram of the junction between a metal and an n-type semiconductor. A Schottky barrier Φ_B exists between the metal Fermi level and the conductance band edge.

Schottky-Mott rule is, however, useful as a conceptual tool in understanding barrier height at a metal-semiconductor junction, and with some material combinations it can predict barrier height to a first approximation.

If the Schottky barrier is very low compared to the thermal energy kT, charge carriers can very easily pass between the metal and semiconductor in either direction. In this case, the junction is non-rectifying and the current-voltage curve is linear. In other words, the junction follows Ohm's law, and thus these types of contacts are called ohmic contacts.

If the Schottky barrier is high compared to the thermal energy, the junction is classified as a Schottky junction. In this case, the Schottky barrier causes a depletion region to form at the interface, as free carriers diffuse from the semiconductor to the metal to occupy lower energy states. This leaves the charged impurity atoms near the surface of the semiconductor, which induces an electric field at the junction that tends to counteract the diffusion of free carriers. When the drift and diffusion of electrons balance each other out, the junction is in thermodynamic equilibrium and the Fermi levels are equalized. This leaves a depletion region near the metal-semiconductor junction. This type of contact acts in a qualitatively similar way to a p-n junction: under forward bias, the Schottky barrier is lowered and current flows relatively easily from the semiconductor to the metal. Under reverse bias, the Schottky barrier gets higher and the depletion region widens, causing no current to flow. As with p-n junctions, breakdown occurs and a current starts flowing through the junction when the reverse bias grows large enough.

While Schottky diodes are classically regarded as unipolar devices, *i.e.*, devices where only one type of carrier is involved in current transport, significant minority carrier injection has also been reported in certain Schottky-type diodes. [43]

3 LED structures

The operation of all LEDs is based on radiative recombination, where electron-hole pairs recombine by emitting a photon. A simple p-n junction made of a suitable material can thus be used as an LED, but the efficiency that can be achieved with this arrangement is rather limited. Therefore, practically all commercial LEDs employ some additional structures intended to improve their efficiency. This chapter presents the most common types of structures found in commercial LEDs, as well as some novel experimental structures currently being researched by our group.

3.1 DHJ LEDs

The most common approach to improving the efficiency of an LED is to grow a separate epitaxial layer having a different material in between the n- and p-type layers to act as the active region of the LED, where most of the recombination and light emission takes place. This is known as a double heterojunction (DHJ) LED. If the active region consists of one or more layers that are so thin (nm scale) that the energy levels in them become quantized in the growth direction, the structure is called single- or multi-quantum well (SQW or MQW) LED. The principle is the same, regardless of whether the heterojunction consists of quantum wells or a thicker semiconductor layer – by making the active region its own layer and fabricating it out of a material with a smaller bandgap than the surrounding layers, charge carriers can be confined to the active region by the energy barriers caused by the bandgap mismatch. This is illustrated in Figure 15. This type of arrangement leads to a much better control of the densities of both types of charge carriers in the active region compared to a homojunction, where the carriers are spread out over several diffusion lengths. The time between radiative recombination events is thus more optimal throughout the active region, which results in improved efficiency. Another advantage of this double heterostructure arrangement is that the cladding layers surrounding the active region do not absorb a significant amount of light emitted from the active region, as the bandgap energy is larger than the energy of the emitted photons. [16]

The electrical contacts are also an important factor in the efficiency of an LED. Apart from effects such as series resistance and stray capacitances affecting the electrical performance of the LED, the contacts can also absorb some of the emitted light, reducing the extraction efficiency of the LED. One solution to this problem involves making the contacts from a material that is transparent to the wavelength of light emitted by the LED. Some often-used materials for transparent contacts are indium tin oxide (ITO) and aluminum-doped zinc oxide (AZO). Another approach that is common in modern commercial LEDs is to use a flip-chip arrangement, depicted in Figure 16, where both contacts are on the bottom of the LED. The active area is still between the p- and n-type sides of a p-n junction, but the n-type contact is placed adjacent to the active area, instead of on top of it. This arrangement involves etching through the active region to deposit the n-type contacts, but avoids the problem of the contacts occluding the light emitted from the active region. [16]

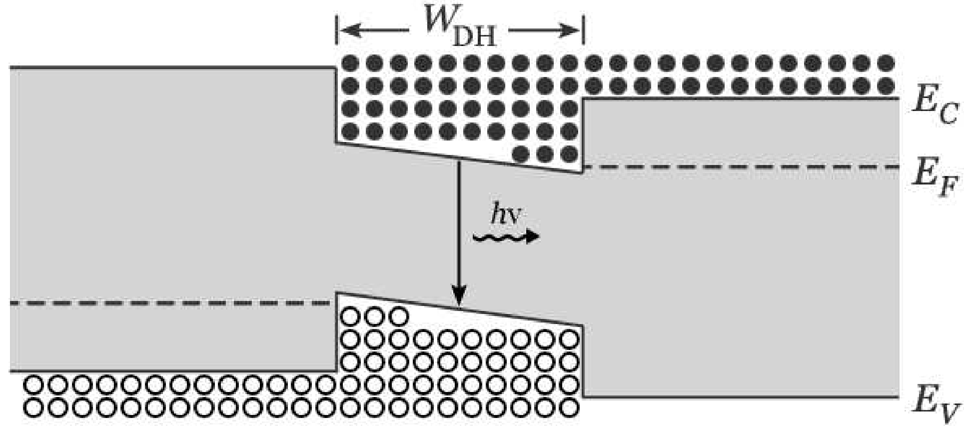

Figure 15: Schematic illustration of the band structure of a DHJ LED. W_{DH} refers to the thickness between junctions in the double heterostructure, h is Planck's constant and v is the frequency of the emitted photon.

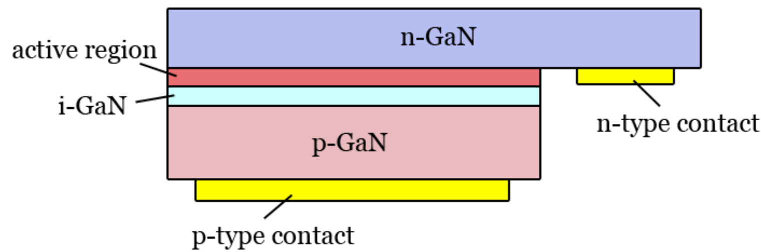

Figure 16: Schematic illustration of the flip-chip DHJ LED structure commonly used in commercial LEDs.

The flip-chip DHJ structure has set the standard for efficiency in commercial high-power LEDs. There are some limitations to the design, however. As mentioned above, the contact arrangement necessitates etching through the active region, reducing its size. It also relies on lateral current transport to inject carriers into the active region, which causes the current density to be higher near the contacts and gradually lower as the distance from the contacts increases. This phenomenon is known as current crowding, and it limits the performance of LEDs in several ways. First, it causes some parts of the active region to not be utilized optimally or at all because of the low number of injected carriers. At the same time, the areas near the contacts can have excessively high current density, which causes efficiency droop and Joule heating, reducing the efficiency and lifespan of the device. The first problem can be alleviated by designing the LED with a dense enough contact grid, which keeps the lateral distances between n- and p-type contacts small. However, the DHJ LED

design is such that achieving this would require etching densely spaced channels through the active region for the n-type contacts. [16, 44]

3.2 DDCT LEDs

One novel way to avoid the contacts absorbing the emitted light is to use diffusion currents to inject charge carriers into an active region that is outside the p-n junction. This current injection scheme was developed by our group, and LEDs that utilize it are called a diffusion-injected LEDs (DILED) or diffusion-driven current injection (DDCT) LEDs. The advantage of this scheme is that etching through the active layer is not required, which conveys a potential efficiency boost by increasing the volume of the active region while eliminating sidewalls, where non-radiative surface recombinations could take place. It has also been calculated that this current injection scheme could eliminate the problem of current crowding, which is one of the most significant sources of efficiency loss in high-power LEDs. This could also make it feasible to make large-area devices that have dense contact grids without needing to etch through the active region. [45]

Figure 17 shows an example of a GaN-based DILED where the active region is below the p-n junction and electrical contacts. This structure has been fabricated and tested successfully, and simulations indicate that very high efficiencies could be reached by optimizing the layer thicknesses and electrical contacts. This is a proof-of-concept structure – the ultimate goal is to move the active layer to the LED surface, with both contacts on the bottom face. One way this could be accomplished would be to use an epitaxial lift-off method to separate the device layer from the substrate. The measured efficiency of this DILED structure was also low due to the fact that the device layer compositions and thicknesses weren't fully optimized. These factors have a significant effect, as DDCT is more sensitive to layer thickness and doping than the standard current injection method used in traditional DHJ LEDs. [44, 46]

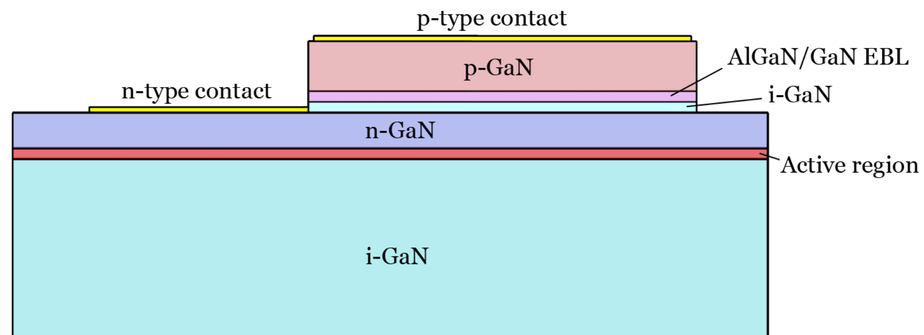

Figure 17: Schematic illustration of a DILED where the active region is below both contacts and the p-n junction. Current injection into the active region is driven by diffusion currents.

This thesis explores the possibility of utilizing Zn diffusion as a technique to

realize GaAs-based LEDs that incorporate the DDCT scheme described above. One possible device structure would involve alternating p- and n-type regions of GaAs, where p-type wells are diffused into an n-type substrate. This would form lateral p-n junctions in the GaAs layer, and these could be used to inject current into an active region on the surface. A proposed test structure with lateral p-n junctions is presented in Figure 18. One advantage to using diffusion doping to make the p-type wells is that it eliminates the need to etch through epitaxial layers. This has the potential to improve efficiency, as etching leaves exposed sidewalls that have a large number of surface states that cause non-radiative recombination losses. The effect is especially prominent in rough surfaces, such as those caused by dry etching processes, because of their larger surface areas.

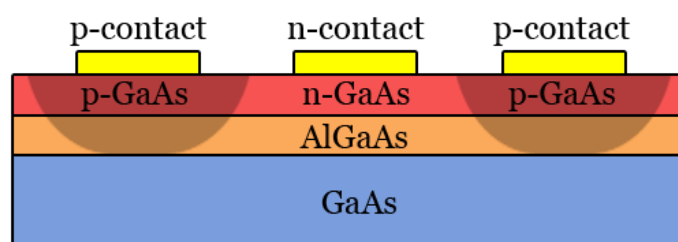

Figure 18: Schematic illustration of a GaAs based lateral p-n junction structure where the p-type wells (shaded areas in the illustration) are fabricated by diffusion doping.

An alternative approach to fabricating lateral junction LEDs that is explored in this work involves simply depositing ZnAu-based contacts onto an n-type substrate and using them to inject holes into the device. This approach could be used to develop efficient devices by using a structure such as the one shown in Figure 19. To enable the same benefits as in conventional DHJs the hole injection to the structure could take place through an optimized moderately doped AlGaAs layer, to be discussed in more detail in chapter 5.6.2.

Contacts of this kind are typically used to make ohmic contacts to p-type GaAs, but as is shown later in this work, they can also be used to achieve hole injection into n-type GaAs. There are two possibilities for the precise mechanism of this process. One is that some Zn atoms from the contact diffuse into the GaAs substrate, causing a shallow heavily p-doped layer to form near the contact. The metal layer forms an ohmic contact with this p-type layer and the device acts as a p-n junction LED. The other possibility is that the Schottky barrier at the metal-semiconductor junction is so high that the metal Fermi level is closer to the valence band edge, causing significant minority carrier injection into the n-type GaAs.

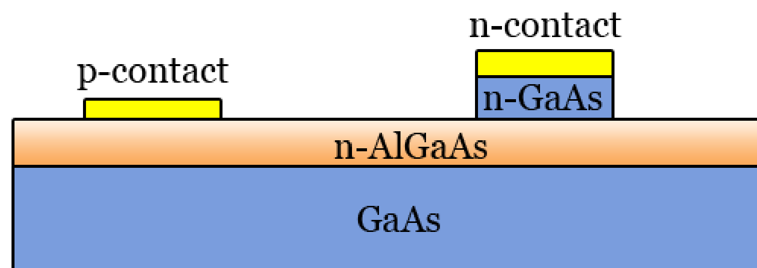

Figure 19: Schematic illustration of an alternative hole injection scheme that does not require diffused p-type wells. The AlGaAs layer has a graded composition to minimize the barrier to holes.

4 Fabrication and characterization methods

This section describes the methods used to fabricate and characterize the samples studied in this thesis. There are a number of different methods that are commonly utilized for fabricating diffusion doped GaAs samples, as described in the section 2.4.1. Initial experiments involved attempts to diffuse Zn into a GaAs sample by heating metallic Zn in a semi-sealed container with the sample. Due to poor success with this method, a spin-on glass approach was adopted, as it was deemed to be simple, fast and inexpensive enough to be workable in the limited timeframe of this thesis. The most common technique of using a sealed ampoule was discounted due to the amount of time, expense and effort required to acquire the tools, perfect the process and fabricate the samples.

Characterization methods were also chosen largely on the basis of what was available at the time the experimental work was conducted. As no ECV or SIMS results could be acquired within the timeframe of this work, CV measurements were attempted in order to establish the initial view of the doping profiles. Hall effect measurements were conducted to measure doping density and carrier mobility, as well as resistivity of the samples, which together constitute the most straightforward and powerful method to probe the results of the diffusion tests. Some initial electrical measurements were also conducted with a simple IV measurement setup, to establish whether and to what extent diffusion of dopants had occurred.

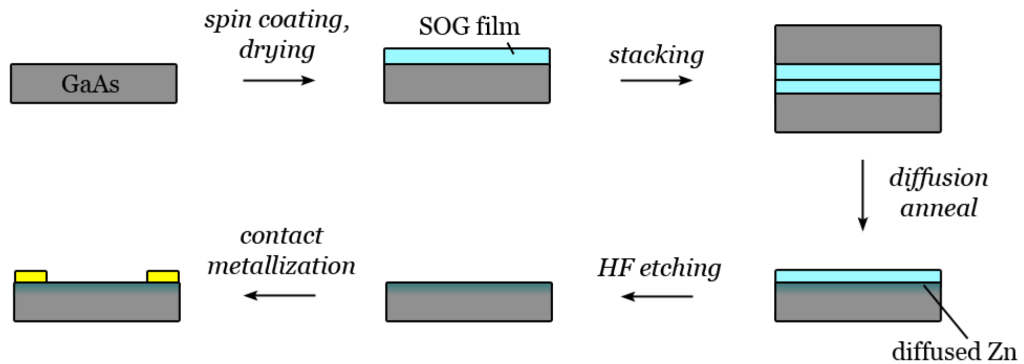

Figure 20: Process flow chart for the spin-on glass process used to fabricate the samples in this work.

The general process flow used for fabricating the samples is illustrated in Figure 20, with the preparation of the SOG emulsion omitted from the flow. The following chapters describe each step in more detail.

4.1 Spin-on glass preparation

Diffusion doping of the samples was achieved by using a spin-on glass (SOG) method. The method involves dispersing SiO_2 and Zn atoms in a solvent and spin-coating the

resulting emulsion onto the sample. After drying the film, the Zn atoms are diffused into the sample by annealing. The SOG film is then removed from the sample surface by etching in hydrofluoric acid (HF).

The SOG emulsion was prepared from fumed silica powder with a surface area 175-225 m^2/g and an average particle size of 0.2–0.3 µm. The fumed silica was dispersed into an ethanol/water solution by manual stirring and ultrasonication in a fume hood. Upon adding the silica powder, the solution becomes highly viscous, taking on a consistency similar to wet sand. Continued stirring while applying ultrasonic energy thins the solution until a dilute gel-like consistency is reached. The best practice for adding the silica was found to be to add it in two or three increments, stirring the solution between each in an ultrasonic bath until it looked visually homogenous. This was found to reduce clumping and shorten total stirring time. It also caused more effective wetting of the silica powder, preventing the extremely fine dust from scattering into the air during stirring. Once the full amount of silica had been added, the solution was stirred for 5 minutes under ultrasonication. The total stirring time for each batch was approximately 10 minutes.

A solution of ethanol and water was used to disperse the silica for two reasons. First, the stability of silica suspensions in a mixture of water and ethanol is greater than that in pure ethanol. [47] Secondly, a purely ethanolic solution would evaporate too fast in the spin-coating stage, leading to uneven and inconsistent results. Adding 10–20 % water slows down the evaporation sufficiently to allow the diffusant solution to spread evenly to the entire sample surface before all liquids have evaporated.

Zinc nitrate hexahydrate was used as the Zn source in the SOG. The dopant was added into the SOG solution by first dissolving the nitrate in ethanol, and then stirring this into the silica suspension prepared in advance. The amount of Zn nitrate solution can be varied to tune the ZnO/SiO_2 ratio and achieve the desired doping density. The different dopant densities and dilution ratios used in this work are listed in section 5.2, Table 2.

4.2 Spin coating and diffusion anneal

The SOG emulsion was deposited onto chips cleaved from a GaAs wafer by spin coating at 3000 rpm for 20 s. Diluting the solution with ethanol is typically required to achieve a sufficiently thin coating of 200-900 nm. Thicker films than this have a tendency to form cracks during the annealing steps, due to the difference between the thermal expansion coefficients of the film and the substrate. This can lead to uneven doping and substantial surface damage to the samples. The sample was then dried in a furnace in air ambient for 30 minutes or more at 250 °C to evaporate any remaining water and solvents. This densifies and stabilizes the film, which minimizes the probability of cracking and out-diffusion of Ga, As and Zn atoms during the diffusion bake.

The next step in the diffusion doping process is the diffusion anneal, which drives in the dopant atoms from the SOG film. This was performed in a quartz tube furnace in a nitrogen ambient at 600–650 °C, with varying diffusion times. The samples were annealed either face up on a dummy wafer, or stacked with another sample such that

the coated sides were facing each other. This stacking arrangement was found to help in reducing surface damage, as it suppressed out-diffusion of atoms from the sample surface.

The final step in the diffusion process was to remove the spin-on glass coating from the surface of the sample. This was done by etching the samples in 5 % HF for one minute. The HF etches away the SiO_2 film and leaves the sample surface clean.

4.3 Contact metallization

After stripping the diffusant layer from the sample surface with HF, electrical contacts were deposited in order to facilitate characterization of the samples. The contacts consisted of either elemental indium or a stack composed of layers of ZnAu alloy and Zn.

The layered contacts consisted of 5 nm of ZnAu alloy, 10 nm of Zn, and 95 nm of ZnAu. The ZnAu layers were deposited by electron beam evaporation from a ZnAu source, while the Zn layer was thermally evaporated from a metallic Zn source in the same vacuum chamber. A shadow mask was used to pattern the contacts as required. After evaporation, the samples were annealed for 5 minutes at 400 °C in a nitrogen ambient. This contact arrangement was found to reliably produce good ohmic contacts to p-type GaAs, which is especially crucial for making reliable Hall effect measurements.

The indium contacts were deposited by simply pressing a piece of indium metal onto the sample. The metal piece deforms and readily adheres to the sample surface. After this, the sample was placed on a hot plate at 300 °C for approximately two minutes to anneal the contacts. This method is a fast and simple way to fabricate contacts for characterization purposes. The contacts are mechanically rather weak, electrically suboptimal and susceptible to corrosion, but these considerations weren't deemed critical for the purposes of this work. Ohmic indium contacts could be fabricated for both n- and p-type GaAs, but the results were less consistent compared to the evaporated contact scheme.

4.4 Electrical characterization

Characterization of the samples was performed primarily using IV, CV and Hall effect measurements. Initial samples were fabricated with two contacts to perform the first rudimentary conductivity measurements, but later samples had four contacts to facilitate Hall effect measurements using the van der Pauw method. CV measurements were performed on p-n samples using two contacts, one on the p-type side and one on the n-type side.

4.4.1 IV measurement

The initial characterization of the first samples was performed using simple current-voltage (IV) measurements. This involved using a four-point probe setup as depicted in Figure 21. The outer (source) leads are used to supply a current through the

material while the inner (sense) leads are connected to an instrument that measures the voltage across the sample. The reason for using this arrangement is to minimize the effect that the resistance of the leads and contacts have on the measurement. As almost no current runs through the sense leads, the voltage drop in them is negligible. Thus, only the voltage drop across the sample itself is measured.

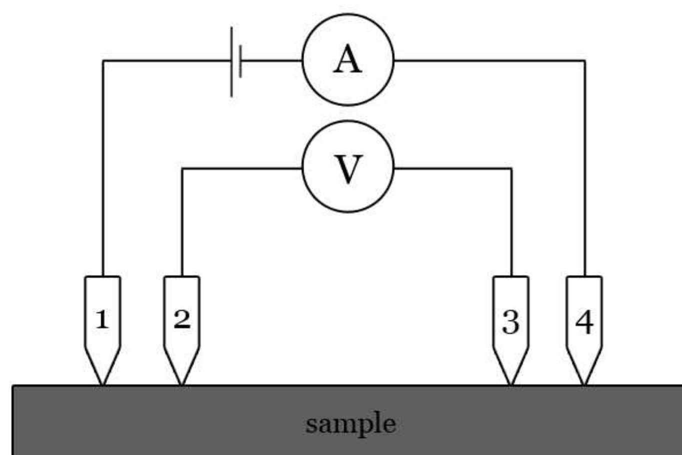

Figure 21: Schematic illustration of the four-point probe setup. Current is supplied through the outer source leads, labeled 1 and 4. The inner sense leads, labeled 2 and 3, measure the voltage across the surface. Contact with the sample is made by probe needles at the ends of the leads.

Two-terminal measurements were also employed for samples which had contacts on the top and bottom faces. This setup involved contacting the top contact with a probe needle, while the bottom contact was connected via the conductive chuck that the sample was resting on. The measurement setup is otherwise identical to the four-point probe, but the same leads are used to both supply current and measure the voltage, so the lead resistances affect the results to a degree. However, as the purpose of these measurements was mainly to assess the qualitative IV behaviour of the samples, not to acquire precise resistivity values, the precision of the two-terminal method was adequate for this purpose.

The shape of the IV curve offers some insight into a sample. A linear IV curve implies that the contacts and the sample itself approximately follow Ohm's law. This is an important factor in Hall effect measurements, for example, where Ohmic contacts are required to ensure accurate results. A Schottky barrier will cause the sample to be rectifying, with a threshold voltage for conductivity in the forward direction. In the case of an n-type sample with a diffused p-type layer on top, a suitable diode-like IV curve can confirm that the doping has been successful and a layer of the sample has been converted to p-type.

With the current and voltage data, the resistance of the sample can be calculated from Ohm's law. When measuring thin films, the four-point probe can be used to determine the sheet resistance of the sample, but it cannot be used to accurately

determine the doping profile, dopant concentration or carrier mobility in the sample. It also does not indicate whether the majority charge carriers are holes or electrons. To characterize these aspects of samples, Hall effect measurements and CV profiling were used.

4.4.2 Hall effect

Placing a conductor with a current running through it in a magnetic field causes a voltage across the sample that is perpendicular to both the direction of the current and the magnetic field lines. This is because the magnetic field exerts a force on the moving charge carriers in the conductor, pushing them in a direction that is perpendicular to both the magnetic field and current flow. This causes a greater concentration of charges at one end of the conductor, and thus a potential difference, called the Hall voltage, is formed across the sample. Measuring this voltage is the basis of the Hall effect measurement method, enabling access to analyzing the carrier mobility and concentration. The effect is illustrated schematically for a bar-shaped conductor in Figure 22.

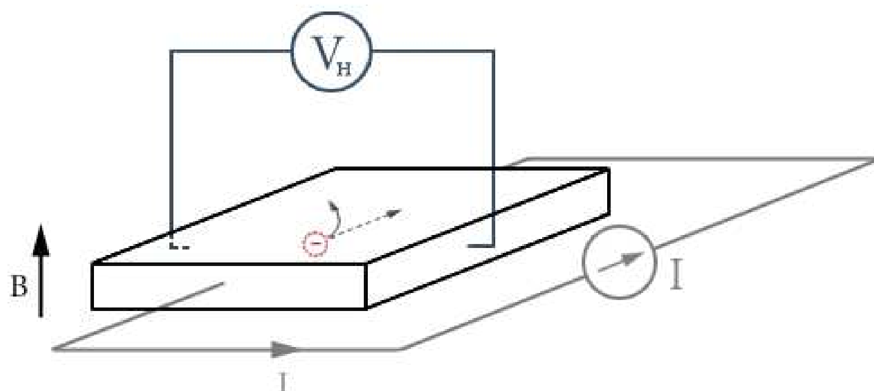

Figure 22: Schematic illustration of the Hall effect in a bar-shaped conductor. The magnetic field (B) causes the moving charge carriers in the conductor to follow a curved path, resulting in a Hall voltage (V_H).

While bar-shaped samples can be used for Hall measurements, they do have a number of disadvantages. Most importantly, the measurement results are especially sensitive to any variations in the shape and dimensions of the sample and contacts. Thus, the exact width of the bar and the distance between the contacts must be known in order to obtain accurate resistivity values.

For these reasons, the resistivity, carrier concentration and carrier mobility of thin film samples is usually measured using samples where four contacts are placed on the sample surface along the perimeter of the sample. This type of sample geometry is often called the van der Pauw geometry, after the conformal mapping method developed by van der Pauw. [48] Some examples of van der Pauw samples are illustrated in Figure 23. Using this method, it is possible to determine resistivity,

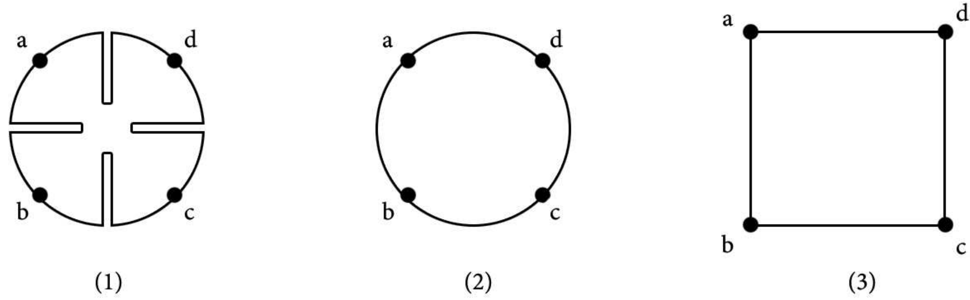

Figure 23: Three typical van der Pauw sample geometries: (1) cloverleaf, (2) disc, and (3) square. The samples fabricated for this work utilized the square geometry.

carrier concentration and mobility of any arbitrarily shaped flat sample, given the following conditions are met:

- The contacts are on the circumference of the sample
- The contacts are sufficiently small
- The sample is of uniform thickness, and
- The sample is singly connected (no geometrical holes).

The contacts must also be ohmic, as any rectifying behaviour would lead to asymmetric voltage results when the polarity of the injected current is reversed. If the conditions are met, the resistivity of the sample can first be determined without applying the magnetic field using the expression

$$\rho = \mathrm{Fd}\frac{(\mathrm{V_{da2}} - \mathrm{V_{da1}} + \mathrm{V_{cd2}} - \mathrm{V_{cd1}})}{\mathrm{I}}, \tag{9}$$

where F is a geometrical correction coefficient, d is sample thickness, I is a constant current, and $\mathrm{V_{xy1/2}}$ is the voltage between contact x and y with forward (1) or backward (2) injection current.

The coefficient F describes the shape of the sample. It is a function of the ratio $\frac{\mathrm{R}_{AB,CD}}{\mathrm{R}_{BC,DA}}$, where $\mathrm{R}_{AB,CD}$ is defined as the potential difference between contacts D and C per unit current between A and B. Thus, the ratio can be understood as a sort of aspect ratio that describes how resistive the sample is in the horizontal direction compared to the vertical direction. For a square sample with perfectly uniform resistivity, F is unity. The value of F as a function of the ratio $\frac{\mathrm{R}_{AB,CD}}{\mathrm{R}_{BC,DA}}$ is plotted in Figure 24.

An advantage of this method is that relatively simple geometries can be used and there is no need to measure sample size or distance between contacts. This eliminates

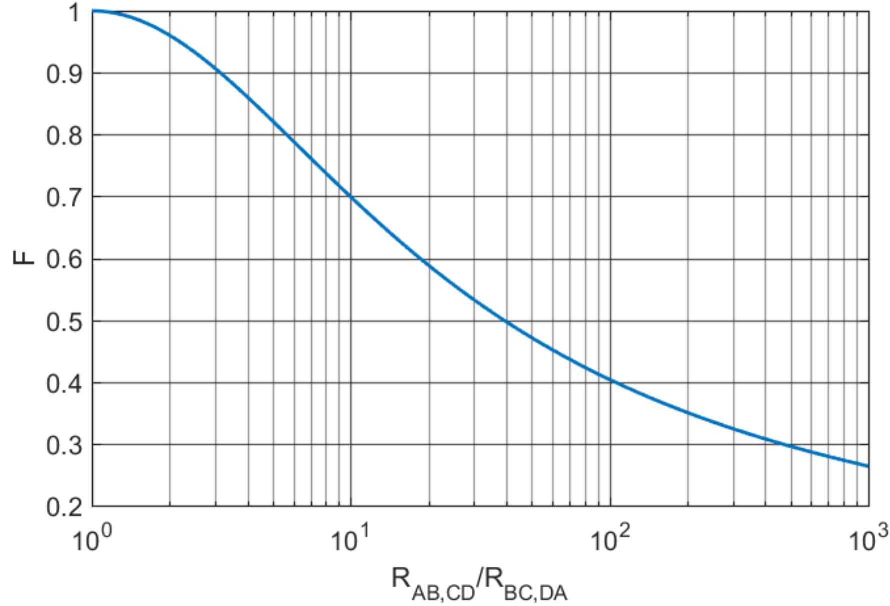

Figure 24: Van der Pauw factor F as a function of $\frac{\mathrm{R}_{AB,CD}}{\mathrm{R}_{BC,DA}}$.

any measurement error caused by inaccurate geometry measurements. The error caused by the electrical contacts having a finite size can be reduced by using the cloverleaf geometry, depicted in Figure 23(a). Such a sample geometry reduces the effect of contact size, as the current from each of the contacts must pass through the relatively small area in the center, making the effective contact size small.

To measure doping density and carrier mobility, new measurements are made with the setup described above under an applied magnetic field. A constant current is injected across the sample between contacts a and c, and the Hall voltage caused by the applied magnetic field is measured between contacts b and d. The measurement is repeated with the direction of the current reversed. Finally, this sequence of measurements is repeated with the polarity of the applied magnetic field reversed. Using the results from these measurements, the Hall coefficient $\mathrm{R_H}$ can be calculated from the expression

$$R_H = \mathrm{d}\frac{(\mathrm{V_{mbd2}} - \mathrm{V_{mbd1}} + \mathrm{V_{-mbd1}} - \mathrm{V_{-mbd2}})}{\mathrm{B\ I}}, \tag{10}$$

where d is sample thickness, $\mathrm{V_{\pm mbd1/2}}$ is the measured voltage between b and d under an applied magnetic field (sign of subscript denotes field polarity) and constant current between a and c (1 for forward and 2 for backward injection current), B is the applied magnetic flux density and I is the magnitude of the injected current.

A positive Hall coefficient indicates that the majority carriers in the material are holes, *i.e.*, the material is p-type. Correspondingly, a negative Hall coefficient indicates that the material is n-type. With access to the Hall coefficient, carrier density can be calculated from the expression

$$N = \frac{1}{q\mathrm{R_H}}, \tag{11}$$

where q is the elementary charge. Carrier mobility can likewise be calculated using the Hall coefficient and resistivity ρ, with the expression

$$\mu = \frac{\mathrm{R_H}}{\rho}. \tag{12}$$

4.4.3 CV measurement

Capacitance-voltage (CV) characterization involves varying the voltage across a Schottky diode or p-n junction while measuring the capacitance across it. As the voltage is varied, the width of the depletion region changes and this causes a measureable change in capacitance. Depletion region width is also affected by doping density, with higher doping densities leading to lower depletion width and vice versa. This makes it possible to determine the doping profile from the capacitance-voltage behaviour of the sample.

In a conventional CV characterization setup, a Schottky barrier is formed at the surface of the sample, either by using a deposited metal contact or a mercury probe. A reverse DC bias voltage V_A is applied to this contact, which establishes a space-charge region of width W. A small-amplitude AC signal (typically 10 to 20 mV at 10 kHz to 1 MHz) v_{ac} is superimposed onto this signal, which causes the space-charge region width to vary slightly. This can be used to calculate the capacitance response to the change in voltage, and ultimately the free carrier density. Assuming a p-type Schottky barrier and modelling the system as a parallel plate capacitor, we get the acceptor density

$$N_A = -\frac{C^3}{q\epsilon_r\epsilon_0 A^2 dC/dV} = \frac{2}{q\epsilon_r\epsilon_0 A^2 d(1/C^2)/dV}, \tag{13}$$

where C is capacitance, V is the applied voltage, q is the carrier charge, ϵ_r is the dielectric constant, ϵ_0 is the vacuum permittivity and A is the area of the device. This equation assumes total depletion of majority carriers in the space-charge region and perfect charge neutrality beyond it. The effect of minority carriers is neglected. [35]

For the width of the space-charge region as a function of capacitance, we get

$$W = \frac{\epsilon_r\epsilon_0 A}{C}. \tag{14}$$

These equations can be used to establish the doping profile from the CV measurements at different DC bias voltages. The slope dC/dV of a $C - V$ curve or the slope $d(1/C^2)/dV$ of a $1/C^2 - V$ curve is used to obtain the doping density. The latter is the preferred method, as the $1/C^2 - V$ curve more readily shows any changes in the doping profile. This can be seen in Figure 25a, where a clear discontinuity can be seen around $V = 3$ in the $1/C^2 - V$ curve, but this is hard to tell from the $C - V$ curve. [35]

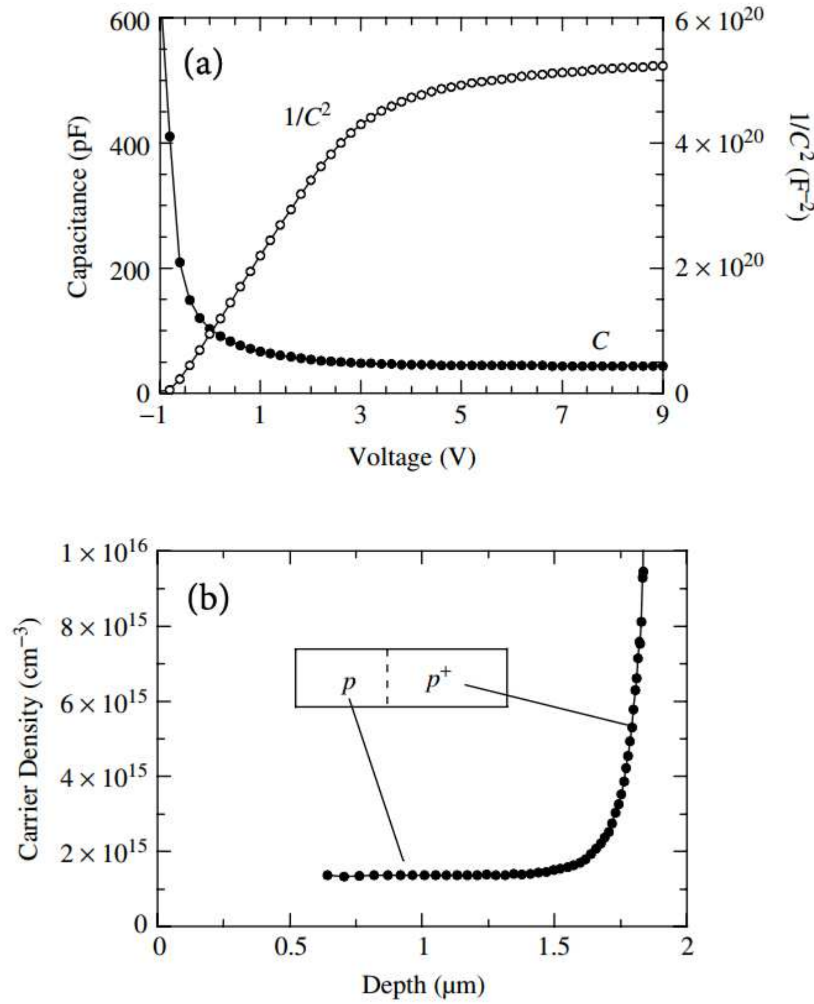

Figure 25: CV measurement results for a Si pp^+ junction: (a) the $C-V$ and $1/C^2-V$ curves and (b) the carrier density as a function of depth. [36]

Equation 14 gives the depth at which the doping density is evaluated. As such, it can be used to calculate the doping density as a function of depth, as seen in Figure 25b. The equation only works in this form in the case of a Schottky junction or an asymmetrical p-n junction, where one side of the junction has a doping density more than 100 times that of the other side. This is because in these cases, the spreading of the space-charge region into the metal or the more heavily doped side of the p-n junction is totally negligible and there is no ambiguity about the depth of the measurement. In other cases, the space-charge region spreads into both sides of the junction and both doping density and depth measurements will be much less accurate unless a correction is made to the equations. It is, however, not a simple correction to make, and it has been suggested that no unique doping profile can be derived from the measurements in this case, unless the doping profile of one side of the junction is already known. [36, 49, 50]

It should be noted that as this method measures changes in capacitance caused by the moving charges in the sample, *i.e.*, the majority carriers, it measures the carrier density instead of the dopant density. In a uniformly doped sample these would be equivalent, but in non-uniformly doped samples the free carrier density changes occur less abruptly than the doping density, so the profiles are slightly different. There are computational methods, based on more sophisticated models than the depletion model used here, that can correct for this effect to some degree. [36]

5 Results and discussion

This section examines the experimental results from each stage of sample processing and characterization. First, the different sample types are presented. In the next section, SOG solutions and process parameters used for the spin-coating are discussed, and the results are examined. After this, the effects of different annealing conditions to the diffusion doping results are examined. Lastly, the IV, CV and Hall effect measurements are presented for representative examples of three types of sample: a diffusion doped intrinsic GaAs sample, a diffusion doped n-type GaAs sample and a sample with ZnAu/Zn/ZnAu contacts deposited directly on an n-type GaAs substrate.

5.1 Samples

All of the samples fabricated for this thesis used 50 mm GaAs wafers as the substrate. Approximately square chips were cleaved from the wafer using a diamond scribe. These chips were then processed according to the procedure described in chapter 4. After the diffusion anneal and SOG film stripping, the diffusion doped samples were typically cleaved into smaller squares, in order to obtain more samples for experimenting with different contact types, or to remove edge areas that were damaged during the anneal.

Most of the experimental work, including all of the development work for the SOG process, was performed with undoped double-side polished GaAs wafers. The first diffusion tests were performed using undoped samples, as it was more straightforward to measure whether diffusion had taken place from an insulating substrate. The first samples were fabricated with two evaporated contacts, with later samples having four evaporated or indium contacts in the corners. The IV and Hall effect measurement results from these samples can be seen in section 5.4.

After successful doping was achieved with undoped samples, diffusion doping of n-type GaAs was attempted. Chips were cleaved from an n-type single side polished wafer with a doping density of 10^{17} cm^{-3}, and the samples were processed as above. Square samples with indium or evaporated contacts were fabricated for Hall effect measurement. Rectangular samples with contacts on the top and bottom were fabricated to measure IV and CV characteristics. The IV, CV and Hall effect measurements from these samples are presented in section 5.5.

Finally, samples with 200 µm diameter circular ZnAu/Zn/ZnAu contacts evaporated directly on the surface of a pristine n-type substrate through a shadow mask were fabricated. Light emission from this structure was observed using an IR camera, and the IV characteristics were measured. The results from this sample are presented in section 5.6.

5.2 Spin-on glass coating

Different formulations of SOG emulsion were prepared, with varying molar concentrations of ethanol, zinc nitrate, silica and water. Table 2 lists the molar compositions

of the different batches of SOG emulsions prepared and used for coating samples, along with the ZnO/SiO_2 ratio of each.

Table 2: Spin-on glass solutions used and their chemical compositions.

Solution	Ethanol content (wt%)	ZnO content (Mol)	SiO_2 content (Mol)	ZnO/SiO_2 ratio
Sol 1	68.4	0.0185	0.0832	0.222
Sol 1.1	77.2	0.0102	0.0458	0.222
Sol 1.2	79.5	0.00986	0.0444	0.222
Sol 2	71.8	0.0113	0.0389	0.291
Sol 2.1	71.8	0.0170	0.0583	0.291
Sol 3	79.6	0.00485	0.0166	0.291

As the table shows, different amounts of ethanol dilution were experimented with until an optimal layer thickness was achieved. A thick layer is generally preferable to prevent out-diffusion and increase the availability of zinc at the sample surface, but the different thermal expansion coefficients of the film and the GaAs substrate can cause cracking in the annealing steps if the layer is too thick. Thus, the layer should be thick enough to protect the sample surface and act as an effectively infinite diffusion source, but thin enough to survive the strain caused by the annealing steps – in practise, thickness values below 1 µm were found to produce satisfactory results. The film thickness was found to decrease in an approximately linear fashion as a function of ethanol dilution. This is plotted in Figure 26, and is consistent with results in the literature. [51]

The initial coating emulsion (Sol 1) was found to be much too thick, with severe surface cracking seen in the film after annealing. This can be seen in Figure 27. After removing the film, surface damage on the sample itself was observed as a darkening and roughening visible with the naked eye. Pits and roughness were also observed on the surface using SEM.

After diluting Sol 1 with ethanol to make Sol 1.1, the coating thickness was reduced from around 4 µm to around 1.4 µm. Diluting the solution further to produce Sol 1.2 reduced this to around 900 nm, and the amount of cracks in the film was dramatically reduced, as seen in Figure 27. Some cracks could still be seen in the thicker parts of the film around the edges, but the bulk of the film was relatively uniform. After the diffusion bake, samples coated with the diluted solution were found to have only a modest increase in conductivity, likely due partially to surface damage and partially to the rather small fraction of Zn in the SOG.

A larger Zn fraction was attempted for Sol 2, but all attempts to spin-coat with this formulation failed, producing very uneven films with radial striations and agglomerations of particles several microns in diameter. This can be seen in Figure 28.

A possible explanation for these results could be that the SiO_2 particles were not completely dispersed in the solution. This would cause the solution to be inhomogenous, resulting in poor quality spin-coated films. There are many factors that could have caused this. The stirring of the silica into the water/ethanol solution

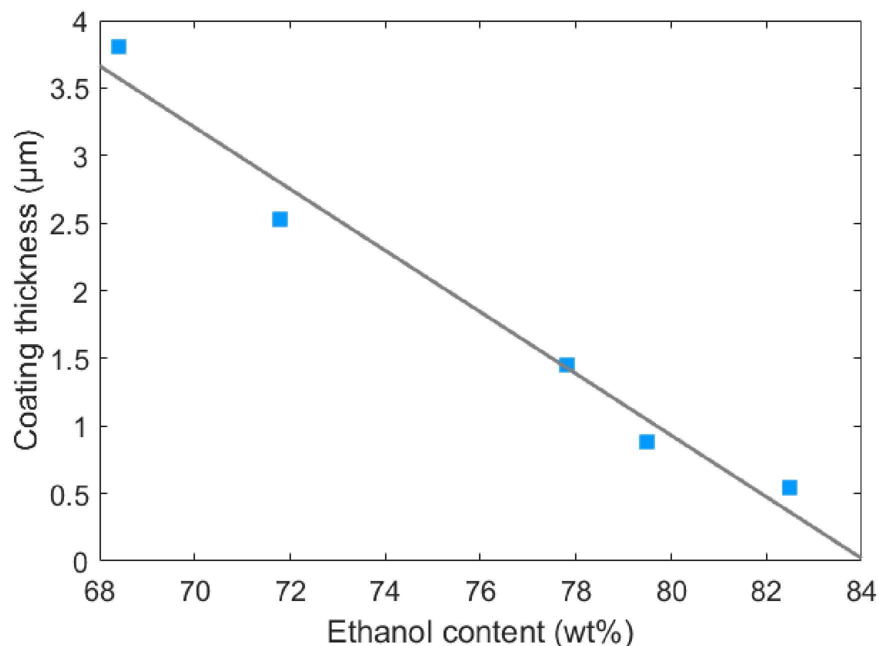

Figure 26: Average SOG film thickness (after drying) as a function of ethanol content. Data points are plotted as blue squares, with a linear fit in grey.

was done by hand, so some variation between each batch of solution was inevitably introduced into the process. Developing a repeatable process for dispersing fumed silica into aqueous and ethanolic solutions is notoriously difficult even when using automated industrial processing equipment, and this is a problem that has been studied extensively. [47, 52] The batch of Sol 2 was also smaller in volume, which may have reduced the efficiency of stirring as a greater fraction of the solution was stationary during stirring, adhering to the walls of the container.

Another difference between Sol 2 and the previous solutions was that the nitrate solution was added to the SiO_2 dispersion immediately, whereas in solution 1 the dispersion was allowed to settle overnight before adding the Zn nitrate. Some sources recommend allowing the solution to rest before diluting it or adding any dopant solutions, typically for 24 hours. [53,54] Others do not consider a rest period necessary, or neglect to mention it. [51, 55] The subsequent solutions were allowed to rest for at least 12 hours before adding the nitrate. This improved the success rate, but some variation between batches remained and occasional batches still failed to produce uniform, continuous coatings.

For Sol 2.1, both the amount and intensity of mixing were increased in the silica dispersion stage. This resulted in a uniform and repeatable composition, but slightly excessive coating thickness, in the 2–3 µm range. The ethanol content was increased for Sol 3, resulting in a coating thickness of approximately 0.7 µm. This was found to behave well in annealing steps, with no visible cracking or peeling. Sol 3 was also found to provide the best diffusion doping results, and thus it is the solution that was used for fabricating many of the samples described in the results section. All of

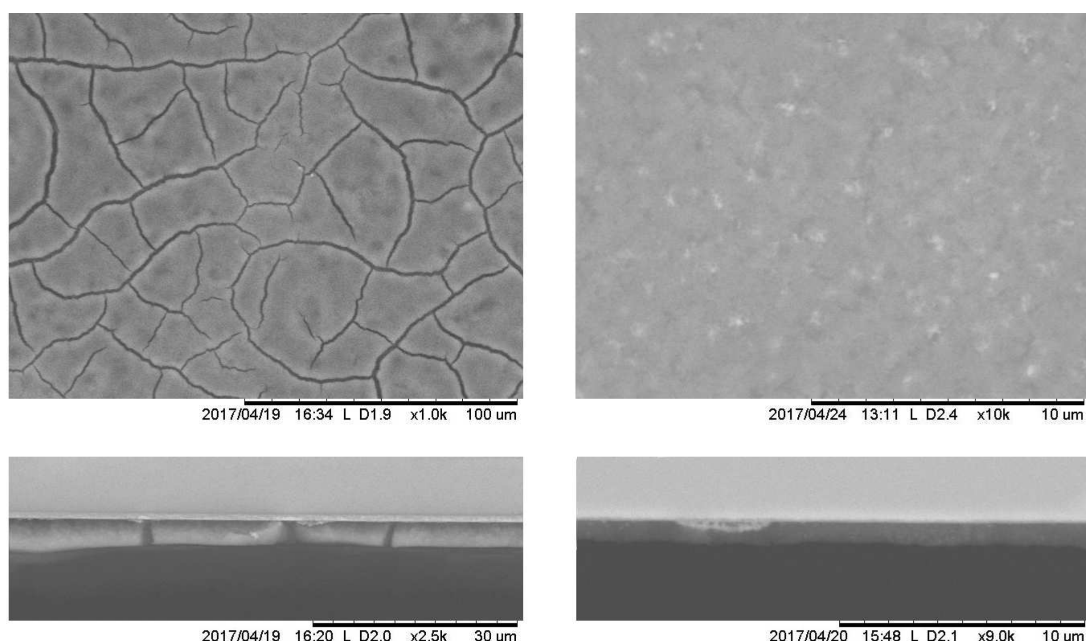

Figure 27: SEM images of samples coated with Sol 1 (left) and Sol 1.2 (right). Top images are taken along the surface normal, bottom images are cross-sections.

the subsequent solutions prepared were also based on Sol 3, with only minor changes in dilution and Zn content.

Storage time was not found to have a large effect on coating quality. A layer of thicker gel was found to accumulate on the bottom of the storage vessel after a number of days, but as the SOG was always stirred and ultrasonicated prior to spin coating, this was not found to be an issue. However, after a storage time of two weeks, Sol 1.1 could no longer diffuse measurable amounts of Zn into any samples. The reason for this is unknown, but one possible explanation is that the Zn atoms in the solution had agglomerated into larger particles, preventing them from forming a uniform diffusant coating on the samples.

The problem of large batch-to-batch variation in coating quality most likely originates from the step of dispersing the fumed silica, as this is the step most likely to produce the large agglomerations of particles observed in the poor coatings. It is also a process that is known to exhibit poor repeatability even in commercial facilities. Taking this into consideration, the reliability of the coating process could be improved by preparing the SOG emulsion using a commercial water-silica dispersion. Another possibility is to synthesize the SiO_2 using the well-known Stöber process. This potentially offers the highest quality suspension and the greatest amount of flexibility in choosing the particle size and composition of the SOG, but is also a more labor-intensive process that requires specialized equipment. [55]

The next step to fabricating laterally doped structures, such as the LED structure described in section 3.2, would require patterning the film to achieve selective doping. This could be achieved by standard photolithography processes to achieve a patterned resist mask on top of the SOG film. The SOG could be patterned by HF etching,

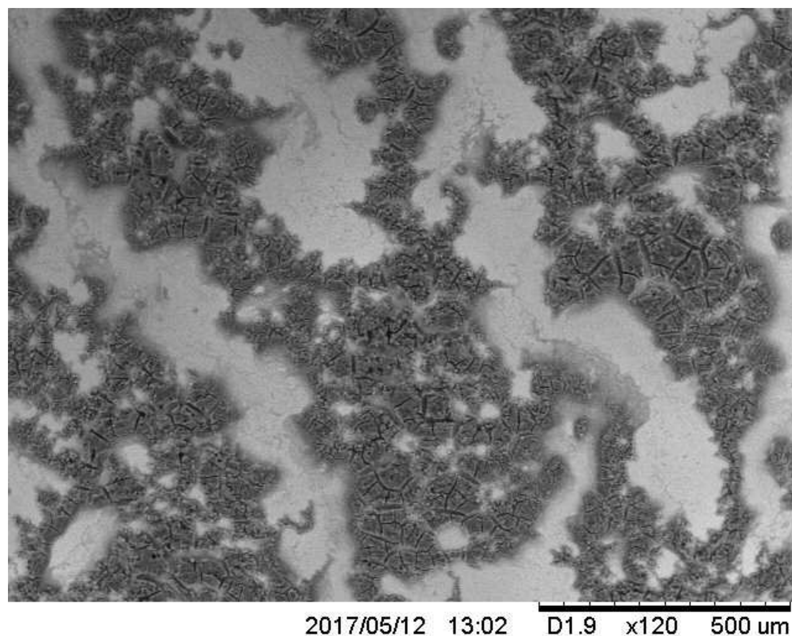

Figure 28: SEM image of the sample spin-coated with Sol 2. Large areas of substrate are exposed between the darker areas that have a thick, cracked coating on them.

while the resist mask protects the parts of the film where diffusion doping is desired. An HF-resistant photoresist must be used. To protect the exposed parts of the sample surface from damage in the diffusion bake, it must be coated with a protective film, *e.g.*, an undoped SOG layer.

5.3 Diffusion annealing

Initial diffusion bake tests were performed in an air ambient, as some sources in the literature have found that the SOG alone is sufficient to protect the sample surface even with no inert gas atmosphere. This was not the case for the SOG process described here, and the samples annealed in air ambient exhibited severe surface damage. This is likely due to pinholes or micro-cracks in the film allowing oxidation to occur at the sample surface, as GaAs readily oxidizes in air at the temperatures used for the samples in this work. [56] All subsequent bakes were performed in N_2 ambient for this reason.

Some surface damage was seen in samples even if the inert gas ambient was used. If the diffusion bake was performed with a single face-up sample, instead of the pair of face-to-face samples, the amount of surface damage was found to be greater, with an increase in either diffusion time or temperature increasing the surface damage on the samples. This could be observed by the appearance of the sample surface turning more cloudy and dark, as well as an increase in the surface roughness visible in SEM imaging. No significant conductivity could be measured in samples annealed for longer than 1 hr at 650 °C without the protective face-down sample. This also

occurred when increasing the temperature, and it is assumed that this was caused by a combination of the surface damage being deeper than the diffusion depth (leading to no intact conductive layer) and out-diffusion of Zn atoms. The surface damage may also have caused issues with contact formation.

With the face-to-face annealing arrangement, some darkening and roughening of the surface near the edges of the sample could be observed, but the extent of the damage was reduced significantly, as can be seen in Figure 29. In the middle of the sample, the samples had some minor discolored spots, but retained their original mirror polish even after 5 hours at 650 °C.

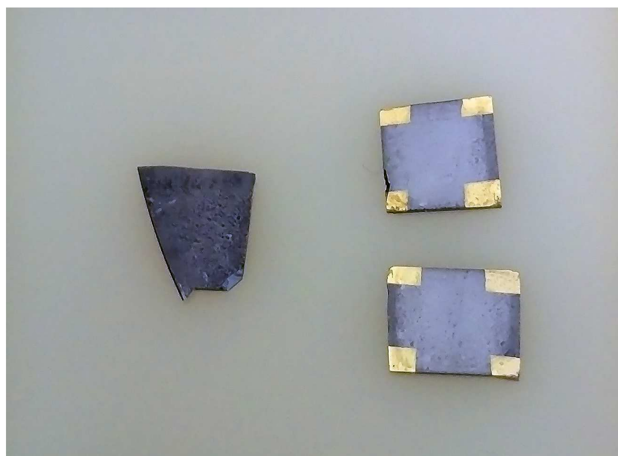

Figure 29: Samples annealed at 650 °C for 5 hours in a N_2 ambient. The sample on the left was face-up during the anneal, and appears darkened and rough. The samples on the right were stacked facing each other. They retain their mirror finish, reflecting the white cleanroom paper above them. The samples on the right have evaporated ZnAu/Zn/ZnAu contacts in the corners for Hall effect measurements.

SEM images of the surface damage can be seen in Figure 30. The damage appears to have a spotty pattern throughout the sample, which may suggest that out-diffusion through pinholes in the diffusant film may be the cause.

5.4 Diffusion doping on undoped substrate

The first tests of diffusion doping were conducted on GaAs samples cleaved from a 50 mm undoped wafer. The goal of these experiments was to achieve a conductive p-type layer on intrinsic GaAs. Characterization results from these samples could be used to establish the parameters of the diffusion process before attempting diffusion on doped substrates and more complex device structures.

5.4.1 IV measurement results

Initial IV measurements were conducted on samples with a p-type layer diffused on an undoped substrate. The sample was coated with Sol 1.1 and annealed at 600 °C for one hour. Two ZnAu/Zn/ZnAu contacts were then evaporated onto the sample,

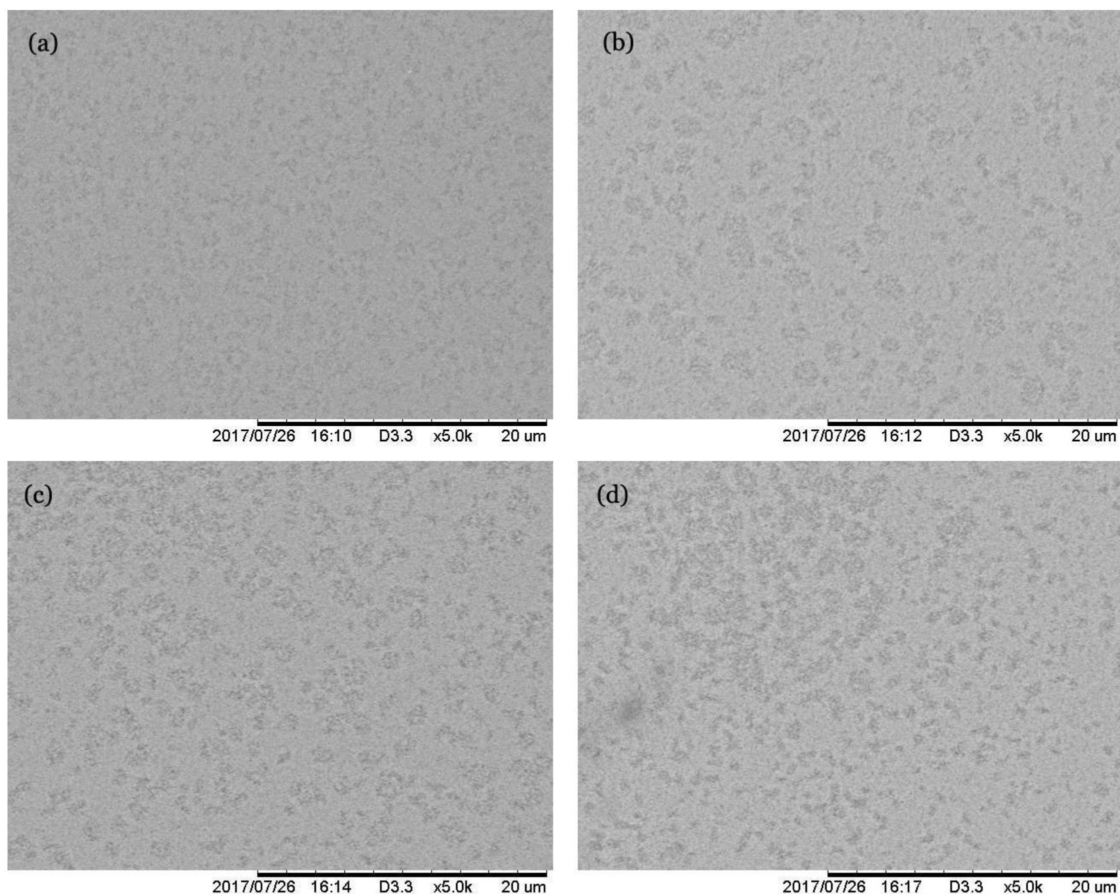

Figure 30: SEM images of samples annealed at 650 °C for (a) 30 minutes, (b) 60 minutes, (c) 90 minutes and (d) 120 minutes. Some damage can be seen in all samples, but the damaged areas are deeper in the samples that were annealed for longer durations.

and electrical characterization was performed with a four-point probe. Figure 31 shows the IV curve from the first successful sample fabricated in this manner.

The sheet resistance of the sample was calculated from the IV data to be around 350 Ω/□, corresponding to an estimated resistivity of 3.5×10^{-2} Ω cm with a diffusion depth of 1 µm. The resistivity specification given by the manufacturer for the unprocessed undoped wafers is $\geq 10^7$ Ω cm, and they were too resistive to measure with the equipment available. This shows that some diffusion of dopants occurred, causing a clear decrease in resistivity. However, the resistivity of the samples was still about an order of magnitude higher than desired, indicating that only moderate doping was achieved.

5.4.2 Hall effect measurement results

Hall effect measurements were carried out for samples coated with Sol 3, annealed at 600 °C for 2 h and 5 h. Some results of the Hall effect measurements carried out

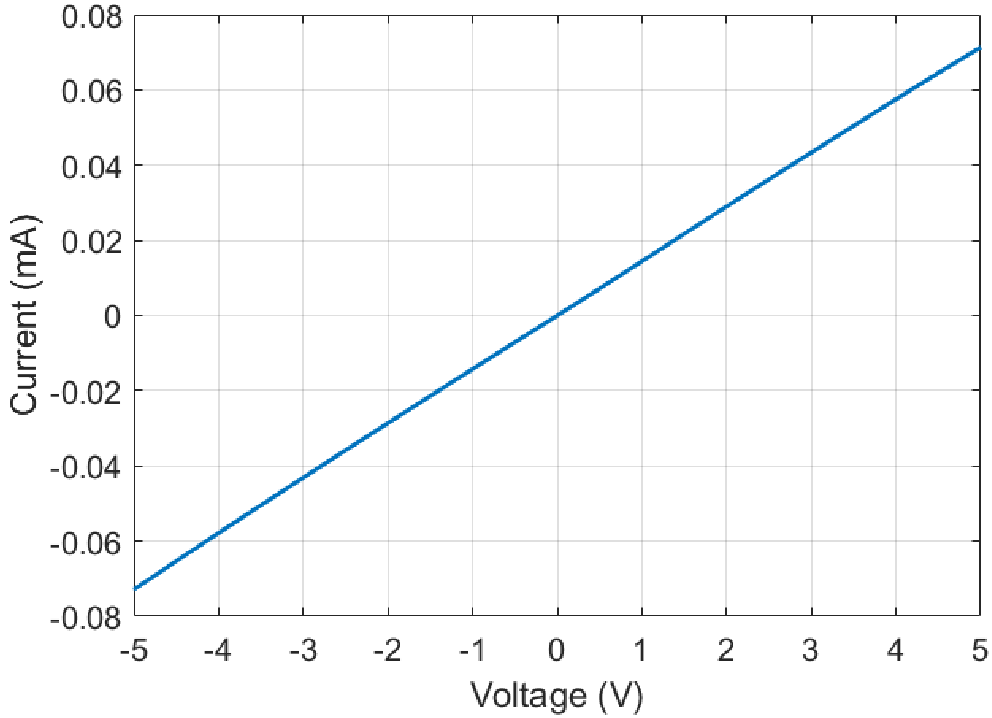

Figure 31: IV curve of the first sample showing an increase in conductivity after diffusion doping. The linear behaviour suggests that the sample and the contacs are ohmic.

using the method described in section 4.4.2 are listed in Table 3.

Table 3: Hall measurement results for Zn diffusion doping into intrinsic GaAs samples.

Diffusion time (h)	Diffusion depth (μm)	Sheet concentration (cm^{-2})	Bulk concentration (cm^{-3})	Sheet resistance ($\Omega/\Box$)	Resistivity ($\Omega\,cm$)
2	2.2	1.87E+14	8.51E+17	9.71E+01	2.14E-2
5	4.0	1.38E+14	3.44E+17	1.29E+03	5.17E-1

The Hall measurement data shows successful p-type doping of initially undoped samples. The diffusion depths were estimated using the diffusivity values and equations in section 2.4.1 and assuming a film density of 1.88 g/cm^3 for the spin-on film during the anneal. [57] The film density was used in conjunction with the ZnO/SiO_2 ration to estimate the Zn concentration at the sample surface. As the diffusion depth is estimated, the doping concentration and bulk resistivity figures are also estimated. The sheet resistance and sheet concentration are measured values.

The results show that the samples annealed for a longer duration unexpectedly exhibit lower dopant concentrations and higher resistivity. This may be due to the surface damage causing the conductive layer to effectively be shallower at longer diffusion times.

5.5 Diffusion doping on n-type substrate

After successfully doping intrinsic GaAs samples, doping of n-type samples was attempted. The goal was to diffuse Zn into the samples to a sufficient degree to overcome the background doping on the wafers and achieve a p-doped layer on the surface. The 50 mm n-type wafers that the samples were cleaved from were Si-doped to a doping density of $1\text{–}10\times10^{17}$ cm^{-3}.

5.5.1 IV measurement results

An n-type sample with a p-type diffused layer was also characterized. The sample was coated with Sol 3 and annealed at 600 °C for two hours. Indium contacts were fabricated on the top (p-type) and bottom (n-type) faces of the sample. Two-terminal IV measurements were conducted to characterize the sample. The top contact was contacted with a probe needle, and contact with the bottom contact was made via the conductive chuck that the sample was resting on. The IV curve obtained can be seen in Figure 32.

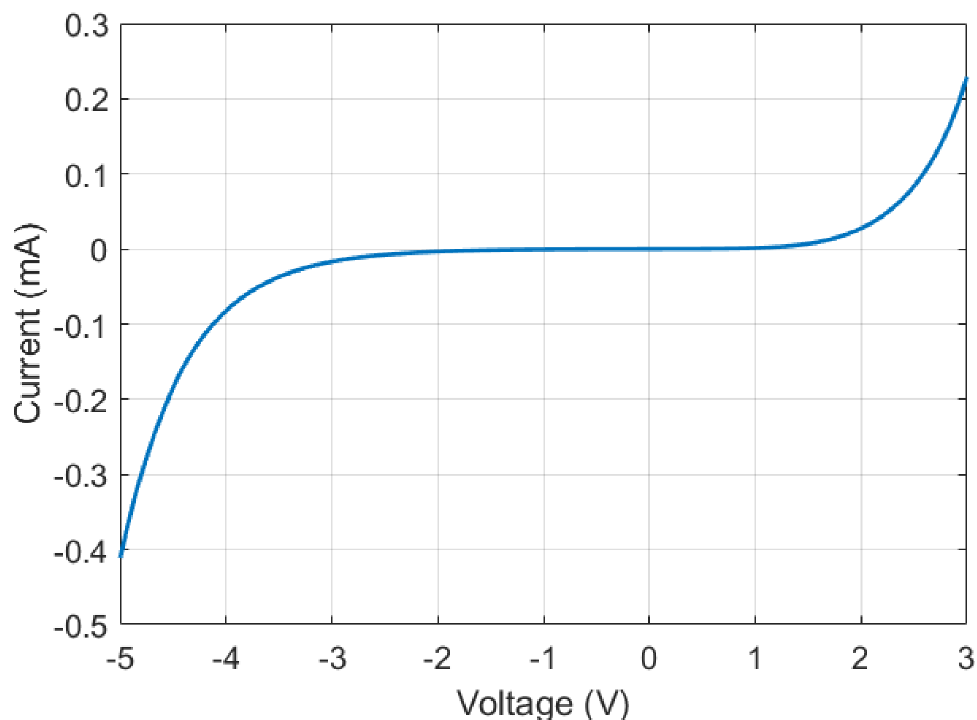

Figure 32: IV curve of n-type sample with Zn diffused layer and indium contacts.

The IV curve shows typical rectifying behaviour, with forward conductivity after a threshold voltage of around 2 V is reached, and reverse conductivity at a higher breakdown voltage. This could result from a p-n junction formed by diffusion doping. However, the threshold voltage is slightly higher than expected, as a typical GaAs p-n diode has a threshold voltage of around 1.2 V. [16] Furthermore, additional tests revealed that for these samples the In contacts were non-linear, indicating

that the observed rectifying behaviour could be attributed to the Schottky barriers of the contacts. A follow-up sample with verified ohmic contacts confirmed this, showing linear IV behaviour for the sample. It can thus be concluded that the doping densities obtained using the SOG solutions prepared in this work were not high enough to compensate for the n-type background doping. This is, however, most likely a problem that can be solved by increasing the amount of Zn in the SOG, improving the film quality or using some of the other reported Zn diffusion methods. In the time frame of this work, however, these further investigations were not feasible.

5.5.2 CV measurement results

CV measurements were conducted on the same n-type sample that showed diode-like IV characteristics when first characterized. CV measurements were performed at 100 kHz and the same probe configuration as the IV measurement. The resulting CV curve is shown in Figure 33.

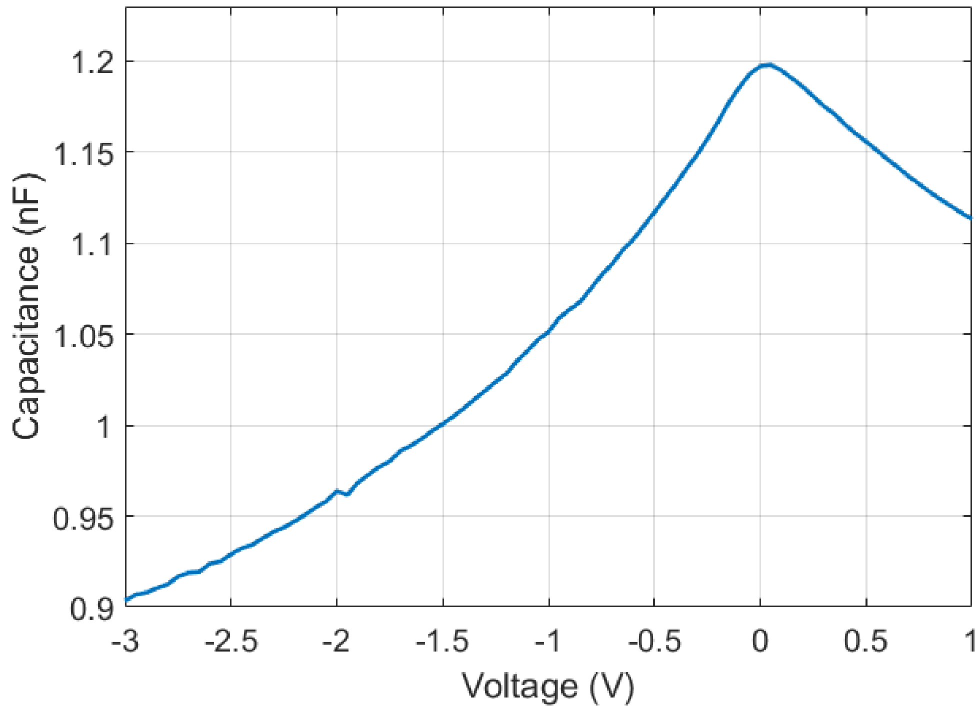

Figure 33: CV curve of n-type sample with Zn diffused layer and indium contacts.

The CV behaviour of the sample also appears to confirm that the sample is not a typical p-n junction diode. In a normal diode, the capacitance would ramp up and saturate in the forward bias regime. Instead, the studied sample exhibits an almost symmetrical peak around 0 V. This resembles the CV behaviour of a heterostructure barrier varactor, a structure that consists of two Schottky diodes connected back-to-back in an antisymmetric arrangement. [58] Intuitively, this matches the sample studied, if one assumes that no p-n junction has been formed and there are Schottky

barriers at both contacts. This appears to reinforce the hypothesis formed on the basis of the IV results, that the Zn diffusion was not sufficient to convert the n-type sample into p-type.

As the sample did not conform to the assumptions of the depletion model, the diffusion depth could not be calculated from the CV data.

5.5.3 Hall effect measurement results

The Hall effect measurement results for an n-type sample where p-type diffusion doping was attempted are listed in Table 4. The sample was coated with Sol 3 and the diffusion anneal duration was 2 hours. The results from an unprocessed n-type sample from the same wafer are listed for comparison. Both samples had indium contacts that were verified to be ohmic prior to the measurement.

Table 4: Hall measurement results for Zn diffusion into n-type samples.

Sample	Sheet concentration (cm^{-2})	Bulk concentration (cm^{-3})	Sheet resistance ($\Omega/\square$)	Resistivity ($\Omega\,cm$)
unprocessed n-type	-9.20E+15	-2.63E+17	8.41E-1	2.94E-2
diffusion doped n-type	-4.78E+14	-1.37E+16	2.20E+3	7.72E+1

The sample thickness used for calculating the resistivity and bulk doping concentration is the wafer thickness, 350 µm, as the whole wafer is conductive and no p-type channel has been formed. These results are congruent with the IV and CV measurement results, indicating that Zn diffusion did not occur to a sufficient degree to convert the sample to p-type, and the conductivity of the sample surface is still n-type. A shallow p-type region may exist close to the surface, but the leakage current to the underlying n-type substrate is large enough that the Hall measurements cannot detect it. However, the sample resistivity is higher and carrier concentration lower than in the unprocessed control sample. This could indicate that a significant portion of the free electrons in the n-type substrate have recombined with the excess holes introduced into it by the diffused Zn, causing an overall reduction in free charge carriers. The estimated diffusion depth is only a small fraction of the overall wafer thickness however, so, assuming that the current flows through the entire cross-sectional area of the substrate, it is more likely that this difference is caused by irregularities in the metal contacts. Possible causes may be nonlinear IV behaviour in one or more of the contacts, or error caused by the size and placement of the contacts deviating from the point-like contacts on the perimeter assumed by the van der Pauw model.

5.6 ZnAu contacts on n-type substrate

A sample with ZnAu/Zn/ZnAu contacts deposited directly onto an n-type substrate was fabricated and characterized in order to test the viability of such a scheme for hole injection into DDCT LED structures. If successful, this new approach could provide an extremely simple method to fabricate working devices without the need for any additional doping. IV measurements and IR microscopy were performed to characterize the behaviour of the sample.

5.6.1 IV measurement results

The IV characteristics of the sample were determined with a two-terminal method, with one probe needle contacting the evaporated contact on the top face of the sample, and the other needle making contact with the backside indium contact via the conductive copper chuck on which the sample was placed. The IV curve of this sample is shown in Figure 34.

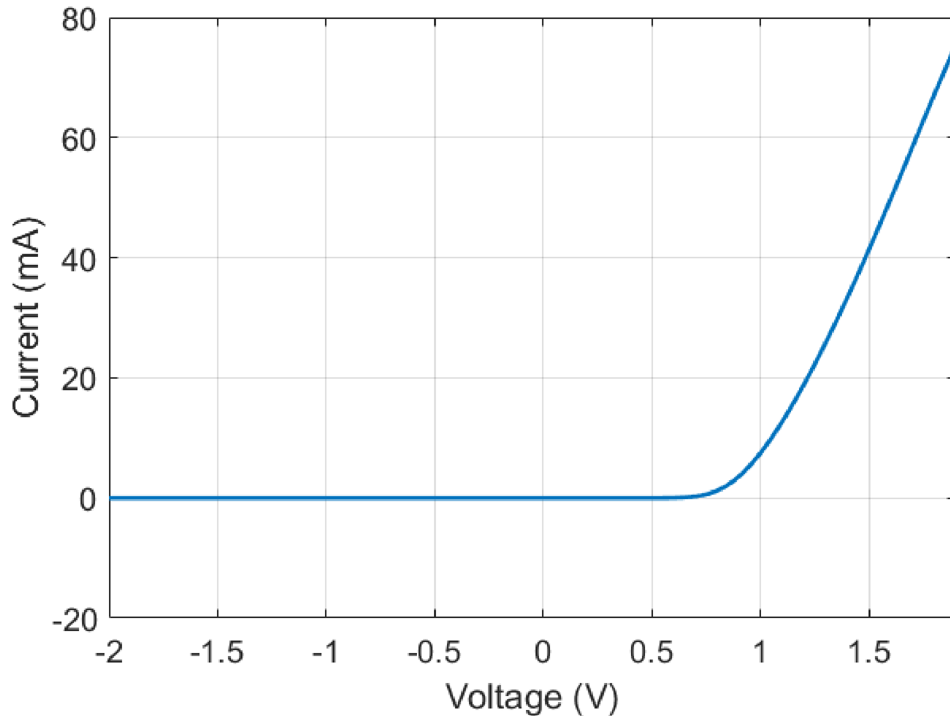

Figure 34: IV curve of a sample with ZnAu/Zn/ZnAu contacts deposited on n-type GaAs.

The sample exhibits rectifying IV behaviour, with a threshold voltage of around 0.8 V. This is lower than the 1.2 V threshold that would be expected for a GaAs p-n junction, and closer to the 0.75 V observed in Au/n-type GaAs Schottky diodes. [16,59] This could suggest that the device is acting as an n-type Schottky diode, and the mechanism for hole injection into the substrate is minority carrier injection into the valence band from the Schottky-type metal contacts themselves, not a p-type

doped layer caused by Zn diffusion from the contacts. This is not conclusive evidence, however, and more experiments are required to ascertain the precise mechanism.

5.6.2 Light emission

In order to determine whether the current was due to minority or majority carriers, we also observed the sample using an IR microscope while passing a current through it. Light emission was observed, as shown in Figure 35. The light was emitted in a uniform ring around the evaporated circular contacts when a current was passed through the sample via contacts on the top and bottom faces.

Figure 35: Infrared micrograph of light emission around a circular ZnAu/Zn/ZnAu contact deposited on an n-type substrate.

This result confirms that holes were successfully injected into the n-type GaAs via this simple contact scheme, showing that this type of structure is a feasible option for fabricating GaAs LEDs like the one described in section 3.2. These structures are an attractive option to explore for further research into GaAs DDCT LEDs, as they are simple and relatively easy to fabricate. However, the efficiency that can be reached with this type of structure depends on the minority carrier injection mechanism. In the literature, the ratio of minority to majority carriers observed to

be participating in current transport in Schottky diodes is rather small, on the order of 1–3 %, so this may be an inefficient hole injection scheme. [43] However, the hole injection efficiency could be significantly improved by employing a graded AlGaAs layer on the surface, which would reduce the barrier for minority carrier injection while preventing majority carrier leakage across the interface.

The light emission may also be based on Zn diffusion from the contacts. The contacts were annealed for a short time (5 min) at a relatively low temperature (400 °C), so any diffused layer would only be tens of nanometers deep at most. Some sources have successfully done such low-temperature Zn diffusions on other III-V semiconductors, but little data exists for GaAs. [60, 61] Further investigation into this device type is thus merited.

6 Summary

This work explored the possibilities of using Zn diffusion doping to fabricate novel high-efficiency GaAs-based LED structures with substantial potential to improve the high-power operation of existing LED technologies. A literature review was conducted into the process of Zn diffusion in the relevant III-V materials and the techniques used to characterize doping in semiconductors. The most important theoretical background related to the diffusion doping and operation of LEDs was also discussed, and selected state-of-the-art LED structures were presented as an introduction to the studied new DDCT LED structures. To enable the fabrication of these structures, a spin-on glass process for diffusion doping was developed and characterized, along with a new method to directly inject minority carriers to n-type GaAs.

The diffusion doping process developed for this thesis is based on a spin-on glass method, in which SiO_2 and ZnO particles are suspended in a solvent-based solution. This solution is spin-coated onto the substrate and the coated sample is annealed in an inert atmosphere at a temperature of 600 °C or more. During the anneal, Zn atoms diffuse from the film into the substrate, converting it into a p-type material. After annealing, the glass film is removed from the sample surface by briefly etching it in HF. Contacts are then deposited either by evaporation or soldering on indium dots. Electrical characterization is then performed using IV, CV and Hall measurements. Further characterization is performed by optical and electronic microscopy.

The results obtained by this process were presented and discussed in Chapter 5. Successful p-type doping of the order 10^{17}–10^{18} cm^{-3} was achieved with initially undoped GaAs samples. Diffusing a p-type layer onto Si-doped (n-type) GaAs substrates was also tested, but the diffused Zn concentration was not yet sufficient to overcome the background doping concentration in the n-type samples.

Successful hole injection into an n-type substrate was achieved, however, with an alternative sample structure. This sample had ZnAu/Zn/ZnAu contacts evaporated directly onto an unprocessed n-type substrate. This sample exhibited rectifying IV characteristics, and light emission was observed from it, confirming that radiative recombination was taking place in the sample and that it was possible to directly inject minority carriers into the n-type substrate. The exact mechanism for the hole injection is not clear, but it likely involves either shallow p-doping of the substrate by Zn diffused from the metal contacts or direct minority carrier injection from the metal contacts. This result provides a promising framework for further analysis and testing of the structure.

The goal of this work, to develop and characterize a fabrication process that could be used to realize experimental high-efficiency GaAs-based LED structures, was successful in all aspects apart from finding a suitable SOG formulation to overcompensate the background doping in n-type substrates within the work's timeframe. In addition, the work lead to the identification of an alternative method to directly inject minority carriers into n-type substrates using plain ZnAu metal contacts. For intrinsic substrates, the fast and inexpensive SOG-based Zn diffusion doping process allowed p-type doping of the initially undoped wafers. However, the

doping density achieved was not yet high enough to convert the surface of initially n-type doped wafers into p-type. Improving the coating quality by using a different SiO_2 source and possibly increasing the Zn fraction in the film should make it possible to achieve the required higher doping concentrations. Once this can be demonstrated, the only additional steps required to make a functional DDCT LED are growing the required semiconductor layers, patterning the SOG film via standard photolithography and etching the excess away in HF before the diffusion anneal, and depositing the p- and n-type contacts onto the sample.

For the alternative hole injection method based on ZnAu contacts deposited directly on n-type GaAs, strong light emission was observed under forward biasing. This presents another promising avenue for further research into high-efficiency GaAs DDCT LED structures. However, some remaining questions regarding the mechanism of the minority carrier injection must be answered before the viability of this structure can be fully assessed.

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