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Automatic Reference Clock Duty Cycle Calibration System for Dual Edge Sampling RF Circuits

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***Abstract*—Duty cycle error of the sampling clock may cause distortion or gain and phase error in RF dual edge samplers, downconverting analog-to-digital converters and time-interleaved sampler arrangements. This results in degradation of system performance in forms of IQ mismatch, additional noise aliasing and spurious tones. This paper describes a fully automated reference clock duty cycle tuning system for low-power RF circuits. To achieve energy-efficient operation, the method utilizes signal slope and resistor based offset tuning combined with digital feedback system to compensate for measured duty cycle error. The system achieves 22–75 % tuning range and jitter less than 30 fs over the desired 40–60 % range for the targeted 24 GS/s sampling rate.**

***Index Terms*—duty cycle calibration, dual edge sampling, double sampling, RF sampling**

I. Introduction

FIFTH GENERATION and beyond communications systems are aiming for higher frequency ranges and bandwidths, which necessitates energy efficient high-speed RF samplers, downconverters and high resolution analog-to-digital converters (ADCs). The increasing frequency and bandwidth escalates the requirements for the clock signals as the power consumption increases and non-idealities degrade the overall system performance. For example, sampling jitter degrades the signal-to-noise ratio (SNR) of an ADC [1]–[5], thus in order to achieve high resolution, low-jitter clocks are required.

As shown in Fig. 1, the low-jitter clocks can be implemented using only one of the clock edges (i.e. rising or falling) or by using both edges [6]–[8]. The former, denoted as a single edge, has the benefit of duty cycle insensitivity, with the cost of higher power consumption and noise as the clock frequency has to be doubled. Dual edge sampling (i.e. using both the rising and falling edges), doubles the sampling frequency without a major increase in power consumption. However, deviations from 50 % duty cycle causes unwanted spectral components and signal aliasing in vicinity of sampling signal frequency [8], [9].

In order to achieve the potentially significant power savings of dual edge sampling, duty cycle detection and correction has received vast amount of research. Various implementations have an analog comparator, result of which is used in feedback to automatically fix the duty cycle, such as [10]–[13]. Analog charge pumps are used for the duty cycle error detection and pulse width adjustment with an adjustable delay, i.e. [14]–[17]. Alternatively, phase detectors and a digitally controlled delay line can be used as in [18]–[20]. Fully digital implementations have been researched as well, such as [21]–[25].

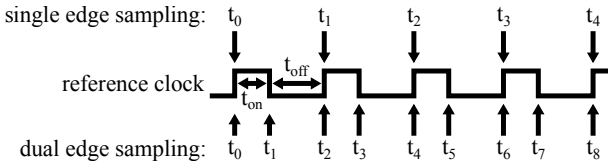

Fig. 1. Sampling instants when sampling on rising edges or on both edges of a nonideal reference clock

This paper proposes an automated low-power digital-intensive duty cycle calibration for a downconverting dual edge RF sampling system, that ensures a 50 % clock duty cycle regardless of processing corner, supply voltage and operating temperature (PVT). A comparator is used to detect the duty cycle, and to maximize control accuracy and supported local oscillator (LO) frequency range, logic that optimizes comparator operation point is used. The implementation is shown to drastically improve the performance of a high-speed sampling circuit, with negligible increase in power consumption and sampling jitter.

The rest of this paper is structured as follows. Section II discusses downconversion with dual edge sampling. Section III introduces the proposed duty cycle calibration system and its components. The system is simulated in Section IV, and the paper is concluded in Section V.

II. Downconversion Using Dual Edge Sampling

Due to its significant power saving potential, dual edge sampling proves to be useful in systems that downconvert an RF signal by sampling. A signal may be downconverted by Δf by sampling at Δf or by sampling at $2\Delta f$ and inverting every second sample, similarly to switching mixers. The latter case has the benefit of a halved noise floor as the folded noise spreads evenly over the bandwidth twice as large. By using dual edge sampling, the lower noise floor can be achieved without doubling the reference clock frequency which is already high in RF applications. However, using dual edge sampling with a reference clock whose duty cycle is not 50 % results in nonuniform sampling which normally leads to a spurious tone in the sampled signal. This distortion can be reduced or entirely avoided by averaging samples, at the cost of reduced bandwidth, lower amplitude and a phase shift.

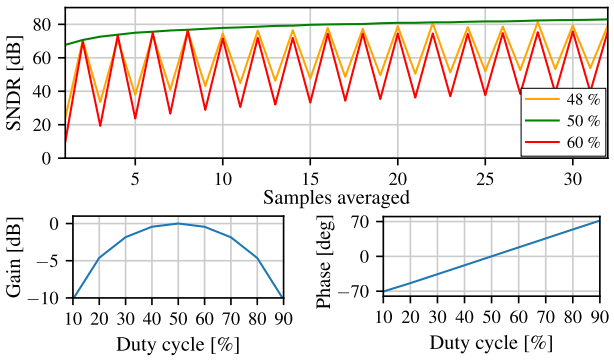

Fig. 2. Ideal sampler SNDR, gain and phase as functions of duty cycle

Fig. 2 shows the output of an ideal downconverting sampler driven with an incorrect duty cycle. The sampler is modeled in Python with noise added to the input signal. The top plot depicts the signal-to-noise-and-distortion ratio (SNDR) at various numbers of samples averaged at different duty cycles, and the bottom plots show the gain and phase shift when two samples are averaged. At odd number of samples combined, the nonuniform sampling distortion is present and the SNDR collapses even at small duty cycle errors. The effect is more pronounced for lower number of samples averaged. At even number of samples combined the distortion cancels out and duty cycle error shows only as a loss and a phase shift, leading to high SNDR. Combining samples reduces the output bandwidth which folds noise from the removed high frequencies to the remaining low frequencies. However, due to the low pass filtering effect inherent to averaging, not all high frequency noise folds to baseband, which results in a noise floor that is still lower than if the signal was initially sampled at the lower frequency. The effect is seen in the top plot as an increased SNDR for higher number of samples combined.

Therefore, using dual edge sampling in downconversion lowers the noise floor, and averaging samples reduces linearity problems introduced by incorrect duty cycle at the cost of reduced output sample rate. Such system benefits from a perfect 50 % duty cycle even in the cases where linearity problems are avoided. Correct duty cycle ensures that the sampling clock does not limit the output amplitude and that the bootstrapped switch required to take accurate samples is not limited by shorter-than-intended tracking time. Therefore, we propose a low-jitter duty cycle correction system.

III. Proposed Duty Cycle Calibration System

Fig. 3 depicts a downconverting dual edge sampling system, in which the dual edge sampling is implemented by extracting the high and low states of the LO into separate active low pulses that are given to bootstrapped track-and-hold switches. One full baseband sample consists of 32 averaged RF samples in this system.

For such dual edge downconverting sampling system to avoid the issues discussed in Section II, all sampling pulses should have equal duration. This is ensured with our proposed

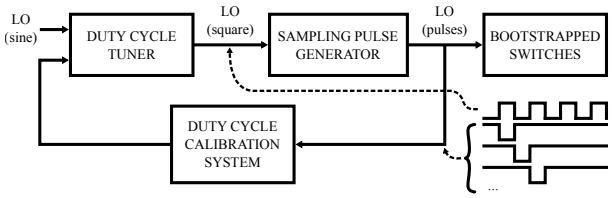

Fig. 3. Example dual-edge downconverting sampling system with the proposed automatic LO duty cycle correction

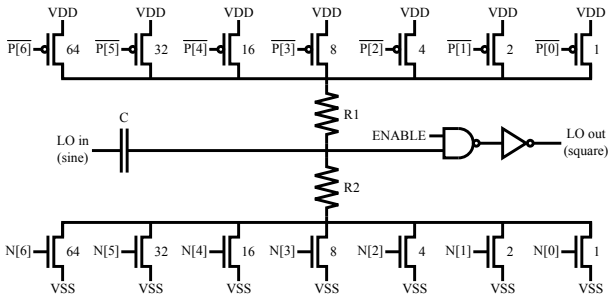

Fig. 4. The proposed duty cycle tuning circuit

duty cycle correction system that automatically tunes the LO clock duty cycle so that uniform sampling is achieved. The system consists of a duty cycle tuning circuit and a calibration system that detects the duty cycle from the sampling pulses and controls the tuner accordingly.

A. Duty cycle tuner

The duty cycle tuning circuit is presented in Fig. 4. The circuit takes in an LO signal that has significant transition times, shifts its DC value up or down, and quantizes it using digital logic gates to produce a square wave output clock signal. The input signal DC level is removed using a capacitor and a new one is produced using tunable resistive biasing. The transistors act as resistors that can be switched on or off, resulting in a tunable DC value that together with the input signal determines the output clock duty cycle. In order to reduce power consumption and noise, the output clock can be disabled when it is not required.

The system can adapt to any input signal shape that has significant transition times between its minimum and maximum values, for example a sine or a triangle wave. Longer transition times improve the tuning range of the circuit and thus a square wave with fast transitions is a poor choice. The input amplitude is not critical but a higher amplitude lowers the jitter of the output clock. This is because the rate of change of the shifted signal will be higher at the logic switching voltage, reducing uncertainty in the transition instant. Higher input frequency also results in lower jitter for the same reason.

The components are sized for low static power consumption. The switches have minimum width and the resistors $R1$ and $R2$ are large. The resistors are used to design the DC point in the case where all switches conduct and to reduce the DC point dependency of the switches, improving the resolution of tuning. The DC blocking capacitor is chosen large enough to

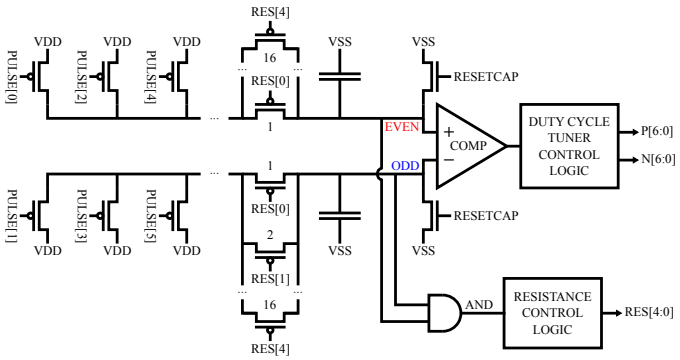

Fig. 5. The proposed automatic duty cycle detection and calibration system

pass the lowest target frequency but small enough so that the circuit would settle to a new operation point quickly enough for automatic control. The digital gates are chosen as large as possible to improve transition times for low jitter.

B. Duty cycle calibration system

The duty cycle calibration system, shown in Fig. 5, consists of duty cycle detection switches, tunable resistors, integration capacitors and related reset switches, a StrongARM comparator [26], [27] and digital logic. The analog part up to the comparator consists of two identical halves, one being driven with even sampling pulses and the other with odd pulses. The sampling pulses control the duty cycle detection switches that charge two capacitors through tunable resistors. The amount of charge stored to the capacitor by each pulse is proportional to the pulse width which is determined by the LO frequency and duty cycle. Incorrect duty cycle results in the even and odd capacitors being at different voltages at the end of sampling. The effect of sampling pulse jitter is low because multiple pulses charge the same capacitor, making the voltage proportional to the average pulse width. After sampling, the capacitor voltages are compared using a comparator and the result reveals if the duty cycle is above or below 50 %. The comparator output is given to digital logic that will change the duty cycle tuner control signals toward the optimum. After the comparator decision the capacitors are reset to zero for next iteration.

The full calibration sequence consists of two phases: a resistance tuning phase and a duty cycle tuning phase. The first phase that happens after a reset is the resistance tuning phase which extends the LO frequency range of the calibration system and reduces PVT dependency. Resistance tuning is implemented with parallel PMOS transistors and is optimized using binary search where the control code is solved bit by bit from MSB to LSB. The resistance is considered optimal when the two capacitors settle to just above half of supply voltage which is the comparator noise optimum [28]–[31]. To ensure that the capacitor voltages are not too high and resistance too low, resistance control logic is used. The logic consists of an AND gate and a successive approximation register (SAR).

Fig. 6 exemplifies the resistance tuning phase and shows the capacitor voltages, AND gate output and resistor control

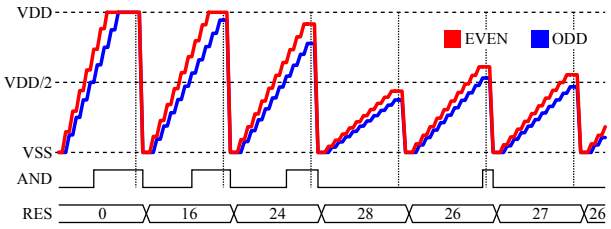

Fig. 6. Resistance tuning phase of the calibration system

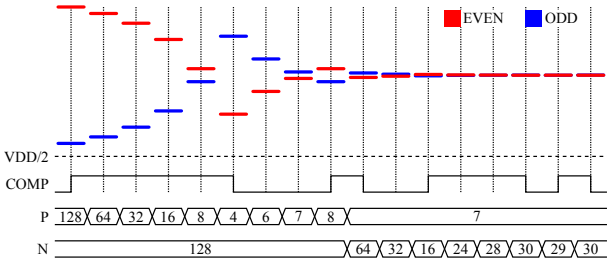

Fig. 7. Duty cycle tuning phase of the calibration system

signals of Fig. 5. Before optimization, the SAR used to implement the binary search is reset to all zeros, leading to minimal resistance as all PMOS fingers conduct. In this case both capacitors saturate to supply voltage and the voltage difference cannot be properly detected, meaning that the resistance must be increased for duty cycle correction to be possible at this LO frequency. The optimization begins when the MSB is switched high, disabling half of the transistors and increasing resistance such that the capacitors settle to a lower voltage. For the next sample, based on the AND gate value the MSB is either kept high or switched back low while the next bit is switched high, resulting in a higher or lower resistance than previous iteration. This process repeats until the LSB has been solved and capacitors settle to slightly above half of supply voltage.

The resistance tuning phase is followed by the duty cycle tuning phase, in which the optimal duty cycle tuner configuration is solved using two binary searches, one for each side of the tuner. Fig. 7 shows the voltages that the capacitors settle to after each iteration, as well as the comparator output of Fig. 5 and the tuner control signals of Fig. 4. The calibration begins at a state where both N and P side SARs are set to all ones, i.e. all switches conduct on both sides (PMOS controls are inverted). The comparator is then triggered the first time, revealing if the duty cycle is initially too high or too low and determining which binary search is done first. In this example the comparator output is high indicating that duty cycle is above optimum, thus the P side binary search is done first to lower the duty cycle. At the end of the first binary search the corresponding SAR is at the minimum value at which the comparator gives the original result. Subtracting one from this value flips the duty cycle from too high to too low, allowing the second binary search to optimize the configuration further. After the second binary search finishes, the duty cycle correction is done and the clock of the comparator and digital parts is disabled to cut

power consumption. This one-time calibration can be repeated periodically to keep the duty cycle optimal under transient behaviors such as temperature and supply drift.

Duty cycle detection accuracy relies on the matching of the two halves of the calibration circuit. Layout techniques such as constructing the capacitors out of small units in a common centroid pattern and packing the switches as close to each other as possible can improve calibration accuracy. Making the capacitors large further reduces the effect of mismatches as well as reducing thermal noise at the comparator inputs. Large detection capacitors have negligible effect on the total system power consumption as they get charged a limited number of times during the calibration.

IV. Simulation Results

The proposed duty cycle calibration system was implemented in the GlobalFoundries 22nm FDSOI technology and verified with transistor level simulations of duty cycle tuner, pulse generator and calibration system, with an ideal sampling circuit. Fig. 8 shows the even and odd capacitor voltages of the calibration circuit and sampling pulses during one full calibration with a 12 GHz sinusoidal reference that results in 24 GS/s sampling rate before averaging the samples. The resistance tuning phase consists of the first six samples and the duty cycle tuning phase from the remaining samples. In the beginning of the simulation the duty cycle is incorrect, leading to different capacitor voltages and pulse widths, and in the late simulation the capacitors settle to the same voltage and pulses have equal width. Fig. 9 shows the duty cycle convergence in several PVT corners. The effect of the correction system to the sampled baseband signal range is shown in Fig. 10 where the input duty cycle is the time the reference sinusoid is above half of supply voltage compared to period. Without correction, the gain resulting from incorrect pulse widths reduces amplitude, and at low and high duty cycles the pulse generator is unable to function. It is notable that the pulse generator shifts duty cycle by a small amount due to the fact that even and odd pulses are generated using different circuitry, and the correction system adapts to this shift. The tuning system functions properly on LO frequencies up to 22 GHz in the typical PVT corner while the pulse generator has a more limited range.

The duty cycle tuner was simulated separately to extract its tuning range and jitter which are presented in Fig. 11 as functions of active NMOS and PMOS fingers. The simulations were performed using a 12 GHz full-scale sinusoidal reference and the typical PVT corner. The tuner achieves both high range and high accuracy by combining coarse and fine tuning. The coarse tuning is accomplished by disabling most fingers on one side and fine tuning by disabling some fingers on the opposite side. The tuning range is 22–75 % where the minimum is achieved with two PMOS conducting and maximum with two NMOS conducting. Noise was enabled on a 250 GHz bandwidth in jitter simulations to ensure that thermal noise is present in sufficient extent. Jitter remains low in all configurations but increases if the duty cycle is changed significantly beyond the desired range of 40–60 %. When all

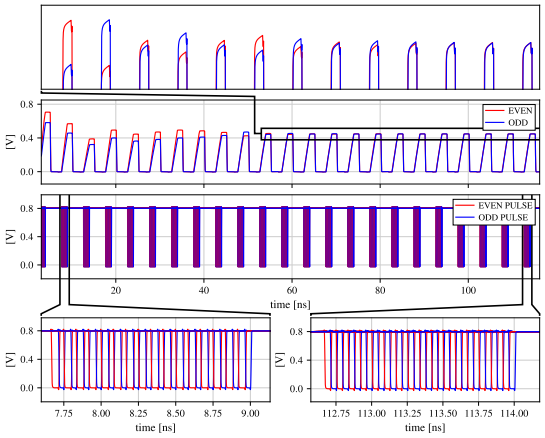

Fig. 8. Transient simulation of the proposed sampling system

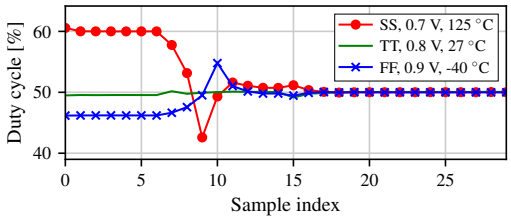

Fig. 9. Duty cycle of sampling pulses as a function of sample index

switches conduct, the tuner consumes 752 µW when enabled and driving a 30 fF load representing the pulse generator and additional parasitics, and 231 µW when disabled. In other configurations the static power decreases as the total resistance is higher. It is notable that the tuner is effectively the only power consuming component in the tuning system as the clock

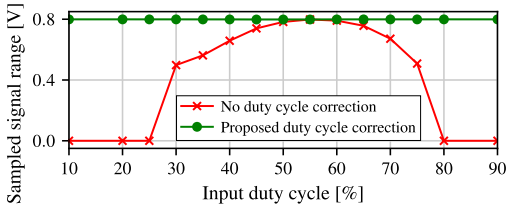

Fig. 10. Effect of duty cycle calibration system on sampled signal range

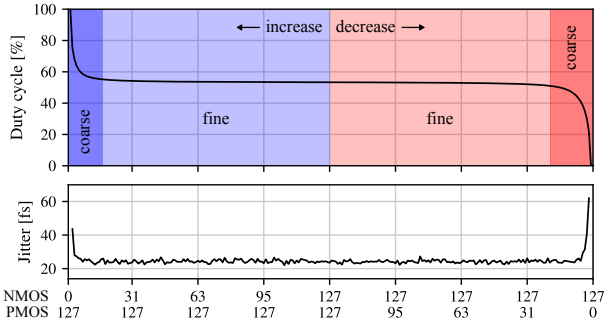

Fig. 11. Duty cycle tuner output range and jitter

of the correction logic is disabled after the calibration finishes.

V. Conclusion

This paper proposed an automatic reference clock duty cycle calibration system for low power RF dual edge sampling circuits. The use of both clock edges has the potential to significantly reduce power consumption, with the requirement of an accurate 50 % duty cycle in order to not degrade the performance. The proposed system comprises a duty cycle detection circuit used together with digitally-intensive calibration, which ensures correct duty cycle with tuning range of 22–75% for the targeted 24 GS/s sampling rate, while achieving jitter performance of less than 30 fs in the target tuning range of 40–60 %, with power consumption of at most $752\,\mu\mathrm{W}$.

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