TKK Dissertations 121
Espoo 2008

ANALOG BASEBAND CIRCUITS FOR SENSOR SYSTEMS

Doctoral Dissertation

Jere Järvinen

Helsinki University of Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences

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Dissertation for the degree of Doctor of Science in Technology to be presented with due permission of the Faculty of Electronics, Communications and Automation for public examination and debate in Auditorium S1 at Helsinki University of Technology (Espoo, Finland) on the 16th of May, 2008, at 12 noon.

Helsinki University of Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences

Teknillinen korkeakoulu
Elektroniikan, tietoliikenteen ja automaation tiedekunta
Mikro- ja nanotekniikan laitos

Distribution:
Helsinki University of Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences
P.O. Box 3000
FI - 02015 TKK
FINLAND
URL: http://www.ecdl.tkk.fi/
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ISBN 978-951-22-9364-3
ISBN 978-951-22-9365-0 (PDF)
ISSN 1795-2239
ISSN 1795-4584 (PDF)
URL: http://lib.tkk.fi/Diss/2008/isbn9789512293650/

TKK-DISS-2468

Multiprint Oy
Espoo 2008

ABSTRACT OF DOCTORAL DISSERTATION	HELSINKI UNIVERSITY OF TECHNOLOGY P.O. BOX 1000, FI-02015 TKK http://www.tkk.fi

Author Jere Järvinen

Name of the dissertation
Analog Baseband Circuits for Sensor Systems

Manuscript submitted 14.01.2008	Manuscript revised 23.04.2008
Date of the defence 16.05.2008	
☐ Monograph	☒ Article dissertation (summary + original articles)

Faculty	Faculty of Electronics, Communications and Automation
Department	Department of Micro and Nanosciences
Field of research	Electronic Circuit Design
Opponent(s)	Professor Ari Paasio
Supervisor	Professor Kari Halonen
Instructor	-

Abstract

This thesis is composed of six publications and an overview of the research topic, which also summarizes the work.
The research presented in this thesis focuses on research into analog baseband circuits for sensor systems.
The research is divided into three different topics: the integration of analog baseband circuits into a radio receiver for sensor applications; the integration of an ΔΣ modulator A/D converter into a GSM/WCDMA radio receiver for mobile phones, and the integration of algorithmic A/D converters for a capacitive micro-accelerometer interface. All the circuits are implemented using deep sub-micron CMOS technologies.

The work summarizes the design of different blocks for sensor systems. The research into integrated analog baseband circuits for a radio receiver focuses on a circuit structures with a very low power dissipation and that can be implemented using only standard CMOS technologies.

The research into integrated ΔΣ modulator A/D converter design for a GSM/WCDMA radio receiver for mobile phones focuses on the implications for analog circuit design emerging from using a very deep sub-micron CMOS process.

Finally, in the research into algorithmic A/D converters for a capacitive microaccelerometer interface,
new ways of achieving a good performance with low power dissipation, while also minimizing the silicon area of the integrated A/D converter are introduced.

Keywords CMOS, sensor, baseband, ΔΣ modulator, algorithmic A/D converter

ISBN (printed) 978-951-22-9364-3	ISSN (printed) 1795-2239
ISBN (pdf)	ISSN (pdf)
Language English	Number of pages 122 p. + app. 78 p.
Publisher Helsinki University of Technology, Faculty of Electronics, Communications and Automation	
Print distribution Helsinki University of Technology, Department of Micro and Nanosciences	
☒ The dissertation can be read at http://lib.tkk.fi/Diss/2008/isbn9789512293650/	

VÄITÖSKIRJAN TIIVISTELMÄ	TEKNILLINEN KORKEAKOULU PL 1000, 02015 TKK http://www.tkk.fi
Tekijä Jere Järvinen	
Väitöskirjan nimi Analogiset kantataajuuspiirit sensorijärjestelmissä	
Käsikirjoituksen päivämäärä 14.01.2008	Korjatun käsikirjoituksen päivämäärä 23.04.2008
Väitöstilaisuuden ajankohta 16.05.2008	
☐ Monografia	☒ Yhdistelmäväitöskirja (yhteenveto + erillisartikkelit)

Tiedekunta	Elektroniikan, tietoliikenteen ja automaation tiedekunta
Laitos	Mikro- ja nanotekniikan laitos
Tutkimusala	Piiritekniikka
Vastaväittäjä(t)	Professori Ari Paasio
Työn valvoja	Professori Kari Halonen
Työn ohjaaja	-

Tiivistelmä

Tämä väitöskirja koostuu kuudesta julkaisusta ja tutkimusaiheen yhteenvedosta. Väitöskirjassa esitetty tutkimus keskittyy sensorijärjestelmiin tarkoitettujen analogisten kantataajuuspiirien tutkimukseen. Yksityiskohtaisemmin tutkimusalueet ovat: kantataajuuspiirien integrointi sensorijärjestelmään tarkoitettuun radiovastaanottimeen, ΔΣ-modulaattori A/D-muuntimen integrointi matkapuhelimen GSM/WCDMA radiovastaanottimeen sekä algoritmisten A/D-muuntimien integrointi kapasitiivisten kiihtyvyysanturien lukemiseen tarkoitettuun rajapintaan. Kaikki totetutetut piirit on toteutettu käyttämällä kapean viivanleveyden CMOS teknologioita.

Työ vetää yhteen eri sensorijärjestelmälohkojen suunnittelun. Sensorijärjestelmään suunnitelluissa radiovastaanottimissa tutkitaan kantataajuusosien integrointia, joilla on erittäin matala tehonkulutus ja jotka ovat toteutettu pelkästään standardia CMOS teknologiaa käyttäen.

Matkapuhelimen GSM/WCDMA radiovastaanottimeen suunnitellussa integroidussa ΔΣ-modulaattori A/D-muuntimessa tutkitaan erittäin kapean viivanleveyden CMOS teknologian aiheuttamia vaikutuksia analogiapiirien suunnitteluun.

Lopuksi, kapasitiivisten kiihtyvyysantureiden lukemiseen tarkoitettuihin rajapintojen toteutuksessa esitetään uusia tapoja saavuttaa hyvä suorituskyky sekä erittäin matala tehonkulutus, mikä samalla minimoi toteutetun integroidun algoritmisen A/D-muuntimen käyttämän piipinta-alan.

Asiasanat CMOS, sensori, kantataajuus, ΔΣ-modulaattori, algoritminen A/D-muunnin			
ISBN (painettu) 978-951-22-9364-3		ISSN (painettu) 1795-2239	
ISBN (pdf)		ISSN (pdf)	
Kieli	Englanti	Sivumäärä	122 s. + liit. 78 s.
Julkaisija	Teknillinen korkeakoulu, Elektroniikan, tietoliikenteen ja automaation tiedekunta		
Painetun väitöskirjan jakelu Teknillinen korkeakoulu, Mikro- ja nanotekniikan laitos			
☒ Luettavissa verkossa osoitteessa http://lib.tkk.fi/Diss/2008/isbn9789512293650/			

Preface

The research for this thesis was carried out at the Electronic Circuit Design Laboratory of the Helsinki University of Technology during the period 2002-2006. The research was supported by the Nokia Research Center, VTI Technologies, and the Finnish Funding Agency for Technology and Innovation (TEKES). I would also like to thank the Ulla Tuominen Foundation and the Jenny and Antti Wihuri Foundation for their support.

I want to thank my supervisor Professor Kari Halonen for giving me the opportunity to work in the laboratory among very many talented design engineers. Professor Halonen provided me a unique opportunity to work on what are the most challenging and interesting current research topics. The reviewers of this thesis, Kimmo Koli, D.Sc. from ST Microelectronics, Finland, and Professor Svante Signell from the Royal Institute of Technology, Sweden, also deserve warm thanks for their comments and suggestions.

I thank all my former colleagues at the Electronic Circuit Design Laboratory for the many great memories I'm left with from the past eight years since I started to work as a research assistant in the laboratory. First of all, I want to thank Jussi Pirkkalaniemi, my friend and colleague from the beginning of my studies at Helsinki University of Technology. I want also to thank my team members during these studies. Jarkko Jussila, D.Sc. deserves thanks for the many valuable things he taught me. Professor Jussi Ryynänen also deserves thanks for taking care of the project management and giving valuable advice over the past five years or so. Jouni Kaukovuori deserves my special thanks for his great co-operation in various projects. I have really enjoyed our teamwork. Mika Kämäräinen, Matti Paavola, Mika Laiho, D.Sc. and Mikko Saukoski, D.Sc., you were a great team to work with. I want especially to thank Mikko Saukoski for many interesting discussions and for pushing me to give my best.

For the great laboratory spirit I want to thank in particular Väinö Hakkarainen, Lauri Koskinen, Pikkis, Harri Pellikka, Artturi Kaila, Ville Saari, Mikko Hotti, Jonne Lindeberg, Mikko Kaltiokallio, Mikko Kärkkäinen, Mikko Talonen, Mikko Varonen,

Lauri Sumanen, Saska Lindfors, Teemu Salo and Mika Länsirinne. I also want to thank Helena Yllö for the most enjoyable coffee room company and for keeping the laboratory working.

Of course, there has to be some balance between work and leisure. Therefore, I would like to thank my brother Juho and my dear friends Toni, Rami, Antti and Riku for all the free-time activities we have enjoyed during these years.

I am so grateful for the help given to me by my father Klaus Järvinen† and my mother Marjo Järvinen. Your love and support have brought me this far. I also wish to thank my grandparents Dagny Järvinen, Maija and Heikki Miettinen for believing in me. My parents-in-law Raili and Juha Hämäläinen are acknowledged for taking part in our family's life, not forgetting the great Sunday meals.

Finally, I would like to thank my beloved wife Tanja. Without your love this road would have been rocky and lonely. I want also to thank you for our lovely children Jasmin and Alex, who have brought so much happiness to my life.

Espoo, May 2008

Jere Järvinen

Contents

List of publications

[P1] J. A. M. Järvinen, J. Kaukovuori, J. Ryynänen, J. Jussila, K. Kivekäs, M. Honkanen, and K. A. I. Halonen, “2.4-GHz receiver for sensor applications,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 7, pp. 1426–1433, July 2005.

[P2] J. Kaukovuori, J. A. M. Järvinen, J. Ryynänen, J. Jussila, K. Kivekäs, and K. A. I. Halonen, “Direct-conversion receiver for ubiquitous communications,” in *Proc. IEEE Radio and Wireless Symposium*, 17-19 Jan. 2006, pp. 103–106.

[P3] J. Järvinen and K. Halonen, “A 1.2V dual-mode GSM/WCDMA $\Delta\Sigma$ modulator in 65nm CMOS,” in *Proc. IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, 5-9 Feb. 2006, pp. 488–489.

[P4] J. A. M. Järvinen, M. Saukoski, and K. Halonen, “A 12-bit 32μW ratio-independent algorithmic ADC,” in *Proc. Symposium on VLSI Circuits*, 15-17 June 2006, pp. 58–59.

[P5] M. Paavola, M. Kämäräinen, J. A. M. Järvinen, M. Saukoski, M. Laiho, and K. A. I. Halonen, “A 62μA interface ASIC for a capacitive 3-axis microaccelerometer,” in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, Dec. 2007, pp. 2651–2665.

[P6] J. A. M. Järvinen, M. Saukoski, and K. Halonen, “A 12-bit ratio-independent algorithmic A/D converter for a capacitive sensor interface,” in *IEEE Transactions on Circuits and Systems – I*, vol. 55, no. 4, Apr. 2008, accepted for publication.

Contribution of the author

[P1] **2.4-GHz Receiver for Sensor Applications**

The receiver was designed, implemented, and measured by a research team which consisted of four members, including the author. The other members were Prof. J. Ryynänen, Mr. J. Kaukovuori, and D.Sc J. Jussila. The author is responsible for the design and implementation of the baseband circuits together with D.Sc J. Jussila. The measurements were made together with Mr. J. Kaukovuori, who was responsible for the design and implementation of the radio frequency (RF) front-end together with Prof. J. Ryynänen. The writing of the manuscript was done by the whole research team together. The other authors, D.Sc K. Kivekäs and Mr. M. Honkanen, are mainly responsible for writing about details conserning the sensor system. Prof. K. Halonen made valuable comments on the manuscript. The circuit was originally published in [1]

[P2] **Direct-conversion Receiver for Ubiquitous Communications**

This paper is an improved version of [P1]. As in [P1], the author is responsible for the design and implementation of the baseband circuits together with D.Sc J. Jussila, who had the main design responsibility for the limiting amplifier and current reference designs. The measurements were made together with Mr. J. Kaukovuori. The writing of the manuscript was done by the whole research team together. Prof. K. Halonen made valuable comments on the manuscript.

[P3] **A 1.2V Dual-Mode GSM/WCDMA $\Delta\Sigma$ Modulator in 65nm CMOS**

The author was responsible for all the work regarding this paper. Prof. K. Halonen supervised the author and made valuable comments on the manuscript.

[P4] **A 12-bit 32μW Ratio-Independent Algorithmic ADC**

The author is responsible for the design and implementation of the analog-to-digital (A/D) converter topology. The writing of the manuscript and the design of the dynamically biased operational amplifier were performed in co-operation with Mr. M. Saukoski. Prof. K. Halonen made valuable comments on the manuscript.

[P5] **A 62μA Interface ASIC for a Capacitive Three-Axis Microaccelerometer**
The interface ASIC was designed, implemented, and measured by a research team which consisted of five members, including the author. The other team members were Lic.Sc M. Paavola, Lic.Sc M. Kämäräinen, Mr. M. Saukoski, and D.Sc M. Laiho. The author is responsible for the design and implementation of the A/D converter. Lic.Sc M. Paavola designed the clock generators and voltage, current, and temperature references under the supervision of D.Sc M. Laiho and Mr. M. Saukoski. Lic.Sc M. Kämäräinen was responsible for the design of the capacitive sensor front-end under the supervision of Mr. M. Saukoski. Mr. M. Saukoski also contributed to the system level design and, with the author, co-designed the dynamic amplifiers for the A/D converters. The writing of the manuscript was done by the whole research team together. Prof. K. Halonen made valuable comments on the manuscript. The whole system was originally published in [2] and the designed A/D converter is published separately in [P6,3].

[P6] **A 12-bit Ratio-Independent Algorithmic A/D Converter for a Capacitive Sensor Interface**
This is a more detailed description of the A/D converter presented in [P5,3]. As in [P4], the author is responsible for the design and implementation of the A/D converter. The author designed the dynamically biased operational amplifier in co-operation with Mr. M. Saukoski. The writing of the manuscript was done together with Mr. M. Saukoski. Prof. K. Halonen made valuable comments on the manuscript.

Symbols and abbreviations

β	Feedback factor
ΔV_G	Voltage change at the transistor gate
$\Delta\Sigma$	Delta-Sigma
γ	MOS transistor process-dependent noise excess factor
∞	Infinity
μ_n	NMOS transistor carrier mobility
μ_p	PMOS transistor carrier mobility
ω_c	Gain stage corner frequency
ω_n	Pole frequency
$\omega_{1,2}$	Two-tone test signal frequencies
ω_{bb}	Baseband passband edge corner frequency
ω_{FB}	-3-dB corner frequency of the feedback loop
$\overline{\phi_{1,2}}$	Inverted clock phases
$\overline{\phi_{1a,2a}}$	Advanced inverted clock phases
$\overline{clk}$	Inverted clock signal
$\phi_{1,2}$	Clock phases
$\phi_{1a,2a}$	Advanced clock phases
τ	Settling time constant
ξ	Damping factor
A	Area

$A(s)$	Amplifier transfer function in s-domain
A_0	Amplifier gain at zero frequency
a_0	DC gain of low-pass second-order system transfer function
$A_F(s)$	Transfer function of an amplifier in a feedback loop
A_s	Gain stage gain at zero frequency
$A_{0,tran}$	Limiter transient gain at zero frequency
$a_{1,2}$	Integrator gain coefficients
A_{FB}	DC gain of the feedback loop
$A_{LP}(s)$	Transfer function of a low-pass second-order system
A_{MAX}	Maximum transient gain
A_{tot}	Total gain of M-stage cascade
$b_{1,2}$	Feedback scaling coefficients
$BIT(i)$	Bit on the i_{th} cycle
clk	Clock signal
D	Duty cycle
DNL	Differential nonlinearity
DR	Dynamic range
e	Quantization error
$E(z)$	Quantization error in z-domain
$E^2(f)$	Quantization noise power spectral density
e_n^2	MOS transistor noise mean square value
e_{rms}^2	Quantization error mean square value
$ENOB$	Effective number of bits
f	Frequency
f_s	Sampling frequency

f_{bb}	Baseband bandwidth
f_{bw}	Signal bandwidth
f_{clk}	Clock frequency
f_{IN}	Input signal frequency
FOM_A	Area figure of merit
FOM_F	Filter figure of merit
FOM_P	Power figure of merit
FOM_{PA}	Figure of merit including both power and area
G	Passband gain
g_m	Transistor transconductance
g_{ds}	Transistor drain-source conductance
GBW	Gain-bandwidth product
$H(f)$	Brick wall filter response
$H_{1,2}(z)$	Digital filters in z-domain
$H_{AC}(s)$	AC coupling transfer function
$H_{casc}(s)$	Transfer function of cascaded gain stages
$H_{FB}(s)$	Feedback loop transfer function
$H_S(s)$	Total DC feedback loop transfer function
i	Number of the cycle
I_B	Bias current
I_D	Drain current
$I_{1,2}$	Signal currents
I_{IN}	Input signal current
I_{OUT}	Output signal current
I_{slew}	Operation amplifier slewing current
I_{supply}	Current from power supply

ICP	Input compression point
$IIP2$	Second-order input intercept point
$IIP3$	Third-order input intercept point
IMD	Intermodulation distortion
INL	Integral nonlinearity
k	Boltzmann constant
k_0	DC offset coefficient
k_1	Linear gain coefficient
$k_2,\ k_3, \ldots, k_n$	Nonlinearity coefficients
KF	Process-dependent MOS transistor flicker noise parameter
L	MOS transistor gate length
L	Order of $\Delta\Sigma$ modulator loop filter
L_{ov}	MOS transistor channel overlap of the drain/source regions
LSB	Least significant bit
M	Number of cascaded gain stages
MSB	Most significant bit
N	Number of digitized bits
n_{bw}^2	Noise power in the signal band
$n_{thermal}^2$	Sampled thermal noise power
N_{steps}	Maximum number of operation steps per bit
NF	Noise figure
NF_{RF}	Front-end noise figure
NF_{RX}	Receiver noise figure
$NTF(z)$	Noise transfer function in z-domain

OCP	Output compression point
$OIP2$	Second-order output intercept point
$OIP3$	Third-order output intercept point
$Order$	Filter order
OSR	Oversampling ratio
p_1	Single-pole frequency
p_2	Non-dominant pole frequency
P_D	Power dissipation
P_{1dB}	1-dB compression point
P_{casc}	Total power dissipation of cascaded gain stages
$P_{IMD2,IN}$	Second-order *IMD* component at the input
$P_{IMD3,IN}$	Third-order *IMD* component at the input
P_{IN}	Input power
P_{OUT}	Output power
Q	Pole quality factor
Q_C	Charge in capacitor C
Q_{ch}	MOS switch transistor channel charge
S	Settling accuracy
$SFDR$	Spurious-free dynamic range
$SNDR$	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
$STF(z)$	Signal transfer function in z-domain
T	Absolute temperature
t	Time
t_b	Delay required to implement bottom plate sampling
t_o	Delay between the non-overlapping clock signals

T_s	Settling time
t_{duty}	Duration that the output signal is non-zero
T_{period}	Signal period
V	Test signal amplitude
$V(i)$	Voltage signal on the i_{th} cycle
v_C^2	Total thermal noise mean-squared value sampled to capacitor C
$v_{n,opamp}^2$	Total thermal noise mean-squared value of the operational amplifier
$V_{sine,rms}^2$	Sine wave mean square value
V_B	Bias voltage
V_G	Transistor gate voltage
V_{CMFB}	Common-mode feedback voltage
V_{ctrl}	Transistor gate control voltage
V_{DD}	Supply voltage
$v_{ds,sat}$	Transistor drain-source saturation voltage
V_{FS}	Full-scale voltage input range
V_{GS}	MOS transistor gate-source voltage
V_{IMD2}	Second-order intermodulation distortion
V_{IMD3}	Third-order intermodulation distortion
$V_{IN,min}$	Minimum input signal voltage
V_{INM}	Negative input signal voltage
V_{INP}	Positive input signal voltage
V_{IN}	Input signal voltage
V_{LSB}	Quantization step size
$v_{n,out,BB}$	Noise voltage density at the baseband output

V_{od}	MOS transistor gate overdrive voltage
V_{OFF}	Offset voltage
V_{OUTM}	Negative output signal voltage
V_{OUTP}	Positive output signal voltage
V_{OUT}	Output signal voltage
V_{REF}	Reference voltage
V_{SIG}	Signal amplitude
V_S	MOS transistor source voltage
V_{tn}	NMOS transistor threshold voltage
W	MOS transistor gate width
$X(z)$	Input signal in z-domain
$Y(z)$	Output signal in z-domain
3G	Third generation
A/D	Analog-to-digital
AC	Alternating current
Active-RC	Filter technique that uses resistors, capacitors, and operational amplifiers
ADC	Analog-to-digital converter
AGC	Automatic gain control
AM-to-PM	Amplitude variation to phase deviation
ASIC	Application-specific integrated circuit
BB	Baseband
BiCMOS	Bipolar CMOS
C	Capacitor
C_{bd}	MOS transistor channel-to-bulk and junction capacitance at drain

C_{bs}	MOS transistor channel-to-bulk and junction capacitance at source
C_C	Pole-splitting capacitor
C_{eff}	Effective load capacitance
C_{gd}	MOS transistor gate-to-drain and gate-to-channel capacitance
C_{gs}	MOS transistor gate-to-source and gate-to-channel capacitance
C_H	Sample-and-hold capacitor
C_{in}	Total OTA input capacitance
C_i	Integrating capacitor
C_L	Total load capacitance, load capacitor
C_{n1}	Parasitic capacitance at node n1
C_{ov}	MOS transistor overlap capacitance
C_{ox}	MOS transistor gate oxide capacitance
C_o	Total OTA output capacitance
C_s	Sampling capacitor
CDS	Correlated double sampling
CMFB	Common-mode feedback
CMFF	Common-mode feed-forward
CMOS	Complementary metal oxide semiconductor
CT	Continuous-time
D/A	Digital-to-analog
DC	Direct current
DEM	Dynamic element matching
DLL	Delay locked loop
DSP	Digital signal processor

DT	Discrete-time
FSK	Frequency-shift keying
g_m-C	Filter technique that uses transconductors and capacitors
g_m-C-OTA	Filter technique that uses transconductors,capacitors, and OTAs
GPRS	General packet radio service
GSM	Global system for mobile communication
ISM	Industrial, scientific and medical
K	Current-mirror ratio
LNA	Low-noise amplifier
LO	Local oscillator
$M_{1...n}$	MOS transistor number
MASH	Multi-stage noise shaping
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
MOSFET-C	Filter technique that uses MOSFETs, capacitors, and operational amplifiers
NMOS	N-channel metal oxide semiconductor
OTA	Operational transconductance amplifier
PDA	Personal digital assistant
PMOS	P-channel metal oxide semiconductor
R	Resistor
R_{ON}	MOS switch transistor on-resistance
R_S	Receiver input impedance
RF	Radio frequency
RFID	Radio frequency identification

rms	Root-mean-square
RSD	Redundant sign digit
RSSI	Received signal strength indicator
RX	Receiver
S^2I	Current-mode double-sampling
$S_{1\ldots n}$	Switch number
S/H	Sample-and-hold
SC	Switched-capacitor
SI	Switched-current
SO	Switched-opamp
SoC	System on chip
UWB	Ultra wideband
WCDMA	Wideband code division multiple access
WLAN	Wireless local area network

Chapter 1

Introduction

1.1 Motivation for the Thesis

Wireless sensors are small devices, intended to operate for several years without a battery change. Since they are wireless, they are optimal for monitoring hte environment and weather. Devices present in everyday life, such as a mobile phone or personal digital assistant (PDA) could act as a terminal and a gateway to internet and mobile networks for different sensors and short-range applications, as shown in Figure 1.1.

Extremely low power dissipation and material costs are the key requirements for battery-powered sensor modules. With modern deep sub-micron complementary metal oxide semiconductor (CMOS) processes, the cost-effective integration of a whole system on chip (SoC) is possible. Hence, for long stand-alone operation and cost-effective realization, minimizing power dissipation and silicon area are the main design targets.

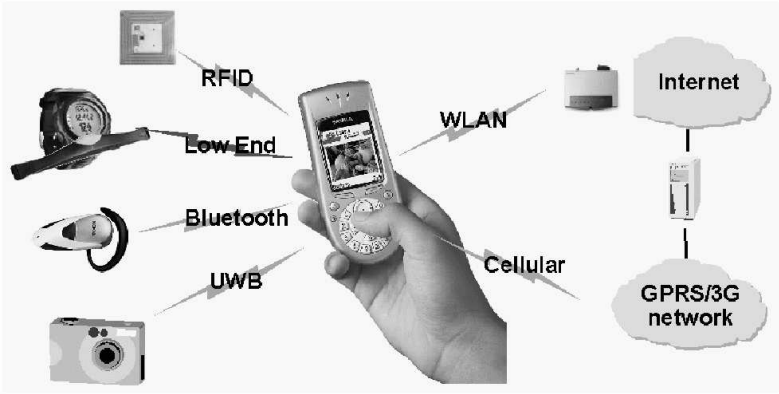

Figure 1.1 Mobile phone as a gateway to internet and mobile networks.

From the sensor radio receiver point of view, a high integration level can be achieved by using, for example, the direct conversion receiver architecture. The demand for low costs requires the use of CMOS technology without additional process options, such as high-quality resistors or capacitors. However, what makes the realization challenging is the fact that in deep sub-micron processes the available gain from a single transistor is only moderate. In addition, in a CMOS direct conversion receiver, the flicker noise increases the noise figure (NF) significantly. These two facts reduce the available operating range. However, since sensors are typically short-range devices, the reduction in operating range can be tolerated [4].

There are different solutions for wireless sensor networks on the market. However, the large number of radios required by various wireless standards makes the mobile phone design challenging. In addition, most of the solutions consume too much power for applications, such as wristtop computers. Hence, to fulfill the requirements for low power dissipation and to be able to utilize existing short-range radios in mobile phones, new low-power solutions based on existing short-range radios are required.

A mobile terminal used as a terminal should be capable of operating in the widely used global system for mobile communications (GSM) networks, as well as in third-generation wideband code division multiple access (WCDMA) networks, while having very low power dissipation in order to extend the life-time of the battery.

For sensor interfaces designed to read actual sensors, for example accelerometers, the design targets are rather similar. In every sensor interface, to be able to use digital signal processing, the measured analog data have to be converted into digital form. Hence, an A/D converter is required that is capable of meeting stringent requirements for both power dissipation and silicon area. In addition, flexibility in the A/D converter topology is preferred, since it enables the same circuit block to be used for tasks with different requirements for speed and accuracy.

1.2 Analog Circuit Design in Deep Sub-Micron CMOS

When deep sub-micron processes are used for analog design, most of the technology changes make the analog design even more challenging. With deep sub-micron processes, the available power supply is 1.2 V or less, and therefore the signal headroom required in analog designs is relatively small. The signal range in most of the analog blocks is reduced and cascode structures cannot be used, forcing the circuit solutions toward folded and cascade structures. Furthermore, as the supply voltage is reduced, the achievable linear range is narrowed, thus reducing the linear operation range. This makes the operation of metal oxide semiconductor (MOS) switches and MOS-resistances critical. With very short channel lengths, the source/drain contacts are reduced to only one, which can lead to increased resistance which is not desirable

especially in fast-operating switches. Furthermore, the matching of very short-channel transistors is poor, and in pure analog design, transistors with a minimum channel length are seldom, if ever, utilized.

One of the benefits of technology scaling in analog design is the increased bandwidth, which makes possible better RF and high frequency operation. On the other hand, the achievable speed can also be traded for reduced power dissipation. Even though amplifiers, for example, can be designed for higher bandwidth, the increase is only proportional to the scaling of the channel length. As a drawback, in deep submicron processes, the gain from a single transistor is moderate, making the design of applications requiring a high gain hard. Fortunately, some of the processes have options for high-voltage transistors, which can operate with higher supply voltages. With these transistors, analog applications requiring a large headroom can be implemented, while digital blocks can benefit from the technology scaling.

In this thesis, several solutions from different design aspects are presented to overcome the design challenges in deep sub-micron design. Some solutions are based on new circuit structures that are capable of operating with very low supply voltages [P1, P2, 1]. Some solutions utilize existing circuit structures whose operation is optimized for low-voltage operation, and take advantage of increased speed in deep sub-micron CMOS [P3]. Finally, some solutions utilize high-voltage transistors to implement analog circuits requiring supply voltages over 1.2V, while having very low power dissipation [P4, P6, P5, 2, 3].

1.3 Research Contribution

The research described in this thesis focuses on low-power sensor applications.

The author has designed and implemented baseband circuitry for direct conversion receivers for ubiquitous communications. The first prototype was published in [P1, 1]. The whole system was implemented in [P2]; however, only the receiver part implemented by the authors was reported. The other team members were Mr. J. Kaukovuori, D.Sc J. Jussila, and Prof. J. Ryynänen. Mr. J. Kaukovuori and Prof. J. Ryynänen were responsible for the RF front-end design. The author was responsible for the analog baseband circuitry, together with D.Sc J. Jussila. The project demonstrated that in ubiquitous communications, the power dissipation can be reduced significantly from that found in the solutions presently on the market.

The design possibilities with deep sub-micron CMOS processes were studied in a project in which a low-pass $\Delta\Sigma$ modulator was designed and implemented for a direct conversion receiver [P3]. The main objective was to find out, what the design challenges are and what kind of performance can be achieved. The other team members were Mr. J. Kaukovuori and Prof. J. Ryynänen, who were responsible for the

RF front-end. The author was responsible for the $\Delta\Sigma$ modulator design. The project demonstrated, that with deep sub-micron CMOS processes, high-performance designs can be achieved using robust circuit structures with careful design.

Sensor applications were again studied in a project in which the author designed and implemented algorithmic A/D converters for a capacitive sensor interface. Various innovative A/D converter topologies were developed by the author in order to minimize the power dissipation and silicon area of the A/D converter [P4, P6, 3]. The whole system was published in [P5, 2]. The other team members were Lic.Sc M. Paavola, Lic.Sc M. Kämäräinen, Mr. M. Saukoski, and D.Sc M. Laiho.

1.4 Organization of the Thesis

This thesis is divided into two parts. In the first part, the issues related to direct conversion receiver design are covered. The existing solutions for ubiquitous communications are briefly covered and the proposed system is described. The main focus is on the baseband circuit design.

The second part considers low-power A/D converter design. The emphasis is on the design and implementation of A/D converter topologies suitable for sensor applications and mobile terminals.

Chapter 2

Baseband Circuits for Wireless Sensors

2.1 General

In recent years, wireless sensor networks that do not require high speed or accuracy have been gaining more attention in the field of wireless data transmission and networking [5–18]. Sensor networks can be made up of hundreds of nodes, and therefore each sensing node needs to be inexpensive and compact, while still providing reliable and accurate sensing and data transmission. Sensors are typically short-range devices [4] and data are transmitted in a peer-to-peer fashion over short distances ($\sim$10 m) at relatively low data rates ($<$500 kbps). Typically, the main design target for these systems is a very low power dissipation. Since sensors are typically battery-powered devices, to achieve stand-alone operation for over one year, extremely small active and stand-by currents are required. Furthermore, the requirement to implement an inexpensive and compact system leads to a small device with a minimum number of external components. A high integration level can be achieved by using, for example, a direct-conversion receiver.

Sensors can be utilized in different places such as office buildings, homes, and schools. Wireless sensors are convenient for monitoring the environment and weather. Sensors can monitor, for example, temperature, wind, pressure, direction, and acceleration. The actual sensing element can be integrated into the sensor itself, or the sensor can be used to transfer the data from an external measurement instrument to a user interface. In addition to different measurement applications, other small devices would also benefit from the short range, low data rate, and wireless connectivity. A mobile terminal is a suitable user interface for the sensors, since most people carry

one with them all the time. Standard Bluetooth radio [19] is implemented in most modern mobile terminals. However, the standard Bluetooth radio's power dissipation and capability of handling a large number of sensor nodes power efficiently are not suitable for low-power wireless sensor systems. Hence, to fulfill requirements for low power dissipation and to be able to utilize existing Bluetooth radios in mobile phones, a low power version of Bluetooth radio with slight changes in the radio parameters was introduced [20].

The architecture of the implemented wireless direct-conversion sensor receiver is shown in Figure 2.1. The total system architecture and system specifications are presented in [20], and the receiver design is presented in [P1, P2]. The implemented baseband circuits in this thesis include a mixer-baseband interface, channel-select filter, 1-bit limiters for the A/D conversion, and a one-level received signal strength indicator (RSSI) for signal level detection. The 1-bit resolution, together with the large modulation index, makes the receiver insensitive to strong reception signals [20]. In the following sections, specifications and an overview of the implemented building blocks are given.

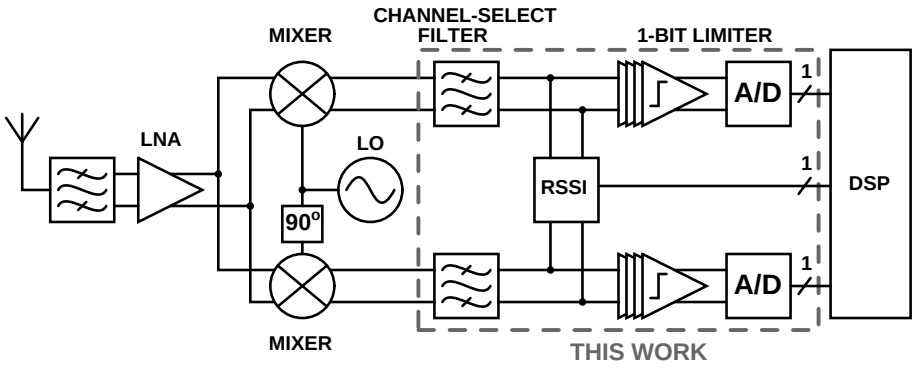

Figure 2.1 Direct-conversion wireless sensor receiver.

2.2 Specifications for Sensor Baseband Circuits

In this section, important specifications used to measure radio receivers are reviewed. The emphasis is on specifications that are important for baseband building blocks. Some measures that enable different filter and limiter realizations to be compared are also given.

2.2.1 Noise Figure and Baseband Noise

In low-power direct-conversion wireless receivers implemented using deep sub-micron CMOS processes, the *NF* of the receiver is typically dominated by the flicker noise in direct-conversion mixers. However, in order not to further degrade the *NF* of the whole receiver, the noise contribution of the baseband circuits should be minimized. The output noise of the baseband (BB) referred to receiver (RX) input can be calculated using (2.1) [21]

$$v_{n,out,BB} = A_{V,RX}\sqrt{\left(10^{(NF_{RX}/10)} - 10^{(NF_{RF}/10)}\right) kT2 f_{bb} R_S}, \tag{2.1}$$

where NF_{RX} is the receiver *NF*, NF_{RF} is the front-end *NF*, k is the Boltzmann constant, T is the absolute temperature, f_{bb} is the baseband bandwidth, and R_S is the receiver input impedance.

2.2.2 Linearity

The output signal of a memoryless nonlinear system can be expressed using a Taylor series expansion

$$V_{OUT} = k_0 + k_1 V_{IN} + k_2 V_{IN}^2 + k_3 V_{IN}^3 + \cdots + k_n V_{IN}^n, \tag{2.2}$$

where V_{IN} is the input signal voltage, the coefficient k_0 is a DC offset, k_1 is the linear gain of the system, and the coefficients $k_2,\ k_3, \ldots, k_n$ represent the system nonlinearity.

Typically, a two-tone test is used to measure the linearity of a radio receiver. In the two-tone test, two sinusoidal test signals with equal amplitude V and some frequency offset are fed into a nonlinear system described by (2.2). The resulting input signal with input signal frequencies ω_1 and ω_2 is

$$V_{IN}(t) = V\big(\cos(\omega_1 t) + \cos(\omega_2 t)\big) \tag{2.3}$$

At the output, only second- and third-order distortion components are taken into account. The resulting low-frequency second-order *intermodulation distortion (IMD)* that falls into the baseband filter passband is

$$V_{IMD2}(t) = k_2 V^2 \cos\big((\omega_1 - \omega_2)t\big). \tag{2.4}$$

The frequencies are chosen to be such that $\omega_1 - \omega_2 < \omega_{bb}$, where ω_{bb} is the baseband passband edge corner frequency. The resulting low-frequency third-order *IMD* that

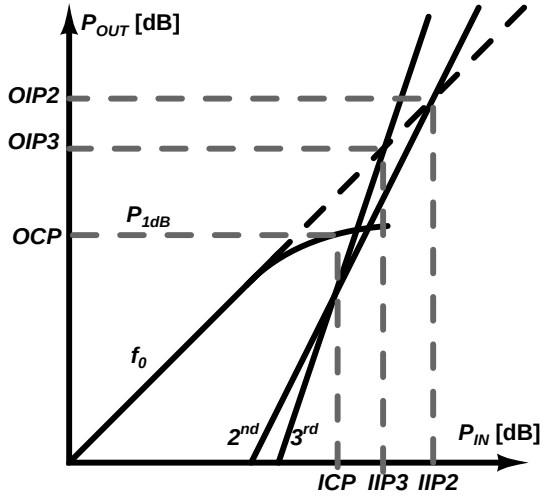

Figure 2.2 The definition of the intercept points and the 1-dB compression point.

falls into the baseband filter passband is

$$V_{IMD3}(t) = \frac{3}{4} k_3 V^3 \cos\left((2\omega_1 - \omega_2)t\right) \tag{2.5}$$

Here the frequencies are chosen to be such that $\omega_1 < \omega_2$, and $2\omega_1 - \omega_2 < \omega_{bb}$.

The definitions of the intercept points and the 1-dB compression point at the input and the output are shown in Figure 2.2. The second- and third-order intercept points are defined as the input powers, where the extrapolated output signal crosses the second- or third-order *IMD* lines.

The *second-order input intercept point (IIP2)* is given by

$$IIP2 = 2P_{IN} - P_{IMD2,IN} = OIP2 - G, \tag{2.6}$$

where P_{IN} is the input power of each two-tone test signal, $P_{IMD2,IN}$ is the second-order *IMD* component at the input, G is the passband gain, and $OIP2$ is the second-order output intercept point.

The *third-order input intercept point (IIP3)* is given by

$$IIP3 = \frac{3P_{IN} - P_{IMD3,IN}}{2} = OIP3 - G, \tag{2.7}$$

where $P_{IMD3,IN}$ is the third-order *IMD* component at the input, and $OIP3$ is the third-order output intercept point.

When a single-tone signal with an amplitude V and a frequency of ω_1 is fed into a

nonlinear system described by (2.2), the resulting fundamental output signal at ω_1 is

$$V_{OUT} = \left(k_1 V + \frac{3k_3 V^3}{4}\right)\cos(\omega_1 t). \tag{2.8}$$

If the coefficients k_1 and k_3 have opposite signs, the output starts to compress at some input signal level. The input signal power at which the gain is reduced by 1 dB compared to the linear gain is called the *input compression point (ICP)*. The *OCP* is the output compression point.

2.2.3 Duty Cycle

A duty cycle is an important parameter in limiting amplifiers, since deviation from 50% in the duty cycle degrades the achievable signal-to-noise ratio [22]. In limiter design, the duty cycle is measured to define how much the limited output differs from the ideal with a sine wave input signal. The duty cycle shown in Figure 2.3 is defined as

$$D = \frac{t_{duty}}{T_{period}} \cdot 100\% \tag{2.9}$$

where t_{duty} is the duration that the output signal is non-zero, and T_{period} is the signal period. For a pure sine wave input signal with a zero offset, the limited output duty cycle is ideally 50%. In reality, some offset voltage exists at the limiter input and degrades the duty cycle, as shown in (2.10).

$$D = \frac{t_{duty}}{T_{period}} \cdot = \frac{1}{2}\left(1 + \frac{V_{OFF}}{V_{SIG}}\right) \cdot 100\%, \tag{2.10}$$

where V_{OFF} is the offset voltage and V_{SIG} is the amplitude of the signal. For a limited signal, the signal amplitude is half of the signal range.

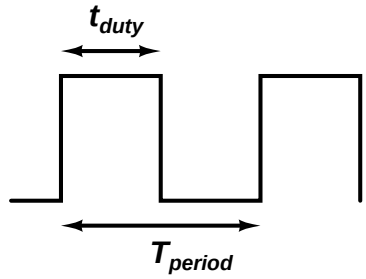

Figure 2.3 Duty cycle.

2.2.4 Group Delay and AM-to-PM conversion

The group delay is defined as a signal propagation delay variation through the system with different input signal levels, causing phase shift. However, for limiting amplifiers, the propagation delay depends on the signal level, whereas the group delay variation as a function of input signal frequency is negligible. Hence, limiting amplifiers convert amplitude variation into phase fluctuations, phenomena also called amplitude variation to phase deviation (AM-to-PM) [22, 23]. Amplitude variation can result from the user abruptly moving the receiver terminal nearer to or away from the sensor. This can potentially degrade the signal-to-noise ratio in a phase-sensitive FSK detector [22]. In this work, group delays measured in [P1,P2] are considered as a AM-to-PM conversion and measured as a variation in the propagation delay at a single input signal frequency with different input signal levels, as was also done in [22].

2.2.5 Start-up Time

In sensor systems, the receiver can be idle for long periods of time and will wake up only when something has to be received. Hence the stand-by time of the system can be significantly improved if the power dissipation in the idle mode can be designed to be negligible. However, if the system often alternates between active and idle modes, the system start-up time must be kept short in order to minimize power dissipation [P1]. The start-up time is defined as the time from the wake-up signal until the system has started. In this work, the start-up time was measured in [P1] from the baseband filter output, which excludes the start-up delay caused by the limiter. In [P2], the start-up time was measured from the limiter output, which gives the real start-up time of the whole system.

2.2.6 Filter Performance Comparison

To be able to compare different filter realizations for short-range communications, a figure of merit that gives the filter power dissipation per pole is given by

$$FOM_F = \frac{P_D}{Order \cdot f_{bb}}, \tag{2.11}$$

where P_D is the filter power dissipation, $Order$ is the filter order, and f_{bb} is the baseband bandwidth.

2.3 Sensor Baseband Circuits

In a wireless direct-conversion sensor receiver, the baseband typically includes channel-select filters, some sort of A/D conversion, and input signal level detection. In sensor receivers, the A/D conversion can be implemented using a limiter, giving a 1-bit A/D conversion. The benefit of 1-bit A/D conversion is insensitivity to strong reception signals, since the input signal is always limited. Hence the A/D converter, namely the limiter, is never overloaded. Input signal level detection is used to control the received and transmitted power levels. In this section, an introduction to the channel-select filters, limiters, and input signal level detection circuits for wireless sensor receivers is given. The sensor baseband circuits designed in this thesis are published in papers [P1, P2, 1].

2.3.1 Mixer-Baseband Interface

The mixer predominantly used in direct-conversion receivers is a Gilbert-cell mixer. The output of a Gilbert-cell mixer is current. Hence, the mixer-baseband interface can be a current- or voltage-mode interface. In a voltage-mode interface the signal current is driven to a high-impedance node, resulting in a voltage swing at the mixer output. The front-end voltage gain is now determined from the low-noise amplifier (LNA) input to the mixer output. In a current-mode interface the signal current is driven to a low-impedance node. Hence there is no voltage swing at the mixer output, and the signal current is converted to a voltage at the output of the first baseband stage. Therefore, the front-end voltage gain will be merged with the gain of the first baseband stage, and is now determined from the LNA input to the output of the first baseband stage. Next, some voltage- and current-mode interface topologies are discussed.

Two voltage-mode mixer-baseband interfaces are shown in Figure 2.4. The high-impedance interface required for the voltage-mode operation can be implemented using an operational amplifier [7, 16] or just a MOS transistor [8]. The voltage-mode mixer-baseband interface with load resistors in Figure 2.4 a) is implemented in [7, 8, 16]. In this solution, the resistance values determine the voltage gain from the LNA input to the mixer output. However, the mixer bias current and supply voltage limit the feasible resistance values. Adding current sources in parallel with the resistances would reduce the bias current flowing through the resistors, allowing higher resistance values, and would result in an increased impedance level and voltage gain. However, additional current sources will add another noise source to the interface. The voltage-mode mixer-baseband interface with floating load resistors and current sources in Figure 2.4 b) is implemented in [11, 22]. Now the whole current drawn by the mixer flows through current source transistors, resulting in increased noise. However, the resistance values can be increased for larger voltage gain. Resistances also take care of the common-

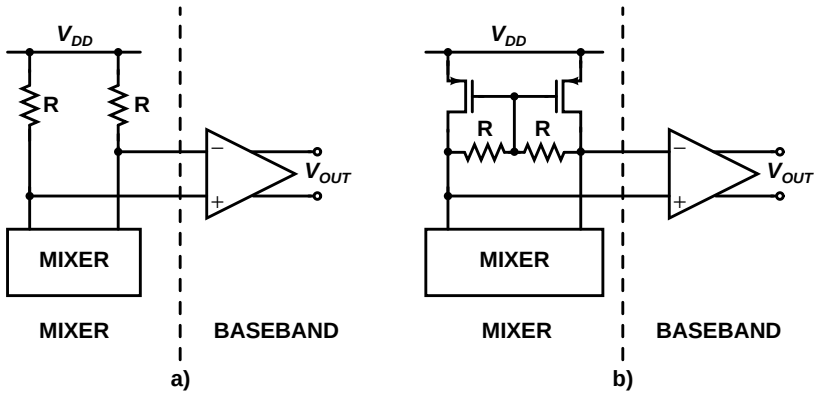

Figure 2.4 Different voltage-mode mixer-baseband interfaces.

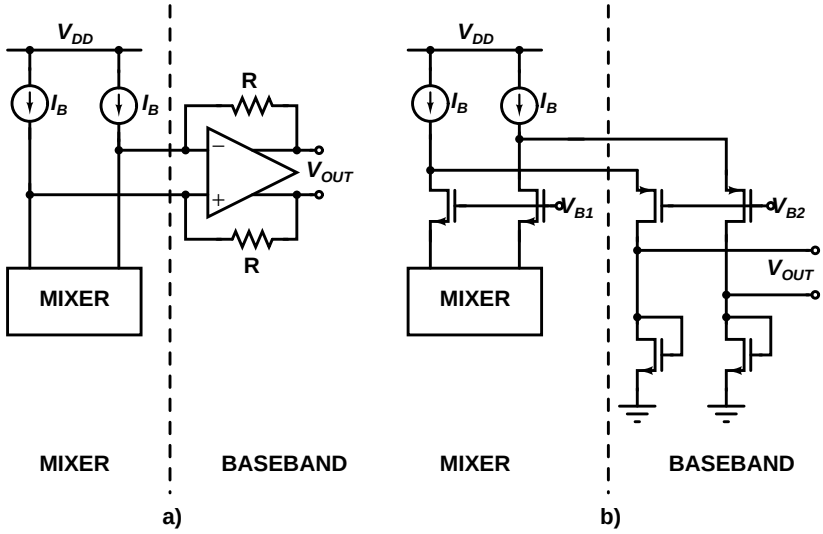

Figure 2.5 Different current-mode mixer-baseband interfaces.

mode feedback circuit (CMFB). For all-MOS realization, the resistances would have to be removed and the transistors would have to have separate diode-connections, making the mixer load impedance $\sim 1/g_m$, where g_m is the transistor transconductance. In many cases, the impedance level is insufficient, resulting in poor voltage gain and increased *NF* in the receiver. The impedance level could again be increased by adding current sources in parallel, again adding another noise source to the interface.

Two different current-mode mixer-baseband interfaces are shown in Figure 2.5. The low-impedance node required for the current-mode operation can be, for example, a transimpedance amplifier input or a cascode transistor source. Furthermore the mixer bias current can be optimized, since the biasing is based purely on current sources [P1]. The current mode mixer-baseband interface can be implemented using current source

loads, as shown in Figure 2.5 a) [24]. In this realization, the low-impedance node is implemented using a transimpedance amplifier. This transimpedance amplifier can be used as the first stage of a lossy active-RC integrator [24], in which integrating capacitors are added in parallel with the feedback resistor. If a lossless active-RC integrator is used, an additional DC feedback loop has to be implemented to provide appropriate biasing.

The current mode mixer-baseband interface can also be implemented using cascode transistors, as shown in Figure 2.5 b) [P1, P2]. N-channel MOS (NMOS) cascode transistors can be removed for operation with a very low power supply. If required, the impedance level at the P-channel MOS (PMOS) cascode transistor sources can be lowered using regulated PMOS cascode transistors, in which a feedback amplifier is used to keep the cascode transistor drain-source voltage as stable as possible [25, 26]. Compared to the topology in Figure 2.5 a), the current through the PMOS current sources is larger, resulting in increased noise. However, neither operational amplifiers nor resistors are required, making the topology suitable for all-MOS realizations. Furthermore, the topology is well suited to operation with a very low supply voltage.

It can be concluded, that for low-voltage applications, a current-mode interface is more suitable, since there is no voltage signal at the mixer output. Hence the mixer does not require additional headroom for voltage swing. The noise contribution of the current-mode interface is equal to or larger than that in the voltage-mode interface [21]. However, in sensor applications, some operating range can be traded for noise. Finally, the current-mode interface topology shown in Figure 2.5 b) is well suited for all-MOS realizations.

2.3.2 Continuous-Time Active Filters

The most popular baseband filter architectures for sensor receivers are active-RC [7, 11, 14, 27] and g_m-C [8, 12, 28, 29]. Next, the two filter topologies are introduced.

2.3.2.1 Active-RC

A very popular continuous-time filter topology is based on an inverting active-RC integrator shown in Figure 2.6. In practice, the fully differential structure shown in Figure 2.6 b) is used, since it is less sensitive to power supply noise and even-order harmonic distortion. However, the required silicon area is approximately doubled. The active-RC integrator requires a resistor, an operational amplifier, and a capacitor in a negative feedback loop. As a result of the negative feedback loop, there is a virtual ground at the operational amplifier inputs. When the input signal voltage is applied, the input resistor R transforms the input voltage into a current, which is integrated by the feedback capacitor C. The resulting transfer function for the active-RC integrator

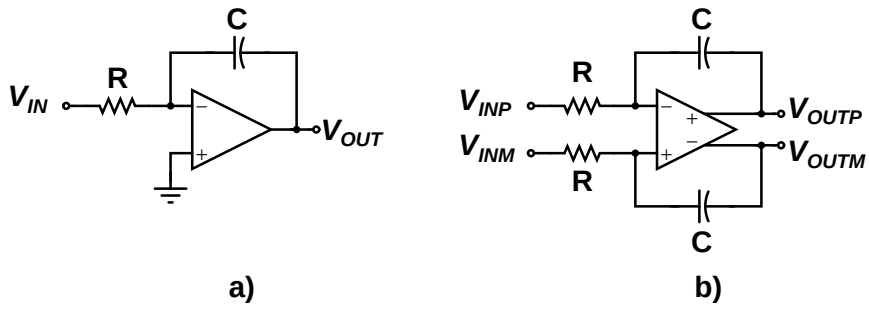

Figure 2.6 a) A single-ended active-RC integrator. b) A fully differential active-RC integrator.

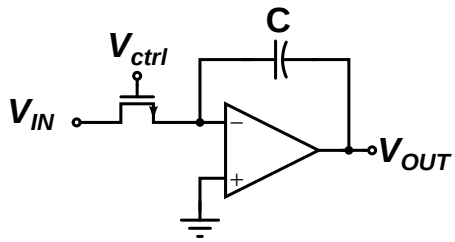

Figure 2.7 a) A single-ended MOSFET-C integrator.

in the s-domain is

$$V_{OUT}(s) = -\frac{1}{sRC}V_{IN}. \tag{2.12}$$

The benefits of the active-RC integrator are that as a result of the virtual ground, different input signals can be summed at the operational amplifier input without any additional active components by adding an another input resistor. In addition, lossy integrators can be implemented, without any additional current, by adding a resistor in parallel with the integrating capacitor. Additionally, the active-RC integrator is insensitive to parasitic capacitances, since the input and the output of the operational amplifier have well-controlled voltages. The drawback of active-RC integrators is that the filter time constant varies considerably as a result of variations in temperature and process, since the variations in the resistors and capacitors do not correlate. Hence, in practice, the time constants are tuned using parallel integrating capacitors, resulting in increased silicon area. The silicon area can be reduced using MOSFET-C integrators, in which the resistor is replaced with a MOS-transistor operating in a triode-region, as shown in Figure 2.7. The area required by the transistors is much less than that required by the resistors. In addition, the filter time constants can be tuned by changing the control voltage V_{ctrl} at the MOS-transistor gate. The drawback of the solution is a reduced linear signal range.

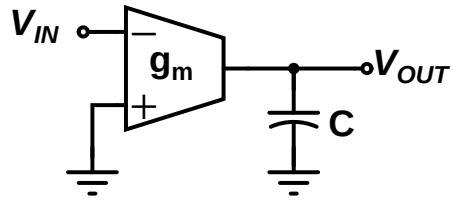

Figure 2.8 The single-ended g_m-C integrator.

2.3.2.2 g_m-C

Another widely used continuous-time integrated filter technique is a g_m-C filter. A single-ended inverting g_m-C integrator used in g_m-C filters is shown in Figure 2.8. The input voltage at the input of a voltage-to-current converter or transconductor [30] with a transconductance g_m is converted to a current at the transconductor output, where it is integrated by the capacitor C. The resulting transfer function for the g_m-C integrator in the s-domain is

$$V_{OUT}(s) = -\frac{g_m}{sC} V_{IN}. \tag{2.13}$$

Typically, for linear transconductors , a combination of several transistors is used, each contributing noise. Hence, compared to the RC integrator, the noise of the g_m-C integrator is significantly higher, with values of 2 to 3 being common [31]. While the active-RC integrator does not require additional active components for input signal summing and for lossy integrators, the g_m-C integrator requires additional parallel transconductors for summing different input signals and for realizing the lossy integrator shown in Figure 2.13.

Because of their better immunity to power supply noise and even-order harmonic distortion, g_m-C filters are also implemented using a fully differential g_m-C integrator as shown in Figure 2.9 a). The fully differential structure doubles the total capacitance, as is the case for active-RC realizations (Figure 2.6), where the resistance is also doubled. Fortunately, a fully differential g_m-C integrator with a floating capacitor, as shown in Figure 2.9 b), can be used to reduce the total capacitance to one quarter of the original capacitance. In applications, where the silicon area should be minimized, this gives a great advantage over active-RC realizations.

The g_m-C filter time constant also varies as a result of temperature and process variations. However, tuning the g_m-C filters time-constants is possible by using capacitor arrays, as in active-RC filters, or tuning the bias currents, in which case continuous tuning becomes possible. Invariably, the use of continuous tuning brings some loss of maximum signal handling capability [31, 32]. However, the savings in silicon area and the much better tuning accuracy act in favor of bias current tuning.

g_m-C integrators are sensitive to parasitic capacitances at the output of a transcon-

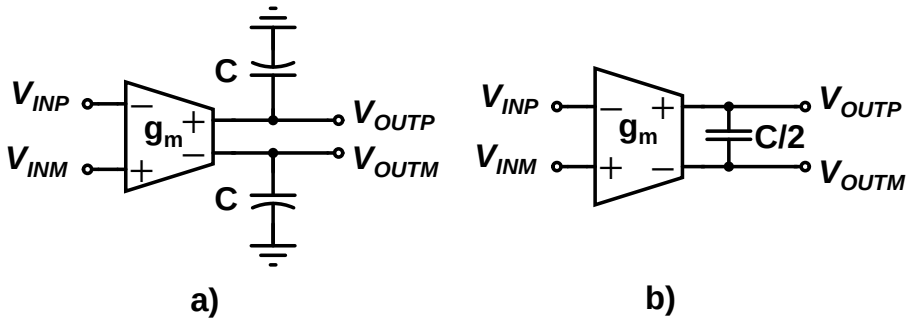

Figure 2.9 a) A fully differential g_m-C integrator. b) A fully differential g_m-C integrator with a floating capacitor.

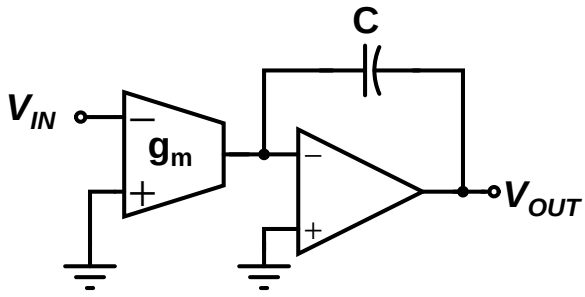

Figure 2.10 A single-ended g_m-C-OTA integrator.

ductor. The effect of the parasitic capacitances can be greatly reduced by using an operational transconductance amplifier (OTA), discussed later in Section 3.3.1, in the g_m-C-OTA integrator shown in Figure 2.10 [33].

For modest linearity applications, such as sensor receivers, MOS transistors may replace the capacitors, thus allowing a high capacitance per unit area and implementation in fabrication processes intended for purely digital very large-scale integration [34]. However, floating capacitors are hard to implement using only MOS transistors. Hence, in all-MOS realizations, structures with grounded capacitors are preferred, eliminating structures with floating capacitors, such as the fully differential g_m-C integrator with a floating capacitor in Figure 2.9 b) and in the g_m-C-OTA integrator. However, the g_m-C-OTA integrator can be implemented using PMOS transistors operating in the triode region, since the common-mode levels at the input and output of the OTA can be different, making possible the appropriate voltage over the PMOS transistors [35].

2.3.2.3 All-MOS g_m-C Filter

For sensor receivers operating on a single button cell battery, the key requirements are extremely low power dissipation and material costs. In addition, the receiver has to

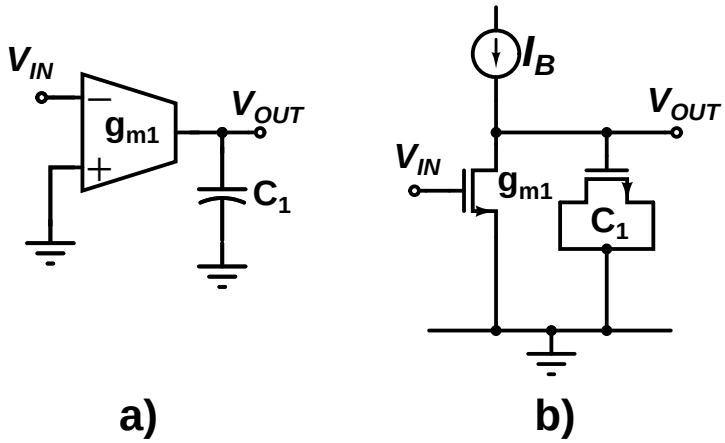

Figure 2.11 a) The single-ended lossless inverting g_m-C integrator. b) Equivalent all-MOS transistor implementation.

be able to operate with a supply voltage limited to 1.0–1.5 V. Taking these specifications into account, a suitable filter architecture for sensor receivers is the g_m-C filter. Furthermore, a simple realization using only MOS transistors results in a small area and compatibility with processes optimized for digital signal processing. Even though the fully differential structures are less sensitive to noise and distortion, the use of two single-ended circuits without intermediate cross-connections, a so-called pseudo-differential structure [28], is a good alternative. This structure does not need a CMFB circuit, which helps the design when using low supply voltages. However, the structure offers no common-mode rejection. Hence, mismatches in the pseudo-differential signal chains convert some of the common-mode signal to differential. Next, basic single-ended building blocks for all-MOS g_m-C filters are discussed.

A single-ended lossless inverting g_m-C integrator and its equivalent all-MOS transistor implementation are shown in Figure 2.11. A non-inverting counterpart is shown in Figure 2.12. The MOS capacitor is implemented using a NMOS transistor in inversion. An accumulation region PMOS transistor would be more linear [34], but implementing both the transconductor and MOS capacitor with the same type of transistor results in better matching in process variations. To make it possible to implement a lossy g_m-C integrator, an additional transconductor is required, as shown in Figure 2.13.

Using the building blocks described above, the single-ended all-MOS g_m-C biquad shown in Figure 2.14 can be implemented [P1]. A biquad using similar building blocks to those described above is presented in [36]. However, this biquad structure requires floating capacitors, making an all-MOS implementation difficult.

Higher even-order filters can be implemented by cascading the biquad stages. For

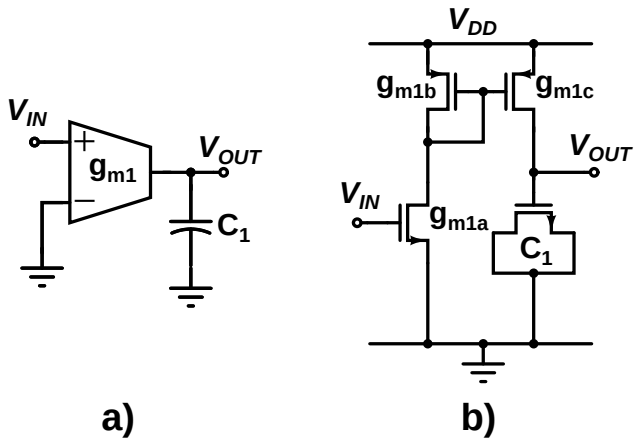

Figure 2.12 a) The single-ended lossless non-inverting g_m-C integrator. b) Equivalent all-MOS transistor implementation.

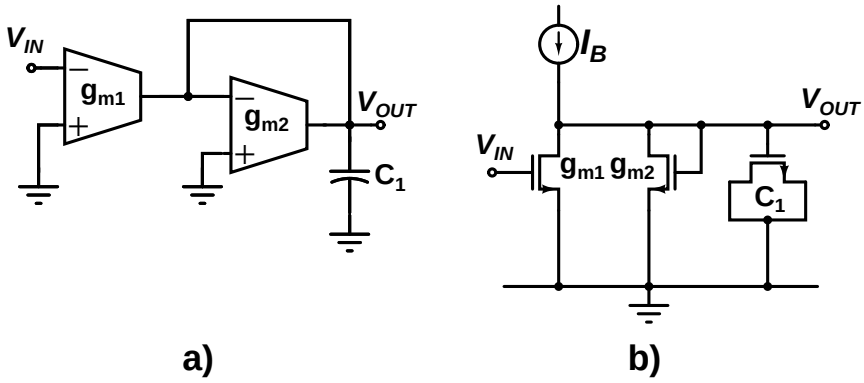

Figure 2.13 a) The single-ended lossy inverting g_m-C integrator. b) Equivalent all-MOS transistor implementation.

the odd-order filters, one of the poles lies on the real axis of the s-plane. Thus the pole can be realized by using passive components available in an analog process [37, 38]. In an all-MOS realization, the pole can be implemented for a current-mode input signal I_{IN} with a diode-connected MOS transistor and a MOS capacitor, as shown in Figure 2.15. This kind of structure is used in [P1, P2] to implement the real pole in the mixer-baseband interface. In [P2], a second real pole is implemented to provide an additional attenuation of strong out-of-band interfering signals. Using the building blocks described above, higher-order filters can also be implemented with a leapfrog structure, resulting in lower sensitivity to component variations.

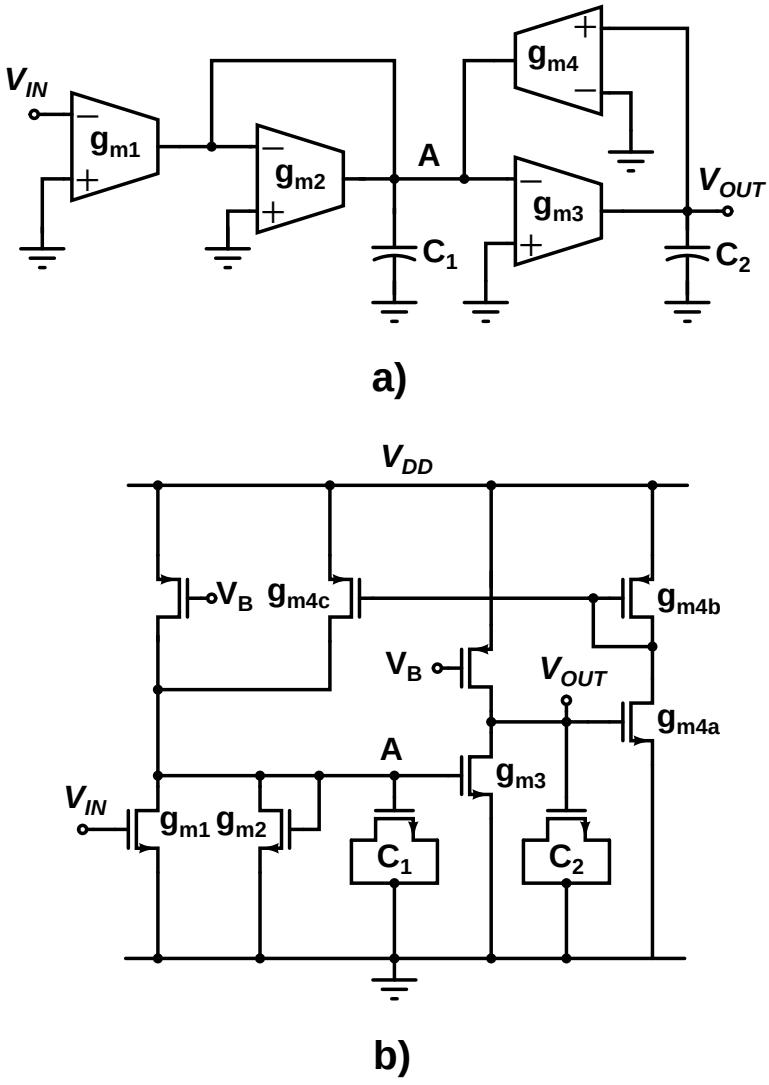

Figure 2.14 a) The single-ended g_m-C biquad prototype. b) Equivalent all-MOS transistor implementation.

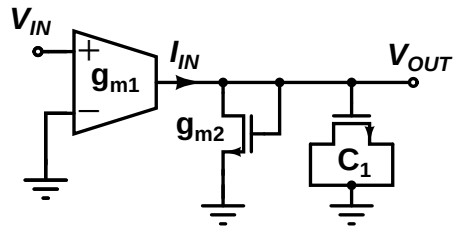

Figure 2.15 An all-MOS real pole with a current-mode input signal.

2.3.2.4 Comparison of Active-RC and g_m-C Filters

At low frequencies, where sensor applications are used, g_m-C filters dissipate less power and have smaller silicon area than active-RC filters, whereas active-RC filters have better dynamic range and noise properties [21, 31, 32]. As mentioned earlier, extremely low power dissipation and material costs are the key requirements for battery-powered sensor modules. Hence, in sensor receivers, good dynamic range and noise properties can be traded for low power and a reduced silicon area. The continuous-time filters for sensor receivers are compared using (2.11) in Table 2.1. Table 2.1 shows that the top four filters in terms of low energy dissipation per pole (FOM_F), are g_m-C filters. Furthermore, the top five filters in terms of low power dissipation are g_m-C filters.

Table 2.1 Comparison of Continuous-Time Filters

Ref.	Year	Gain [dB]	P_D [μW]	$f_{bb}[kHz]$	Order	Arch.	FOM_F [nJ]
[28]	1999	0	10.5	100	5	g_m-C	0.02
[7]	2000	20	210	25	4	Active-RC	2.10
[8]	2001	0	100	100	5	g_m-C	0.20
[11]	2003	12.4	2520	2200	5	Active-RC	0.23
[12]	2003	20	4000	500	4	g_m-C	2.00
[29]	2003	0	167	50	3	g_m-C	1.11
[14]	2004	20	600	120	3	Active-RC	1.67
[27]	2004	55	4860	1000	6	Active-RC	0.81
[P1]	2005	9.5[1]	78[2]	550	3	g_m-C	0.05
[P2]	2006	9.5[1]	48[2,3]	546	4	g_m-C	0.02

[1] Gain after the mixer-baseband interface.
[2] Includes the mixer-baseband interface current consumption, which is approximately half of the total filter current consumption.
[3] Simulated.

2.3.3 Limiter and Received Signal Strength Indicator

In wireless systems, detecting the strength of the incoming signal enables both the receiver gain and the transmitted power to be adjusted in order to optimize the system performance. The gain control can be implemented using either an automatic gain control (AGC) amplifier or a limiter. A limiter or a limiting amplifier is a chain of cascaded gain stages that saturate the input signal to a constant value. For wireless sensor networks, the limiter is preferred to AGC since it can handle a larger dynamic range while consuming less power [39]. In addition, limiters can be used for 1-bit A/D-conversion [P2, 20]. Since the limiter limits the incoming signal, it loses the incoming signal strength information. However, a RSSI can be used together with the limiter to detect the level of the incoming signal. Hence the adjustment of either the gain of the limiter or the transmitted power is possible. Since limiters are typically implemented

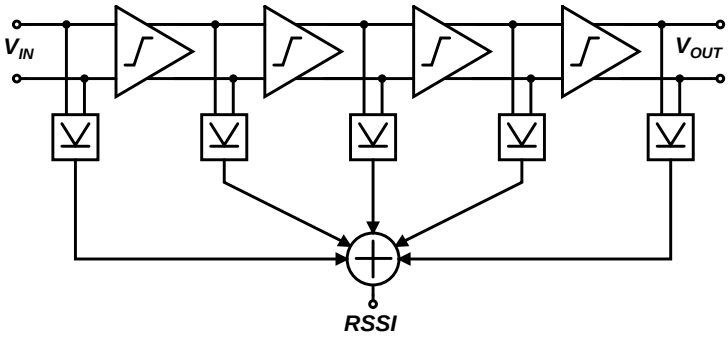

Figure 2.16 Limiter with logarithmic RSSI.

together with RSSI circuits, both are next discussed simultaneously.

A successive-detection logarithmic amplifier [40], shown in Fig. 2.16, is typically used in RSSI implementations in wireless receivers. In this kind of structure, the logarithmic response is achieved via piecewise linear approximation. The benefits of the logarithmic amplifier are that it can handle a wide dynamic range, together with accurate signal level detection. If accurate signal level detection is not required, the RSSI can implement only a single detection level [P2].

2.3.3.1 DC Offset Compensation Techniques for Limiters

Since a limiter is a chain of cascaded gain stages and has a very high gain, even a small offset voltage resulting from mismatches or from preceding stages may saturate the output of the limiter. Hence, DC offset compensation techniques have to be used. Next, some DC offset compensation schemes from the literature are discussed.

The AC coupling technique removes DC offset from the circuit output [41]. A circuit that performs AC coupling is shown in Figure 2.17. The transfer function of the circuit is

$$H_{AC}(s) = \frac{sRC}{1+sRC}. \tag{2.14}$$

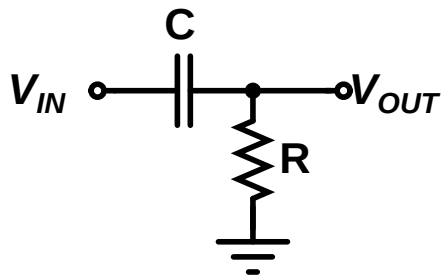

Figure 2.17 AC coupling.

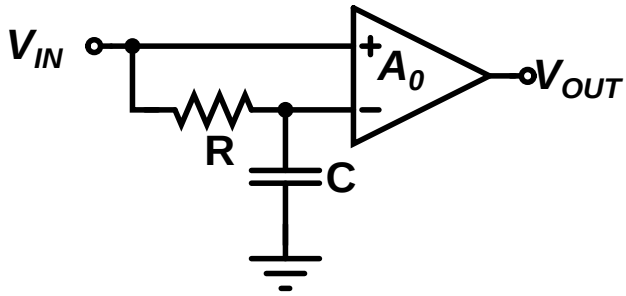

Figure 2.18 The feed-forward offset cancellation technique.

In an all-MOS implementation, the resistor can be implemented using a MOS transistor operating in a triode region. However, the floating capacitor is hard to implement with only MOS transistors. Hence, the silicon area of the AC coupling circuit can be large, especially in a balanced structure, where the number of capacitors is doubled. The AC coupling circuit high-pass filters the input signal, and hence removes the offset voltage from the output. Hence, the AC coupling circuit can be used in cases where the input offset voltage does not have to be canceled or removed.

Another way to remove the offset voltage at the circuit output is a feed-forward offset cancellation technique [42]. Feed-forward offset cancellation has been used in [43]. In the feed-forward offset cancellation technique the input offset is detected with a separate circuit and removed at the output. The principle is shown in Figure 2.18. The drawback of the technique is that it does not remove the offset voltage of the amplifier. The idea of feed-forward offset cancellation can also be used to implement common-mode feed-forward (CMFF) circuits to replace CMFB circuits [44, 45]. In this work, a CMFF circuit is used in the RSSI design in [P2].

A way to realize DC offset compensation that removes or cancels the offset voltage at the circuit input is to use a DC feedback loop, as shown in Figure 2.19. The offset voltage from the preceding stage is canceled, as well as the offset voltage of the amplifier A_0. However, the offset voltage of the feedback path is not canceled, and is treated in the same way as the signal. This issue is also discussed in Section 3.5. The transfer function of the circuit is

$$H_S(s) = \frac{A_0}{1 + A_0 H_{FB}(s)}, \tag{2.15}$$

where A_0 is the amplifier gain at zero frequency and $H_{FB}(s)$ is the transfer function of the feedback loop. It is assumed that the amplifier bandwidth does not limit the operation of the signal band of interest. The feedback loop transfer function $H_{FB}(s)$

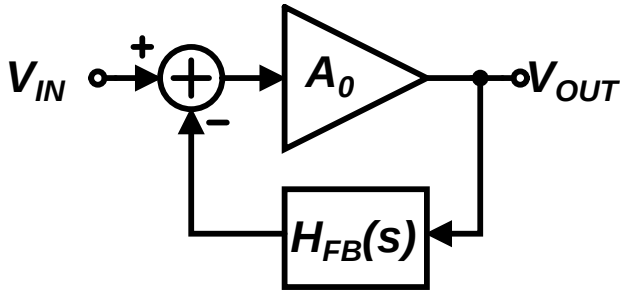

Figure 2.19 DC feedback loop.

for a single-pole low-pass system is given by

$$H_{FB}(s) = \frac{A_{FB}(s)}{1+\frac{s}{\omega_{FB}}}, \tag{2.16}$$

where A_{FB} is the DC gain of the feedback loop and ω_{FB} is the -3-dB corner frequency of the feedback loop. Substituting (2.16) into (2.15) gives

$$H_S(s) = \frac{A_0}{1+A_0A_{FB}} \cdot \frac{1+\frac{s}{\omega_{FB}}}{1+\frac{s}{(1+A_0A_{FB})\omega_{FB}}} \approx \frac{1}{A_{FB}} \cdot \frac{1+\frac{s}{\omega_{FB}}}{1+\frac{s}{A_0A_{FB}\omega_{FB}}}. \tag{2.17}$$

The system has a DC gain

$$H_S(0) = \frac{1}{A_{FB}}, \tag{2.18}$$

and a left half-plane zero at ω_{FB}. As can be seen, the low-pass filter in the feedback loop creates a high-pass filter with a -3-dB corner frequency approximately at $A_0A_{FB}\omega_{FB}$. It should be noticed that the corner frequency moves to a higher frequency with a factor A_0A_{FB}. Hence, in order to keep the high-pass filter -3-dB corner frequency below the desired signal band, the -3-dB corner frequency of the low-pass filter in the feedback loop has to be low, resulting in a large silicon area. The high-pass corner frequency can be lowered by reducing the gain of the feedback loop A_{FB} or the gain of the main amplifier A_0. If the feedback has attenuation ($A_{FB} < 1$), the input-referred offset voltage of the feedback path is increased. Hence large attenuation factors may not be acceptable if the output signal V_{OUT} is small. However, this is not the case in limiting amplifiers, where the output is always limited to supply voltages. Moreover, it should be noted that the attenuation does not affect the feedback offset voltage shown at the input, which is typically a more critical parameter. Reducing the gain of the main amplifier A_0 could also be used to lower the high-pass corner frequency. However, the gain A_0 is typically either optimized or maximized for the system, allowing very little room to play with. Next, the properties and trade-offs of

different feedback mechanisms used in the literature are discussed.

The low-pass filter in the feedback loop has been implemented in designs [22, 39, 41, 46–49] using an RC filter in the feedback loop. Since the area of an integrated passive RC pole is very large when the -3-dB corner is low, an external capacitor has to be used. Fully integrated implementation can be achieved by replacing the passive RC pole with an integrator [P1, 50, 51]. Furthermore, the required silicon area can be effectively reduced with a DC feedback loop implemented using digital circuitry [P2, 52].

An interesting case of the a DC feedback loop is when the amplifier A_0 is a limiter, which limits the signal at the last stages. If we have a minimum input signal $V_{IN,min}$, which is amplified to the limited output with a maximum transient gain A_{MAX}, the transient gain of the limiter at zero frequency is

$$A_{0,tran} = \frac{V_{IN,min}}{V_{IN}} A_{MAX} \tag{2.19}$$

Now, (2.17) changes to the form

$$H_S(s) \approx \frac{1}{A_{FB}} \cdot \frac{1+\frac{s}{\omega_{FB}}}{1+\frac{s}{\frac{V_{IN,min}}{V_{IN}} A_{MAX} A_{FB} \omega_{FB}}}. \tag{2.20}$$

The resulting -3-dB high-pass corner frequency is approximately $\frac{V_{IN,min}}{V_{IN}} A_{MAX} A_{FB} \omega_{FB}$. The corner frequency depends on the input signal level, and moves to a lower frequency as the input signal level increases. In order to minimize signal distortion, the input signal should be at a much higher frequency than the high-pass filter corner frequency. Hence, in a limiter, the highest signal distortion occurs with the minimum input signal.

According to (2.17) and (2.20), the DC offset suppression, namely the DC gain of the feedback system, remains the same, regardless of the input signal. Hence, if the DC offset is signal-independent, the offset seen at the output of the limiter stays unchanged. Furthermore, since the signal at the limiter output is limited to a fixed amplitude, according to (2.10), the duty cycle at the output of the limiter remains the same, regardless of the amplitude of the input signal.

It can be concluded that if the high-pass filter corner frequency is designed to fulfill the signal distortion and duty-cycle requirements with the minimum input signal, the requirements are fulfilled with higher input signal levels, assuming that the offset at the limiter input is signal-independent. If the offset voltage at the limiter input increases with the input signal, the duty cycle is degraded.

2.3.3.2 Limiter Gain and Bandwidth

The gain and bandwidth of each gain stage in a limiter determine the overall performance of the limiter. In addition, the number of cascaded gain stages has an effect on the overall power dissipation. Next, the effect of cascading multiple gain stages on overall performance is discussed.

A basic limiter gain stage is a single-pole amplifier which has a low-pass transfer function

$$A(s) = \frac{A_s}{1+\frac{s}{\omega_c}}, \tag{2.21}$$

where A_s is the amplifier gain at zero frequency and ω_c is the gain stage corner frequency. For an M-number of cascaded gain stages in (2.21), the transfer function is

$$H_{casc}(s) = \frac{A_0^M}{\left(1+\frac{s}{\omega_c}\right)^M}. \tag{2.22}$$

To determine the -3-dB corner frequency of the cascaded gain stages, we have to calculate the magnitude response of $H_{casc}(j\omega_{casc})$

$$|H_{casc}(j\omega_{casc})| = \frac{A_0^M}{\left|\sqrt{\left(1+\frac{\omega_{casc}}{\omega_c}\right)^2}\right|^M}. \tag{2.23}$$

At the corner frequency, the gain should be $\frac{A_0^M}{\sqrt{2}}$. Hence, the denominator in (2.23) must equal to $\sqrt{2}$, resulting in a new -3-dB corner frequency of

$$\omega_{casc} = \omega_c \cdot \sqrt{2^{1/M}-1}. \tag{2.24}$$

As can be seen from (2.24), the -3-dB corner frequency of the cascaded gain stages is shifted to a lower frequency with a factor $\sqrt{2^{1/M}-1}$. If the gain stage -3-dB corner frequency is normalized with respect to the -3-dB corner frequency of the cascade ω_{casc}, we get

$$\omega_{norm} = \frac{1}{\sqrt{2^{1/M}-1}}, \tag{2.25}$$

and if we express the total gain of the M-stage cascade with $A_{tot} = A_0^M$ and calculate a gain-bandwidth product (GBW) for a single gain stage, we get

$$GBW = A_s\omega_{norm} = \frac{A_{tot}^{1/M}}{\sqrt{2^{1/M}-1}}. \tag{2.26}$$

Furthermore, for a transconductance amplifier, we can express GBW by

$$GBW = \frac{g_m}{C_L}, \tag{2.27}$$

where g_m is the transconductance of the amplifier and C_L is the total load capacitance at the amplifier output. The transconductance g_m of a saturation region MOS transistor depends on the drain current I_D through the relation $g_m \sim \sqrt{I_D}$, which can be expressed as a function of power dissipation

$$g_m \sim \sqrt{\frac{P_D}{V_{DD}}}, \tag{2.28}$$

where P_D is the power dissipation and V_{DD} is the supply voltage. Hence, the *GBW* and power dissipation of a transconductance amplifier operating in the saturation region have the relation

$$P_D \sim GBW^2. \tag{2.29}$$

If we then estimate the total power dissipation of the cascaded gain stages using (2.26) and (2.29), we can write for an M-stage cascade

$$P_{casc} = M \cdot GBW^2 = M \cdot \left(\frac{A_{tot}^{1/M-1}}{\sqrt{2^{1/M}-1}} \right)^2. \tag{2.30}$$

The result from (2.30), with a total gain of 48 dB, is shown in Figure 2.20. As shown in Figure 2.20, the optimal power dissipation is achieved using five gain stages, as is the case in the designs [P1, P2].

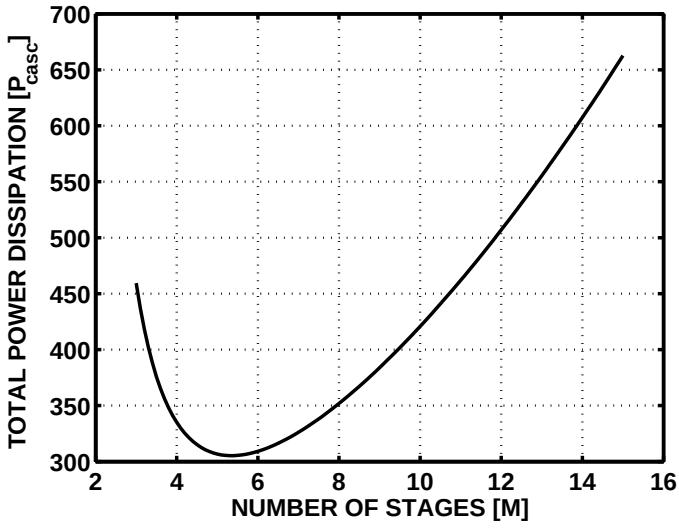

Figure 2.20 Limiter power dissipation vs. number of gain stages.

Chapter 3

Analog-to-Digital Converters for Sensor Applications

3.1 General

Commercial wireless communication is driven by consumers, who want higher data rates to support newer applications. In order to meet this demand, one part of this thesis is a low-pass $\Delta\Sigma$ modulator A/D converter for a mobile terminal GSM/WCDMA receiver, which benefits from the technology scaling in terms of increased bandwidth and reduced power dissipation [P3]. Even though the technology scaling results in increased bandwidth and improved digital signal processing capabilities, the drawbacks are that the available gain from a single transistor is reduced, and the supply voltage is reduced, making the design of analog circuits more difficult. However, the $\Delta\Sigma$ modulator A/D converter designed in [P3] demonstrates that with a robust design, a good analog performance can be achieved when using deep sub-micron technologies.

In contrast to the high-speed A/D converters required for wireless communications, A/D converters with medium resolution (8–12 bits) at sample rates up to a few megahertz have emerged recently. Such A/D converters can be used in applications that require a small die area and low power dissipation at the cost of reduced accuracy. Possible applications are, for example, sensors, toys, and different measurement and control systems.

When A/D converters are being designed for sensor applications, the energy consumption of the sensor nodes will determine both the lifetime of the individual nodes and the scope of possible applications, as already discussed in Chapter 2. In addition to low power dissipation, the size and cost of individual sensor nodes is critical, and hence the silicon area should be minimized. Finally, in order to extend the lifetime of

Figure 3.1 Mobile phone as a terminal in a sensor system.

the sensor, the A/D converter should be as flexible as possible, so as to be able to reduce power dissipation when the maximum speed or accuracy is not required. Different solutions for these applications are presented in [P4, P5, P6].

Both the A/D converters described above can be used in the sensor systems shown in Figure 3.1, where the mobile phone operates as a terminal for different sensors.

3.2 Specifications for A/D Converters

In order to be able to compare and characterize the performance of different A/D converters, some specifications are needed [53]. Specifications can be divided into two categories: static and dynamic specifications. Static specifications measure the DC characteristics of the A/D converters, which are important, for example, in very low-frequency sensor systems. Dynamic specifications measure frequency properties, which are important, for example, in audio and telecommunication systems.

3.2.1 Static Specifications

The static performance of the A/D converter is characterized measuring *differential nonlinearity (DNL)* and *integral nonlinearity (INL)*. With these specifications, the accuracy, quantization errors, and linearity of the A/D converter can be measured. The *DNL* and *INL* are specified from the A/D converter transfer curve and can be presented as a function of output code, as a single maximum value or as a range between the most positive and negative values. However, presentation as a function of output code gives information about the quantization errors and linearity of the A/D converter. The relationship between the input signal and the output values for an ideal A/D converter is a discrete staircase transfer curve. The full-scale voltage input range V_{FS} of the A/D converter is divided into uniform intervals, with an ideal step size equal to the least significant bit (*LSB*). The number of code transition levels in the discrete transfer function is equal to $2^N - 1$, where N is the number of digitized bits of the A/D converter. The step size depends on the full-scale voltage input range and on the number of digitized

bits, and is given by

$$V_{LSB} = \frac{V_{FS}}{2^N}. \tag{3.1}$$

The *DNL* is the difference, after correction for static gain, between a measured step size and the ideal step size, divided by the ideal step size. So *DNL* measures the variation of the step size relative to the ideal step size. The *DNL* also shows, if the A/D converter has missing codes. If for a certain code the $DNL \leq -0.9$, the code is specified as a missing code [53]. The *INL* is a cumulative *DNL* and can be computed by integrating the *DNL* data. The *INL* is defined as the difference between the ideal and measured code transition levels after correction for static gain and offset. A monotonic A/D converter has output codes that do not decrease (increase) for a uniformly increasing (decreasing) input signal, disregarding random noise. To fulfill this specification, the *INL* should not deviate by more than $\pm 1/2$ *LSB* or the *DNL* should not deviate by more than ± 1 *LSB*. Both *DNL* and *INL* are usually expressed in units of *LSBs*.

3.2.2 Dynamic Specifications

With dynamic specifications, the noise, distortion, dynamic linearity, settling errors, and sampling time uncertainty of the A/D converter are characterized.

Signal-to-noise ratio (SNR) for a pure sine wave input of specified amplitude and frequency is specified as the ratio of the root-mean-square (rms) amplitude of the A/D converter output signal to the rms amplitude of the output quantization noise in decibels. The quantization noise caused by quantization errors depends on the quantization step size V_{LSB}. If the quantization error is considered uncorrelated and signal-independent, it is evenly distributed in the range $\pm V_{LSB}/2$. The mean square value of the quantization error is given by

$$e_{rms}^2 = \frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{V_{LSB}/2} e^2 de = \frac{V_{LSB}^2}{12}. \tag{3.2}$$

If the A/D converter input signal is a pure sine wave with a full-scale peak-to-peak amplitude, the signal mean square value is given by

$$V_{sine,rms}^2 = \frac{V_{FS}^2}{\left(2\sqrt{2}\right)^2}. \tag{3.3}$$

Combining (3.1), (3.2), and (3.3), the *SNR* is given by

$$SNR = 20\log\left(\sqrt{\frac{3}{2}}2^N\right) = 6.02N + 1.76\ dB. \tag{3.4}$$

Equation (3.4) is independent of the sampling frequency and assumes that the quantization noise of (3.2) is evenly distributed over the signal bandwidth. According to the Nyquist criteria, all the sampled quantization noise power folds over the Nyquist band $[0, f_s/2]$, where f_s is the sampling frequency. Now, the power spectral density of the quantization noise is given by

$$E^2(f) = \frac{2e_{rms}^2}{f_s}. \tag{3.5}$$

If the desired signal bandwidth is limited to the frequency range $[0, f_{bw}]$ using a digital filtering with a brick wall response $H(f)$, the noise power in the signal band is

$$n_{bw}^2 = \int_0^{f_{bw}} E^2(f)\,|H(f)|^2\,\mathrm{d}f = \frac{2e_{rms}^2}{f_s}\,f_{bw} = \frac{e_{rms}^2}{OSR}, \tag{3.6}$$

where the *oversampling ratio (OSR)* is defined as a ratio of signal bandwidth and sampling frequency, and is given by

$$OSR = \frac{f_s}{2f_{bw}}. \tag{3.7}$$

From (3.6) it can be noticed, that for a sinusoidal signal, the in-band rms noise is reduced by the square root of the *OSR*. Hence, doubling the *OSR* halves the quantization noise power, which denotes an increase of 3 dB or 0.5 bits in the accuracy of the A/D converter. In the event of oversampling, (3.4) can be written in the following form:

$$SNR = 6.02N + 1.76 + 10\log(OSR). \tag{3.8}$$

Oversampling also relaxes the requirements for the input anti-aliasing filter required to band-limit the input signal frequencies below one half of the sampling frequency f_s, and for large *OSR* ratios a simple RC-filter may be adequate. According to the Nyquist criteria, A/D converters with a signal band $f_{bw} = f_s/2$ are called Nyquist-rate converters. However, in practice A/D converters with a low *OSR* (<8) are classified as Nyquist-rate converters and A/D converters with a higher *OSR* are classified as oversampling converters.

The definition of the *signal-to-noise and distortion ratio (SNDR)* is similar to *SNR*; however, the noise is defined to include not only random quantization errors but also

nonlinear distortion and the effects of sampling time errors. In practice, the achievable *SNDR* is somewhat reduced by noise, distortion, and other non-idealities in the realized A/D converter. The *effective number of bits (ENOB)* is a measure of the *SNDR* used to present the actual accuracy of the A/D converter in bits. *ENOB* is defined as

$$ENOB = \frac{SNDR - 1.76}{6.02}. \tag{3.9}$$

The *dynamic range (DR)* shows the available input signal range of the A/D converter. It is specified as the ratio between a full-scale input signal and the minimum input signal detectable at the output of the A/D converter. The dynamic range is obtained by measuring the *SNDR* of the A/D converter as a function of input signal power. The dynamic range is the difference between the full-scale input signal power and the input signal power where $SNDR = 0$.

The *spurious-free dynamic range (SFDR)* is the ratio of the amplitude of the output-averaged spectral component of the A/D converter at the input signal frequency f_{IN} to the amplitude of the largest harmonic or spurious spectral component observed over the full Nyquist band.

3.2.3 A/D Converter Performance Comparison

The static and dynamic specifications described above characterize the performance of the A/D converter very accurately. However, these specifications do not take the power dissipation of the A/D converter into account. Furthermore, in many applications the required silicon area is also a key factor. To be able to compare different A/D converters, the widely accepted modified Walden figure of merit is used [54]. In addition, a new figure of merit that takes both power dissipation and silicon area into account is introduced.

A figure of merit that takes the power dissipation into account by calculating energy per conversion step is given by

$$FOM_P = \frac{P_D}{2^{ENOB} \cdot 2 \cdot f_{bw}}, \tag{3.10}$$

where P_D is the power dissipation of the A/D converter and f_{bw} is the signal bandwidth. If the performance (*ENOB*) degrades at higher input signal frequencies, the FOM_P should be calculated with a minimum *ENOB* at the signal bandwidth.

The FOM that takes the silicon area into account is given by

$$FOM_A = \frac{A}{2^{ENOB} \cdot 2 \cdot f_{bw}}, \tag{3.11}$$

where A is the silicon area of the A/D converter.

The figures of merit FOM_P and FOM_A take only either the power dissipation or the silicon area into account. As discussed earlier, in Section 1, both the power dissipation and the silicon area are important parameters in sensor systems. Hence a figure of merit that takes both the power dissipation and the silicon area into account is introduced. The figure of merit is given by

$$FOM_{PA} = \frac{P_D \cdot A}{2^{ENOB} \cdot 2 \cdot f_{bw}}. \tag{3.12}$$

3.3 Building Blocks for Switched-Capacitor Circuits

3.3.1 Operational Amplifiers

Operational amplifiers are the main building blocks in traditional switched-capacitor (SC) circuits. They need to fulfill the speed, settling accuracy, gain, noise, current consumption, supply voltage, and output voltage swing requirements for the application in question. A brief introduction to different operational amplifier topologies is given here.

3.3.1.1 Operational Amplifier Properties

Operational amplifiers have several properties that affect the performance of SC circuits. In SC circuits the operational amplifier does not have to drive resistive loads, only capacitive loads. The benefit of driving solely capacitive loads is that no output voltage buffers are required. In addition, if all the amplifier internal nodes have low impedance, and only the output node has high impedance, the speed of the amplifier can be maximized. Amplifiers with these kinds of properties are referred to as operational transconductance amplifiers (OTA) [30].

The DC gain and *GBW* of the operational amplifier affect the settling accuracy of SC circuits. The requirements for DC gain are much higher for algorithmic A/D converters than for $\Delta\Sigma$ modulator A/D converters, whereas the *GBW* requirements are much more stringent for $\Delta\Sigma$ modulator A/D converters because of the high *OSR*. In addition to DC gain and *GBW*, the settling properties also depend on the slew rate capabilities of the operational amplifier. If the slewing current I_{slew} is too small, the time for exponential settling determined by *GBW* is reduced.

With low supply voltages, the output swing of operational amplifiers becomes very important, since it determines how large a signal swing can be used, setting one limit

for the achievable *SNR*. In addition, a large output swing helps to keep the operational amplifier output signal in a linear region, thus reducing distortion.

The MOS transistors used in operational amplifiers introduce noise, which can be expressed as [55]

$$e_n^2 = \frac{4\gamma kT}{g_m} + \frac{KF}{WLC_{ox}f}, \tag{3.13}$$

where k is the Boltzmann constant, T is the absolute temperature, g_m is the transistor transconductance, γ is a process-dependent noise excess factor, with a typical value of 2/3, KF is a process-dependent flicker noise parameter, C_{ox} is the transistor gate oxide capacitance, f is the frequency, and W and L are the width and length of the transistor gate, respectively. The first term in (3.13) describes the thermal noise of the MOS transistor and the second term describes the flicker noise or 1/f-noise. The flicker noise parameter KF is smaller for PMOS transistors, and hence PMOS input transistors are often preferred when a low noise level at low frequencies is important. The noise contribution of thermal noise can be reduced by increasing the transistor g_m, whereas the flicker noise can be reduced by increasing the size of the transistor.

3.3.1.2 Single-Stage Operational Amplifiers

Single-stage operational amplifiers offer high speed with moderate gain. To make the comparison easier, some properties of the single-stage OTAs that are discussed next are collated in Table 3.1 on page 38. To make the noise comparison easier, the input stages of all the amplifiers are biased using same current. The output stages are also biased with the same current to make the comparison of power dissipation easier. It is also assumed that the load capacitance C_L at the output of each amplifier is the same.

The operational amplifier gain can be increased by using cascode transistors, at the cost of reduced voltage swing. A simple and fast telescopic cascode OTA is shown in Figure 3.2. The telescopic cascode OTA has low current consumption, relatively high gain, low noise, and very fast operation. However, as it has five stacked transistors, the topology is not suitable for low supply voltages.

Another single-stage operational amplifier topology that is better suited to low supply voltages is a folded cascode OTA, shown in Figure 3.3. The current consumption is doubled compared to the telescopic cascode OTA, but the output voltage swing is increased, since there are only four stacked transistors. The noise of the folded cascode OTA is slightly higher than in the telescopic cascode OTA as a result of the added noise from the current source transistors M_{10} and M_{11}. In addition, the folded cascode OTA is somewhat slower than the telescopic cascode OTA and has a slightly smaller DC gain.

A push-pull current-mirror OTA, shown in Figure 3.4, has much better slew-rate properties, and potentially larger bandwidth and DC gain than the folded cascode OTA.

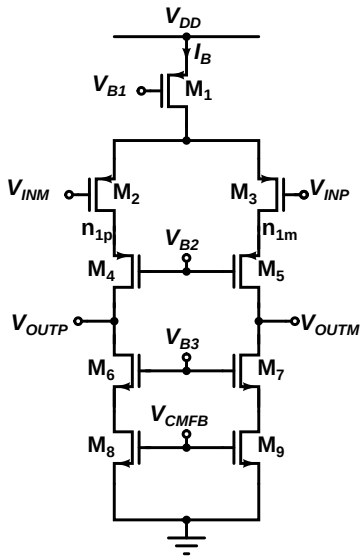

Figure 3.2 A telescopic cascode OTA.

The slew rate and DC gain depend on the current-mirror ratio K. However, too large a current-mirror ratio increases the parasitic capacitance at the gates of the transistors M_{12} and M_{13}, pushing the non-dominant pole to lower frequencies and limiting the achievable *GBW*. As shown in Table 3.1, the noise and current consumption of the current-mirror OTA are larger than in the telescopic cascode OTA or in the folded cascode OTA. A current-mirror OTA with dynamic biasing [56] can be used to make the amplifier biasing be based purely on its small signal behavior, as the slew rate is not limited. In dynamic biasing, the biasing current of the operational amplifier is controlled on the basis of the differential input signal. With large differential input signals, the biasing current is increased to speed up the output settling. Hence, no slew rate limiting occurs, and the *GBW* requirement is relaxed. As the settling proceeds, the input voltage decreases and the biasing current is reduced. The biasing current needs to be kept only to a level that provides enough *GBW* for an adequate small-signal performance. In addition to relaxed *GBW* requirements, the reduced static current consumption makes the design of a high-DC-gain amplifier easier. The dynamically biased current-mirror OTA was used in designs [P4, P5, P6] where large variations in capacitive loads would have resulted in a non-optimal current consumption with a slew-rate limited operational amplifier.

3.3.1.3 Two-Stage Operational Amplifiers

With very low supply voltages, the use of the cascode output stages limits the available output signal swing too much. Hence, two-stage operational amplifiers are used, in

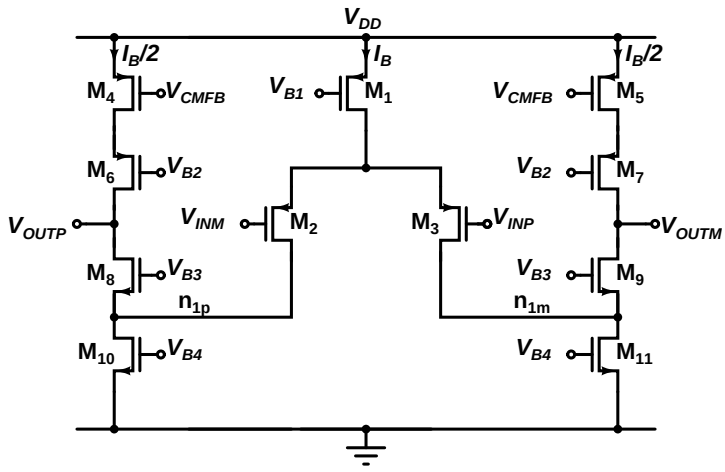

Figure 3.3 A folded cascode OTA.

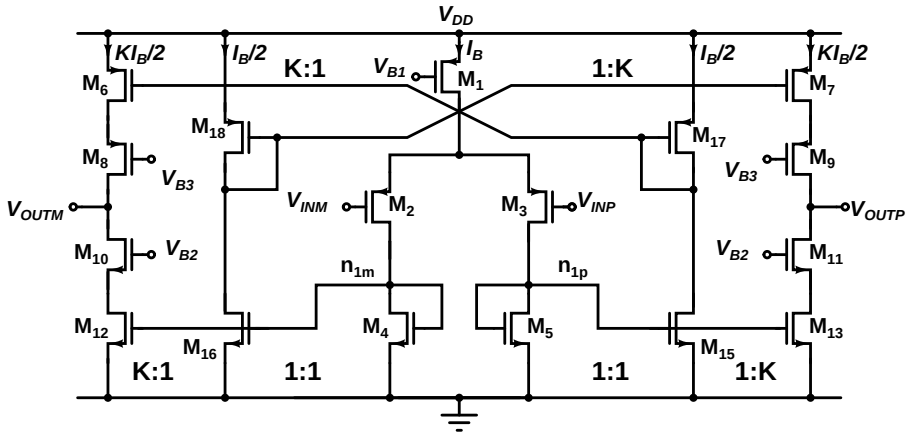

Figure 3.4 A push-pull current-mirror OTA with a cascode output stage.

which the operational amplifier gain is divided into two stages, where the latter stage is typically a common-source output stage. Unfortunately, with the same power dissipation, the speed of the two-stage operational amplifiers is typically lower than that of single-stage operational amplifiers. To help the comparison, some properties of the two-stage operational amplifiers that are discussed next are collated in Table 3.2 on page 38. Again, to make the comparison easier, the biasing is similar to that in the single-stage amplifiers.

A two-stage Miller-compensated operational amplifier with a continuous-time input-stage CMFB circuit is shown in Figure 3.5. To achieve very fast operation, local CMFB circuits are preferred instead of only one being used. However, a drawback of the continuous-time input stage CMFB circuit is that it reduces the available gain from

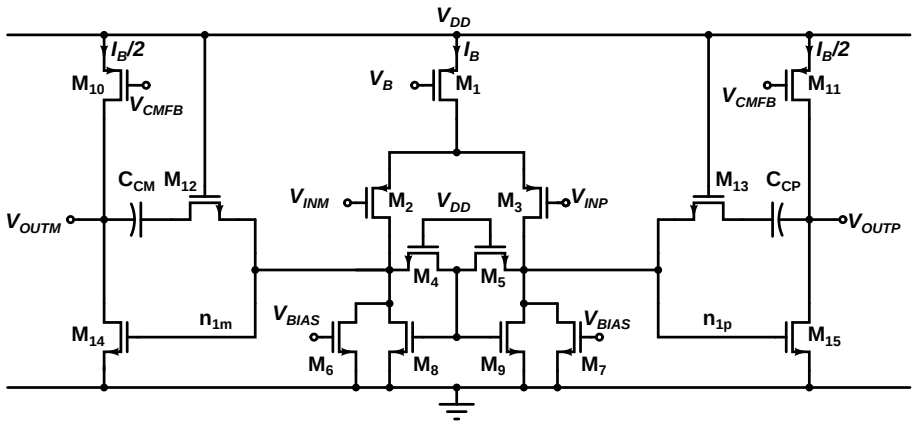

Figure 3.5 A Miller-compensated operational amplifier.

the input stage, since the impedance level at the output of the input stage is reduced compared to a traditional fully differential pair with current source loads. However, the impedance level can be increased by using a gain enhancement technique [57] in which the constant biased NMOS load transistors M_6–M_7 attenuate the current through the CMFB transistors M_8–M_9. As a result, the impedance level is increased, and the gain of the input stage can be designed to be only slightly lower than for the traditional differential pair. The Miller compensation is implemented with the pole-splitting capacitors C_{CP} and C_{CM} and lead-compensation NMOS resistors M_{12} and M_{13}. The output stage is a common-source stage so as to maximize the output signal swing. The noise properties of the two-stage Miller-compensated operational amplifier are comparable to those of the telescopic cascode OTA and better than those of the folded cascode OTA. The speed of a Miller-compensated amplifier is determined by its pole-splitting capacitor C_C. With the same biasing and assuming C_C=C_L, the speed and power dissipation of a Miller-compensated amplifier are comparable to those of single-stage amplifiers. This kind of operational amplifier was used in [P3] to be able to operate with a 1.2-V supply voltage.

If the gain from the two-stage Miller-compensated operational amplifier is inadequate, a folded cascode OTA with a common-source output stage and Miller compensation, shown in Figure 3.6, could be used. The input stage is replaced with a folded cascode OTA. This circuit gives much better gain than the operational amplifiers described above. However, the current consumption and transistor count are also increased. The noise properties are comparable with those of the folded cascode OTA. If a cascode input stage is used, the lead-compensation resistor can be merged with the cascode transistors. An example of this is the folded cascode OTA with a common-source output stage and Ahuja-style compensation [58] shown in Figure 3.7. The operation of the Ahuja-style compensated operational amplifier is suitable for larger

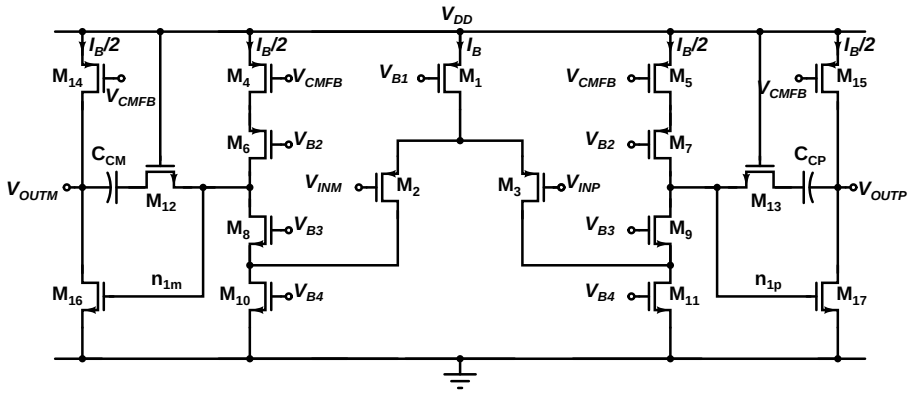

Figure 3.6 A folded cascode OTA with a common-source output stage and Miller frequency compensation.

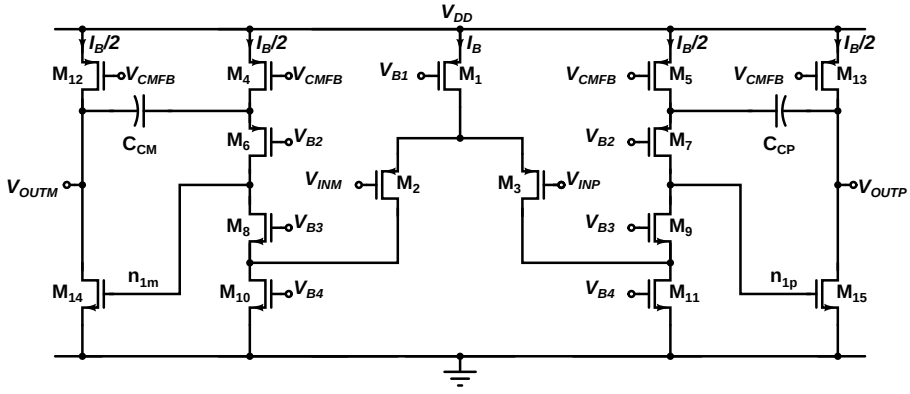

Figure 3.7 A folded cascode OTA with a common-source output stage and Ahuja-style frequency compensation.

capacitive loads than the Miller-compensated one and it has a better power supply rejection, since the substrate noise coupling through the gate-source capacitance of the output stage gain transistors is not coupled directly through the pole-splitting capacitors to the operational amplifier output [58].

3.3.2 Latched Comparators

In this section, the properties of different kinds of latched comparators presented in the literature are discussed. The latched comparator architectures are compared in terms of power dissipation, speed, and kickback noise generation. The latched comparators are divided into static, Class AB, and dynamic latched comparators.

Table 3.1 Comparison of different operational amplifier topologies 1/2

Topology	Telescopic	Folded cascode (FC)	Push-pull current-mirror
Stages	1	1	1
DC gain	$\frac{g_{m3}}{\frac{g_{ds3}\cdot g_{ds5}}{g_{m5}}+\frac{g_{ds7}\cdot g_{ds9}}{g_{m7}}} \sim \frac{gm^2}{2g_{ds}^2}$	$\frac{g_{m3}}{\frac{g_{ds5}\cdot g_{ds7}}{g_{m7}}+\frac{g_{ds9}(g_{ds3}+g_{ds11})}{g_{m9}}} \sim \frac{gm^2}{3g_{ds}^2}$	$\frac{K\cdot g_{m3}}{\frac{g_{ds7}\cdot g_{ds9}}{g_{m9}}+\frac{g_{ds11}\cdot g_{ds13}}{g_{m11}}} \sim \frac{Kgm^2}{4g_{ds}^2}$
GBW	$\frac{g_{m3}}{C_L}$	$\frac{g_{m3}}{C_L}$	$\frac{K\cdot g_{m3}}{C_L}$
2^{nd} pole	$\frac{g_{m5}}{C_{n1m}}$	$\frac{g_{m9}}{C_{n1m}}$	$\frac{g_{m3}}{C_{n1p}}$
I_{slew}	$I_B/2$	$I_B/2$	$K\cdot I_B/2$
I_{supply}	I_B	$2I_B$	$(2+K)I_B$
Output swing	$V_{DD}-5v_{ds,sat}$	$V_{DD}-4v_{ds,sat}$	$V_{DD}-4v_{ds,sat}$
Noise $\frac{8kT}{g_{m3}}\cdot$	$\left(\gamma_3+\gamma_9\frac{g_{m9}}{g_{m3}}\right)$	$\left(\gamma_3+\frac{g_{m5}}{g_{m3}}\gamma_5+\frac{g_{m11}}{g_{m3}}\gamma_{11}\right)$	$(\gamma_3+\frac{g_{m5}}{g_{m3}}\gamma_5+\frac{g_{m15}}{g_{m3}}\gamma_{15}+\frac{g_{m7}}{Kg_{m3}}\gamma_7+\frac{g_{m13}}{Kg_{m3}}\gamma_{13})$

Table 3.2 Comparison of different operational amplifier topologies 2/2

Topology	Miller comp.	FC Miller comp.	FC Ahuja comp.
Stages	2	2	2
DC gain	$\frac{g_{m3}}{g_{ds3}+g_{ds7}}\cdot\frac{g_{m15}}{g_{ds11}+g_{ds15}} \sim \frac{gm^2}{4g_{ds}^2}$	$\frac{g_{m3}}{\frac{g_{ds5}\cdot g_{ds7}}{g_{m7}}+\frac{g_{ds9}(g_{ds3}+g_{ds11})}{g_{m9}}}\cdot\frac{g_{m17}}{g_{ds15}+g_{ds17}} \sim \frac{gm^3}{6g_{ds}^3}$	$\frac{g_{m3}}{\frac{g_{ds5}\cdot g_{ds7}}{g_{m7}}+\frac{g_{ds9}(g_{ds3}+g_{ds11})}{g_{m9}}}\cdot\frac{g_{m17}}{g_{ds15}+g_{ds17}} \sim \frac{gm^3}{6g_{ds}^3}$
GBW	$\frac{g_{m3}}{C_C}$	$\frac{g_{m3}}{C_C}$	$\frac{g_{m3}}{C_C}$
2^{nd} pole	$\frac{g_{m15}}{C_{n1p}+C_L\left(1+\frac{C_{n1p}}{C_C}\right)}$	$\frac{g_{m17}}{C_{n1p}+C_L\left(1+\frac{C_{n1p}}{C_C}\right)}$	$\frac{C_C}{C_{n1p}}\cdot\frac{g_{m15}}{C_C+C_L}$
I_{slew}	$I_B/2$	$I_B/2$	$I_B/2$
I_{supply}	$2I_B$	$3I_B$	$3I_B$
Output swing	$V_{DD}-2v_{ds,sat}$	$V_{DD}-2v_{ds,sat}$	$V_{DD}-2v_{ds,sat}$
Noise $\frac{8kT}{g_{m3}}\cdot$	$\left(\gamma_3+\gamma_{7,9}\frac{g_{m7,9}}{g_{m3}}\right)$	$\left(\gamma_3+\frac{g_{m5}}{g_{m3}}\gamma_5+\frac{g_{m11}}{g_{m3}}\gamma_{11}\right)$	$\left(\gamma_3+\frac{g_{m5}}{g_{m3}}\gamma_5+\frac{g_{m11}}{g_{m3}}\gamma_{11}\right)$

3.3.2.1 Static Latched Comparators

The static latched comparator has a constant current consumption during operation. The static latched comparator presented in [59] is shown in Figure 3.8. Since the input transistors are isolated from the regeneration nodes through the current mirror, the kickback noise is reduced. However, the speed of the regeneration circuit is limited by the bias current and is not suitable for low-power high-speed applications. A suitable static latched comparator for low-voltage operation is shown in Figure 3.9 [60]. The drawback of this approach is that the input transistors are connected directly to the regeneration nodes, and hence this type of comparator is more susceptible to kickback noise than the comparator in Figure 3.8.

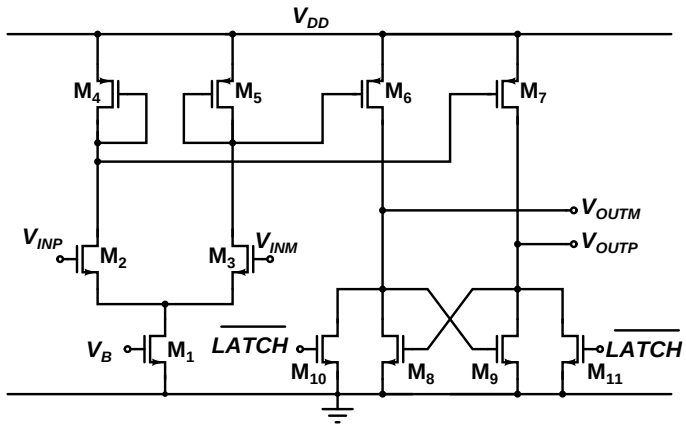

Figure 3.8 The static latched comparator [59].

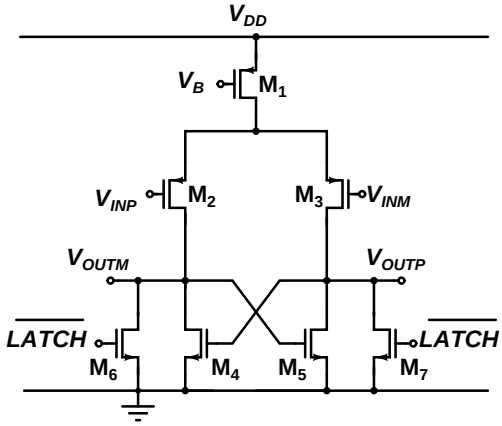

Figure 3.9 The static latched comparator suitable for low-voltage operation [60].

3.3.2.2 Class AB Latched Comparators

The Class AB latched comparator consumes static current during the reset phase and after the regeneration phase. Since the current consumption increases momentarily during the regeneration process the comparator has the Class AB operation. A similar Class AB latched comparator to the one presented in [61, 62] is shown in Figure 3.10. In the reset phase the current flow through the transistors M_7 and M_8 is prevented, and the reset switch M_3 keeps the latch outputs equal. When the comparator is latched, the reset switch M_3 is opened, and the switch M_9 is closed. The transistors M_1 and M_7, and M_2 and M_8 form two back-to-back inverters that rapidly regenerate the small voltage difference at the latch output to pure logic value. The power efficiency and speed are better than for the static latched comparator. However, Class AB latched comparators generate more kickback noise, since the drains of the input transistors are connected

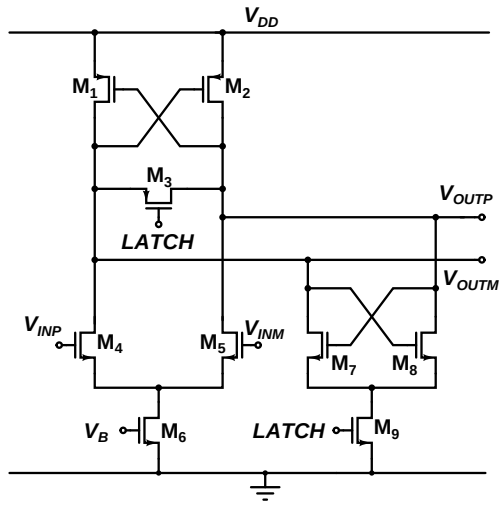

Figure 3.10 The Class AB latched comparator.

directly to the regeneration nodes. The static current consumption of the circuit in Figure 3.10 can be reduced using the circuit configuration shown in Figure 3.11 [32]. Again, during the reset phase, the outputs are shorted with a switch transistor M_3. After the reset phase, the PMOS loads M_1 and M_2 are allowed to regenerate the voltage across the reset switch before the comparator is latched. After some delay, the switch M_{11} is opened, and the comparator will turn into latch phase, which will rapidly generate pure logic values at the latch outputs. During the latch phase, the static current flow through the input pair M_6 and M_7 is prevented using the PMOS switches M_4 and M_5. Hence the static current flow after the regeneration phase is eliminated. Furthermore, the kickback transients caused by the variations at the input transistor drains are reduced. This kind of comparator was utilized in [P3].

3.3.2.3 Dynamic Latched Comparators

The dynamic latched comparator shown in Figure 3.12 does not consume any static power, and thus is well suited to low-power applications [63, 64]. In the reset phase, the PMOS switch transistors M_8 and M_9 pull the comparator outputs to the supply voltage. The current through the NMOS input pair M_2 and M_3 is prevented with the NMOS switch transistor M_1. When the comparator is latched, the two back-to-back inverters formed by the transistors M_4–M_7 rapidly generate full-scale digital levels at the outputs. After the regeneration phase, the positive and negative outputs are at the supply voltages and no static current flow occurs. Hence the power efficiency is maximized. Furthermore, the dynamic latched comparator is as fast as Class AB latched comparators, since the output regeneration is not limited by any bias current.

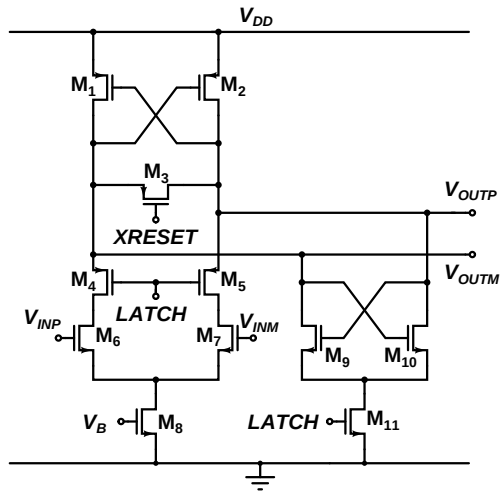

Figure 3.11 The Class AB latched comparator with reduced static current consumption [32].

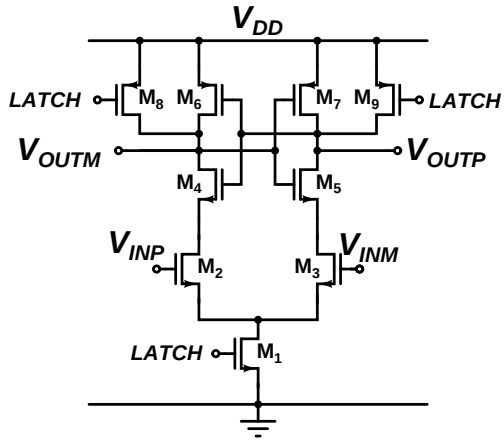

Figure 3.12 The dynamic latched comparator [63].

However, the drawback of the dynamic latched comparator is its large kickback noise. This results from the fact that when the comparator is latched, the drain voltages vary between supply voltages and the large transients are coupled to the input through the gate-drain capacitances. In addition, the input transistors change the operating region from the cut-off to the active region when the comparator is latched.

3.3.2.4 Preamplifier for Latched Comparators

There are different techniques to reduce the effect of the kickback noise; the most popular one is to use a preamplifier, which attenuates the kickback transients entering the driving circuitry [65, 66]. If the comparator offset needs to be eliminated, the pream-

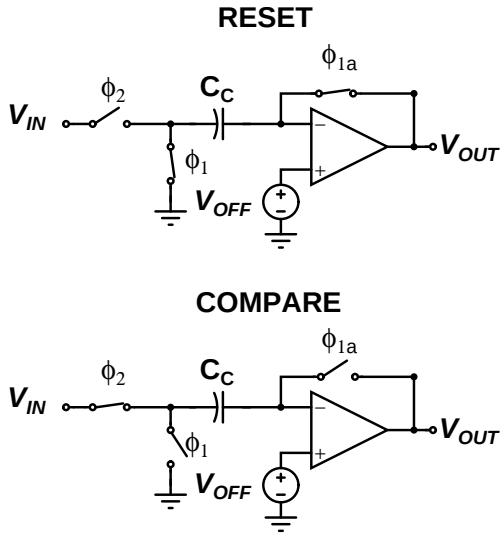

Figure 3.13 The preamplifier with offset voltage cancellation.

plifier can be implemented using the circuit configuration shown in Figure 3.13. In the reset phase (ϕ_1), the preamplifier offset voltage is stored in a capacitor C_C. The switch ϕ_{1a} is a slightly more advanced version of ϕ_1 to make it possible to utilize bottom plate sampling. In the comparison phase (ϕ_2), the input signal is connected to the bottom plate of capacitor C_C. The preamplifier offset voltage is canceled at the preamplifier input and the preamplifier output goes toward the negative supply voltage with positive input signals and toward the positive supply voltage with negative input signals. This circuit configuration cancels the preamplifier offset voltage, but does not take into account the offset of the following comparator. Hence, the preamplification should be designed to be large enough to overcome the offset voltage of the following comparator even with the *LSB* input signal. The preamplifier with offset voltage cancellation is used together with dynamic latched comparators in the designs [P4, P5, P6]. It should be noted that in [P5, P6] the preamplification with offset voltage cancellation requires no additional hardware, only one extra clock step.

3.3.3 Clock Generation

The non-overlapping clock signals required to implement SC circuits can be generated using a simple circuit constructed of logic gates, as shown in Figure 3.14. The delay required to implement bottom plate sampling is denoted by a t_b, and the delay between the non-overlapping clock signals is denoted by a t_o. The main advantages of this circuit are its simplicity and robustness. However, the non-overlapping times have to have some margin to accommodate the process and temperature variations. A delay

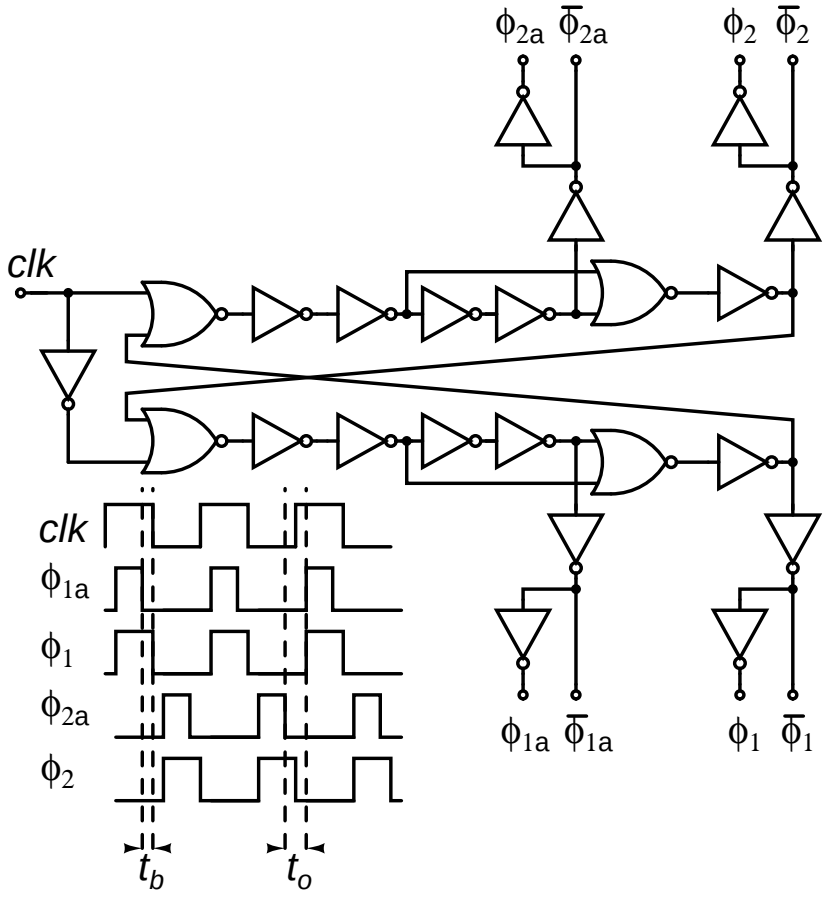

Figure 3.14 A non-overlapping clock signal generator.

locked loop (DLL) could be used to generate the required clock signals, but a DLL-based clock generator is more complex and also consumes more area and power [67]. Thus, the simple structure shown in Figure 3.14 is used in the designs [P3, P4, P5, P6].

While $\Delta\Sigma$ modulators do not require complex clock generators and can be operated almost totally with the circuit in Figure 3.14, algorithmic A/D converters require more complex clock generation. Algorithmic A/D converters may require more than one clock cycle (phases ϕ_1 and ϕ_2), so the generation of non-overlapping clock pulses is more complex. In addition, algorithmic A/D converters require a counter that handles the total number of bits to be converted. Finally, the final steering clock signals require additional logic. Hence, clock generation for algorithmic A/D converters is not as simple and robust as it is for $\Delta\Sigma$ modulators.

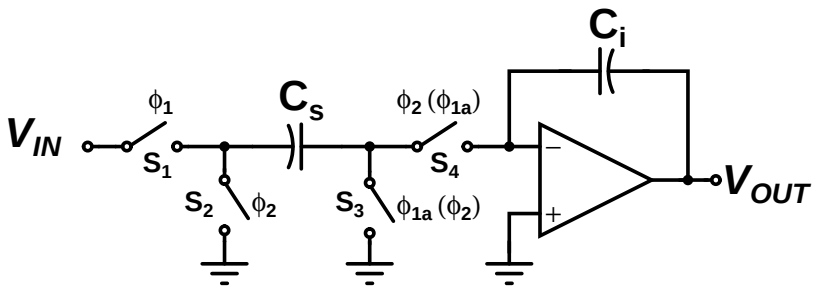

Figure 3.15 switched-capacitor integrator.

3.3.4 Basic SC circuits

The basic structures used to build SC circuits are SC integrators and sample-and-hold circuits. Next, a short overview of these structures is given.

3.3.4.1 SC Integrator

One of the most important building blocks in SC circuits is an SC integrator. Figure 3.15 presents a parasitic-insensitive non-inverting and inverting SC integrator [55]. The clock phases for the inverting integrator are in parentheses. Bottom plate sampling [68], discussed later in Section 3.4, is implemented with the clock phase ϕ_{1a}, which is a slightly more advanced version with respect to the clock phase ϕ_1. The parasitic capacitances at the top plate of the capacitor C_s and at the input of the operational amplifier are always connected to a fixed potential through the switches S_3 and S_4, and therefore do not affect the operation of the circuit. Parasitic capacitances at the input and output of the operational amplifier only have an effect on the settling speed of the operational amplifier, and do not introduce error, if taken into account in the characterization of the settling time of the operational amplifier. The effect of the parasitic capacitances at the bottom plate of the capacitor C_s is also canceled. Even though the parasitic capacitances are charged to the input voltage V_{IN} in phase ϕ_1, the parasitic capacitances are discharged to a fixed potential in the clock phase ϕ_2 through the switch S_2, and no discharge current flows through the capacitor C_s.

3.3.4.2 Sample and Hold

A sample-and-hold (S/H) circuit is an important building block for A/D converters. The task of the S/H circuit is to sample an input voltage and hold it so that the difference between the actual signal and the sampled and held signals is as small as possible. Otherwise, non-linear distortion may occur. In high-speed applications, the speed and sampling time uncertainty of the S/H circuit become essential. On the other hand, in systems operating at low frequencies, the accuracy in the hold mode can be critical as

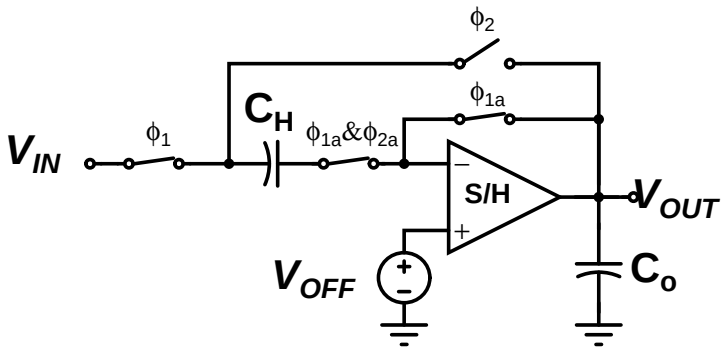

Figure 3.16 Switched-capacitor S/H circuit.

a result of transistor leakage currents. Other important parameters are dynamic range, linearity, and offset error. Since the S/H speed required in the designs [P4, P5, P6] is relatively low, the high-speed properties of S/H circuits are not covered in this thesis. Hence, the main S/H design parameters are dynamic range, linearity, and offset error.

A single-ended auto-zeroing S/H circuit is shown in Figure 3.16. To cancel even-order harmonic distortion, a differential version of the S/H circuit was implemented in the designs [P4, P5, P6]. The bottom plate sampling, discussed later in Section 3.4, is utilized in Figure 3.16 with the clock phases ϕ_{1a} and ϕ_{2a}, which are slightly more advanced versions of the sample and hold clock phases ϕ_1 and ϕ_2, respectively. In the sampling phase, the input signal V_{IN} is sampled and concurrently the S/H amplifier offset voltage V_{OFF} is stored in the capacitor C_H, resulting in the charge

$$Q^S_{C_H} = C_H(V_{OFF} - V_{IN}), \tag{3.14}$$

where V_{IN} is the input signal and V_{OFF} is the amplifier offset voltage. The drawback of this approach is that when V_{OFF} is sampled, the amplifier noise is also sampled to the capacitor C_H. In the second phase, the amplifier is in hold mode. The charge in the capacitor C_H is

$$Q^H_{C_H} = C_H(V_{OFF} - V_{OUT}). \tag{3.15}$$

As a result of the charge conservation law $Q^S_{C_H} = Q^H_{C_H}$ the output voltage is

$$V^H_{OUT} = V_{IN}. \tag{3.16}$$

Hence the amplifier offset voltage is canceled, which means that the S/H circuit also cancels flicker noise. This is a very important feature in applications with signals near DC.

3.3.5 OTA Loading

Here the implications of capacitive loading for an OTA in a closed-loop system are discussed. Let us assume a single-pole OTA. The transfer function for such an amplifier is given by

$$A(s) = \frac{A_0}{1+\frac{s}{p_1}}, \tag{3.17}$$

where A_0 is the amplifier gain at zero frequency and p_1 is the single-pole frequency. For the single-pole system, the *GBW* is given by

$$GBW = A_0 p_1. \tag{3.18}$$

If the amplifier is put into a feedback loop, the transfer function is given by

$$A_F(s) = \frac{A(s)}{1+\beta A(s)}, \tag{3.19}$$

where the factor β in the feedback loop is called a feedback factor. Substituting (3.17) into (3.19), we get

$$A_F(s) = \frac{\frac{1}{\beta}}{1+\frac{s}{\beta GBW}}. \tag{3.20}$$

The settling time constant is then given by

$$\tau = \frac{1}{\beta GBW}. \tag{3.21}$$

From (3.21) it can be seen, that the *GBW* is reduced by the factor β. Hence the settling time depends on the feedback factor and the *GBW*. A special case would be a voltage follower, in which $\beta = 1$. Then the settling depends only on the *GBW*. For a transconductance amplifier, we can express the *GBW* by

$$GBW = \frac{g_m}{C_L}, \tag{3.22}$$

where g_m is the transconductance of the amplifier and C_L is the total load capacitance at the amplifier output. Thus, the settling time constant can be written in the form

$$\tau = \frac{C_L}{\beta g_m}. \tag{3.23}$$

From (3.21) and (3.23) it can be seen, that the settling time constant increases as the feedback factor decreases. Moreover, the change in capacitive loading can be

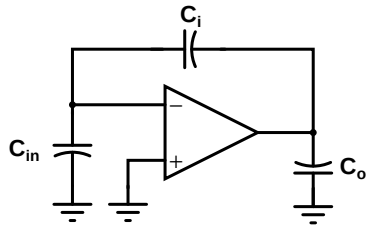

Figure 3.17 OTA capacitive loading.

expressed using an effective load capacitance for the transconductance amplifier. The effective load capacitance is given by

$$C_{eff} = \frac{C_L}{\beta}. \tag{3.24}$$

Equation (3.24) gives the real load seen by the transconductance amplifier in the feedback loop and takes the *GBW* reduction resulting from β into account. Next, some example calculations for an SC integrator are presented.

An example circuit is shown in Figure 3.17. The capacitor C_{in} presents the total OTA input capacitance. The capacitor C_i is the integrating capacitor and the capacitor C_o presents the total OTA output capacitance. For the given circuit, the feedback factor

$$\beta = \frac{C_i}{C_{in} + C_i}. \tag{3.25}$$

The total load capacitance C_L of the OTA is formed by C_o, together with the series combination of C_i and C_{in}, and can be written as

$$C_L = C_o + \frac{C_{in} \cdot C_i}{C_{in} + C_i}. \tag{3.26}$$

Now the effective load capacitance C_{eff} is

$$C_{eff} = \frac{C_L}{\beta} = \frac{C_o(C_i + C_{in})}{C_i} + C_{in}. \tag{3.27}$$

The interesting part is that if the output capacitance $C_o = 0$, the effective load of the OTA is equal to the input capacitance C_{in}. In other words, if the output capacitance $C_o = 0$, the loading is independent of the feedback factor β. On the other hand, if the output capacitance $C_o \neq 0$, the effective loading of the output capacitance C_o increases as the feedback factor decreases. Hence, for optimum power dissipation, the output capacitance C_o should be minimized when the feedback factor $\beta < 1$. This information can be used to optimize the loading of the amplifier, if applicable. In [P3], the operation was designed in such a way that the output capacitance $C_o = 0$ when the feedback factor $\beta < 1$.

3.3.6 OTA Settling Requirements

First, the settling requirement is derived for a single-pole system. For a single-pole system, where the OTA settling requirement is N bits, the requirement for settling error is given by

$$e^{-\frac{T_s}{\tau}} = 2^{-N}, \tag{3.28}$$

where T_s is the settling time, τ is the settling time constant, and N is the target accuracy in bits. If we take a natural logarithm from both sides, (3.28) transfers to the form

$$\frac{T_s}{\tau} = -\ln S, \tag{3.29}$$

where the settling accuracy $S = 2^{-N}$. Using the settling time constant from (3.23), the relation can now be written in the form

$$GBW = -\frac{\ln S}{\beta T_s}, \tag{3.30}$$

where β is the feedback factor of the closed-loop system.

If the OTA is modeled with a more accurate second-order system, the fastest settling accuracy without overshoot and ringing is achieved when the system is critically damped, with a damping factor $\xi = 1$. The phase margin of the critically damped system is 76° [P6, 69]. The dominant pole turns the phase 90°, so the non-dominant pole p_2 has to turn the phase an additional 14° at the frequency βGBW. Assuming $\beta A_0 \gg 1$, we have

$$\tan^{-1}\left(\frac{\beta GBW}{|p_2|}\right) = 14^\circ, \tag{3.31}$$

which gives $|p_2| = 4\beta GBW$. Using (3.18), this results in the condition

$$p_2 = 4\beta A_0 p_1. \tag{3.32}$$

The general transfer function of a low-pass, second-order system in the s-plane is

$$A_{LP}(s) = \frac{a_0\omega_n^2}{s^2 + (\omega_n/Q)s + \omega_n^2}, \tag{3.33}$$

where a_0 is the DC gain of $A_{LP}(s)$, ω_n is the pole frequency, and Q is the pole quality factor [69, 70]. The pole quality factor Q depends on the damping factor through the relation $Q = 1/(2\xi)$

Now, if an inverse Laplace transform is taken from the step response of the critically

damped second-order system ($Q = 1/2$), the relative settling error can be written as

$$\mathcal{L}^{-1}\left\{\frac{1}{s}\cdot\frac{\omega_n^2}{s^2+2\omega_n s+\omega_n^2}\right\} = e^{-\omega_n t}+\omega_n t e^{-\omega_n t}, \tag{3.34}$$

with ω_n defined in a closed-loop system [69] as

$$\omega_n = \sqrt{p_1 p_2(1+\beta A_0)}. \tag{3.35}$$

Using (3.32), ω_n can be written as

$$\omega_n = \sqrt{p_1\cdot 4\beta A_0 p_1\cdot \beta A_0} = 2\beta\cdot GBW, \tag{3.36}$$

with $\beta A_0 \gg 1$.

If the required settling accuracy is S, and the settling time is T_s, the minimum GBW requirement can now be solved from

$$e^{-2\beta\cdot GBW\cdot T_s}+2\beta\cdot GBW\cdot T_s\cdot e^{-2\beta\cdot GBW\cdot T_s} = S. \tag{3.37}$$

This equation cannot be solved for GBW in a closed form, but can be evaluated numerically.

The results from (3.30) and (3.37) are compared in Fig. 3.18 with $T_s = 0.5\mu$s and $\beta = 0.5$. It can be seen that the single-pole system GBW requirement is roughly 1.5 times higher than for the critically damped second-order system. This information is used in the designs [P4, P5, P6] to optimize power dissipation for the given settling accuracy.

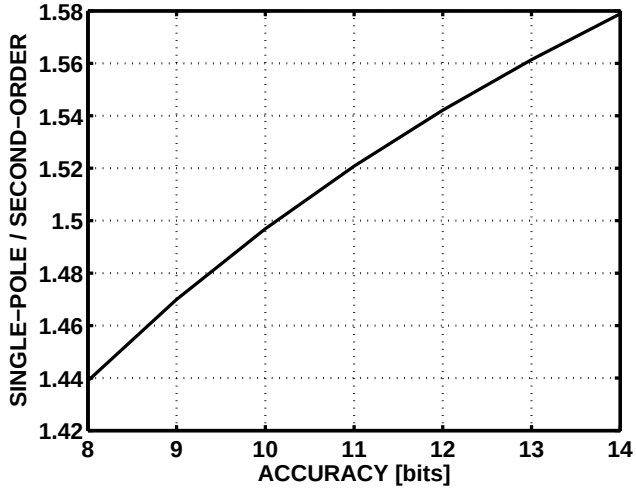

Figure 3.18 Single-pole system GBW requirement versus critically damped second-order system GBW requirement.

3.4 Properties of Switched-Capacitor Circuits

To be able to understand the limitations of SC circuits, a brief overview of the MOS transistor properties and non-idealities in SC circuits is given here. In addition, the noise properties of the SC circuits are discussed.

3.4.1 MOS Switch Transistor Properties in SC Circuits

In SC A/D converters the input signal is sampled using switches and capacitors. The switches are typically implemented as MOS switches. An SC sampling circuit is shown in Figure 3.19. On the left is the sampling circuit with a MOS switch transistor and on the right an equivalent RC circuit. The capacitances C_{bs} and C_{bd} include parasitic capacitance from channel to bulk and source and drain junction capacitances, respectively. The capacitances C_{gs} and C_{gd} include parasitic capacitances from gate to channel and overlap capacitances from gate to source and drain nodes, respectively. The parasitic capacitances introduce nonidealities such as capacitive coupling from the clock signals to each side of the switch through gate capacitances. The resistance R_{ON} models the finite on-resistance of the MOS switch transistor.

First, the impact of the MOS switch transistor on-resistance R_{ON} is discussed. The NMOS switch on-resistance depends heavily on the applied overdrive voltage $V_{od} = V_{GS} - V_{tn}$. The NMOS transistor on-resistance operating in linear region is given by

$$R_{ON} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{tn})}, \tag{3.38}$$

where μ_n is the NMOS transistor carrier mobility, C_{ox} is the NMOS transistor gate oxide capacitance, V_{GS} is the NMOS transistor gate-source voltage, V_{tn} is the NMOS transistor threshold voltage and W and L are the NMOS transistor gate width and length, respectively. For PMOS switch transistors, the signs of all voltages are changed. Typically, the gate voltage V_G is limited by the supply voltage. As can be seen from (3.38), with low supply voltages the on-resistance increases, increasing the sampling circuit

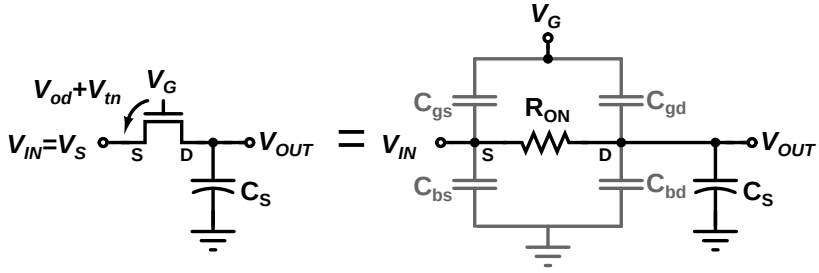

Figure 3.19 Switched-capacitor sampling circuit with MOS switch.

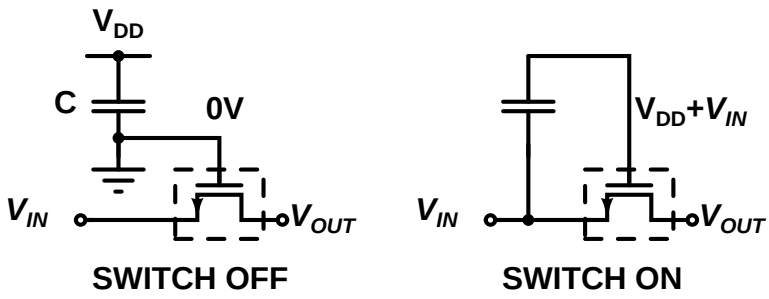

Figure 3.20 Basic principle of bootstrapping.

RC time constant. Hence, the tracking speed and settling time of the sampling circuit, which are both important parameters in high-speed designs, are limited by the sampling circuit RC time constant. Furthermore, the dynamic range is also reduced. In addition to increased on-resistance and reduced dynamic range, the MOS switch on-resistance depends on the signal through the voltage V_{GS}, which causes harmonic distortion when tracking continuous time signals. The signal dependence can be somewhat relaxed by using a CMOS switch that consists of parallel NMOS and PMOS transistors. However, in high-resolution A/D converters, the linearity requirements are more stringent.

There are a couple of known techniques to overcome the problems associated with MOS switch transistor on-resistance. The switch on-resistance can be reduced by increasing the switch gate control voltage over the supply voltage. The gate control voltage is typically increased using charge pumps. This can be done either locally or globally for all control voltages. To avoid possible cross-talk, the voltage generation should be done locally. The drawback of this solution is that the transistor V_{GS} should not exceed the maximum allowed voltage for a given process, or the transistor may break down or at least have reduced long-term reliability. In addition, this solution does not take the switch on-resistance signal dependency into account. A solution that tackles this problem is the bootstrapping technique [71], shown in Figure 3.20. In this solution, the switch transistor V_{GS} is made to track the input signal with an offset voltage, typically close to the supply voltage. A practical solution is shown in Figure 3.21 [72]. In a triple well process, the switch bulk effect can be eliminated by connecting the switch transistor bulk to the input node during the tracking phase. For the circuit in Figure 3.21, this can be done by connecting the bulks of the transistors M_S and M_1 to the node n_1 so as also to avoid the forward biasing of the two transistors [67]. Implementations that eliminate the bulk effect using the standard CMOS process are presented in [67].

As can be seen from Figure 3.19, the MOS switch has non-linear parasitic capacitances to ground (bulk) and to gate. In addition, there are parasitic capacitances at the top and bottom plates of the integrated capacitor, and in practice these capacitances

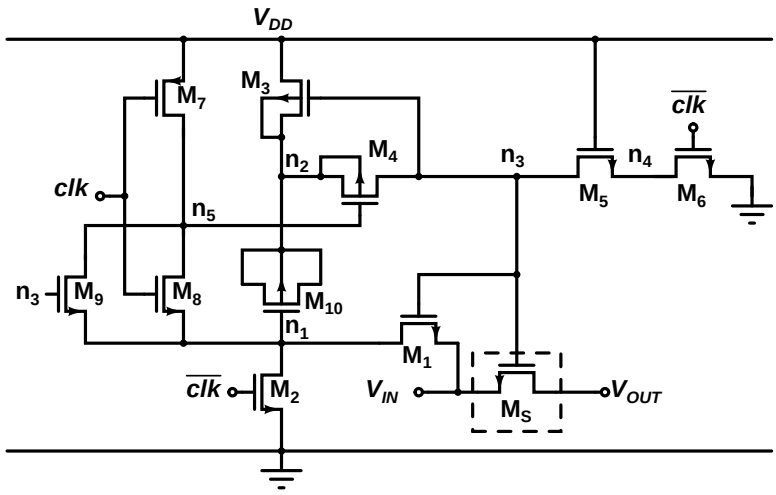

Figure 3.21 Long-term reliable bootstrapped switch [72].

are not equal. The effect of parasitic capacitances can be canceled by using parasitic-insensitive structures, such as the one presented in Section 3.3.4.1.

In addition to finite and signal-dependent on-resistances and non-linear parasitic capacitances, MOS switch transistors have another significant non-ideality, called charge injection. When the MOS switch transistor is turned off, unwanted charges are injected into the circuit. The charge injection is mainly caused by the charge stored in the channel region flowing out to the source and drain areas. For an NMOS transistor operating in the linear region, the channel charge is given by

$$Q_{ch} = -WLC_{ox}(V_{GS} - V_{tn}). \tag{3.39}$$

As can be seen, the channel charge depends on the signal through the voltage V_{GS}. In order to keep the channel charge signal-independent, the V_{GS} should be kept constant. A second, much smaller charge is due to the MOS switch transistor overlap capacitances shown in Figure 3.19. When the switch is closed, the charge is divided between the overlap capacitor portion of C_{gd} and the sampling capacitor C_s causing a charge in the capacitor C_s

$$Q_{ov,C_s} = \frac{-\Delta V_G C_{ov} C_s}{C_{ov} + C_s}, \tag{3.40}$$

where ΔV_G is the voltage change at the switch gate when it is turned off and C_{ov} is the overlap capacitance given by

$$C_{ov} = WL_{ov}C_{ox}, \tag{3.41}$$

where L_{ov} is the channel overlap of the drain/source regions. As can be seen from (3.40), the charge injection resulting from the overlap capacitances can be reduced by

increasing the size of the sampling capacitor.

The charge injection can be either canceled or made signal-independent by using several well-known techniques. Charge injection can be canceled by using half-sized dummy switches with their drain and source terminals short-circuited and clocked at the opposite clock phase compared to the sampling switch. A similar effect happens when CMOS switches are used, as the charges from equally-sized NMOS and PMOS switch transistors cancel each other. The drawbacks of both of these methods are that they both rely on the matching of different transistor parameters and on the accurate timing of the gate control clock edges.

An efficient way to make the charge injection signal-independent is bottom plate sampling [68], shown in Figure 3.15 on page 44, in which the clock phase ϕ_{1a} is a slightly more advanced version with respect to the clock phase ϕ_1. The reason for this is that when the input signal V_{IN} in a non-inverting case is sampled to the capacitor C_s, the switch S_3 opens slightly before the switch S_1. This leaves the top plate of the capacitor C_s floating. The charge injected by the switch S_3 is constant, since the switch is always connected to a fixed voltage, and hence the V_{GS} of the switch is constant. When the switch S_1 is opened, the charge in the capacitor C_s cannot change, since the top plate of the capacitor is floating. Bottom plate sampling is not needed in the clock phase ϕ_2, since both switches, S_2 and S_4, are always connected to a fixed potential, namely ground or operational amplifier virtual ground. The idea is similar in the inverting integrator case. Finally, the resulting constant charge injection can be made common-mode by using differential structures and then suppressed by the common-mode rejection of the operational amplifier.

For the reasons mentioned above, parasitic-insensitive switching structures, bottom plate sampling and the bootstrapped switch presented in [72] were utilized in [P3]. According to the measured results in [P3], the performance was not limited by the distortion in GSM mode and only a minor reduction caused by distortion can be seen in WCDMA mode. Bottom plate sampling was also utilized in [P4, P5, P6].

3.4.2 Noise in SC Circuits

The sampling in SC circuits generates noise. As already described in Section 3.3.1, there are two important noise sources: thermal and flicker noise. The effect of flicker noise can be reduced by increasing the area of the MOS transistor, as discussed in Section 3.3.1, and, for example, by using the auto-zeroing circuit described in Section 3.3.4.2. This analysis concentrates on the effects of thermal noise on the basic SC circuits presented in Section 3.3.4.

3.4.2.1 Noise in SC Integrator

The sampling noise can be evaluated from Figure 3.19, where the MOS switch is modeled with a resistor with a thermal noise source equal to $4kT\mathrm{R_{ON}}$, where k is the Boltzmann constant, T is the absolute temperature, and $\mathrm{R_{ON}}$ is the switch on-resistance. The sampled noise in the capacitor $\mathrm{C_s}$ has a noise power according to the following integral

$$n_{thermal}^2 = \int_0^\infty \frac{4kTR_{ON}}{1+(2\pi f R_{ON}C_s)^2}\mathrm{d}f = \frac{kT}{C_s}. \tag{3.42}$$

As can be seen from (3.42), the result does not depend on the switch on-resistance $\mathrm{R_{ON}}$. Hence, the only way to reduce thermal noise from the switches is to use larger capacitance.

If a a parasitic-insensitive SC integrator shown in Figure 3.15 on page 44 is used, the total thermal noise mean-squared value sampled to the capacitor $\mathrm{C_s}$ in phase ϕ_1 coming from the switches $\mathrm{S_1}$ and $\mathrm{S_3}$ is

$$v_{C_s}^2 = \frac{kT}{C_s}. \tag{3.43}$$

In phase ϕ_2, there are two thermal noise sources: noise from the switches and operational amplifier noise. In this analysis, it is assumed that a single-stage operational amplifier is used, and the settling time is limited by the operational amplifier, not the sampling switches, resulting in the condition $\mathrm{R_{ON}} \ll 1/g_m$. In addition, if a capacitive load is connected to the integrator output in phase ϕ_2, the capacitance $\mathrm{C_s}$ should be replaced with the effective load capacitance $\mathrm{C_{eff}}$. In phase ϕ_2, the noise contribution of the switches $\mathrm{S_2}$ and $\mathrm{S_4}$ is

$$v_{C_s,sw}^2 = \frac{kT}{C_s}2g_mR_{ON}. \tag{3.44}$$

If the noise of the operational amplifier input pair dominates, the total thermal noise mean-squared value at the operational amplifier input, with a typical value of $\gamma = 2/3$, is

$$v_{n,opamp}^2 = \frac{16kT}{3g_m}. \tag{3.45}$$

In phase ϕ_2, the operational amplifier noise mean-squared value sampled to the capacitor $\mathrm{C_s}$ is

$$v_{C_s,opamp}^2 = \frac{4kT}{3C_s}. \tag{3.46}$$

The total thermal noise in the capacitor $\mathrm{C_s}$ is

$$v_{C_s,tot}^2 = \frac{kT}{C_s}\left(1+\frac{4}{3}+2g_mR_{ON}\right) \approx \frac{7kT}{3C_s}, \tag{3.47}$$

If the settling in phase ϕ_2 is limited by the operational amplifier, the noise coming

from the switches S_2 and S_4 is bandwidth limited by the operational amplifier ($R_{ON} \ll 1/g_m$). Hence, the factor $2g_m R_{ON} \ll 1$ and the noise contribution of the switches in phase ϕ_2 is negligible. As a result, the total noise is dominated by the operational amplifier, and the total noise of the integrator is

$$v_{C_s,tot}^2 \approx \frac{7kT}{3C_s}. \tag{3.48}$$

By combining (3.3), (3.6), and (3.48) the dynamic range limited by the thermal noise is

$$DR^2 = \frac{1}{8} \cdot \frac{V_{FS}^2 \cdot OSR}{\frac{7kT}{3C_s}}. \tag{3.49}$$

From (3.49) it can be concluded that the ways to increase dynamic range limited by thermal noise are to increase the full-scale signal V_{FS}, the size of the sampling capacitor C_s, or *OSR*.

In the case of a two-stage operational amplifier, the settling speed is limited by the pole splitting capacitor C_C, and in phase ϕ_2, the capacitor C_s should be replaced with C_C. As a result, (3.48) and (3.49) are transformed to

$$v_{C_s,tot}^2 \approx \frac{kT}{C_s} + \frac{4kT}{3C_C}, \tag{3.50}$$

and

$$DR^2 = \frac{1}{8} \cdot \frac{V_{FS}^2 \cdot OSR}{\frac{kT}{C_s} + \frac{4kT}{3C_C}}. \tag{3.51}$$

3.4.2.2 Noise in SC S/H Circuit

Here, the noise properties of the SC S/H circuit shown in Figure 3.16 on page 45 are analyzed. It should be noted that the same assumptions are made as in the analysis of the SC integrator. In the sampling phase, the noise contribution of the switches is

$$v_{C_H,sw}^2 = \frac{kT}{C_H} 2g_m R_{ON}. \tag{3.52}$$

The operational amplifier noise mean-squared value sampled to the capacitor C_H is

$$v_{C_H,opamp}^2 = \frac{4kT}{3C_H}. \tag{3.53}$$

In the hold phase, the noise contribution of the switches is

$$v_{C_o,sw}^2 = \frac{kT}{C_o} 2g_m R_{ON}. \tag{3.54}$$

The operational amplifier noise mean-squared value sampled to the output capacitor

C_o is

$$v^2_{C_o,opamp} = \frac{4kT}{3C_o}. \tag{3.55}$$

As can be seen from the noise equations above, the noise contribution of both phases is equal if the capacitors C_o and C_H are equally sized. Given this assumption, the total thermal noise mean-squared value sampled to the capacitor C_o is

$$v^2_{C_o,tot} = \frac{kT}{C_H}\left(\frac{4}{3} + 2g_m R_{ON}\right) + \frac{kT}{C_o}\left(\frac{4}{3} + 2g_m R_{ON}\right) \approx \frac{8kT}{3C_o}. \tag{3.56}$$

By combining (3.3), (3.6), and (3.56), the dynamic range limited by the thermal noise is

$$DR^2 = \frac{1}{8} \cdot \frac{V^2_{FS} \cdot OSR}{\frac{8kT}{3C_L}}. \tag{3.57}$$

In the case of a two-stage operational amplifier, the settling time in both phases is limited by the pole-splitting capacitor C_C, and the total thermal noise mean-squared value sampled to the capacitor C_o is

$$v^2_{C_o,tot} = \frac{kT}{C_C}\left(\frac{8}{3} + 4g_m R_{ON}\right) \approx \frac{8kT}{3C_C}. \tag{3.58}$$

By combining (3.3), (3.6), and (3.58), the dynamic range limited by the thermal noise in a two-stage operational amplifier case is

$$DR^2 = \frac{1}{8} \cdot \frac{V^2_{FS} \cdot OSR}{\frac{8kT}{3C_C}}. \tag{3.59}$$

3.5 ΔΣ Modulator A/D Converters

In many applications, accurate (>12 bits) A/D conversion is required. As discussed in Section 3.2, the accuracy of the A/D conversion can be increased using oversampling. However, this requires a considerable amount of digital signal processing, and hence the requirements of the analog components are relaxed at the expense of increased digital circuitry. Fortunately, advances in integrated circuit technology have made fast and cheap digital circuits feasible. In theory, any A/D converter can be used as an oversampling converter. However, as discussed in Section 3.2, for a sinusoidal input signal, doubling the *OSR* increases the resolution by only 0.5 bits. Hence, in practice the oversampling is limited by the dynamic performance of the A/D converter. To increase resolution without an excessive *OSR*, ΔΣ modulators that utilize noise shaping can be used.

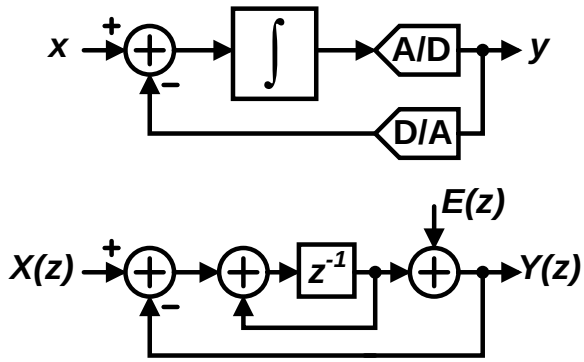

Figure 3.22 First-order ΔΣ modulator and its linear discrete-time z-domain model.

3.5.1 Noise Shaping in ΔΣ Modulators

In ΔΣ modulators, the oversampling advantage is combined with noise shaping to further improve performance. A first-order ΔΣ modulator is shown in Figure 3.22. In a linear discrete-time z-domain model the quantization error resulting from A/D conversion is replaced by the quantization error $E(z)$. The first-order ΔΣ modulator transfer function in the z-domain is given by

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)E(z) \tag{3.60}$$

$$= STF(z) \cdot X(z) + NTF(z) \cdot E(z), \tag{3.61}$$

where $STF(z)$ is the signal transfer function and $NTF(z)$ is the noise transfer function. The input signal $X(z)$ is only delayed, whereas the quantization error $E(z)$ is high-pass filtered with a zero at DC frequency. If the loop filter has a high gain in the signal band, the in-band nonlinearities, such as integrator nonlinearity and quantization error, are greatly suppressed. However, the nonlinearities in the feedback loop, such as digital-to-analog (D/A) converter nonlinearities, are not affected by the noise shaping and hence limit the performance. For this reason, single-bit feedback ΔΣ modulator topologies are preferred, since the feedback D/A conversion is performed using only two quantization levels and is inherently linear. The thermal noise caused by the sampling is also unaffected by the noise shaping, and should be taken into account using (3.49) and (3.51), as appropriate.

A linear discrete-time z-domain model for a second-order ΔΣ modulator is shown in Figure 3.23. The transfer function for the second-order ΔΣ modulator in the z-domain is given by

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^2 E(z). \tag{3.62}$$

Again, the input signal is only delayed. The quantization error, however, is noise

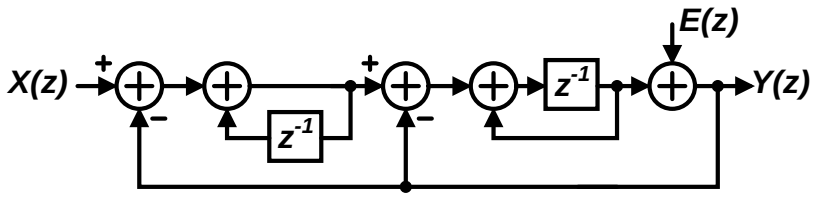

Figure 3.23 Second-order ΔΣ modulator linear discrete-time z-domain model.

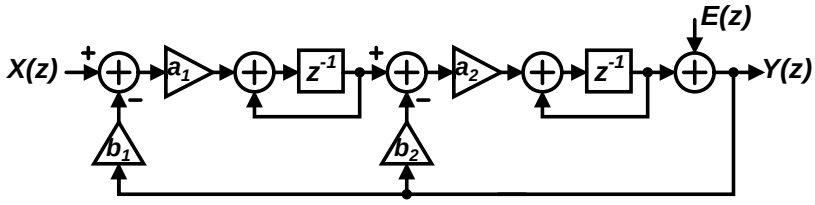

Figure 3.24 Second-order ΔΣ modulator with delaying integrators.

shaped with a second-order high-pass filter.

In addition to the second-order ΔΣ modulator structure shown in Figure 3.23, there exist a number of alternative ways to implement a second-order ΔΣ modulator. A linear discrete-time z-domain model for a second-order ΔΣ modulator that uses two similar delaying integrators [73] is shown in Figure 3.24. Using delaying integrators relaxes the integrator loading, thereby relaxing the settling requirements of the operational amplifier. Furthermore, the input sampling capacitor can also be used as a feedback D/A conversion capacitor, resulting in a smaller silicon area and reduced noise. The transfer function for the second-order ΔΣ modulator in the z-domain is given by

$$Y(z) = \frac{a_1 a_2 z^{-2}}{D(z)} X(z) + \frac{\left(1-z^{-1}\right)^2}{D(z)} E(z), \tag{3.63}$$

where

$$D(z) = \left(1-z^{-1}\right)^2 + a_2 b_2 z^{-1}\left(1-z^{-1}\right) + a_1 a_2 b_1 z^{-2}. \tag{3.64}$$

To make the $STF(z) = z^{-2}$ and $NTF(z) = \left(1-z^{-1}\right)^2$, the conditions $a_1 a_2 b_1 = 1$, $a_1 a_2 = 1$ and $a_2 b_2 = 2$ must be fulfilled. One possible solution is $a_1 = a_2 = b_1 = 1$ and $b_2 = 2$. These factors are used in [P3] to keep the capacitor values at the output of the first integrator as small as possible.

More aggressive noise shaping can be achieved using higher-order ΔΣ modulator loop filters. A general noise transfer function for an L-order noise shaping loop filter is given by

$$NTF(z) = (1-z^{-1})^L. \tag{3.65}$$

If we replace $z^{-1} = e^{-j\frac{2\pi f}{f_s}}$, and have large OSR ($f_s \gg 2 \cdot f_{bw}$), we may approximate

the exponential function with the first two terms of the Maclaurin series, giving $z^{-1} \approx 1 - j\frac{2\pi f}{f_s}$. The noise transfer function is then

$$NTF(f) = \left(\frac{j2\pi f}{f_s}\right)^L. \tag{3.66}$$

Now, the quantization noise power spectral density $E^2(f)$ from (3.5) on page 30 is noise shaped with a noise transfer function $NTF(f)$ and the in-band noise power is given by

$$\begin{aligned} n_{bw}^2 &= \int_0^{f_{bw}} E^2(f)\,|NTF(f)|^2\,\mathrm{d}f \\ &= \int_0^{f_{bw}} \frac{2e_{rms}^2}{f_s}\left|\frac{j2\pi f}{f_s}\right|^{2L}\mathrm{d}f \\ &= \frac{\pi^{2L}}{2L+1}\frac{e_{rms}^2}{OSR^{2L+1}}. \end{aligned} \tag{3.67}$$

Hence, the *SNR* for the L-th order ΔΣ modulator is given by

$$SNR = 6.02N + 1.76 + 10\log\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)\cdot 10\log(OSR). \tag{3.68}$$

As can be seen, doubling the *OSR* improves the *SNR* by $3(2L+1)$ dB or provides $(L+0.5)$ extra bits of resolution. Hence, compared to oversampling without noise shaping, the *SNR* is improved by a factor of $2L+1$. However, there are difficulties in implementing ΔΣ modulators that are higher than second-order, since the ΔΣ operation can be unstable [71]. Hence, the achievable resolution is lower than predicted by (3.68).

3.5.2 The Effect of Operational Amplifier Finite Gain and Settling

In the above discussion, the integrator in the ΔΣ loop is assumed to be ideal. If the first-order ΔΣ modulator shown in Figure 3.22 implemented using the delaying non-inverting SC integrator shown in Figure 3.15 and an operational amplifier with a finite gain A_0 is used, the first-order ΔΣ modulator transfer function from (3.60) changes to

$$Y(z) = \frac{z^{-1}}{1+\frac{z^{-1}}{A_0}}X(z) + \frac{1-z^{-1}\left(1-\frac{1}{A_0}\right)}{1+\frac{z^{-1}}{A_0}}E(z) \tag{3.69}$$

$$= STF(z)\cdot X(z) + NTF(z)\cdot E(z). \tag{3.70}$$

As can be seen from (3.69), as a result of a lossy or leaky integrator the signal and noise transfer functions are attenuated with the factor $\left(1+\frac{z^{-1}}{A_0}\right)$. Furthermore, whereas the

signal transfer function nominator is unchanged, the noise transfer function nominator has changed to

$$NTF(z) = 1 - z^{-1}\left(1 - \frac{1}{A_0}\right). \tag{3.71}$$

From (3.71), it can be seen that with a leaky integrator the noise transfer function zero shifts inside the z-plane unit circle, and hence the attenuation at DC is no longer infinite. Again, approximating the exponential function with the first two terms of the Maclaurin series gives $z^{-1} \approx 1 - j\frac{2\pi f}{f_s}$. The noise transfer function in this case is

$$NTF(f) = \frac{j2\pi f}{f_s} + \frac{1}{A_0}. \tag{3.72}$$

Again, the quantization noise power spectral density $E^2(f)$ from (3.5) on page 30 is noise shaped with the noise transfer function $NTF(f)$ and the in-band noise power is given by

$$\begin{aligned} n_{bw}^2 &= \int_0^{f_{bw}} E^2(f)\,|NTF(f)|^2\,\mathrm{d}f \\ &= \int_0^{f_{bw}} \frac{2e_{rms}^2}{f_s}\left|\frac{j2\pi f}{f_s} + \frac{1}{A_0}\right|^2 \mathrm{d}f \\ &= \frac{\pi^2}{3}\frac{e_{rms}^2}{OSR^3} + \frac{e_{rms}^2}{A_0^2 \cdot OSR}. \end{aligned} \tag{3.73}$$

Comparing the results from (3.67) and (3.73), we see that the second term (3.73) is a result of finite operational amplifier gain. With $A_0 = OSR$, the increase in noise is only $\sim$1.2 dB, and hence the required operational amplifier gain is not stringent. However, even though the $\Delta\Sigma$ noise shaping does not require a large operational amplifier gain, the operational amplifier gain has to be sufficient to suppress the harmonic distortion resulting from nonlinear gain characteristics. Hence, in $\Delta\Sigma$ modulators, this requirement can easily be the dominant one, and should be verified using transistor-level simulations.

In addition to finite operational amplifier gain, the output accuracy also depends on the settling accuracy of the operational amplifier. If the settling of the operational amplifier is linear, finite settling accuracy does not cause distortion [74]. However, in practical realizations the operational amplifier settling is nonlinear, and hence causes distortion. Therefore, a safe approach is to design the operational amplifier settling in such a way as to fulfill the target accuracy in order to keep the settling-induced distortion negligible. In the case of a second-order modulator, the settling accuracy requirement for the second integrator depends on the gain of the first integrator, since the distortion caused by the second integrator is attenuated as a result of the high in-band gain of the first integrator. Therefore, the second integrator has much more relaxed set-

tling requirements, allowing the size and power dissipation to be scaled down. In [P3], the size of the operational amplifier was kept unchanged, but the power dissipation was halved in the second integrator.

3.5.3 ΔΣ Modulator Topologies

Single-stage single-bit first-order ΔΣ modulators are inherently linear and stable, but suffer from idle tones [71]. Single-stage single-bit second-order ΔΣ modulators are widely used, since they are also inherently linear and stable and do not suffer from idle tones [71]. However, in many applications, the performance of the second-order ΔΣ modulator is not adequate. By implementing multi-bit or multi-stage ΔΣ modulators, the performance can be improved without stability problems.

3.5.3.1 Multi-Bit ΔΣ Modulator Topologies

The ΔΣ modulator resolution can be increased by replacing the single-bit quantizer with a multi-bit Nyquist-rate quantizer, for example, a flash A/D converter. The principle of the first-order multi-bit ΔΣ modulator is shown in Figure 3.25. The multi-bit quantization improves the modulator resolution by 6 dB for every bit added to the resolution [74]. Compared to the single-bit quantization, multi-bit quantization reduces the step size in the feedback loop D/A conversion, which improves the stability of the modulator, allowing more aggressive noise shaping in higher-order single-stage modulators [74]. However, it should be noted that in terms of quantization errors, the single-bit quantizer is inherently linear, whereas the multi-bit A/D converter has slight errors in the quantization levels as a result of the limited matching and non-linearity of the components in the A/D converter. Fortunately, the non-idealities in the multi-bit quantizer are suppressed by the preceding high-gain integrator stages. However, the non-idealities in the feedback D/A converter are fed directly to the ΔΣ modulator input, and are processed in the same way as the input signal. Hence, while the stability of the modulator is improved when multi-bit feedback is used, the errors in the feedback D/A converter degrade the performance of the ΔΣ modulator substantially.

The non-idealities in the multi-bit feedback D/A converter can be reduced using dynamic element matching (DEM) techniques. The idea of DEM techniques is to

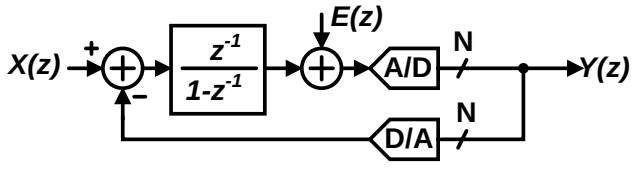

Figure 3.25 The first-order multi-bit ΔΣ modulator.

randomize the element mismatches in the feedback D/A converter so that the mismatch errors are converted to random noise. Hence, the harmonic distortion can be converted into random noise, thus increasing the ΔΣ modulator noise floor. A good overview of different techniques is presented in [32].

3.5.3.2 Multi-Stage ΔΣ Modulator Topologies

In wideband applications, the *OSR* is typically low, reducing the achievable *SNDR* of the first- and second-order ΔΣ modulators. Multi-stage modulators are an easy way to increase the resolution of the ΔΣ modulator without the stability problems that occur in higher-order single-stage ΔΣ modulators. The idea is to cascade stable first- or second-order ΔΣ modulators to implement a higher-order ΔΣ modulator. It should be noted that ΔΣ modulators do not suffer from idle tones if first-order ΔΣ modulators are cascaded with higher-order ΔΣ modulators.

In a multi-stage noise-shaping (MASH) ΔΣ modulator the quantization error from the preceding stage is used as an input signal for the next stage [75]. Ideally, the outputs are combined using digital signal processing in such a way that the output contains only the quantization noise of the last stage. The drawback of the MASH topology is that the performance relies on accurate cancellation of the first-stage quantization error. Integrators with finite gain operational amplifiers are lossy or leaky, and change the analog loop coefficients. Mismatches between analog and digital coefficients result in inaccurate noise cancellation. Therefore, inaccurate noise cancellation is often referred to as noise leakage.

An example of cascading second-order and first-order ΔΣ modulators, referred to as a 2-1 MASH topology, is shown in Figure 3.26. The digital filter stages $H_1(z)$ and $H_2(z)$ are designed in such a way that in the overall output $Y(z)$ the first-stage quanti-

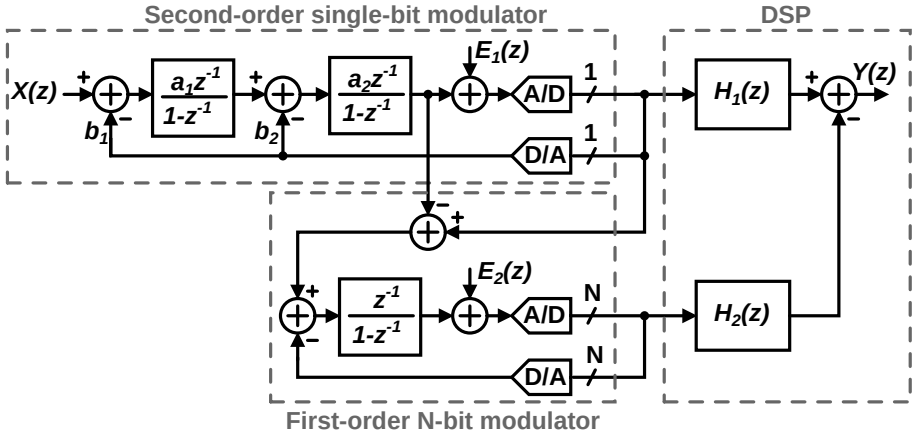

Figure 3.26 2-1 MASH (cascade) topology.

zation error $E_1(z)$ is canceled. The digital filters must satisfy the following condition:

$$H_1(z)NTF_1(z) - H_2(z)STF_2(z) = 0. \tag{3.74}$$

The simplest and most practical way is to choose $H_1(z) = STF_2(z)$ and $H_2(z) = NTF_1(z)$ [74]. With the coefficients $a_1 = a_2 = b_1 = 1$ and $b_2 = 2$, the transfer functions are $H_1(z) = z^{-1}$ and $H_2(z) = \left(1 - z^{-1}\right)^2$. In MASH modulators, it is beneficial to implement the second stage with a multi-bit quantizer, since the input for the second stage is the quantization noise from the first stage, which can be treated as white noise. Hence, no signal-dependent distortion occurs. If the total accuracy requirement is below the achievable matching of the feedback D/A converter (∼10 bits), as in WCDMA operation, the first stage can also be implemented with a multi-bit quantizer [76]. As a result, quantization noise cancellation of the MASH architecture is improved, at the cost of reduced accuracy.

The second stage can also be implemented using a Nyquist-rate A/D converter. The 2-0 MASH topology also known as the Leslie-Singh topology, according to the authors in [77], is shown in Figure 3.27. Here the modulator is implemented using a single-bit feedback and the second stage is used to cancel the first-stage quantization error. The order of the noise shaping is the same as for the first-stage modulator. However, if the cancellation is ideal, only the second-stage quantization error remains at the output. Hence the modulator resolution is increased. The benefit of this structure is the single-bit feedback loop. This kind of structure could be used to increase the resolution in wide-band operation, such as WCDMA. This approach was utilized in [78].

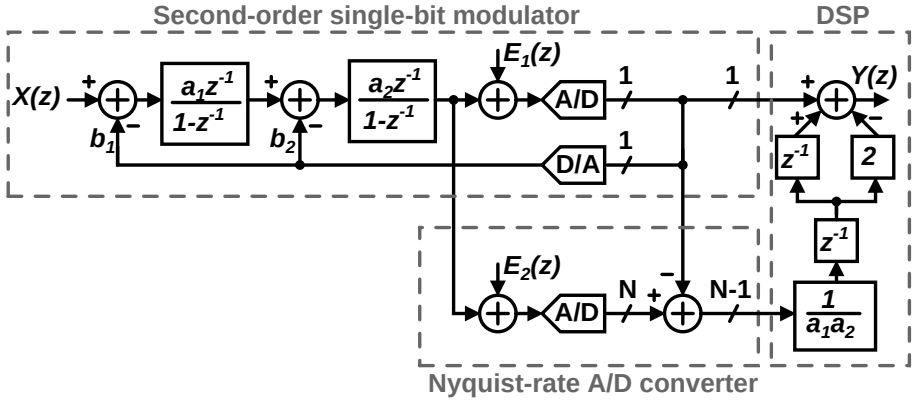

Figure 3.27 2-0 MASH topology or the Leslie-Singh topology.

3.5.4 Discrete-Time vs. Continuous-Time ΔΣ Modulators

ΔΣ modulators can be implemented using discrete-time (DT) SC integrator realization or continuous-time (CT) active-RC or g_m-C integrator realization. SC implementations are attractive, since they exhibit transcendent accuracy and linearity compared to CT implementations. The feedback D/A converter can be implemented by switching charges (DT) or switching currents (CT). In the switched-current case the variation in the amount of charge that is transferred per clock cycle as a result of sampling time uncertainty varies linearly with the variation in timing. Consequently, the switched-current D/A converter is more sensitive to clock jitter than the SC D/A converter [79]. CT modulators have an inherent anti-aliasing filter, which eliminates the need for an additional anti-aliasing filter. Furthermore, CT modulators are insensitive to sampling errors, since the sampling takes place at the output of the loop filter. Hence the sampling errors are attenuated by the loop filter. A CT modulator can theoretically operate with a clock frequency 2–4 times higher than in a DT SC implementation [74]. Despite the advantages of CT modulators, a DT implementation was chosen in [P3]. The main reasons were sensitivity to clock jitter and to demonstrate the technological advances in the realization of DT SC ΔΣ modulator.

3.5.5 ΔΣ Modulators for GSM and WCDMA

To compare the design in [P3] to other ΔΣ modulators targeted for GSM and WCDMA bands published in journals and at conferences, some recently published discrete- and continuous-time ΔΣ modulators, together with their measured results, are collated in Tables 3.3–3.4 and 3.5.

Table 3.3 Discrete-time ΔΣ modulators for GSM/WCDMA 1/2

Reference	[80]	[66]	[76]	[81]
Mode	GSM	GSM/WCDMA	GSM/WCDMA	GSM/WCDMA
Year	2002	2002	2003	2005
Technology [μm]	0.4	0.13	0.13	0.09
Core area [mm^2]	0.4	0.2	0.2	0.4
Modulator order	2-2 MASH	2	2/2-1 MASH	2
A/D resolution [bits]	1	5	1/5	4
Power supply [V]	1.8	1.5	1.2	1.3
Power dissipation [mW]	5	2.4/2.9	2.4*/4.3	2.1
Sampling rate [MS/s]	13	26/46	39/38.4	20/40
Signal bandwidth [MHz]	0.18	0.2/2.0	0.1/1.92	0.2/2.0
OSR	36.1	65/12	195/20	50/10
SNDR [dB]	82	75/49	81/64	72/51
DR [dB]	84	79/50	82/70	77/58
FOM_P [pJ/conv]	1.35	1.31/3.15	1.31/0.86	1.61/1.81
FOM_A [nm^2/conv]	108	109/217	109/40	307/345
FOM_{PA} [pJ·mm^2/conv]	0.54	0.26/0.63	0.26/0.17	0.65/0.72

* Estimated power dissipation with power-down circuitry.

Table 3.4 Discrete-time ΔΣ modulators for GSM/WCDMA 2/2

Reference	[82]	[83]	[P3]
Mode	GSM/WCDMA	GSM	GSM/WCDMA
Year	2005	2006	2006
Technology [μm]	0.09	0.25	0.065
Core area [mm^2]	0.2	-	0.1
Modulator order	2	4	2
A/D resolution [bits]	4	1	1
Power supply [V]	1.2	2.7	1.2
Power dissipation [mW]	1.2	4.0*	3.3/3.6
Sampling rate [MS/s]	76.8	26.0	48.0/96.0
Signal bandwidth [MHz]	0.2/1.94	0.135	0.1/1.92
OSR	192/19.8	96.3	240/25
SNDR [dB]	75/63	84.1	84/49
DR [dB]	-/66	88	85/54
FOM_P [pJ/conv]	0.65/0.19	1.13*	1.27/4.07
FOM_A [nm^2/conv]	109/32	-	38.6/113
FOM_{PA} [pJ·mm^2/conv]	0.13/0.038	-	0.127/0.407

* Includes reference generator buffers.

Table 3.5 Continuous-time ΔΣ modulators for GSM/WCDMA

Reference	[84]	[85]	[86]	[87]
Mode	GSM	GSM/WCDMA	GSM	WCDMA
Year	2002	2003	2004	2004
Technology [μm]	0.18	0.18	0.13	0.13
Core area [mm^2]	0.36[1]	0.18	0.5	0.12
Modulator order	2	5	4	2
A/D resolution [bits]	4	1	3	4
Power supply [V]	1.8	1.8	1.25	0.9
Power dissipation [mW]	1.75	3.8/4.5	3.0	1.5
Sampling rate [MS/s]	20.0	26.0/153.6	26.0	61.44
Signal bandwidth [MHz]	0.2	0.2/3.84	0.24	1.92
OSR	50	65/40	54	32
SNDR [dB]	64	$(92/72)^2$	77	50.9
DR [dB]	75	92/74	90	-
FOM_P [pJ/conv]	3.38	$(0.29/0.18)^2$	1.08	1.36
FOM_A [nm^2/conv]	695	$(13.8/7.2)^2$	180	109
FOM_{PA} [pJ·mm^2/conv]	1.22	$(0.053/0.032)^2$	0.54	0.164

[1] Includes 2^{nd}-order bandpass ΔΣ modulator.
[2] *SNR*.

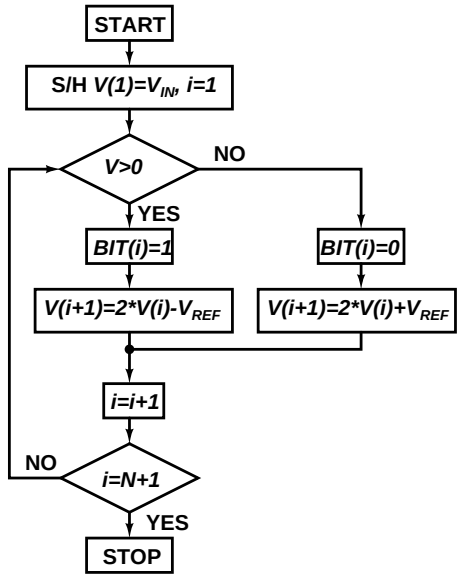

Figure 3.28 Algorithmic A/D conversion principle

3.6 Algorithmic A/D Converters

The algorithmic A/D converter is based on a binary search algorithm, which determines the closest digital word to match an input signal. The basic operation of algorithmic A/D conversion is shown in Figure 3.28. In every cycle, the signal is doubled and a positive or negative reference voltage is added according to

$$V(i+1) = 2 * V(i) + (-1)^{BIT(i)} * V_{REF}, \tag{3.75}$$

where the number of the cycle is $i = 1 - N$, N is the resolution of the A/D conversion, $V(i)$ is the signal on the i_{th} cycle, $V(1) = V_{IN}$, V_{IN} is the input signal, $BIT(i)$ is the i_{th} bit, and V_{REF} is the reference voltage. The algorithmic A/D converter uses the same hardware to perform the A/D conversion in successive cycles. Hence, the algorithmic A/D converter requires very little silicon area and is a suitable candidate for sensor applications. The minimum conversion time for an algorithmic A/D converter is N cycles, where N is the resolution of the A/D converter. However, more than one clock phase is typically required to resolve one bit. In theory, the resolution of an algorithmic A/D converter is infinite. The accuracy is, however, limited by its noise and matching properties.

The first integrated algorithmic A/D converter was proposed by McCharles et al. [88]. It takes two clock phases to resolve one bit. The implementation relies on the intrinsic matching of capacitor ratios. To keep the capacitor ratios accurate under pro-

cess variations, the capacitors should be realized using unit capacitors [89]. Since the matching of on-chip elements is about 0.1%, the achievable accuracy is limited by the capacitor matching to 10 bits [55,90,91]. Since the capacitor matching improves as the area of the capacitor increases, the smallest capacitance in the circuit, the so called unit capacitance, has some minimum value. As a result, the total capacitor area required for an accuracy of over 10 bits can be large.

3.6.1 Algorithmic A/D Converter Speed Requirements

In a fixed system, where an A/D converter operates with a fixed internal system clock, variable sampling rates, and accuracy, some design issues have to be taken into account. The system clock and the maximum sampling rate set the upper limit for the algorithmic ADC operation steps per bit and limit the available topologies. In addition, the proper generation of non-overlapping clock phases requires a duty cycle of 50%. Thus, the internal system clock must be divided by two before the clock is fed to the clock generator. Hence, the maximum number of operation steps per bit N_{steps} is limited to

$$N_{steps} \leq \frac{f_{clk}/2}{N(f_s/2)}, \tag{3.76}$$

where f_{clk} is the frequency of the system clock, N the number of bits, and f_s the sampling frequency. In the designs [P4, P5, P6], the system parameters for A/D conversion with maximum speed and accuracy are $f_{clk} = 2\,MHz, N = 12$, and $f_s = 40\,kHz$. The resulting number of steps $N_{steps} \leq 4.1667$. Therefore, the maximum number of steps per bit in the system is four.

3.6.2 The Effect of Operational Amplifier Finite Gain and Settling

The algorithmic A/D converter operates in consecutive cycles in which the output depends on the output of the previous cycle. Therefore, the conversion errors caused by finite operational amplifier gain and incomplete settling cumulate during the conversion and determine the achievable conversion accuracy. If the capacitor matching and operational amplifier offset voltage are not taken into account, the minimum operational amplifier DC gain for an algorithmic A/D converter using a simple one-bit multiply-by-two gain stage is equal to the requirements in pipeline A/D converters [67, 92] and is given by

$$A_0 > 2^N, \tag{3.77}$$

where N is the number of bits. In decibels the requirement is given by

$$A_0 > 6.02 \cdot N \text{ dB}. \tag{3.78}$$

The operational amplifier gain requirement derived for the algorithmic A/D converter in [P5, P6] is about eight decibels higher. However, it should be noted that in the gain analysis in [P5, P6] capacitor mismatch and operational amplifier offset are taken into account. Compared to the gain requirements for ΔΣ modulators, the gain requirements for algorithmic A/D converters are much more stringent. Therefore, algorithmic A/D converters are not as suitable as ΔΣ modulators for low supply voltages. In order to alleviate the high operational amplifier gain requirements, correlated double sampling (CDS) techniques can be used to increase the effective value of the operational amplifier DC gain to the square of the true value [93].

The settling requirements for algorithmic A/D converters are equal to the algorithmic A/D converter gain requirements, which, according to (3.78), depend on the target accuracy. Therefore, the settling requirements are comparable with those for ΔΣ modulators. However, in some algorithmic A/D converter realizations, as in [94], the requirements are higher, resulting in more stringent settling requirements.

3.6.3 Capacitance Ratio-Independent Principle

The operation of the algorithmic A/D converter requires a multiply-by-two operation, and if the converter is implemented using switched capacitors, the multiply-by-two operation depends on the capacitor ratios, which are hard to implement accurately. However, it is possible to implement an algorithmic A/D converter using a capacitance ratio-independent technique first proposed by Li et al. [94]. This technique makes the algorithmic A/D conversion independent of the capacitance ratios, which reduces silicon area and makes it possible to implement an A/D converter of over 10-bits without digital calibration. The total operation in [94] takes 6 clock phases to resolve one bit, two for S/H and four for ratio-independent multiply-by-two switching. The ratio-independent multiply-by-two switching algorithm presented in [94] is shown, for the sake of simplicity, as a single-ended presentation in Figure 3.29. The S/H circuit shown in Section 3.4 holds the sampled signal during multiply-by-two operation. Phases 1 to 4 in Figure 3.29 describe the operation during the first cycle. In the first phase, the signal held in S/H is stored in the capacitor C_1, together with the amplifier offset voltage. The amplifier offset voltage is also stored in the capacitor C_2. In the second phase, the charge in the capacitor C_1 is transferred to the capacitor C_2. The amplifier offset voltage is canceled, but the charge stored in the capacitor C_2 depends on the ratio of the two capacitor values. In the first cycle the bottom plate of the capacitor C_1 is connected to ground. However, in the following cycles, either a positive or negative reference voltage is connected, depending on the bit resolved in the previous cycle. In the third phase, the signal held by the S/H circuit is sampled again into the capacitor C_1 together with the amplifier offset voltage. The top plate of the capacitor C_2 is floating,

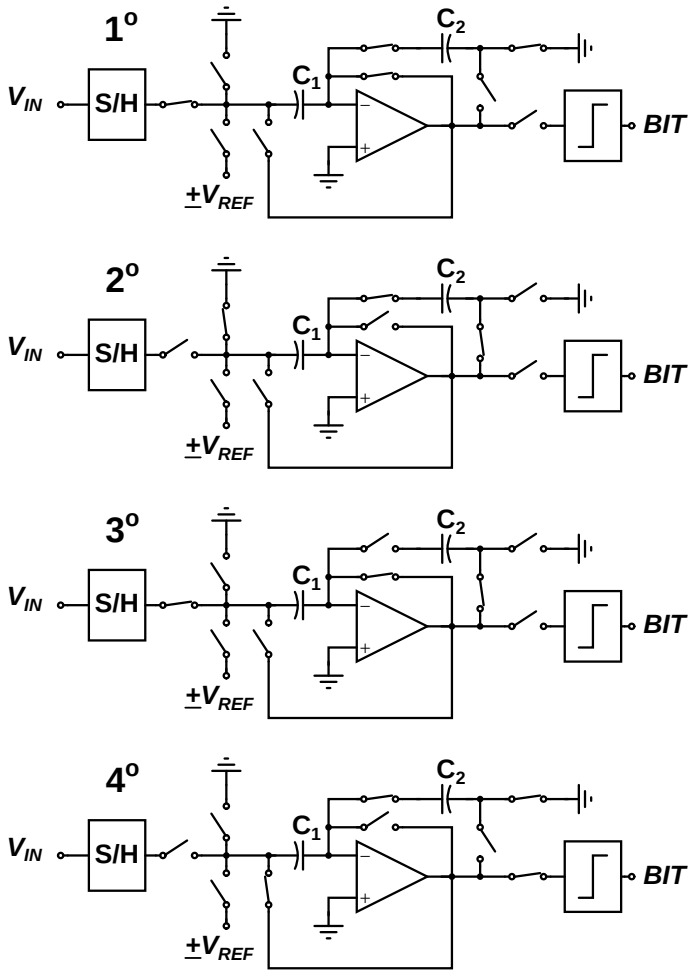

Figure 3.29 Ratio-independent multiply-by-two switching algorithm [94].

so the charge in the capacitor C_2 remains unchanged. In the fourth phase, the charge stored in the capacitor C_2 is transferred back to the capacitor C_1. Since the charge transferred into the capacitor C_2 in Phase 2 is now transferred back to the capacitor C_1, the operation is ratio-independent. The resulting output voltage is now two times the sampled input signal. The output is then sampled by the S/H circuit and the first bit is resolved. In the following cycles, the output changes according to (3.75).

The traditional ratio-independent algorithmic A/D converter uses six clock steps to convert one bit and requires two amplifiers and a comparator [94]. Improvements to the traditional ratio-independent operation, such as reducing the required number of clock steps, relaxing the operational amplifier gain requirements, and increasing the accuracy of the traditional ratio-independent operation have been proposed [95–101].

For sensor systems, the power dissipation and silicon area should be minimized.

Hence the number of operational amplifiers and the number of clock steps required should be reduced. Furthermore, if amplifiers are always processing signals when they are on, no power is wasted.

The designs presented in [95–99] all require two operational amplifiers and a comparator. The circuits in [95, 99] are quite similar to [94]; however, the number of clock steps required per bit is reduced to four by partially combining the sample-and-hold and amplification phases. The A/D converter in [95] is less sensitive to amplifier finite gain, since the closed loop gain error is compensated using a reference refreshing technique. In the reference refreshing technique the reference is sampled only once and in every cycle it is passed through the same loop that the signal goes through. Consequently, the errors in loop gain are also stored in the refreshed reference voltage, thus correcting the loop gain error.

The ratio-independent algorithmic A/D converter in [96] requires three clock steps per bit. The principle is shown in Figure 3.30. The operation is insensitive to capacitance ratios, operational amplifier offset, and parasitic capacitances. The most significant bit (*MSB*) is resolved in Phases 1 to 3 and the rest of the bits are resolved by recycling Phases 4 to 6. The input signal is sampled in Phase 1 to the capacitor C_0. The charge in C_0 is transferred to the capacitor C_1 in Phase 2 and simultaneously sampled to capacitor C_3. In Phase 3, the *MSB* is resolved using the second operational amplifier as a comparator. At the same time, the charge in the capacitor C_1 is transferred to the capacitor C_2 for the next cycle. The operation of the cycles $2-N$ depends on the bit resolved in the previous cycle. Figure 3.30 shows the operating phases 4 to 6, when the previous bit is one. If the previous bit is zero, the controls of the switches connecting the bottom plate of the capacitor C_0 to ground or to V_{REF} are interchanged. In

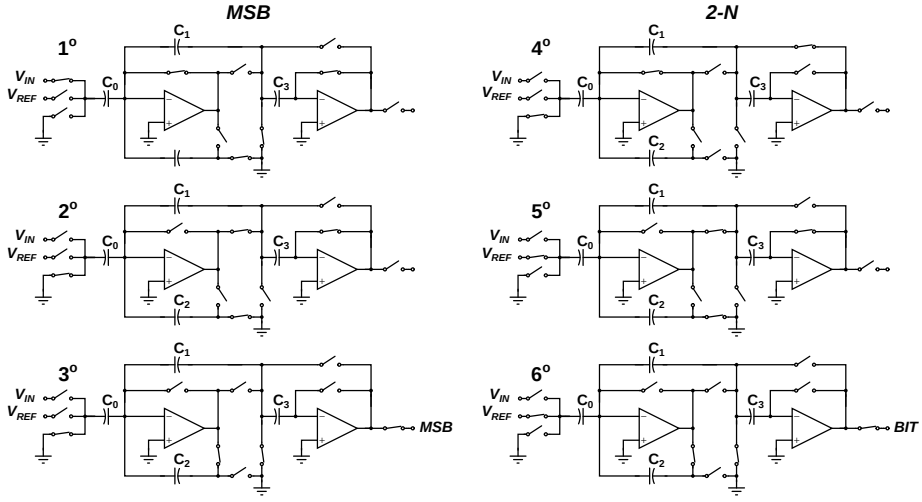

Figure 3.30 Ratio-independent operation requiring three clock steps per bit [96].

Phase 4, the output voltage in C_3 is restored to the capacitor C_1. At the same time, an appropriate voltage is sampled to the capacitor C_0. The bottom plate of the capacitor C_2 is floating, so the charge in C_2 cannot change. In Phase 5, the charge stored in C_2 is transferred back to the capacitor C_1, doubling the charge in the capacitor C_1. The multiplication is accurate, since the same charge that was transferred from the capacitor C_1 to the capacitor C_2 is transferred back. The reference voltage V_{REF} is subtracted from the output voltage through the capacitor C_0. The resulting output is sampled to the capacitor C_3. In Phase 6, the next bit is resolved and the charge in the capacitor C_1 is again transferred to the capacitor C_2. The main disadvantage in this circuit is the use of the capacitor C_0. As a result, the *MSB* cycle is not ratio-independent but depends on the capacitance ratios of the capacitors C_0 and C_1. The same error is introduced when the reference voltage is added or subtracted. The designs [P4, P5, P6] are based on the operation in Figure 3.30. However, in these designs, the second operational amplifier is eliminated and the whole operation is capacitance ratio-independent.

In the designs described above, the auto-zeroing technique [93] is used to cancel the offset and flicker noise of the amplifier. The implementation in [97] uses the CDS technique to square the operational amplifier gain and thus relax the operational amplifier gain requirements. However, the drawback of using CDS to square the effective operational amplifier gain is that the operation requires seven clock steps for one-bit conversion. The architecture presented in [98] utilizes CDS and requires only four clock steps per bit. However, the implementation requires several capacitors and the CDS operation is sensitive to capacitor bottom plate parasitics.

The architecture presented in [101] is different from other voltage-mode techniques, since the capacitance ratio-independent operation is implemented using accurate voltage addition. The principle is shown in Figure 3.31. In the sampling phase the input signal is sampled to one set of capacitors and sequentially the first bit is resolved. In the following cycles, the signal is multiplied by two by using single-ended operational amplifiers as floating buffers. The output is sampled to another set of capacitors

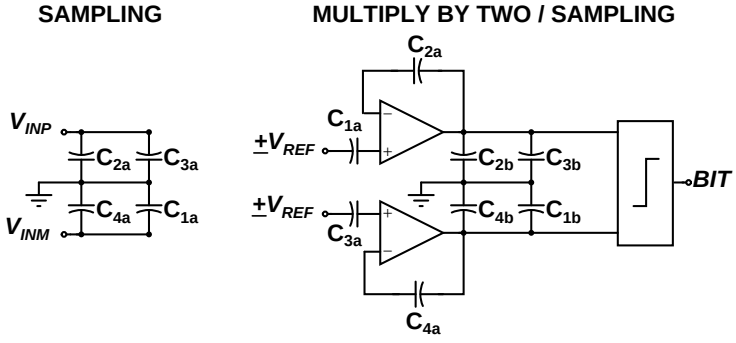

Figure 3.31 Ratio-independent voltage adder [101].

and another bit is resolved. The architecture uses 1.5-bit stage for digital redundant sign digit (RSD) correction [102] to keep the operation insensitive to comparator offset voltage. The architecture requires a total of eight capacitors to implement a pseudo-differential algorithmic A/D converter. The structure requires only one clock step to resolve one bit, and hence is better suited than other ratio-independent structures to high-speed applications. Parasitic capacitance at the operational amplifier input causes voltage division in multiply-by-two operation. Hence the operational amplifier input stage should have low parasitic capacitance with respect to the chosen capacitor values. Furthermore, the operational amplifier input stage has to be able to operate with a full input signal range, since the operational amplifier inputs follow the signal in multiply-by-two operation. While this solution is insensitive to capacitor matching, it does not take the operational amplifier offset voltage V_{OFF} into account. The offset voltage is not canceled in the first multiply-by-two cycle and the cancellation in the following cycles depends on the matching of the offset voltages of the two different amplifiers.

The architecture presented in [100] uses an offset polarity reversing technique to cancel the operational amplifier offset voltage. However, the architecture in [100] is designed for pipeline A/D converters, and has to be modified for algorithmic A/D conversion. A similar offset polarity reversing technique is utilized in the designs in [P4, P5, P6]. The principle is shown in Figure 3.32. The key idea in offset polarity reversing is to exploit the properties of a fully differential amplifier. When a fully differential amplifier is connected to a negative feedback, the total amplifier offset voltage $2V_{OFF}$ is divided equally between the input terminals. Hence, if the the positive and negative terminals are interchanged, the offset polarity changes. This changes the offset sampled to a capacitor at the amplifier output. In [100], the offset is first sampled to the output capacitor in a typical way, as shown in Figure 3.32, and then the polarity is reversed, resulting in zero offset voltage at the output capacitor. In the designs in [P4, P5, P6] offset polarity reversing is utilized only in a single phase to reverse the polarity of the offset sampled by the output capacitor. Hence it is possible to implement ratio-independent operation in three clock steps with a single operational amplifier [P4].

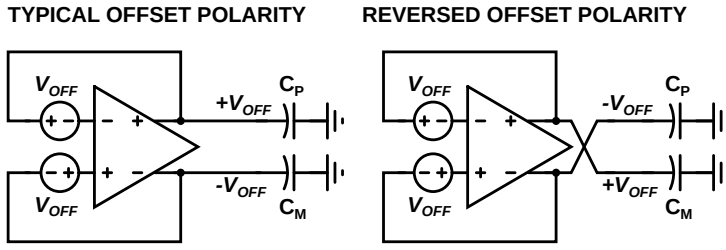

Figure 3.32 Priciple of offset polarity reversing.

The ratio-independent algorithmic A/D converters published in journals and at conferences, together with their measured results, are collated in Tables 3.6–3.7.

Table 3.6 Ratio-independent algorithmic A/D converters 1/2

Reference	[94]	[95]	[96]	[97]
Year	1984	1986	1988	1996
Technology [μm]	5	5	2	0.8
Clock phases/bit	6	4+2	3	7
Resolution [bits]	12	13	8	14
Core area [mm^2]	1.54	1.23	0.79	1.68
Power supply [V]	$\pm$5	$\pm$5	5	$\pm$2.5
Power dissipation [μW]	17000	-	-	50000
Current consumption [μA]	1700	-	-	10000
Sampling rate [kS/s]	8	8	8	10
Signal bandwidth [kHz]	-	-	-	-
SNDR [dB]	-	68[1]	-	-
SFDR [dB]	-	-	-	-
Maximum *INL* [*LSB*]	3.2	2.0	0.5	1.0
Maximum *DNL* [*LSB*]	0.9	1.0	0.2	-
FOM_P [pJ/conv]	-	-	-	-
FOM_A [nm^2/conv]	-	-	-	-
FOM_{PA} [pJ·mm^2/conv]	-	-	-	-

[1] Approximated from the measurement figure.

Table 3.7 Ratio-independent algorithmic A/D converters 2/2

Reference	[101]	[99]	**[P4]**	**[P6]**
Year	2003	2004	2006	2007
Technology [μm]	0.25	0.35	0.13	0.13
Clock phases/bit	1	4	4 (3)	4
Resolution [bits]	12	12	12	12
Core area [mm^2]	0.15	0.3	0.055	0.041
Power supply [V]	2.5	2.7	1.8	1.8
Power dissipation [μW]	5500	351	32	68.4
Current consumption [μA]	2200	130	18	38
Sampling rate [kS/s]	3300	8	41.67	40
Signal bandwidth [kHz]	500	4	20.8	20
SNDR [dB]	64.5	67.8	60	63.3
SFDR [dB]	80	75	80	80.2
Maximum *INL* [*LSB*]	0.8	1.4	-	-1.8
Maximum *DNL* [*LSB*]	0.25	1.4	-	-1.0
FOM_P [pJ/conv]	4.01	21.9	0.94	1.45
FOM_A [nm^2/conv]	109	18694	1615	858
FOM_{PA} [pJ·mm^2/conv]	0.601	6.56	0.052	0.059

3.6.4 Algorithmic A/D Converters with Digital Correction

Algorithmic A/D converters that use various forms of digital correction to improve performance have been presented in [62, 102–116].

Digital background calibration is implemented in [107, 108, 112, 114]. Background calibration may improve the performance of an A/D converter but it requires a lot of silicon area. Looking at Tables 3.8–3.10, it can be seen that the best power and area efficiency are not achieved using digital background calibration.

RSD coding [102] is used in most of the designs, since it relaxes the comparator accuracy requirements with a little excess hardware. The number of comparators is doubled and in the digital domain a small adder is required. The designs in [110, 111, 113, 115, 116] all use some type of RSD correction and have a very small silicon area. In addition, the performances of these designs, shown in Tables 3.8–3.10, are good. It can be stated that to minimize the area in sensor applications only a simple digital correction should be implemented. RSD correction was not implemented in the designs in [P4, P5, P6], since the main objective was to improve analog performance. However, utilizing RSD correction could improve the performance.

Digitally corrected algorithmic A/D converters published in journals and at conferences, together with their measured results, are shown in Tables 3.8–3.10.

Table 3.8 Digitally corrected algorithmic A/D converters (1/3)

Reference	[102]	[103]	[104]	[62]	[105]
Year	1992	1992	1993	1993	1995
Technology [μm]	3	-	0.9	1.6	0.8
Clock phases/bit	2	-	1	0.6	0.6
Resolution [bits]	13	17	10	12	10
Core area [mm^2]	2.94	-	1.0	1.0	1.5
Power supply [V]	$\pm$5	-	5.0	$\pm$2.5	2.7
Power dissipation [μW]	45000	120000	10000	45000	10800
Current consumption [μA]	4500	-	2000	4500	4000
Sampling rate [kS/s]	25	1	667	600	3000
Signal bandwidth [kHz]	12.5	0.5	-	-	1500
SNDR [dB]	-	90[1]	-	-	-
SFDR [dB]	83	87	-	-	-
Maximum *INL* [*LSB*]	0.55	-	0.5	1.0	1.39
Maximum *DNL* [*LSB*]	-	-	0.5	0.6	0.5
FOM_P [pJ/conv]	-	4642.4	-	-	-
FOM_A [nm^2/conv]	-	50292.6	-	-	-
FOM_{PA} [pJ·mm^2/conv]	-	6035.1	-	-	-

[1] *SNR*.

Table 3.9 Digitally corrected algorithmic A/D converters (2/3)

Reference	[106]	[107]	[108]	[109]	[110]
Year	1996	1999	2000	2003	2004
Technology [μm]	0.8[1]	1.5	0.35	0.18	0.18
Clock phases/bit	0.5	1.17	0.5	-	2
Resolution [bits]	10	12	8	10.4	10
Core area [mm^2]	0.93	5.94	0.11[2]	1.44	0.11
Power supply [V]	3.3	5.0	3.0	0.9	1.8
Power dissipation [μW]	15000	16000	23000[2]	9000	9500
Current consumption [μA]	4545	3200	767	10000	5278
Sampling rate [kS/s]	2000	125	13000	1000	10400
Signal bandwidth [kHz]	-	62.5	6500	500	6200
SNDR [dB]	-	71.0	45	55	57.7
SFDR [dB]	-	95	60	75	70
Maximum *INL* [*LSB*]	0.53	0.21	0.62	1.05	0.8
Maximum *DNL* [*LSB*]	0.4	0.34	0.61	0.8	0.6
FOM_P [pJ/conv]	-	44.14	12.18	19.59	1.22
FOM_A [nm^2/conv]	-	16388.2	58.2[2]	3134	14.15
FOM_{PA} [pJ·mm^2/conv]	-	262.2	1.34[2]	28.2	0.134

[1] Bipolar CMOS (BiCMOS).
[2] Off-chip digital calibration not included.

Table 3.10 Digitally corrected algorithmic A/D converters (3/3)

Reference	[111]	[112]	[113]	[114]	[115]	[116]
Year	2005	2005	2005	2005	2006	2006
Technology [μm]	0.25	0.18	0.25	0.25	0.13	0.25
Clock phases/bit	4	0.5	3.67	-	0.5	-
Resolution [bits]	12	12	12	16	11	12
Core area [mm^2]	0.048	1.4	0.031	1.6[2]	0.24	0.044
Power supply [V]	3.3	0.9	3.3	2.5	3.0	3.3
Power dissipation [μW]	430	12000	149	105000[2]	15000	430
Current consumption [μA]	130.3	1333	45.2	42000	5000	130.3
Sampling rate [kS/s]	1000	5000	-	1000	10000	2000
Signal bandwidth [kHz]	-	2500	-	-	5000	-
SNDR [dB]	62.0[1]	50	-	89	56	-
SFDR [dB]	-	77	-	-	69	-
Maximum *INL* [*LSB*]	4.0	1.4	3.79	4.8	3.5	-
Maximum *DNL* [*LSB*]	0.9	0.6	0.78	0.66	0.9	0.81
FOM_P [pJ/conv]	0.42	9.29	-	4.56	2.91	-
FOM_A [nm^2/conv]	46.66	1083.7	-	69.4[2]	46.6	-
FOM_{PA} [pJ·mm^2/conv]	0.020	13.0	-	7.3	0.698	-

[1] *SNR*.
[2] Off-chip digital calibration not included.

3.6.5 Algorithmic A/D Converters using Current-Mode Approach

Current-mode algorithmic A/D converters have been studied alongside voltage-mode converters [117–122]. The benefits of the current-mode approach are its small silicon area and modest operational amplifier gain requirements. Additionally, current-mode A/D converters do not require linear capacitors and have a low voltage swing. However, the current-mode approach requires a voltage-to-current converter and matched current sources. Furthermore, many current-mode realizations are single-ended structures with poor noise immunity.

The ratio-independent current-mode switched-current (SI) algorithmic A/D converter presented in [117] utilizes dynamic current memories to implement accurate multiply-by-two operations. The principle is shown in Figure 3.33. In the first phase, the switches S_2 and S_3 are closed and the current I_1 is set to be equal to the input current I_{IN}. When the switch S_3 at the transistor gate is opened, the transistor gate capacitance holds the correct gate voltage. In the second phase, the current I_2 is set to be equal to the input current I_{IN}. Finally, both currents, I_1 and I_2, are summed, resulting in an output current $I_{OUT} = I_1 + I_2 = 2I_{IN}$. In the algorithmic realization, one additional phase is required for comparison. In actual realization, the gate capacitance is not adequate to hold the charge at the transistor gate. Hence, an additional hold capacitor is required. Furthermore, the charge injection from the switches S_3 and S_5 should be minimized. Another design by the same author is presented in [118]. It requires a conversion cell for each bit and hence operates more like a pipelined A/D converter. However, a new sample is taken only when the previous conversion has ended. Nevertheless, the conversion speed is much faster than in [117]. The realization uses active current mirrors to improve the current mirror accuracy and to offer a very low input impedance. However, the realization does not implement an accurate multiply-by-two operation.

The technique presented in [117] is used with some improvements in designs [120, 122]. In [122], the number of clock phases required is reduced from four to two. Dynamic current memories with a different topology are also used in [119]. The SI algorithmic A/D converter presented in [121] is fully differential. The design uses a current-mode double-sampling (S^2I) technique to reduce signal-dependent charge

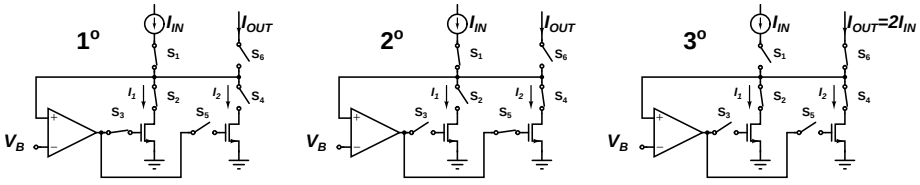

Figure 3.33 Multiply-by-two using dynamically biased current memories.

injection [123]. The S^2I technique also provides a gain-squaring effect, and thus the effective loop gain of the current-mode S/H circuit is increased. However, as a result of using a multi-step SI approach, the A/D converter requires seven clock steps to resolve one bit and requires a large amount of silicon area compared to other current-mode realizations.

Algorithmic current-mode A/D converters published in journals and at conferences, together with their measured results, are collated in Table 3.11.

Table 3.11 Current-mode algorithmic A/D converters

Reference	[117]	[118]	[119]	[120]	[121]	[122]
Year	1990	1990	1991	1997	1998	1999
Technology [μm]	3	3	3	0.8	0.8	2
Clock phases/bit	4	1	4	-	7	2
Resolution [bits]	10	8	14	8	10	12
Core area [mm^2]	0.32	0.74	1.0	0.014	4.0	2.13
Power supply [V]	5	5	5	4	1.5	3.3
Power dissipation [μW]	-	63000	2500	370	2000	1900
Current consumption [μA]	-	12600	500	92.5	1333	576
Sampling rate [kS/s]	25	500	5.7	40	12	800
Signal bandwidth [kHz]	-	-	-	-	6	400
SNDR [dB]	-	-	-	-	49	65
SFDR [dB]	-	-	-	-	65	67
Maximum *INL* [*LSB*]	0.92	0.52	0.5	-	1.4	0.45
Maximum *DNL* [*LSB*]	0.87	0.46	-	1.0	0.63	0.6
FOM_P [pJ/conv]	-	-	-	-	724	1.63
FOM_A [nm^2/conv]	-	-	-	-	1447583	1832
FOM_{PA} [pJ·mm^2/conv]	-	-	-	-	2895	3.481

3.6.6 Other Algorithmic A/D Converters

Algorithmic A/D converters that improve performance using kinds of techniques other than those described above are discussed here [124–128].

The A/D converters described in [124,127] use layout techniques to improve capacitor matching. In addition to layout techniques, in [124], the operational amplifier bias voltages are switchable, resulting in a power saving of 40%. In [127], the performance is further improved using digital RSD correction.

The A/D converter in [125] combines a $\Delta\Sigma$ modulator and algorithmic A/D converters. The converter operates first as a first-order $\Delta\Sigma$ modulator to convert the most significant bits. Then the same hardware is transformed to an algorithmic A/D converter to resolve the remaining least significant bits. With this technique, the digital decimation filter can be replaced with a much simpler digital control and reconstruction logic.

The A/D converter in [126] uses the switched-opamp (SO) technique [129]. In this design, the SO technique is used to reduce power dissipation, rather than the power supply. However, if the operational amplifier is active all the time, no power reduction is gained. The design relies on capacitor matching in multiply-by-two operations, since the target resolution is only 10 bits. Additionally, this design utilizes digital RSD correction logic to cancel the comparator offset.

The A/D converter in [128] uses Gray coding instead of binary coding to reduce accumulated errors typical of algorithmic conversion. In commonly used binary coding, the reference voltage is either reduced from, or added to, the sampled signal, depending on the sign of the bit resolved in the previous cycle. In Gray coding, the reference voltage is kept constant and the sampled signal is either reduced from, or added to, the reference voltage. With fully differential implementation, the sign of the sampled signal can be changed without additional hardware. According to simulated results, the Gray coding is less sensitive to accumulated offset errors than binary coding.

Other types of algorithmic A/D converters published in journals and at conferences, together with their measured results, are collated in Table 3.12.

Table 3.12 Other algorithmic A/D converters

Reference	[124]	[125]	[126]	[127]
Year	1998	2001	2004	2004
Technology [μm]	0.6	0.8	0.8[2]	0.13
Clock phases/bit	-	1.2	1.1	0.38
Resolution [bits]	10	13.5	10	16
Core area [mm^2]	5.5	1.3	0.8	0.5
Power supply [V]	3.3	1.2[1]	2.8	3.0
Power dissipation [μW]	7000	150	17.89	6000
Current consumption [μA]	2121	125	6.39	2000
Sampling rate [kS/s]	200	16	2.9	500
Signal bandwidth [kHz]	100	8	-	250
SNDR [dB]	53	80	52.3	77.4
SFDR [dB]	-	91	59.6	< 90
Maximum *INL* [*LSB*]	1.8	-	0.98	6.1
Maximum *DNL* [*LSB*]	0.8	-	0.67	0.9
FOM_P [pJ/conv]	95.9	1.15	18.32	1.98
FOM_A [nm^2/conv]	75349	9941	819294.7	165
FOM_{PA} [pJ·mm^2/conv]	527.4	1.491	14.65	0.99

[1] Switches driven from a 3.6-V charge pump voltage.
[2] BiCMOS.

Chapter 4

Summary of publications

Here all the publications included in this thesis are summarized:

[P1] 2.4-GHz Receiver for Sensor Applications

A 1.2-V 3.4-mW direct-conversion receiver for wireless sensor applications operating in the 2.4-GHz industrial, scientific and medical (ISM) band. The receiver uses a modified Bluetooth system that has optimized radio parameters for low-power applications. The demonstrator receiver is fabricated in a 0.13-μm standard CMOS process and consists of a merged LNA and mixers, LO buffers, and one baseband channel. The receiver consumes 2.75 mA from a 1.2-V supply. The receiver achieves 47-dB voltage gain, 28-dB *NF*, 21-dBm *IIP3*, and +18-dBm *IIP2*. Special attention is paid to the simultaneous design of the mixer-baseband interface and the current boost method of the mixer. This work demonstrates that it is feasible to design a receiver for sensor applications with extremely small active and stand-by current consumption when the system allows a high noise figure.

[P2] Direct-Conversion Receiver for Ubiquitous Communications

In this paper a direct-conversion receiver operating in a 2.4-GHz sensor network is presented. The receiver uses modified Bluetooth as a radio connection and consumes 4.3 mA from a 1.2-V supply. The receiver achieves 43-dB voltage gain, 25-dB *NF*, 22-dBm *IIP3*, and +11-dBm *IIP2*. Even though power dissipation is increased from [P1], a received signal strength indicator, on-chip current references, and a second baseband channel are added while the active silicon area is not increased. Furthermore, the start-up time, which is very important in ubiquitous communications, was a significant improvement on [P1]. As a result, the overall performance is an improvement on [P1].

[P3] A 1.2V Dual-Mode GSM/WCDMA ΔΣ Modulator in 65nm CMOS

This paper describes a dual-mode ΔΣ modulator for a GSM and WCDMA receiver for a mobile phone. The total core area of the modulator is 0.1 mm^2, and it draws 2.75 mA and 3.0 mA from a 1.2-V supply in GSM and WCDMA modes, respectively. The ΔΣ modulator achieves 84-dB *SNDR* in GSM mode and 49-dB *SNDR* in WCDMA mode. The prototype is fabricated in a 65-nm CMOS technology, using only metal-to-metal capacitors. The design shows that the improvement in the available bandwidth from using the 65-nm CMOS process can be used to improve the performance of the existing solutions to meet the increased demand for higher data rates. In addition, the design shows that high-performance analog design can be carried out using very deep sub-micron CMOS processes.

[P4] A 12-bit 32μW Ratio-Independent Algorithmic ADC

This paper describes a 12-bit capacitance ratio-independent algorithmic A/D converter designed for a capacitive microaccelerometer interface. The implemented circuit uses a new approach to perform capacitance ratio-independent multiply-by-two operation using only one operational amplifier. The power dissipation is minimized using a dynamically biased operational amplifier. As a result, the A/D converter, implemented in a 0.13-μm CMOS, achieves 80-dB *SFDR* and 60-dB *SNDR* with a very low 32-μW power dissipation and an active die area of 0.055 mm^2.

[P5] A 62μA Interface ASIC for a Capacitive 3-axis Microaccelerometer

This paper reports the functionality of an interface application-specific integrated circuit (ASIC) for a capacitive three-axis microaccelerometer. The whole system was integrated on a single chip, excluding the digital signal processor. The sensor interface consists of a front-end that converts the acceleration signal to voltage, two algorithmic A/D converters, two frequency references, and a voltage, current, and temperature reference circuit. At the system level, die area and power dissipation are reduced by using time-multiplexed sampling and varying duty cycles down to 0.3%. The chip, with a 0.51-mm^2 active area, draws 62 μA from a 1.8-V supply while sampling temperature at 100 Hz, and four proof masses, each at 1.04 kHz. The A/D converter designed for this system uses a similar method to perform ratio-independent multiply-by-two operation as in [P4]. However, the number of active and passive components is further reduced, resulting in a smaller silicon area. The A/D converter designed for this system is described in more detail in [P6].

[P6] A 12-bit Ratio-Independent Algorithmic A/D Converter for a Capacitive Sensor Interface

In this paper, the operation and the building blocks designed for the 12-bit ratio-independent algorithmic A/D converter in [P5] are described in more detail. The implemented ratio-independent architecture is insensitive to capacitance ratio, amplifier offset voltage, input parasitics, and flicker noise. For this paper, the A/D converter was measured stand-alone, making it possible to optimize the performance of the A/D converter. Hence, the performance of the A/D converter reported in this paper is somewhat better than that reported in [P5]. The A/D converter was implemented in a 0.13-μm CMOS. With 68.4-μW power dissipation and an active area of 0.041-mm^2, the A/D converter achieves 80.2-dB *SFDR* and 63.3-dB *SNDR*, making it very suitable for low-power sensor applications.

Chapter 5

Conclusions

Wireless sensors are convenient for environmental monitoring. While most people have their own personal mobile phones with them all the time, it is convenient to build sensor networks around them. This thesis concentrated on different kinds of solutions for these kinds of sensor applications. The factors common to all the designs in this thesis are low power dissipation and a small silicon area, both mandatory requirements for fully integrated sensor systems. This thesis demonstrates the functionality of these kinds of sensor networks and shows that they can be integrated using deep sub-micron CMOS processes to meet the cost requirements for mass consumer products.

In the first part of this thesis, wireless direct-conversion receivers for sensor applications are studied. It has been demonstrated that the power dissipation of the existing short-range radios, such as Bluetooth, can be dramatically reduced by optimizing both system and design aspects simultaneously. Deep sub-micron CMOS processes were used to integrate the whole system on a single chip. To be able to keep the manufacturing costs down, the minimum number of additional process options was made available. To meet these requirements, different all-MOS baseband solutions with extremely low power dissipation and a very small silicon area were designed.

The latter part of this thesis concentrates on low-power A/D converter designs for mobile and sensor applications. For mobile applications, the trend is to increase functionality and increase data rates. In order to meet these requirements, a low-pass $\Delta\Sigma$ modulator A/D converter for a mobile terminal GSM/WCDMA receiver using a very deep sub-micron CMOS process was implemented. While the technology scaling results in increased bandwidth and improved digital signal processing capabilities, the design of analog circuits becomes more difficult as a result of the reduced signal swing caused by a reduced supply voltage. The work in this thesis demonstrates that the increased bandwidth can be used to implement robust analog designs that meet the increased requirements.

In sensor systems, medium-resolution A/D converters with very low power dissipation and a small area are preferred. In this thesis, different kinds of algorithmic A/D converters were designed using a deep sub-micron process. In order to meet the strict area requirements, the number of operational amplifiers required was reduced in comparison to the existing solutions and new ways to perform capacitance ratio-independent multiply-by-two operation were designed. The A/D converters were integrated into a whole system to demonstrate the applicability of the designed structures to sensor systems.

It is very probable that in the near future, there will be a boom in different kinds of sensor systems. As for now, there already exist many types of wireless equipment suitable for sensor networks. As the functionalities of mobile terminals move toward interaction with the environment, it is expected that different sensor networks will emerge, with mobile terminals acting as a user interface to these networks.

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ISBN 978-951-22-9364-3
ISBN 978-951-22-9365-0 (PDF)
ISSN 1795-2239
ISSN 1795-4584 (PDF)