# Gate Driver Circuit for Silicon Carbide MOSFET-based Two-Switch Flyback

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Abstract of the master's thesis

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**Abstract**

In a continuously electrifying world, electric power conversion continues to have a significant impact on the overall electricity consumption, due to imperfections in the conversion process. Whether the electric energy needs to be converted for power transmission or charging up electronic devices, the field will remain relevant well into the remote future.

Additionally, semiconductor material improvements, for example from Silicon (Si) to Silicon Carbide (SiC), lead to more efficient and higher power density converter designs. The increased power density enables the development of next-generation power supplies, which can improve the process of electric power conversion even further. However, the new material possesses special characteristics, that must be considered during the design process.

In this master's thesis, a gate driver concept for a two-switch flyback converter equipped with SiC MOSFETs is proposed. The gate driver design is conducted in terms of the specific demands set by the SiC MOSFETs. The thesis consists of an extensive literature review, as well as circuit simulations performed with the LTSpice simulator. The entire design process is presented, starting from the working principle of the selected power converter topology, to the specification of the initial requirements set by Silicon Carbide material, and ending up to the simulation results.

The requirements induce three alternative circuit solutions during the design process, that are compared to each other during the simulations. Additionally, two different SiC MOSFET models are composed for further circuit evaluation.

The derived results evidence the functionality of the proposed concept, as well as identify the main problems of the design process, that have to be resolved. Two of the three solutions were found to contain genuine potential for further development.

**Keywords** DC-DC Conversion, Power Converter, Flyback, MOSFET, SiC, Silicon Carbide, Gate Driver, Switched-mode power supply

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Jatkuvasti sähköistyvässä maailmassa sähköenergian muuttaminen muodosta toiseen vaikuttaa merkittävästi sähkön kokonaiskulutukseen, sillä muutosprosessi sisältää aina häviöitä. Vaikka olisi kyse sähköenergian muuttamisesta sen siirtoa tai elektronisten laitteiden latausta varten, ala tulee pysymään relevanttina vielä kaukaiseen tulevaisuuteen.

Tämän lisäksi puolijohdemateriaalien kehittyminen esimerkiksi piistä (Si) piikarbidiin (SiC) johtaa yhä energiatehokkaampien ja tehotiheämpien muuttajien suunnitteluun. Kasvanut tehotiheys mahdollistaa uuden sukupolven muuttajien kehityksen, jolloin sähköenergian muutosprosessia pystytään parantamaan yhä enemmän. Uusi materiaali omaa kuitenkin erityispiirteitä, jotka täytyy ottaa huomioon suunnittelun aikana.

Tässä diplomityössä ehdotetaan ratkaisua kaksikytkimisen, epäsuoraan tehonsiirtoon perustuvan tasasähkömuuttajan hilaohjainpiirille, jossa muuttajan kytkiminä on käytetty piikarbidi-MOSFETteja. Hilaohjaimen suunnittelu on kauttaaltaan toteutettu piikarbidin tarkkojen vaatimusten mukaisesti. Diplomityö koostuu laajasta kirjallisuuskatsauksesta ja piirien simulaatioista, jotka on toteutettu LTSpice-työkalulla. Työssä esitetään suunnitteluprosessi kokonaisuudessaan alkaen tasasähkömuuttajan toimintaperiaatteesta jatkuen piikarbidin erityisvaatimuksiin ja lopuksi suunnitellun piirin simuloinnin tuloksiin.

Piikarbidin erityisvaatimusten vuoksi prosessissa syntyi kolme vaihtoehtoista ratkaisua, joita vertaillaan simulaatioiden jälkeen. Lisäksi simulaatioita varten rakennettiin kaksi erillistä piikarbidi-MOSFET-mallia, jotta niiden erilaiset ominaisuudet voitaisiin ottaa huomioon jokaisessa piiriratkaisussa.

Saadut tulokset todistavat ehdotetun piirin toiminnallisuuden samalla tunnistaen vakavimmat ongelmat suunnitteluprosessissa. Kahden kolmesta ratkaisusta havaittiin olevan niin lupaavia, että niissä on aitoa potentiaalia jatkokehitykselle.

**Avainsanat** Tasavirtamuutos, muuttaja, epäsuoraan tehonsiirtoon perustuva tasasähkömuuttaja, MOSFET, SiC, piikarbidi, hilaohjain, hakkuriteholähde

# Preface

I would like to thank my supervisor Professor Jorma Kyyrä as well as my advisor, Dr. Jari Leppäaho. Both of you have extremely hectic schedules, but somehow there was always time for my questions and problems during the thesis process. Moreover, I would like to thank ABB Drives for providing an interesting topic for the thesis and my mentor Kjell Ingman for giving me this opportunity and showing his support throughout the process. Also, I'm grateful for the efforts and guidance of Kalyan Gokhale. Finally, I would like to thank my family, as well as girlfriend Eliisa, and everyone else who supported me during this journey.

Helsinki, 22.5.2020

Joni-Markus Hietanen

# Contents

# Symbols and abbreviations

## Symbols

| | |
|---|---|
| $A_{Cu}$ | cross-sectional area of copper |
| $A_e$ | cross-sectional area of core |
| $A_w$ | cross-sectional area of winding |
| $B$ | magnetic flux density |
| $B_s$ | core saturation flux density |
| $b_c$ | width of transformer winding window |
| C | a capacitor |
| $\mathrm{C}_C$ | a coupling capacitor |
| $\mathrm{C}_t$ | a controller configuration capacitor |
| $C_{DS}$ | parasitic drain-source capacitance of MOSFET |
| $C_{GD}$ | parasitic gate-drain capacitance of MOSFET |
| $C_{GS}$ | parasitic gate-source capacitance of MOSFET |
| $C_{iss}$ | parasitic input capacitance of MOSFET |
| $C_{jo}$ | body diode junction capacitance |
| $C_{oss}$ | parasitic output capacitance of MOSFET |
| $C_{rss}$ | parasitic feedback capacitance of MOSFET |
| D | a diode |
| $\mathrm{D}_B$ | a MOSFET body diode |
| $\mathrm{D}_{fw}$ | a free-wheeling diode |
| $\mathrm{D}_n$ | diode $n$, various operations |
| $\mathrm{D}_{off}$ | a turn-off diode |
| $\mathrm{D}_S$ | a Schottky diode |
| $\mathrm{D}_Z$ | a Zener diode |
| $D$ | signal duty ratio |
| $D_{max}$ | maximum duty ratio |
| $D_{pri}$ | primary duty ratio |
| $D_{sec}$ | secondary duty ratio |
| **D** | drain of MOSFET |
| $d_w$ | total diameter of winding |
| $E$ | energy |
| $E_{drive}$ | driving energy loss |
| $E_{off}$ | turn-off energy losses |
| $E_{on}$ | turn-on energy losses |
| $E_m$ | magnetizing energy |
| $f_c$ | crossover frequency |
| $f_s$ | switching frequency |
| **G** | gate of MOSFET |
| $g_{fs}$ | MOSFET transconductance |
| $H$ | magnetic field intensity |
| $h_w$ | height of transformer core |
| $I_{ch}$ | MOSFET channel current |

| | |
|---|---|
| $I_D$ | diode current |
| $I_{DD}$ | channel current on steady-state |
| $I_{DS}$ | drain to source current |
| $I_G$ | gate current |
| $I_{GD}$ | gate to drain current |
| $I_{GS}$ | gate to source current |
| $I_L$ | current through inductor |
| $I_m$ | magnetizing current |
| $I_{out}$ | output current |
| $I_{pri}$ | current to transformer primary |
| $I_r$ | demagnetizing current through reset winding |
| $I_{sec}$ | current through transformer secondary |
| $I_{sw}$ | current through switch |
| $i_c$ | current control signal |
| $i_L$ | inductor current signal |
| $i_{ref}$ | reference current signal |
| $J$ | current density |
| $k_{Cu}$ | copper fill factor |
| L | an inductor |
| $\mathrm{L}_{load}$ | a load inductor |
| $\mathrm{L}_R$ | forward converter transformer reset winding |
| $L$ | inductance |
| $L_D$ | parasitic drain inductance of MOSFET |
| $L_G$ | parasitic gate inductance of MOSFET |
| $L_{leak}$ | leakage inductance |
| $L_m$ | transformer magnetizing inductance |
| $L_{m,crit}$ | critical magnetizing inductance at boundary of DCM and CCM |
| $L_S$ | parasitic source inductance of MOSFET |
| $L_{sec}$ | secondary inductance |
| $l_A$ | average length of winding |
| $l_e$ | length of magnetic path |
| $l_N$ | average length of a single winding turn |
| $l_w$ | length of the winding |
| $\mu_0$ | permeability of free space, $4\pi \cdot 10^{-7}$ H/m |
| $\mu_r$ | relative permeability of material |
| $\mathrm{N}_P$ | number of transformer primary turns |
| $\mathrm{N}_S$ | number of transformer secondary turns |
| npn | p-type semiconductor material doped with two n-type materials |
| $P_{ave}$ | average power requirement |
| $P_{cond}$ | conduction losses |
| $P_{core}$ | core losses |
| $P_D$ | power dissipation |
| $P_{off}$ | turn-off losses |
| $P_{on}$ | turn-on losses |
| $P_{sw}$ | switching losses |

| | |
|---|---|
| $P_{tot}$ | total losses for MOSFET |
| $P_w$ | winding losses per volume |
| $P_{w,tot}$ | total winding losses |
| pnp | n-type semiconductor material doped with two p-type materials |
| $p$ | number of interfaces between windings |
| $\phi$ | magnetic flux |
| Q | a switch (MOSFET) |
| $\mathrm{Q}_{CO}$ | PWM-controller enable MOSFET |
| $\mathrm{Q}_{GD}$ | gate drive circuits main MOSFET |
| $\mathrm{Q}_n$ | MOSFET $n$, various operations |
| $\mathrm{Q}_{UV}$ | voltage cut-off MOSFET |
| $Q$ | SR-latch ouput signal |
| $Q_G$ | gate charge |
| $\overline{Q}$ | inverse of SR-latch output signal |
| $\mathrm{R}_B$ | BJTs base resistor |
| $\mathrm{R}_{BS}$ | base to source bypass resistor |
| $\mathrm{R}_C$ | damping resistor |
| $\mathrm{R}_G$ | MOSFETs gate resistor |
| $\mathrm{R}_{GS}$ | gate to source resistor |
| $\mathrm{R}_{load}$ | a load resistor |
| $\mathrm{R}_S$ | a series resistor |
| $\mathrm{R}_{sense}$ | a current sensing resistor |
| $\mathrm{R}_t$ | a controller configuration resistor |
| $R_A$ | MOSFET accumulation region resistance |
| $R_b$ | body diode ohmic resistance |
| $R_{ch}$ | MOSFET channel resistance |
| $R_D$ | MOSFET drift region resistance |
| $R_d$ | MOSFET drain resistance |
| $R_{DS(on)}$ | MOSFET channel on-resistance |
| $R_G$ | MOSFET gate resistance |
| $R_{GS}$ | gate to source resistance (MOSFET) |
| $R_{G(off)}$ | MOSFET turn-off gate resistance |
| $R_{G(on)}$ | MOSFET turn-on gate resistance |
| $R_{jfet}$ | MOSFET parasitic JFET region resistance |
| $R_S$ | MOSFET source resistance |
| $R_{subs}$ | MOSFET substrate resistance |
| $\rho_{Cu}$ | electrical resistivity of copper, $1.72{\cdot}10^{-8}\Omega$m |
| **S** | source of MOSFET |
| T | a switch (BJT) |
| $\mathrm{T}_n$ | BJT $n$, various operation |
| $T_S$ | signal period |
| $t$ | an arbitrary time instant |
| $t_d$ | controller oscillator discharge time |
| $t_n$ | time instant $n$ |
| $t_{off}$ | signal off-time |

| | |
|---|---|
| $t_{on}$ | signal on-time |
| $t_p$ | signal dead time |
| $t_r$ | controller oscillator rise time |
| $t_{tr}$ | transition time |
| $t_{tr,max}$ | maximum transition time |
| $\tau$ | integration variable |
| $\tau_{iss}$ | parasitic input RC time constant |
| $V_C$ | voltage over coupling capacitor |
| $V_{CC}$ | operating voltage |
| $V_{Cu}$ | copper volume |
| $V_{DC}$ | DC-voltage |
| $V_{DS}$ | drain-source voltage |
| $V_{EE}$ | negative gate voltage |
| $V_{FB}$ | scaled feedback voltage for controller |
| $V_{GG}$ | positive gate voltage |
| $V_{GS}$ | gate-source voltage |
| $V_{in}$ | input voltage |
| $V_{out}$ | output voltage |
| $V_P$ | transformer primary voltage |
| $V_{ref}$ | reference voltage |
| $V_S$ | transformer secondary voltage |
| $V_{th}$ | MOSFET threshold voltage |
| $V_w$ | winding volume |
| $V_Z$ | Zener voltage |
| $v_c$ | voltage control signal |
| $v_{err}$ | error voltage signal |

## Operators

| | |
|---|---|
| $X(0)$ | value of quantity $X$ at time instant 0 |
| $X(t)$ | value of quantity $X$ at time instant $t$ |
| $\hat{X}$ | peak value of quantity $X$ |
| $X_{RMS}$ | RMS-value of quantity $X$ |
| $\sum_{i=1}^{n}$ | summation from index 1 $n$ times |
| $\Delta$ | change in a quantity over time, $\frac{d}{dt}$ |
| $\frac{\mathrm{d}}{\mathrm{d}t}$ | derivative with respect to variable $t$ |
| $\int_a^b f(x)dx$ | definite integral of function $f(x)$ for variable $x$ between values $a$ and $b$ |
| $\int_V f(x)dV$ | volume integral of function $f(x)$ |

## Abbreviations

| | |
|---|---|
| ABB | Asea Brown Boveri |
| AC | Alternating Current |
| BJT | Bipolar Junction Transistor |
| BTI | Bias Temperature Instability |
| CCM | Continuous Conduction Mode |
| DC | Direct Current |
| DCM | Discontinuous Conduction Mode |
| EMC | Electromagnetic Compatibility |
| EMI | Electromagnetic Interference |
| IGBT | Insulated-Gate Bipolar Transistor |
| I-V | Current-Voltage |
| LC | Inductor-Capacitor |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| PCB | Printed Circuit Board |
| PWM | Pulse Width Modulation |
| RC | Resistor-Capacitor |
| RMS | Root-Mean-Square |
| Si | Silicon |
| SiC | Silicon Carbide |
| SR | Set-Reset |
| TO | Transistor Outline |
| UVLO | Undervoltage-Lockout |
| VDMOS | Vertical Diffused Metal-Oxide-Semiconductor |
| ZVS | Zero-Voltage Switching |

# 1 Introduction

The use of electricity for everyday operations, such as charging laptops and smartphones, is often taken for granted; on the other hand, the principle of converting the electricity for such mundane uses is not fully understood by consumers. This act of transforming electrical energy into a different form is commonly known as electronic power conversion. By definition, electronic power conversion refers to transforming one or more characteristics of an electric power system, essentially with minimal power losses. Conversion can be used to change the parameters of electric power, such as voltage, number of phases, or frequency [1].

Electronic power conversion is worthwhile during whole lifespan of electricity, as different forms of electrical energy possess different advantages. For example, high voltage alternating current (AC) has desirable attributes towards energy transmission over a vast distance [2]. On the other hand, small electronic devices, components, or batteries require a low voltage direct current (DC) supply to function properly [3]. Therefore, various kinds of power converters are a part of everyday lives in the obvious forms of electronics chargers, or more discreetly integrated into other electronic devices, appliances, elevators, and electric switchboards in residential buildings. Hence, the characteristics of power converters also have a high impact on overall electric energy consumption.

Switched-mode power supplies are widely used for power conversion due to their inherent low loss operating principle. There are multiple different switched-mode power supply topologies, which can be used for different purposes. The flyback converter topology is commonly used for low power DC-DC conversion applications, as it is straightforward to design and operate [4]. Common flyback converters feature just one switching component but adding a second one enables higher voltage ratings and simplifies parts of the converter [5]. This topology is known as a two-switch flyback converter and is considered in this thesis.

A common choice for the switching component used in the flyback is a Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET). Its advantages include voltage control, stable state preservation, and short switching times, justifying it as a prime candidate for power converters [5].

The traditional semiconductor material used for component manufacturing in MOSFETs is silicon (Si), which has served the purpose for multiple decades [6].However, as Si-based power devices are limited by their internal resistive characteristics, in order to reach higher voltage and current ratings, some alternative materials must be considered. Within the last decade, such an alternative in the form of a silicon carbide (SiC) MOSFET has been introduced to power device markets. The material itself is not a new invention, but its utilization as a chip material for switching components had previously not been widely implemented. Common benefits of SiC-based MOSFETs include a wide bandgap and reduced internal resistances resulting in benefits, such as faster switching, lower losses, and operating capabilities at higher voltages and higher ambient temperatures [7], [8].

However, the new material is not without its limitations. In the power converters, the switching components need to be turned completely on or off. Compared to their

Si-counterparts, SiC MOSFETs require a higher control voltage for turning on in order to minimize conduction losses [9]. They also require lower control voltage for turning them off to prevent them from accidentally entering a conductive state. This is caused by SiC MOSFETs possessing a lower threshold voltage than Si-devices, meaning that they start to conduct at rather low gate voltages [9]. Moreover, as device temperatures increase, the threshold voltage tends to decrease aggravating the situation even further [10], [11]. Therefore, to prevent unwanted conduction of the switch, they are usually turned off with a negative control voltage to ensure correct functionality.

The switches require a controller to operate them and the entity of this control circuit is called a gate driver. The traditional gate driver circuits are only applicable to traditional Si-MOSFETs and do not account for the specific requirements of SiC. This is especially amplified in converter topologies containing multiple switches as in a two-switch flyback. Therefore, identifying common gate driver building blocks and designing a new concept for fulfilling these rigorous needs are necessary.

The importance of a properly functional gate drive circuit should not be underestimated, as it directly affects the entire power converter operation [12]. The circuit additionally affects converter efficiency as well as safe operation boundaries. Poorly constructed gate drivers may lead to converter or component failures, such as a high-power short circuit or temperature runaway.

Therefore, this thesis designs a gate drive circuit to answer the demands of SiC MOSFETs by composing alternative circuit solutions, while maintaining a safe and desirable converter operation. The methodology used to fulfill the objective of this thesis includes an extensive literature review and an implementation part, consisting of circuit simulations. The simulations are carried out for two different switching components, and alternative circuit solutions. Finally, general functionality, as well as the advantages and disadvantages of each solution are evaluated.

The rest of the thesis is structured in the following manner. Chapter 2 depicts the fundamental structure, working principle, and general characteristics of a flyback converter. The basics of a power MOSFET is described in Chapter 3, as well as the used materials, defined. In addition, it justifies the use of SiC over Si in the MOSFETs utilized in the power converter, due to differences in their material properties. Chapter 4 presents the general characteristics of gate drive circuits. Additionally, it portrays some example circuits and their building blocks that can be found in the literature. Furthermore, a proposed gate drive concept is presented. The specific design process of the concept is introduced in Chapter 5 by defining all the building blocks used for the converter operation. It also depicts the different solutions, and simulation parameters. Chapter 6 demonstrates results for the simulations, their evaluation criteria, as well as achieved differences between proposed solutions. Finally, the conclusions for the obtained results are discussed in the final chapter, Chapter 7.

# 2 Flyback Converter

In this chapter, the electrical structure of a flyback converter is introduced, its working principle derived and some of its potential limitations are considered.

## 2.1 Structure

A flyback converter is a DC-DC type converter, which is derived from a Buck-Boost converter (Figure 1a). The main difference between the two topologies is, that flyback includes a transformer instead of a single inductor, enabling galvanic isolation between the inputs and outputs (Figure 1b) [5]. Transformer coils are coupled mutually and oriented in a way, that at the instant of switch turn-off, the current is transferred to secondary side of the transformer to reset the core flux [4].

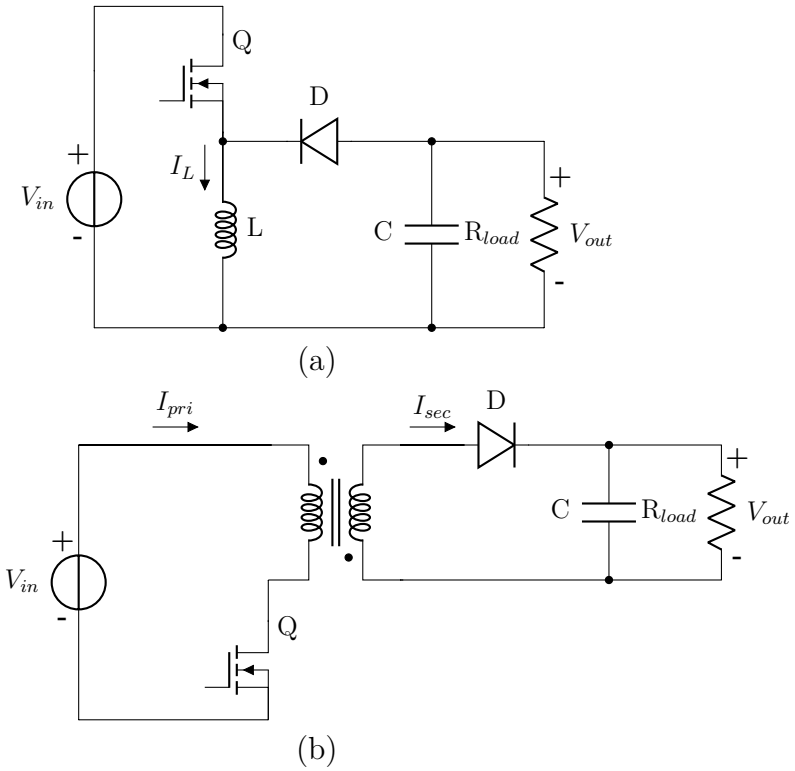


Figure 1: Generic (a) Buck-Boost and (b) Flyback converter schematics.

One advantage of a flyback topology is, that it allows the use of multiple outputs very easily and at a low cost [13]. This is due to the relatively simple secondary circuit, which does not include any additional energy-storage inductors as some other converter types do. However, depending on the nature and number of outputs, cross-regulation between outputs may cause some challenges, since load variation for one output affects others as well. Light load conditions are especially problematic in terms of cross-regulation [13].

## 2.2 Working Principle

The power supply is controlled via switch Q. When the gate control signal of the switch is at high-state, the switch is at on-state and conducts. Similarly, when the gate control signal is at low-state, the switch is not conducting and therefore on off-state. During on-state, current flows through the primary winding and switch. The primary current generates a magnetic flux to transformer core, the value of which at time instant $t$ corresponds to Equation (1). Winding orientation causes the secondary diode D to be reverse biased during this time, so no current flows through the secondary winding during this stage (Figure 2a). After switch turn-off, energy stored in the magnetic field is released to the secondary side and current starts to flow through the secondary winding (Figure 2b). After switch Q changes its state again, output current $i_{out}$ (corresponding to Figure 2a) continues to flow as it is maintained by energy stored in capacitor C [4], [5].

$$\phi(t) = \phi(0) + \frac{1}{\mathrm{N}_P} \int_0^t V_{in}(\tau) d\tau \tag{1}$$

where $\phi(0)$ is the flux at $t = 0$, $\mathrm{N}_P$ number of primary turns and $\tau$ an integration variable.

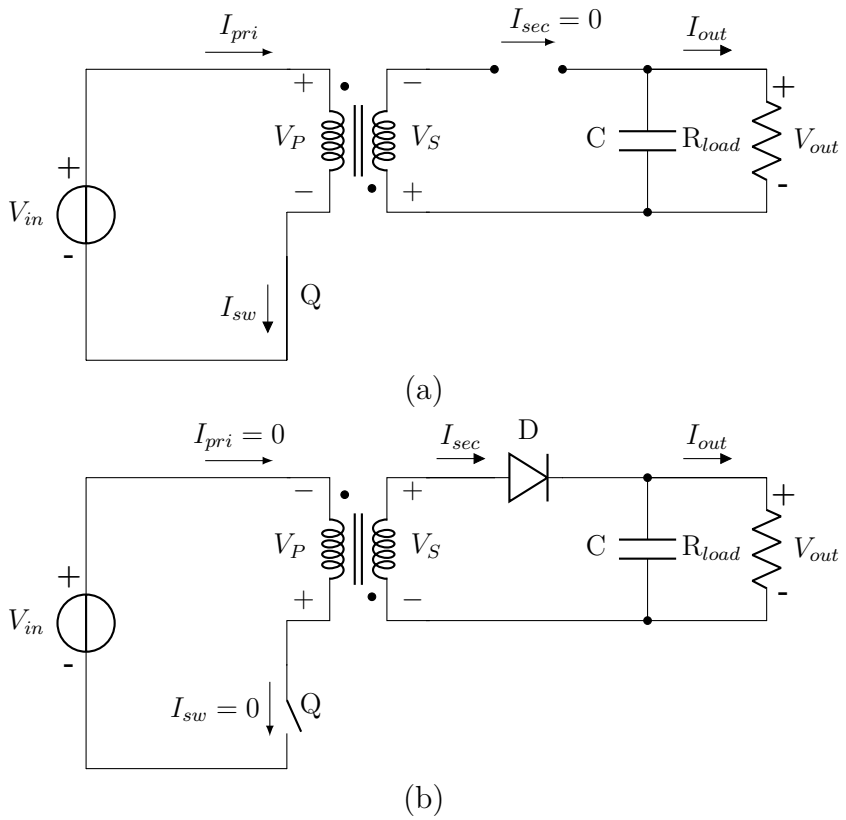


Figure 2: Flyback converter circuit states as switch Q is (a) On (b) Off.

Desired output voltage $V_{out}$ can be reached by modulating the pulse width of the gate driver signal. Longer pulse width corresponds to a higher output voltage, but

depending on the application and operation mode, maximum pulse width, and general pulse width modulation (PWM) control technique must be determined beforehand [4], [5]. Pulse width is presented with a duty ratio $D$, which is defined as a fraction of control signal high-state duration to signal switching period $T_S$. The switching period is inverse of used switching frequency $\frac{1}{f_s}$.

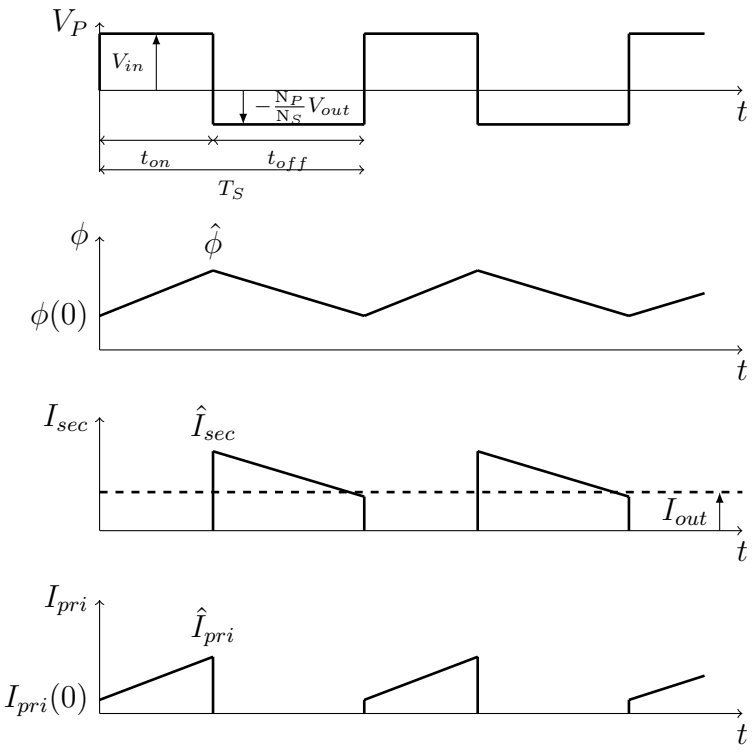


Figure 3: Primary voltage, core flux, secondary and primary current waveforms during CCM.

The power supply may operate either on continuous (CCM) or discontinuous conduction mode (DCM) [5]. On CCM, the transformer core is incompletely demagnetized during each switch-off, and there are no pauses in power flow (Figure 3). On DCM, the transformer core is completely demagnetized at the end of each operation cycle, and power flow to transformer secondary is momentarily terminated (Figure 4). The slope of primary and secondary current waveform depends from transformer primary and secondary inductances as well as input and output voltages, due to inductor characteristics (Equation (2)). The boundary between these two operating modes is defined by the value of transformer magnetizing inductance (Equation (3)) [14].

$$v(t) = L\frac{di}{dt} \tag{2}$$

$$L_{m,crit} = \frac{(1-D)^2 R_{load}}{2f_s}\left(\frac{N_P}{N_S}\right)^2 \tag{3}$$

For CCM, $t_{on}$ states the duration of on-state of the gate signal and therefore the duty ratio can be written as $D = t_{on}/T_S$ for CCM operation. On DCM however, there is a secondary duty ratio to be determined, which indicates the core demagnetization time. Primary duty ratio for DCM is determined according to previous case $D_{pri} = t_{on}/T_S$ and secondary corresponding to low voltage period $D_{sec} = t_{off}/T_S$. During the remaining time period $t_p$, core flux is at zero and no current flows through the primary or secondary winding. Value of $t_p$ can be written as $t_p = (1 - D_{pri} - D_{sec})T_S$ [15]. Voltage transfer ratio is determined between input and output voltages. For CCM applies:

$$\frac{V_{out}}{V_{in}} = \frac{\mathrm{N}_S}{\mathrm{N}_P}\frac{D}{1-D} \tag{4}$$

And for DCM:

$$\frac{V_{out}}{V_{in}} = \frac{\mathrm{N}_S}{\mathrm{N}_P}\frac{D_{pri}}{D_{sec}} \tag{5}$$

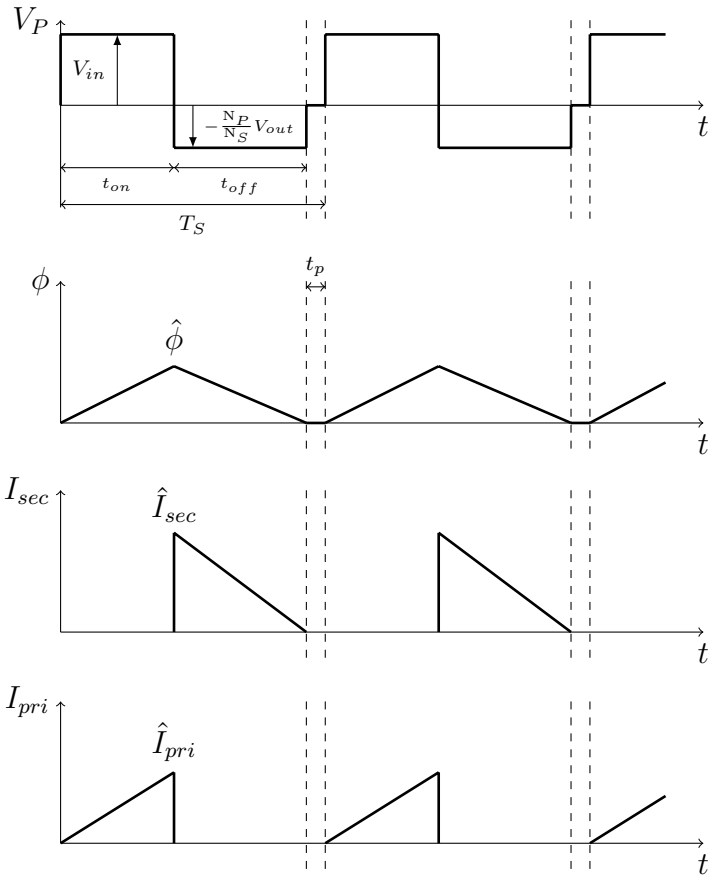


Figure 4: Primary voltage, core flux, secondary and primary current waveforms during DCM.

The selection of operating mode depends on the application. CCM has been determined to be more efficient [14], but DCM has other advantages, for example enabling the use of smaller and less expensive transformers. As long as the selection of operating mode has been done in advance and power supply functions on that operation mode all the time, the functionality of power supply remains predictable with known characteristics. For the power supply discussed in the thesis, the selected operating mode is DCM due to specific voltage and current feedback loop requirements.

## 2.3 Two-Switch Topology

Power supply topology selected for the thesis is a flyback converter, but instead of one switch, a two-switch topology is used (Figure 5). One of the main advantages of this topology is, that since the switches are connected in series, their voltage rating can be lower than the single component case. This helps by dividing the total power dissipation over two components instead of one [5], therefore enabling the use of components with a lower voltage rating, which are often cheaper.

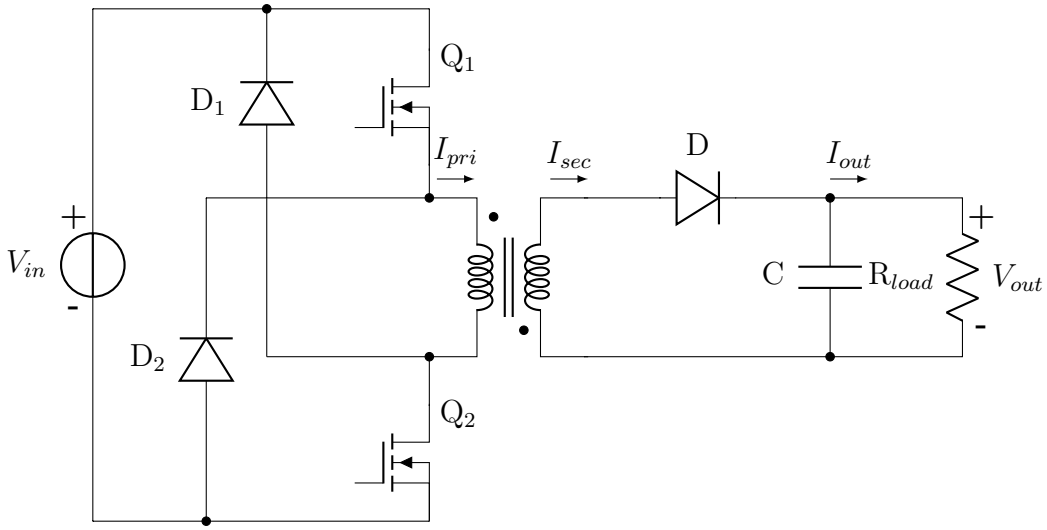


Figure 5: General two-switch flyback converter.

In a typical single-switch flyback design, the switch suffers a high voltage stress during its turn-off period, which increases the switching losses significantly. The voltage consists of direct voltage stress from the input voltage, reflected voltage from transformer secondary, and a high amplitude voltage spike from the turn-off transient. Therefore, a higher component voltage rating must be used to withstand this condition, usually corresponding to higher on-resistance and therefore decreased component current rating, due to increased conduction losses. The transient voltage stress during turn-off is caused by a resonance circuit formed by the transformer leakage inductance and switch output stray capacitance [16]. The effects of the condition can be reduced by implementing the two-switch topology.

In order to get rid of the high transient voltage stress on a two-switch design, some components have to be added to the design. Diodes $D_1$ and $D_2$ are clamping

diodes, which provide a path for transformer leakage energy to return to the input energy source and therefore limit the maximum value of transient voltage. With this configuration, maximum switch voltage stress equals the input voltage $V_{in}$ [16].

Other potential benefits of using a two-switch design include increased efficiency, since the clamping diodes circulate the leakage energy back to input energy source, instead of dissipating it in a snubber circuit as in conventional single-switch flyback designs. Also, the design enables a higher power output level compared to the conventional topology [17].

The working principle of two-switch design is similar to conventional flyback and presented waveforms apply for the two-switch design as well. Both switches $Q_1$ and $Q_2$ are turned on or off simultaneously with uniform, yet isolated gate signals. However, there are some specific demands considering these signals and their characteristics, which will be discussed later.

## 2.4 Limitations

Generally, the conventional flyback topology is a cost-effective topology with low parts count and already widely utilized in industry. Galvanic isolation and simplicity make it a common power supply for low-power applications [14], [16]. The main limitations of the topology include the previously mentioned turn-off voltage stress, relatively high losses, and low output power, all of which can be improved by implementing the two-switch design instead of conventional topology [17]. However, this leads to a fundamentally more complicated design, and the floating gate on the upper switch causes driver complexity to increase [18].

It is notable, that in a two-switch design, overall voltage stress is not always divided equally over both switches. An imbalance may be caused by a delay between upper and lower switch gate signals [19], [20], or nonidentical components [21]. In the case of two-switch flyback topology, a delay is more often found on floating upper switches gate, of course depending on gate driver circuitry. One option to solve this issue is to delay the lower switch signal with a capacitor or a gate resistor accordingly, to achieve coherent switching.

Another cause of imbalance is differences in parasitic parameters of series-connected switches. In this case, two switches are serially connected to each other through the transformer's primary inductor. Even though the parasitic parameters are usually available on devices datasheets, in practice they are never exactly alike. Parameters vary according to device structures, material properties, and manufacturing processes. Dispersion of device attributes has an effect on device switching characteristics and is therefore able to cause voltage imbalances. Different solutions for voltage balancing include RC-snubbers, analog gate drive circuits with magnetic coupling or diodes, and digital balancing solutions [21].

## 2.5 Converter Feedback Control

Typically, a closed-loop design is implemented to operate a power converter in a controlled manner. Closing the loop refers to adding a feedback signal from power output back to the controller, which affects the real-time controller functionality. Fundamentally, voltage or current mode control is utilized to regulate the output voltage and inductor current to desired values. Control consists of feedback loops monitoring these quantities and adjusting the pulse width of PWM-control accordingly [4], [22]. In this section, their general functionality is presented, without going too much into details of control theory. The chosen control mode for this application is current mode control.

### 2.5.1 Voltage Mode Control

On voltage mode control, the output voltage of the power converter is constantly measured and fed back to the control circuit. The measured output voltage is first scaled down and then fed to an error amplifier in the controller circuit, where feedback value is compared to a reference voltage $V_{ref}$. The reference voltage is a constant value, which is often internally defined within the controller circuit and found on the component datasheet. After this comparison, the difference between measured and reference voltages $v_{err}$ is transformed into a control signal $v_c$ within the controller. The control signal defines the required changes in the duty cycle $D$, which is adjusted within the pulse-width-modulator to minimize the error between the reference and measured feedback signals. Then, the gate signal $V_{GS}$ with a new duty cycle is fed to power stage and load, in this case to gate drive circuitry and power converter [4], [22].

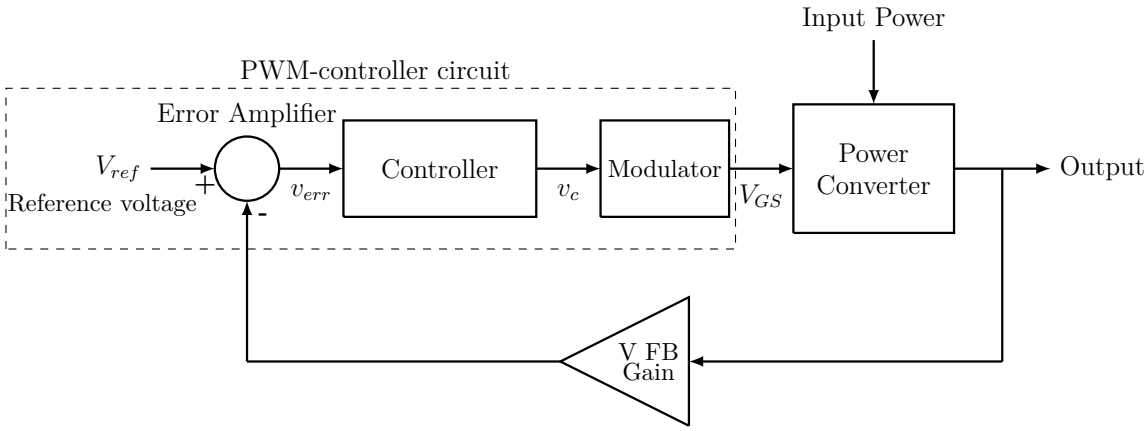


Figure 6: Typical voltage mode control block diagram.

The control loop has a transfer function, which is the relation between output and input signals. It is commonly used to evaluate the robustness of the feedback system via phase and gain margins, which are measures of stability and sensitivity to parameter variation, respectively. These measures are generally determined using Bode plots of transfer functions, which present the frequency response of transfer

functions. Frequency responses depict magnitude, or gain, of feedbacks transfer function alongside its phase angle. Quantities are plotted on a logarithmic scale as a function of frequency, key-value of which is the frequency where feedback system gain equals zero, the crossover frequency $f_c$ [4], [22].

From Bode plots, the phase margin is graphically interpreted at point of crossover frequency. By definition, it is the margin between the value of the phase angle at the crossover frequency, and phase angle of -180°. As previously stated, the amount of phase margin is the measure of system stability. Rule of thumb for adequate phase margin to ensure feedback loop stability is 60°, but depending on the source it may also be less, for example 50° [23]. Similarly to the phase margin, gain margin is also graphically defined from frequency response. It can be measured from loop gain magnitude at the point, where the phase angle exceeds -180°. Generally, a 10 dB margin is found to be satisfactory to prevent major oscillations due to parameter changes. Figure 7 depicts an arbitrary Bode plot, where the definitions of phase and gain margin are graphically presented [4], [22].

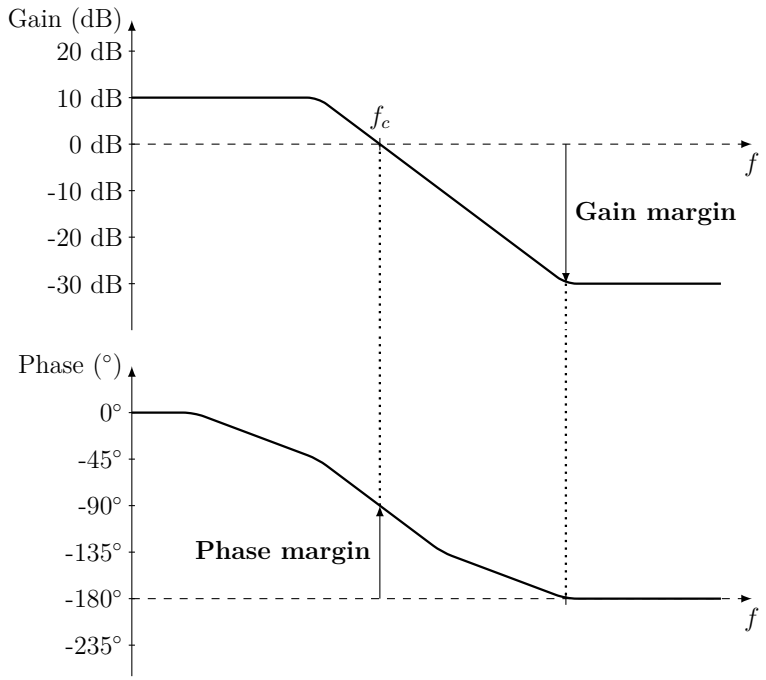


Figure 7: Generic Bode plot defining phase and gain margins.

On a practical two-switch flyback, voltage feedback is measured from the load output of which voltage is to be controlled. The desired output voltage is then scaled to be equal with internal voltage reference of the controller circuit using, for example, a simple voltage divider, and fed to an error amplifier. With an isolated converter topology, there may also be a requirement to isolate the feedback signal.

### 2.5.2 Current Mode Control

Current mode control is often used as an inner feedback loop for voltage mode control described in the previous section. Typically, the inner loop measures inductor current

and outer signal resembles conventional voltage feedback and is utilized as a reference value for peak current allowed to flow through an inductor. More specifically, there are two types of current-mode control techniques: average-current mode control and peak-current mode control, the latter of which functions as previously specified. It is also more commonly used [4], [24].

In peak-current mode control, the controller sets the peak current value from the voltage feedback loop as a form of control signal $i_c$. The control signal is then modified with an external slope compensation signal, the purpose of which is to damp sub-harmonic frequency oscillation. These two signals form a reference signal $i_{ref}$, which is fed to pulse-width-modulator alongside the measured inductor current $i_L$ from the inner feedback loop. The waveform of the inductor current resembles an ascending ramp, and it is used within the modulator to determine a new duty cycle for gate signal $V_{GS}$, by cutting off the output when reference signal $i_{ref}$ and measured signal $i_L$ are equal. Therefore, the maximum current set by voltage feedback is never exceeded, as high-state of gate pulse is cut-off when the peak-current value is reached [4].

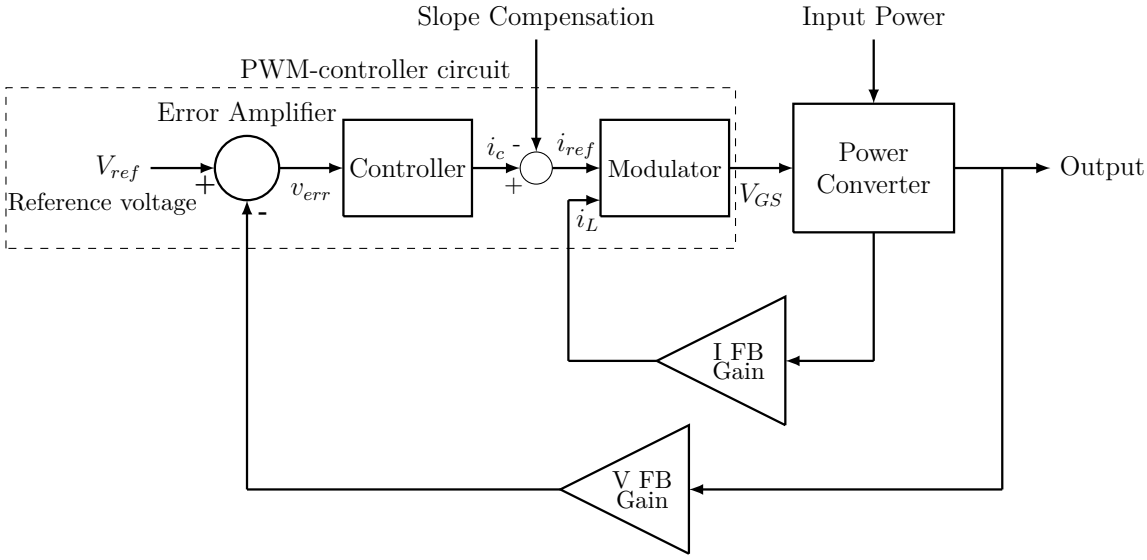


Figure 8: Typical current mode control block diagram.

In the chosen application, the inductor current is monitored via a sensing resistor between lower MOSFET and circuit ground potential. As voltage over a sensing resistor is measured, the result can be easily transposed to current, which can be fed back to the modulator and compared to a reference signal. In general, current-mode control has multiple benefits, which include cycle-by-cycle current limiting capabilities, current sharing with multiple power modules, as well as simpler control dynamics or transfer functions, and therefore less complicated control design [4], [24].

# 3 Silicon Carbide MOSFET

Power MOSFET is a popular component to be utilized as a switch in power converters due to its high switching frequency capabilities. Conventionally, the main manufacturing material is silicon (Si), but new materials have been constantly under investigation. As Si-based power devices are approaching their physical performance limitations, fresh alternatives such as silicon carbide (SiC) have been introduced to power device markets. The essential benefits of SiC-based power devices include a wide bandgap and low on-resistance, and their development makes faster device operation in higher temperatures and voltages a reality.

Lower on-resistance per unit area leads to smaller chip size, which decreases parasitic capacitances while increasing switching speed capabilities. These attributes correspond to lower switching and conduction losses for the device and enable the evolution of power electronic converters towards higher power density and improved efficiency [8]. In addition, SiC-technology makes it possible to develop components with significantly higher voltage ratings compared to the conventional Si-material, thus having a clear focus on 1200V and 1700V rated components. Therefore, SiC MOSFETs mainly compete against Si Insulated-Gate Bipolar Transistors (IGBTs) in applications requiring high voltage ratings, rather than competing against Si MOSFET equivalents. However, since MOSFETs enable the use of higher switching frequency, they widen the application range for this power device.

In this chapter, the structure and working principle of a SiC-based power MOSFET are examined. Moreover, some of its special characteristics or limitations while being incorporated as a switch in a two-switch flyback converter are addressed.

## 3.1 Structure

The structure of SiC MOSFET resembles its Si counterpart. Power MOSFETs are usually packaged discretely, referring to a device containing only one semiconductor chip. The most common packaging types for this purpose are standardized transistor outline (TO) packages: TO-220 and TO-247. Packaging must be able to conduct load current and control signals, dissipate the required amount of heat, and protect the device from environmental conditions and influences [11].

Manufacturing of a discrete switch for previously mentioned package types is carried out by soldering a Si or SiC chip directly to a copper base, which serves as a mounting surface and forms the die of the device. It is notable, that using this technique does not provide any electrical insulation, but keeps the base material revealed. Switches leads, or legs, are then housed and fixed to package using a transfer mould. One lead is connected directly to the device base, others to load and control contact areas within the package, thus forming the gate, source, and drain connectors of the transistor. These leads can be directly attached to a printed circuit board (PCB) and exposed copper base to a heat sink [11]. Packaging is somewhat crucial for semiconductor devices, since it defines the parasitic properties of a device and therefore its switching characteristics and losses.

Common die structure for a power MOSFET is Vertical Diffused MOS (VDMOS),

also known as the planar structure. The name originates from vertical current flow through the semiconductor structure and manufacturing process called diffusion [25]. This technique generates cells consisting of p-wells and diffused $n^+$ areas on the surface of the semiconductor, enabling the functionality of the device channel [11]. Another common MOSFET type is a U-MOSFET structure, which is also known as the trench-gate structure. It differs from its vertical diffused counterpart by its gate structure, which is embedded through $n^+$ and p-regions into the drift region [6]. Their common cross-sectional structures are presented in Figure 9.

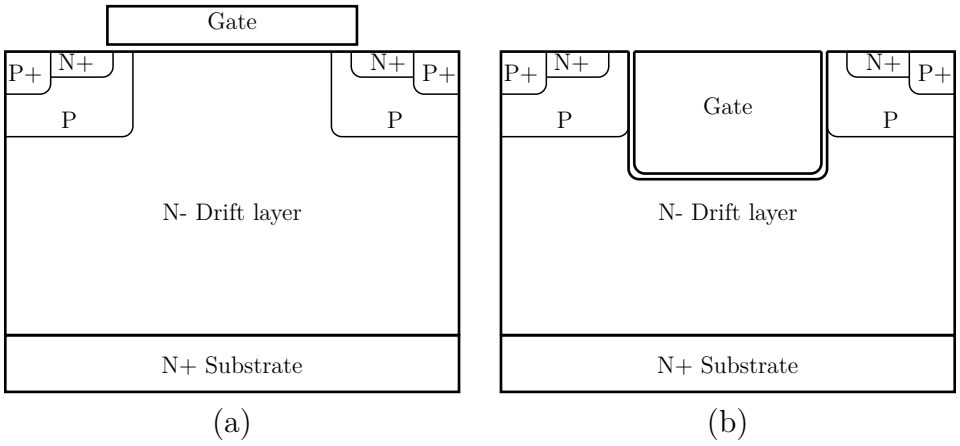


Figure 9: Typical SiC MOSFET structures (a) planar and (b) trench.

The essential difference between planar and trench structures is the amount of on-resistance during forward conduction. Structures include different current flow paths and therefore different resistances, which will be discussed in the next subsection [7].

## 3.2 Working Principle

### 3.2.1 On-state

While the power MOSFET is at its on-state, its gate is excited with positive voltage and allows current to flow between drain and source of the device. This forms a channel between drain and source, which is activated by gate voltage induced electric field within the device structure. Physically, the channel can be referred to be located on p-wells between surface $n^+$ areas and N- drift layer. This is the case on n-channel type MOSFET, which is a commonly preferred device type in the industry due to normally off feature. Also, the n-channel type is more advantageous due to electrons having superior mobility over holes in p-channel type [11]. Current flow is not lossless through a channel as the device contains on-resistance $R_{DS(on)}$ due to imperfect semiconductor materials. The value of on-resistance defines the device conduction losses [7].

On-resistance is formed differently for planar- and trench type MOSFETs, due to their structural differences. The path of current flow is different for the two, and therefore resistive components are determined differently. Details are further

discussed in [7], but main resistive regions are presented in Figure 10, where $R_{ch}$ refers to MOSFET channel resistance, $R_A$ to accumulation region resistance, $R_D$ to drift region resistance, $R_{jfet}$ to parasitically formed JFET region resistance and $R_{subs}$ to substrate resistance [26]. Total on-state resistance for planar type MOSFET can be calculated as:

$$R_{DS(on)} = R_{ch} + R_A + R_{jfet} + R_D + R_{subs} \tag{6}$$

And correspondingly for trench:

$$R_{DS(on)} = R_{ch} + R_D + R_{subs} \tag{7}$$

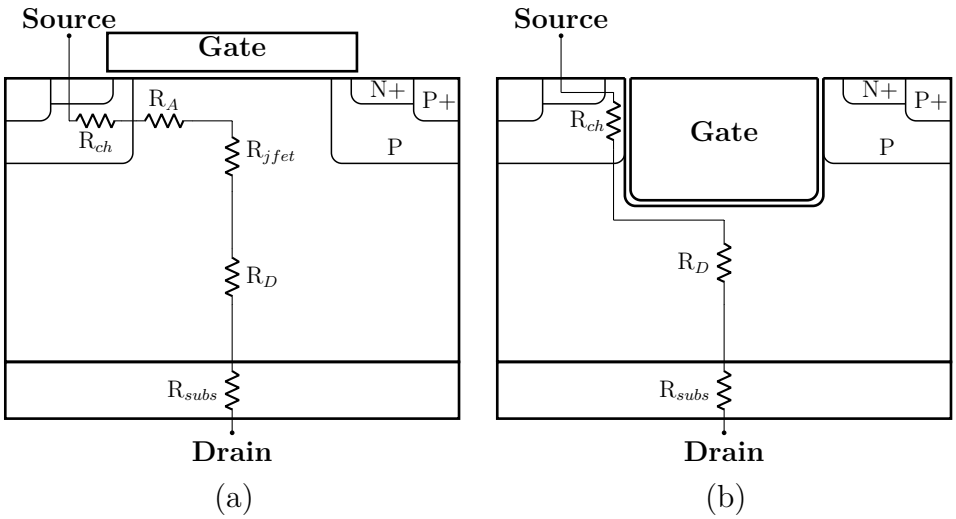


Figure 10: On-resistance components for (a) planar and (b) trench structure.

### 3.2.2 Turn-on and Turn-off

To study the switching characteristics of a power MOSFET, their defining parasitic attributes must be known. The effect of the parasitic attributes is emphasized in the performance of SiC-based devices compared to Si-based, due to potentially faster operation speed [27].

Parasitic capacitances are generated by physical structures inside the power device. As electric conductors with different potentials are located in proximity to each other, electric fields cause charges between them, thus forming undesired capacitance. These capacitances are modelled as capacitors between device terminals, including a gate to source capacitance $C_{GS}$, drain to source capacitance $C_{DS}$ and gate to drain capacitance $C_{GD}$, which is also referred as Miller capacitance [28] (Figure 11). These capacitances comprehensively define the switching characteristics of a power MOSFET. The specific effect of each attribute will be discussed further while analysing the switching waveforms [6], [25].

Parasitic inductances also affect switching transients, either on their own or combined with parasitic capacitances. Inductances originate from internal electric conductors within the device structure and are commonly divided into the parasitic gate, drain and source inductances according to device terminals (Figure 11).

Parasitic inductances can be similarly modelled as components, and they have different contributions towards switching transients. Gate inductance $L_G$ resonates with input capacitors causing oscillation on $V_{GS}$ and is therefore recommended to be minimized by placing it right next to the gate driver circuit. The influence of this parameter is generally limited, but it may cause spurious operation of the device. Drain inductance $L_D$ resonates with output capacitance, causing the oscillation to be coupled to $C_{GD}$. This increases ringing on the gate and drain voltages as well as channel current. However, the parameter has only a minor effect. The most significant component towards switching transients is source inductance $L_S$. As channel current changes during switching, the voltage over $L_S$ opposes the gate voltage simultaneously slowing down the current changes. Additionally, source inductance can be increased to limit oscillation of $V_{DS}$, but this increases switching losses due to lower current slew rate [29].

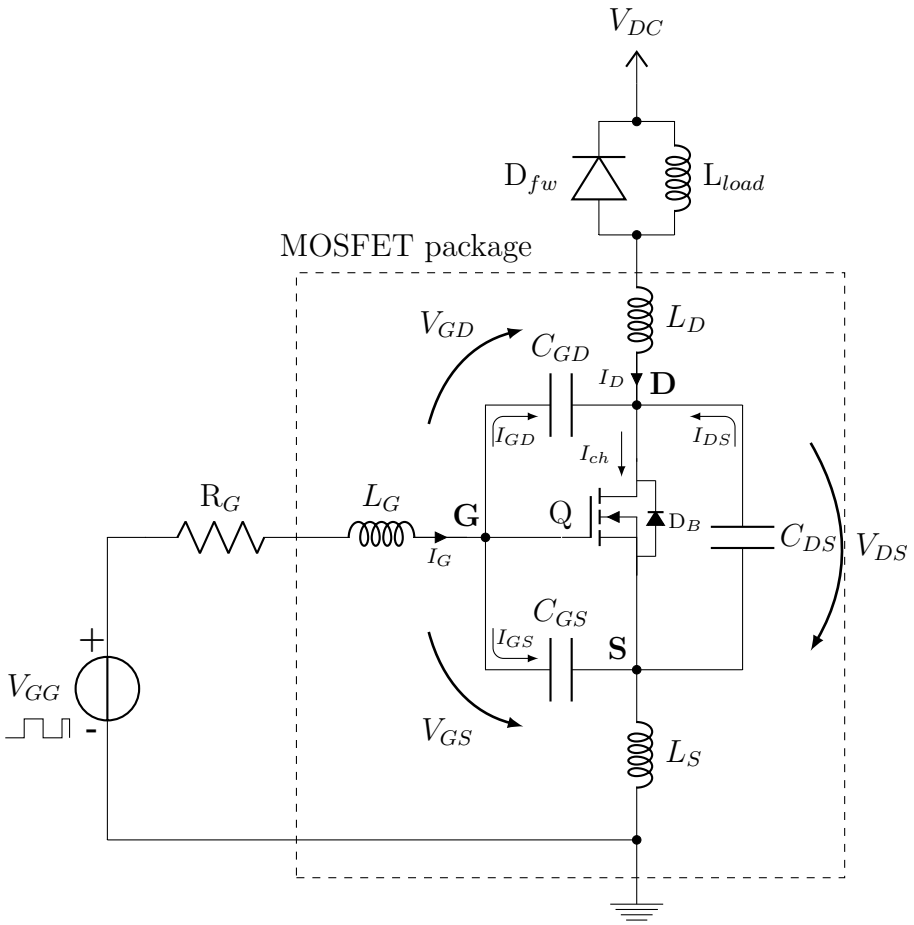


Figure 11: Double-pulse test circuit with inductive load. Parasitic inductances and capacitances are added within MOSFET packaging.

For determining parasitic components of a power MOSFET, a double-pulse circuit (Figure 11) can be used. It is carefully designed for the sole purpose of minimizing circuit parasitics, for reflecting device switching behaviour as authentically as possible [30]. Within the circuit, inductor $L_{load}$ functions as a load, and diode provides the current a path to flow when the MOSFET channel is not conducting. This type of test circuit was utilized in multiple sources i.e. [30]–[35] for defining the characteristics of a power MOSFET.

Parasitic capacitances are later referred with a nonlinear model, where they are described as a form of input ($C_{iss}$), output ($C_{oss}$), and reverse transfer (feedback) capacitances ($C_{rss}$). They are derived from terminal parasitic capacitances in following manner: $C_{iss} = C_{GD} + C_{GS}$, $C_{oss} = C_{GD} + C_{DS}$ and $C_{rss} = C_{GD}$. Dynamic changes of parasitic capacitances during the switching process have a great influence on overall switching behaviour, as they strongly define the turn-on and -off transients and are nonlinear functions of $V_{DS}$ [30]. Therefore, a nonlinear model is applied to refine the illustration of switching characteristics. Figure 12 depicts the turn-on and 13 the turn-off process steps for SiC MOSFET switching [31].

Turn-on period (Figure 12) begins as on-state gate signal with amplitude $V_{GG}$ is applied to device gate, on time instant $t_1$. As this occurs, voltage causes gate current $I_G$ to flow through gate resistor $R_G$. Gate current charges input capacitance $C_{iss}$, and gate-source voltage begins to increase according to:

$$V_{GS} = V_{GG}(1 - e^{\frac{-t}{\tau_{iss}}}) \tag{8}$$

where $\tau_{iss} = R_G C_{iss}$. Between $t_1$ and $t_2$, switch is operating on cutoff-region, as channel is closed and free-wheeling diode $D_{fw}$ is conducting, keeping device drain-source voltage constant. Stage can be referred as turn-on delay time [31], [32].

Channel current starts to increase from zero, as gate voltage $V_{GS}$ exceeds device threshold voltage $V_{th}$ at timepoint $t_2$. When the threshold voltage is exceeded (see period between $t_2$ and $t_3$), MOSFETs channel becomes conductive. At this time, the load current $I_D$ transfers from the free-wheeling diode $D_{fw}$ to channel, corresponding to MOSFET behaving as a voltage-controlled current source. Channel current rises as:

$$I_{ch} = g_{fs}(V_{GS}(t) - V_{th}) \tag{9}$$

where $g_{fs}$ is the transconductance of MOSFET [32]. There may be some visible fluctuation on $V_{GS}$ due to injected charge on $C_{GD}$, but generally voltage continues to increase similarly to stage before (Equation (8)). Moreover, the values of parasitic capacitances increase gradually during this stage because of the nonlinearity of the materials. Simultaneously, $V_{DS}$ reduces slightly from original DC-voltage ($V_{DC}$) due to parasitic inductances [31], [33]:

$$V_{DS}(t) = V_{DC} - (L_S + L_D)\frac{dI_{ch}(t)}{dt} \tag{10}$$

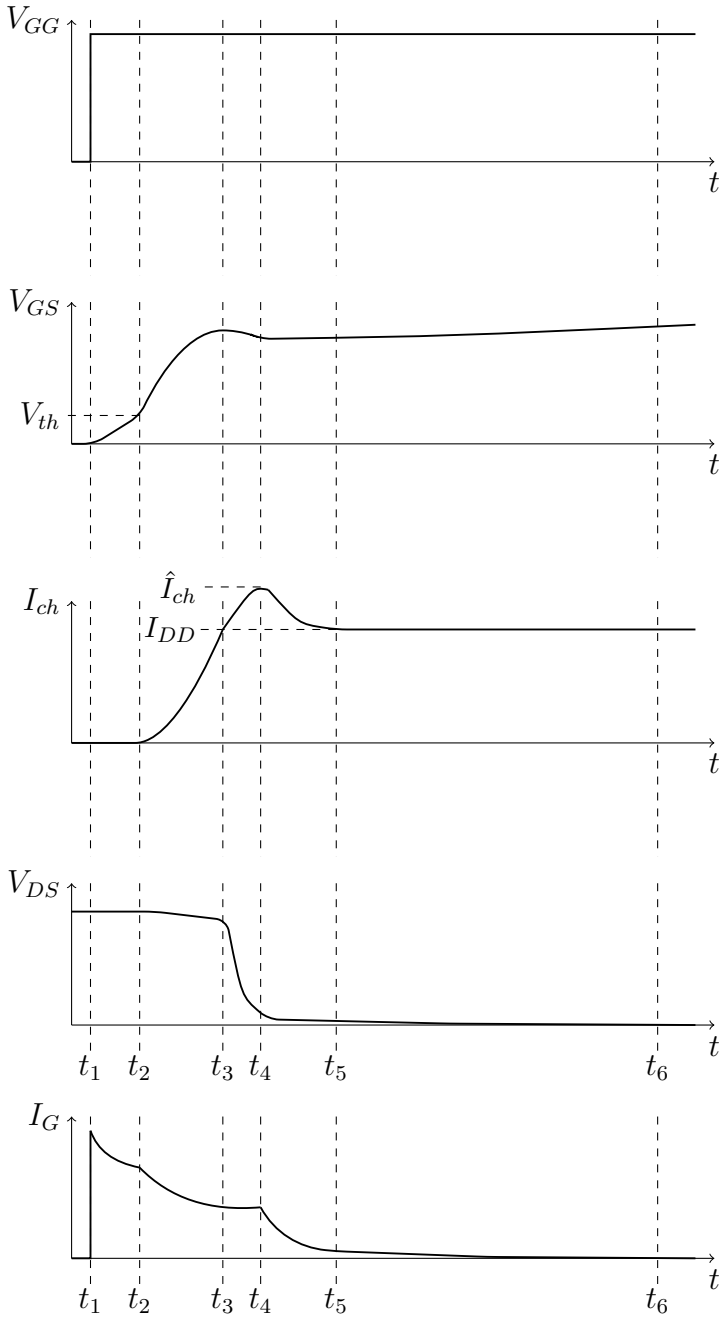


Figure 12: SiC MOSFET turn-on waveforms for low to high gate signal transition ($V_{GG}$), gate to source voltage ($V_{GS}$), channel current ($I_{ch}$) and voltage ($V_{DS}$), as well as gate current ($I_G$).

where:

$$\frac{dI_{ch}(t)}{dt} = g_{fs}\frac{V_{GG}(t) - V_{th}}{\tau_{iss}} \tag{11}$$

During this phase, free-wheeling diode $\mathrm{D}_{fw}$ is still conducting, but the current

flowing through it is gradually decreasing as channel current rises. Current rise time is finished at time point $t_3$, as the steady-state load current $I_{DD}$ is reached by channel current $I_{ch}$. At this instant, free-wheeling diode $D_{fw}$ stops conducting and shifts momentarily to reverse recovery mode, causing current to flow on the reverse direction through the diode. All current from $D_{fw}$ is therefore commutated to the MOSFET drain ($I_D$). During diode conduction, $V_{DS}$ remained constant, so no current was flowing through $C_{DS}$. However, as the diode conduction was finished, energy stored in this capacitor is now able to flow through the device channel:

$$I_{DS} = -C_{DS}\frac{dV_{DS}}{dt} \tag{12}$$

Also, part of $I_G$ still flows through $C_{GD}$ to discharge it and part charges up $C_{GS}$. This causes current flow $I_{GD}$ as well as rise of $V_{GS}$ and therefore $I_{ch}$ (Equation (9)). Combination of parasitic currents from diode reverse recovery, gate current and increased channel current cause the current overshoot visible on Figure 12 between $t_3$ and $t_4$ [32]:

$$\hat{I}_{ch} = I_{DD} + I_{GD} + I_{DS} \tag{13}$$

Simultaneously as current overshoots steady-state load current, the voltage over drain to source $V_{DS}$ decreases with slope:

$$\frac{dV_{DS}}{dt} = -\frac{dV_{GD}}{dt} = -\frac{I_G}{C_{GD}} \tag{14}$$

During this time, MOSFET operates in an active region. Stage is finished, when $I_{ch}$ reaches its peak value $\hat{I}_{ch}$ at time instant $t_4$. Commonly, this switching stage can be referred to as voltage fall time [31].

On the next time period from $t_4$ to $t_5$, channel current $I_{ch}$ reduces from peak overshoot to steady state load current $I_{DD}$. Channel voltage $V_{DS}$ continues to decrease according to Equation (14). On this stage, MOSFET operation transits from saturation to ohmic region, when $V_{DS} < V_{GS}$. Driving gate current $I_G$ flows almost entirely through $C_{GS}$ and is defined approximately as:

$$I_G = \frac{V_{GG} - V_{GS}}{R_G} \tag{15}$$

Since $C_{GD}$ of SiC MOSFET is rather small, there is no clear Miller plateau in $V_{GS}$ waveform compared to the conventional Si-device. This can also be determined in less flat I-V curves for SiC devices in the saturation region [30]. At the end of this stage, the free-wheeling diode remains off, and the switch is close to its ohmic region [31], [32].

During the last step of turn-on from $t_5$ to $t_6$, $V_{GS}$ continues to increase according to Equation (8). Since parasitic capacitances differ over time, also time constant $\tau_{iss}$ is different compared to time period between $t_1$ and $t_2$. At time instant $t_6$, $C_{GD}$ is

fully charged, gate-source voltage $V_{GS}$ has reached driver voltage $V_{GG}$ and device on-state drain-source voltage determining conduction losses is specified as:

$$V_{DS(on)} = R_{DS(on)} I_{DD} \tag{16}$$

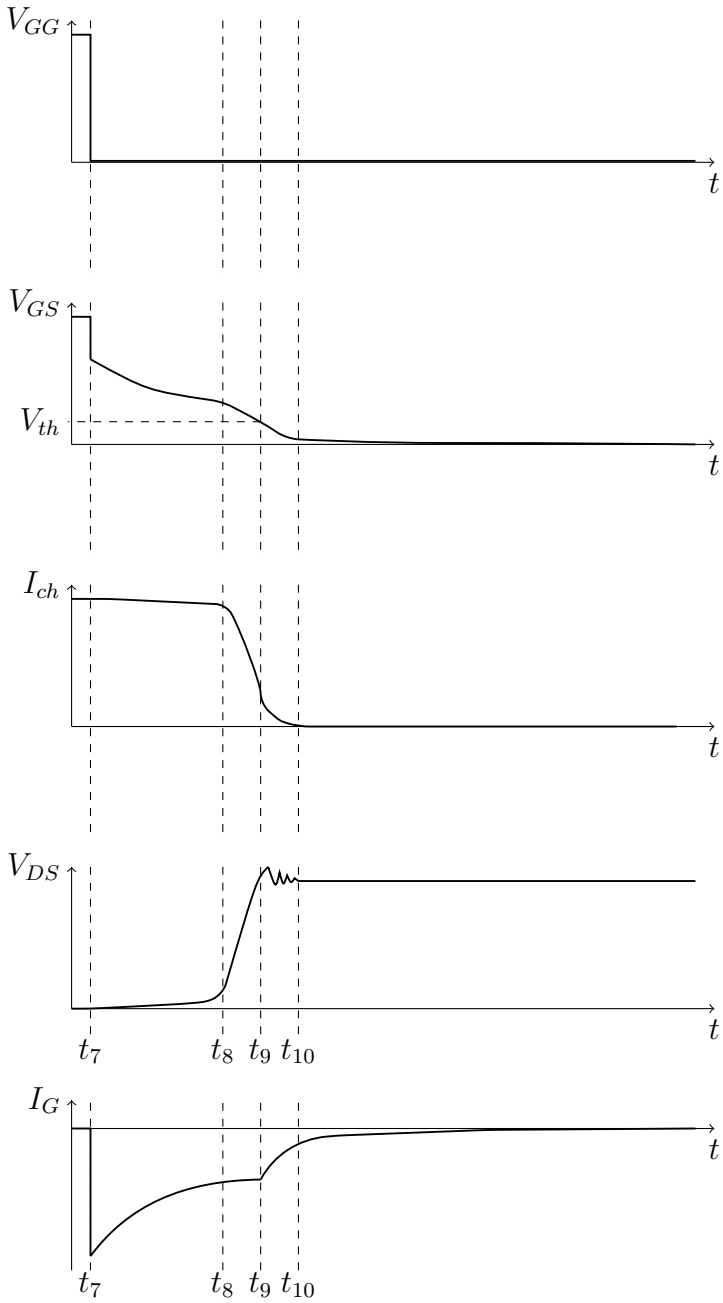


Figure 13: SiC MOSFET turn-off waveforms for high to low gate signal transition($V_{GG}$), gate to source voltage ($V_{GS}$), channel current ($I_{ch}$) and voltage ($V_{DS}$), as well as gate current ($I_G$).

Turn-off process (Figure 13) begins as gate pulse $V_{GG}$ is reduced from high to

low state on time instant $t_7$. This stage is referred to as turn-off delay time. Energy stored in input capacitance $C_{iss}$ discharges through $R_G$ and $L_S$ and gate voltage $V_{GS}$ decreases according to Equation (8). MOSFET operates at the ohmic region and the gate current in this stage is defined as:

$$I_G = (C_{GS} - C_{GD})\frac{dV_{GS}}{dt} \tag{17}$$

While gate pulse is reduced at $t_7$, the body diode of the MOSFET turns forward biased. During period $t_7$-$t_8$, MOSFETs body diode momentarily switches from forward biased to reverse-biased state, causing reverse direction current flow. However, the effect of it is quite limited, as momentary negative current occurs as a MOSFET drain to source path has low impedance and only a slight increase on $V_{DS}$ is visible. Characteristics of body diode negative current transient immunity should however be considered. This phenomenon is based on characteristics of electron carriers and is commonly known as body diode reverse recovery [36], [37].

Between $t_8$ and $t_9$, switch shifts its operation mode from ohmic to the active region. Channel current $I_{ch}$ decreases whereas voltage $V_{DS}$ increases rapidly. Gate voltage $V_{GS}$ declines according to the Miller effect, as drain potential increases and therefore fundamentally $V_{GD}$ also changes, while $V_{GS}$ does not exceed threshold voltage. This produces a current through Miller capacitance $C_{GD}$ determining the slope of gate-source voltage [28]. At $t_9$, the drain-source voltage reaches a nominal value at $V_{DC}$, and the stage is ended. Moreover, at $t_9$ MOSFET body diode current increases from negative to zero, causing slight overshoot on the waveform of $V_{DS}$ [37]. The period is referred to as voltage rise time [31].

From $t_9$ to $t_{10}$ input capacitance $C_{iss}$ discharges until $V_{GS}$ surpasses threshold voltage. $V_{DS}$ overshoots a bit and free-wheeling diode becomes forward biased, switching the current from MOSFET channel to diode. Drain-source overshoot is clamped to $V_{DC}$ and channel current reduces. Afterward, $V_{GS}$ reduces below threshold voltage and continues to decrease, all of the load current flows through the free-wheeling diode, $I_{ch}$ drops to zero and switch operates again at cutoff-region. The period is referred to as current fall time [31], [33].

Switching transient waveforms change according to the value of gate resistance $R_G$. If reduced, delay and fall time of voltage decrease in turn-on circumstances. However, as voltage changes $\frac{dV}{dt}$ are accelerated, channel current overshoot on turn-on increases. Similarly, on turn-off the delay and fall time of current decrease with reduced $R_G$, but voltage oscillation and overshoot on turn-off occasion increase [34].

### 3.2.3 Losses

Losses are a key factor in defining the efficiency of a power converter, and most of the total losses of a converter take place in switches. In the case of a power MOSFET, losses can be divided into conduction and switching losses according to their operational stages. Conduction losses refer to conditions, where the switch is at a conductive stage and switching losses to energy lost on transition states from

on- to off-state and vice versa. Switching losses also define the maximum achievable switching frequency [11].

Conduction losses take place in a power MOSFET, as the channel of the switch is conducting. Channel is not an ideal conductor since it possesses on-resistance as stated in Section 3.2.1. Conventionally, amount of conduction losses are determined by duty cycle $D$, on-resistance (Equations (6) and (7)) or -voltage (Equation (16)) and load current $I_{DD}$ in a following manner:

$$P_{cond} = DV_{DS(on)}I_{DD} = DR_{DS(on)}I_{DD}^2 \tag{18}$$

Switching losses are commonly divided into turn-on and -off occasions, since instants differ by form from each other, as stated in Section 3.2.2. Fundamentally, the amount of lost energy for every state transition pulse can be determined by integrating over product $v(t)i(t)$ during turn-on and -off transients:

$$E = \int_t v_{DS}(t)I_{ch}(t)dt \tag{19}$$

As channel voltage and current are time-variant and irregular functions, their values are commonly mathematically or geometrically evaluated from switching waveforms. After energy loss is determined separately for turn-on and turn-off, switching losses of a MOSFET can be acquired by multiplying that amount by switching frequency $f_s$ (Equation (20)) [11]. Energy losses for turn-on instant are often higher than for turn-off [33], [34].

$$P_{sw} = P_{on} + P_{off} = f_s \cdot (E_{on} + E_{off}) \tag{20}$$

Total losses for a power MOSFET can be obtained by adding all losses together:

$$P_{tot} = P_{cond} + P_{sw} \tag{21}$$

Several factors are affecting the switching losses, which change the aforementioned switching waveform transients. Losses are not constant at different temperatures, as turn-on transient energy loss decreases with increased temperature, and turn-off loss on the other hand rises slightly with the temperature at least with test conditions of maximum 150°C [34]. Also, even as SiC MOSFETs are voltage controlled devices, the maximum gate current affects switching characteristics. Inadequate $\hat{I}_G$ as well as high $R_G$ limit switching speeds and lead to higher switching losses. On the other hand, too low $R_G$ may lead to electromagnetic interference (EMI)-issues due to increased switching frequency. In addition, switching performance has a high sensitivity on the parasitic drain and source inductances $L_D$ and $L_S$, as they influence losses as well as voltage and current overshoots during switching [27], [34].

Under specific conditions and with suitable gate driver, lossless or nearly lossless switching is possible to achieve. This has been demonstrated in case, where channel voltage has reached zero before current rises on turn-on or current has reached zero before the voltage rise on turn-off [35].

## 3.3 Limitations

There are three main limiting requirements on SiC MOSFET compared to its Si counterpart to be considered, while designing a driver circuit for a power converter. These requirements include preferably negative turn-off voltage, high on-state gate voltage, and narrow positive gate voltage range.

A negative turn-off gate voltage is preferred, due to considerably low threshold voltage of a SiC power device, as well as threshold voltage instability. Negative voltage gives some extra margin to prevent false turn-on during switching transients or against high-frequency noise coupled on the driving circuitry. The root cause for threshold instability is commonly poor semiconductor oxidation, which is a manufacturing process, done to enable faster switching capabilities of a device. Poor oxidation mainly causes two types of instabilities to the device: bias temperature instability effects and threshold voltage hysteresis. Bias temperature instability (BTI) causes permanent effects over a long period. As a result, $V_{th}$ may decrease even at lower temperatures than the defined maximum junction temperature of a power device. Hysteresis refers to threshold voltage change following voltage changes during switching. It is caused by the physical properties of the wide bandgap of a SiC device and degenerates threshold voltage as the amount of negativity of the gate pulse goes further. However, the effect of hysteresis towards $V_{th}$ is far less significant compared to temperature instability, and can often be neglected [10], [38], [39].

In addition to BTI effects, there are also other challenges over long-term device operation. Switching stress has been found to increase $V_{th}$ slowly over time. The phenomenon is based on the dynamics of the gate oxide materials, the most influential parameter being the number of switching events. The major impact is increased $R_{DS(on)}$, which corresponds to higher conduction losses on the device [40]. However, the effect is not critical towards the overall functionality of the MOSFET, as the stress does not affect basic functions, such as blocking capabilities, reliability, and switching losses of a device [40]. Additionally, the phenomenon has not been found to occur, if a negative off-voltage is used.

Due to the aforementioned issues, component manufacturers often recommend the low-state gate driving signal to be between 0 and -5V. Recommended turn-off voltage depends on on-state voltage and switching frequency [40]. It has to be noted, that there is also an absolute minimum limit to negative voltage durability, which should not be surpassed even on brief switching transients, such caused by discharging of $C_{GD}$. Also, further lowering the negative gate voltage increases the hysteresis effect. Even if voltage spikes do not cause a false turn-on or exceed absolute maximum negative voltage rating, it is desired to minimize them, as positive spikes may cause thermal stresses to a device and negative ones could degrade oxidation reliability, therefore affecting threshold voltage value [41].

Compared to its Si-counterpart, the transition between ohmic and saturation regions is not defined as clearly for SiC MOSFET (Figure 14). The state transition is more linear, indicating that channel is partly conductive for lower gate voltages, yet opens fully at rather high voltage level (nominally 16V). Moreover, the threshold voltage of a lower boundary can be 2.5V or less, and as previously stated, prone

to instability. In comparison, the threshold voltage for the equivalent Si-device is nominally between 4-6V [9]. Recommended amplitude for high-state gate driving signal is usually between 18-20V for SiC, whereas for Si power device 15V would be sufficient [38]. SiC switch would operate on lower voltage amplitude as well, but on-resistance ($R_{DS(on)}$) decreases significantly as the gate voltage is increased further, corresponding to lower conduction losses [42]. Amplitude is also top-limited since the gate terminal can not endure voltages over around 25V, and higher voltage than 20V does not provide any additional benefits [42]. Therefore, depending on the component model and manufacturer, the acceptable range of voltage may be remarkably narrow. These requirements make traditional gate drivers incompatible with SiC devices, which is especially challenging for some hybrid switch concepts [8].

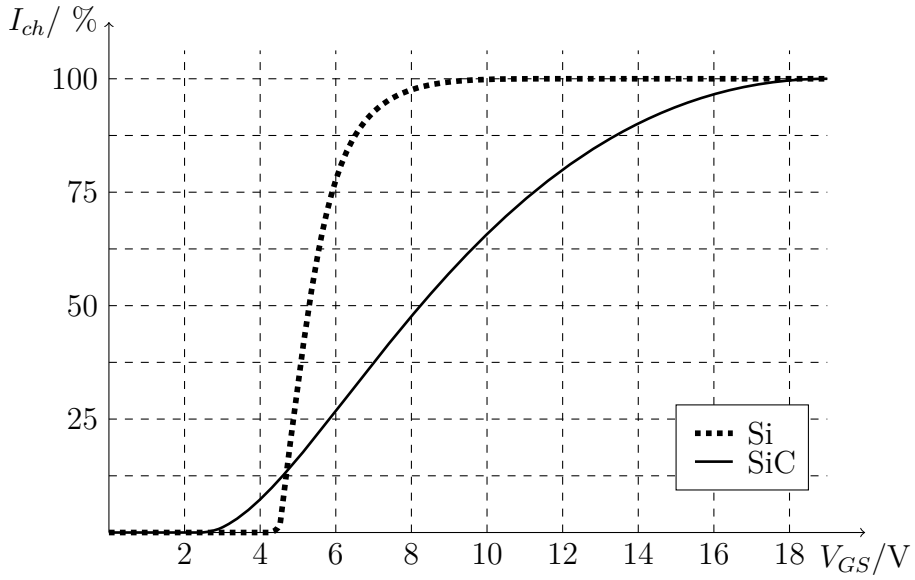


Figure 14: Illustration of transfer characteristic differences between Si and SiC MOSFETs at constant temperature [9].

# 4 Gate Driver Circuit

Traditional gate driver components designed for controlling power MOSFETs are PWM-controllers with different embedded functions. Circuits generally control switches, by connecting them between a supply voltage and circuit ground reference potentials. This action enables the controlling of power, frequency, and voltage of a power converter. Controllers are also used to monitor different quantities, such as current and overvoltage, and react to undesirable situations. Monitoring makes it possible for the converter to remain within specified operation mode and area [43].

To achieve the full benefits of a SiC device, a proper gate driver circuit has to be designed to fit the application in question. As these switches are especially convenient for high-speed and high-voltage applications, loss minimization and isolation requirements should be carefully considered to realize the components' full potential.

In this section, design requirements for power supply topology studied in this thesis as well as switching components are specified. Moreover, the advantages and disadvantages of known gate drive circuits are discussed, and a gate driver proposal is presented.

## 4.1 Requirements

Compared to traditional MOSFET gate drivers, drivers for SiC MOSFETs possess some additional requirements related to voltage levels as well as switching speed, making traditional solutions suitable only for a limited range of SiC MOSFETs [44]. The range of voltage is higher for SiC drivers, due to their peculiar requirement for high on-state voltage and preferably negative off-state voltage. This range is often too wide for traditional PWM-drivers, as their absolute maximum ratings are typically quite low [45]. Higher switching speed creates demands for driver output. In order to keep up with accelerated switching speeds, gate resistance $R_G$ should be minimized. This helps the driver to output high enough current $I_G$ to change the state of the switch. Being a voltage-controlled device, MOSFETs preserve their state so the driver is not required to output steady current, but pulsed $I_G$ at switching transient should have adequate amplitude [39].

A mandatory requirement for the gate driver circuit of a two-switch flyback is isolation. This is due to the characteristics of a two-switch design, where the gate of the upper switch is floating, referring to other than circuit ground potential being used as gate signals reference point. In theory, an integrated non-isolated high side driver could be used, but even though they are practical and take up low space on PCB, they have significant switching delays that are not preferable with SiC MOSFETs [46]. Isolation can be implemented using an optical isolator or a transformer, whichever is most viable for the case in question. As gate signals must be simultaneous for a flyback, a delay caused by isolating components has to be addressed accordingly during device design, in order to ensure correct device operation.

Negative off-voltage may not be compulsory by definition but is all in all extremely beneficial for this case. Previously in Section 3.3 was stated, that threshold voltage of

a SiC MOSFET is initially low, and accounting oxidation quality and bias temperature instability, a strong case for negative voltage switching is made. The downside of implementing negative voltage to the gate driver circuit is increased complexity. The negative voltage is quite straightforward to achieve using different diode-based circuits, but this often requires a high supply voltage, as high on-state amplitude is also required for MOSFET switching.

To achieve sufficient and perpetual amplitude for gate-source voltage on all instants, the supply voltage of the driver circuit has to be constant, even on special occasions such as converter start and turn-off. One way to achieve this goal, is by implementing external circuitry in charge of monitoring the supply voltage level. The amplitude of $V_{GS}$ affects SiC-devices on-resistance and reduces conduction losses, even though the channel of the device would be by definition conductive [9]. Also switching losses should be properly addressed, by minimizing the simultaneity of current and voltage transients during switching (Equation (19) on Section 3.2.3).

Moreover, there is a possibility to add a switch between the gate and source potentials of the power device. This switch enables controlling the Miller current during fast voltage changes and can be used to keep the device completely off by shorting the gate to source paths together. This technique is called active clamping, and it's a viable solution for further increasing the power converter efficiency as well as ensuring low turn-off voltage [41].

## 4.2 Solutions

### 4.2.1 Controller Selection and Driving Current

There are multiple qualified solutions for gate driver circuitry, that are capable of reaching the previously defined requirements. Controller selection is quite important to achieve application-specific demands, such as sufficient driving current and switching frequency. As previously stated, gate resistance is also an important factor in these requirements, as it affects both measures. An optimal value for $R_G$ results to low $V_{GS}$ oscillation, but with fast switching capabilities. It can be evaluated in various ways, for example, according to [9]:

$$R_G \geq 1.4\sqrt{\frac{L_G}{C_{iss}}} \tag{22}$$

where the equation is derived from a simplified gate loop, containing resistive ($R_G$), inductive ($L_G$), and capacitive ($C_{iss}$) components in series. However, this is just a model and the best results are usually achieved by iterative testing process on the design phase. Monitoring the switching waveforms and MOSFET heat dissipation helps with the evaluation [12].

Gate resistance can also be set to be different for turn-on and turn-off transients if manipulation of on- or off-times is desired. By applying a resistor in series with a diode in parallel with $R_G$, resistance can be optimized for the desired transient. Usually, turn-off speed should be higher, corresponding to lower resistance value than

the original $R_G$. Figure 15 presents the common method for implementing separate gate resistances for turn-on and turn-off on *Resistance selection*-block [12].

Required gate driving current can be derived from MOSFETs gate charge $Q_G$, which is listed on component datasheet [42]. It is notable, that value of $Q_G$ will change according to gate voltage $V_{GS}$, so often the total gate charge parameter is utilized. Amount of sufficient gate current depends on the duration desired for charging MOSFET gate completely [26]:

$$I_G = \frac{Q_G}{t_{tr}} \tag{23}$$

where $t_{tr}$ is the gate charge-up time, or transition time. Transition time consists of turn-on delay time and rise time, corresponding to the duration taken from reaching 10% of gate-source voltage to 90% of desired value [47]. Typical values for the rise time and on-delay time under known switching conditions are often given on device datasheets, but slower transitions are also permitted if current must be more strictly limited. Also, slower transition times may be desirable for purposes of electromagnetic compatibility (EMC).

If an adequate amount of current can not be derived directly from PWM-controller output, and transition time would increase too much, a bipolar totem-pole driver can be introduced to gate driver design to amplify current (Figure 15, *Totem-pole*-block). Totem-pole implementation is quite popular due to its cost-effectiveness and additional benefits towards reverse breakdown prevention and self-clamping [46]. It has to be noted, that some versions of a bipolar totem pole can already be implemented within PWM-controller, as it enables higher output current from the controller component as well. However, in this case the reverse breakdown transient has to be accounted for. This can be achieved by placing Schottky diodes between circuit ground and controller output, as well as between output and operating voltage potential [46] (Figure 15, *Schottky protection*-block).

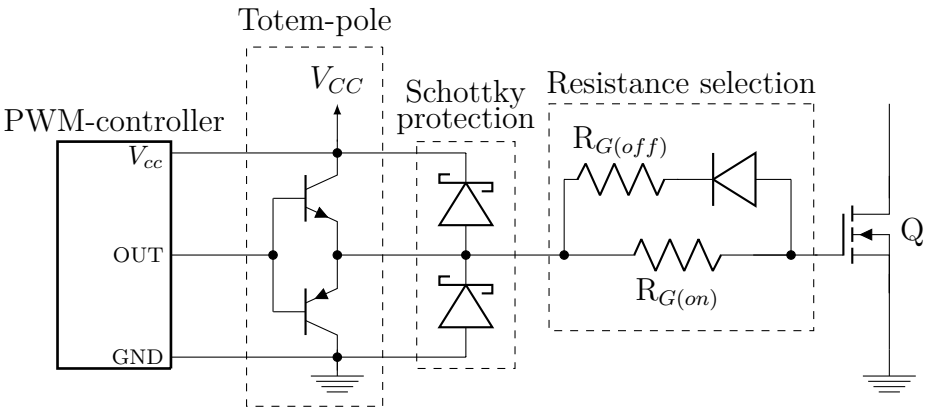


Figure 15: Potential PWM-controller additions for gate driver current and transient optimization.

Bipolar totem-pole consists of two bipolar junction transistors (BJTs), a pnp-type and npn-type. Transistors bases are connected, and channels are in series between

operational voltage $V_{CC}$ and circuit ground potential. In comparison to MOSFETs, bipolar transistors are controlled with the current on their base terminal, rather than the voltage on a gate terminal respectively to MOSFET. As a control pulse is applied from the controller, the upper npn-transistors channel becomes conductive, connecting operation voltage $V_{CC}$ to totem-pole output node. At the same time, the lower pnp-transistor is blocking the voltage. As pulse is terminated by the controller, transistors operation modes switch, corresponding to npn-transistor blocking operational voltage, and pnp connecting the output of the totem-pole to ground.

### 4.2.2 Isolation

In terms of isolation, optical isolation as well as a transformer can be considered. During consideration, the requirement for two identical gate signals to fit the requirements of a two-switch flyback must be acknowledged.

Optical isolation is limited with higher switching frequencies due to propagation delay, which slows down switching transients [48]. Also, since high-frequency optical isolators are often more expensive and may have slight performance differences, the most viable solution to isolate the power circuit from the control circuit and to drive the switches simultaneously is a transformer-coupled gate driver with two secondaries.

Designing a transformer for gate driver circuitry is not different from its design for other applications, apart from lower power output requirements. The complete design process will be discussed later, but some preliminary requirements for this application can already be recognized. First of all, the physical structures of the two secondaries have to be as identical as possible to ensure uniform functionality, which can be achieved by careful and consistent winding. Also, since the component is used for insulation purposes, required clearance and creepage distances should be properly addressed and even over-dimensioned a bit. Additionally, an advantage of a transformer is the option of choosing a winding turns ratio to have desired secondary voltage. This aspect should be kept in mind during the design phase, as it could help in solving the issue with potentially problematic voltage range requirements.

With a transformer implementation, core saturation possesses an additional risk. Saturation can occur due to too small physical size of the transformer, where the maximum achievable magnetic flux is insufficient, or due to undesired DC-component across transformer winding. Core saturation often leads to destruction due to excessive current and temperature, and it should be avoided at all costs [49], and even a rather small DC-voltage in the transformer may cause flux to increase to point of saturation. To remove the DC-component from the transformer, AC coupling must be conducted, for example by adding a coupling capacitor in series with the transformer primary. The capacitor blocks the DC-voltage from the transformer, thus removing the DC-component [12], [46].

AC coupling with a capacitor does not come without some issues of its own. First of all, the coupling capacitor causes a level shift to the gate driving signal, which depends on the controller duty cycle. Amount of voltage offset corresponds to the steady-state voltage over the capacitor and it depends on the duty cycle in the

following manner:

$$V_C = DV_{CC} \tag{24}$$

where $V_C$ is the voltage over the coupling capacitor. Duty cycle dependency may be undesirable, as it has a major effect on output voltage amplitude. For Si MOSFETs, this coupling method was evaluated to be usable for duty cycles between 0-50%, as increased duty cycle corresponds to decreased gate voltage amplitude [12], [46].

The second issue to consider is, that as PWM-controller begins to release gate pulses to the transformer, the first few will not reach intended amplitude, as the bias capacitor requires to be charged. This aspect raises the question of demand for under-voltage lockout, as gate pulses with insufficient amplitude should not be transferred through to MOSFETs gates. Moreover, a capacitor in series with transformer primary forms an effective LC-resonance circuit. Usually, resonance causes the whole gate signal to oscillate at low frequency, which should be properly damped to assure safe operation. Damping can be fulfilled for example by large enough coupling capacitor value, or by adding a low-value resistor in series with the capacitor [12], [46]. Value of resistor can be determined by the characteristic impedance of the resonant circuit:

$$R_C \geq 2\sqrt{\frac{L_m}{\mathrm{C}_C}} \tag{25}$$

where $\mathrm{R}_C$ is the value of damping resistor, $L_m$ the magnetizing inductance of the gate transformer and $\mathrm{C}_C$ the capacitance of the coupling capacitor [46].

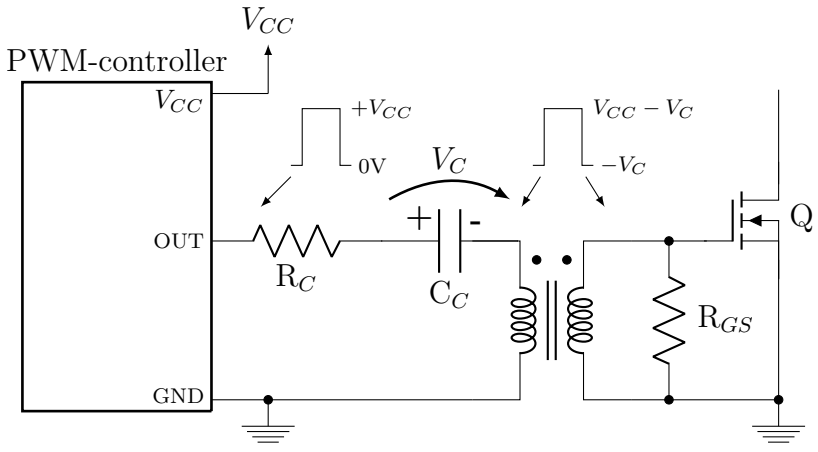


Figure 16: General transformer coupled gate drive circuit with a coupling capacitor and a damping resistor.

Figure 16 depicts a coupled circuit with $V_C$ level shift considerations and damping resistor $\mathrm{R}_C$. $\mathrm{R}_{GS}$ represents a pull-down resistor between MOSFET gate and source, which is required in this specific circuit to offer a path for excess energy on the transformer secondary to discharge to circuit ground [46]. It is notable, that if the

duty cycle remains low enough during converter operation, voltage offset caused by the coupling capacitor could be used to set the negative turn-off voltage value automatically. This would function in cases where the fluctuation of the duty cycle is low, but it would also decrease the turn-on voltage amplitude respectively [12].

It should be clarified, that the coupling capacitor is not by any means a necessity if core saturation can be prevented some other way, or is not perceived to possess a threat. However, this solution and its issues can be used as a point of comparison in evaluating the characteristics of other gate driver solutions and their trade-offs. All in all the use of gate transformer for insulation purposes contains some design aspects to consider, but can fulfill isolation requirements and generate two consistent yet separate gate signals to be used for switches on different potentials.

### 4.2.3 Gate Voltage

For SiC MOSFETs, gate voltage has two main requirements, as stated on Sections 3.3 and 4.1: adequately high turn-on and adequately low turn-off voltage. These prerequisites make sure, that device is operating on a defined region; channel being on the conductive state with minimized on-resistance while on, and channel blocking voltage completely while off. Therefore, sufficient voltage levels must be guaranteed by the gate driving circuitry.

Positive turn-on voltage amplitude is commonly the same as the operating voltage of the PWM-controller if a controller is used to directly drive a MOSFET. Circuitry between the controller and MOSFET gate naturally defines the amount of voltage that is transferred to the switch, so no universal case can be examined. Instead, the effect of every part of the circuitry between the two potentials towards gate signal amplitude should be independently evaluated. Also, the operating voltage of the controller itself must be sufficient and steady before the controller begins to output the gate signal. Moreover, with straightforward turns ratio manipulation on isolation transformer, the amplitude can be boosted up if necessary. However, in this case it has to be noted, that small transformers used for isolating gate signals usually have a low number of turns, so adding one turn to the secondary may cause the voltage to grow quite significantly.

Apart from the transformer-coupled capacitor gate driver, negative turn-off voltage can be produced using various diode-based circuits implemented on the MOSFET gate. First of all, a negative voltage clamper visible in Figure 17a could be used. The idea of the solution is similar to capacitor coupling, only this time instead of removing the DC-component, one is added to the gate signal. Clamper shifts the given AC-signal in such manner, that its whole amplitude shifts to fluctuate on the negative voltage side, apart from the amount of diode forward voltage drop 0.7V [50], [51]. A Schottky diode is used instead of a conventional one to account for fast switching speeds.

The second option is to implement a full-wave Zener clipper circuit, presented in Figure 17b. On the circuit, two Zener diodes are connected in series, with switched polarities. Clipper limits the positive and negative voltage amplitude by the amount of Zener breakdown voltages, generally functioning as a bipolar voltage regulator

shaping the incoming AC-waveform. When the input signal is at a positive state, the upper diode conducts and lower regulates voltage amplitude as Zener breakdown voltage is reached. As signal switches to a negative voltage, diodes operate similarly, yet in reversed fashion. Again, the forward voltage drops of the diodes (0.7V) has to be accounted for on output voltage amplitudes [50]. One of the advantages of this clipper type is, that there is no need for a coupling capacitor.

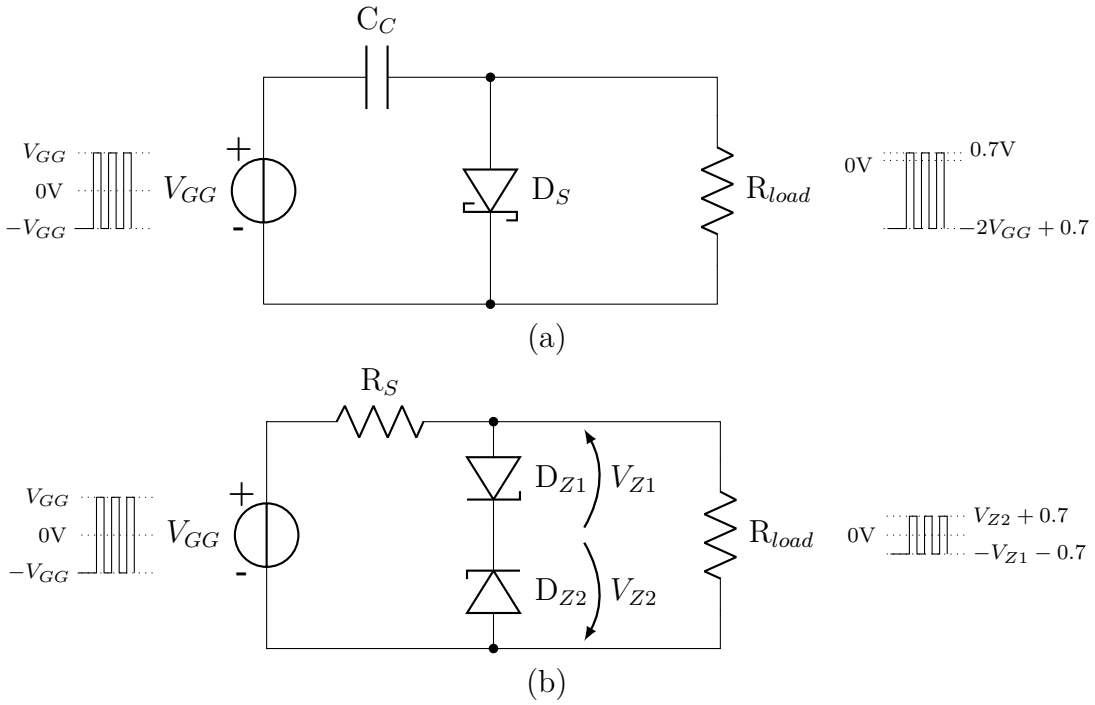


Figure 17: (a) Negative voltage clamper (b) Full wave Zener clipper.

Figure 18 depicts a combined version of previously illustrated circuits, which is widely utilized in cases with a coupling capacitor. It consists of the capacitor and two diodes, a Zener and a Schottky diode. Zener is added to the conventional negative clamper circuit for purposes of controlling exact positive and negative voltage amplitude by setting the existing peak-to-peak signal amplitude to the desired level. With this circuit implementation, Zener voltage determines directly the amplitude of positive voltage, as the rest of the voltage would shift to the negative side. However, the solution does not solve the issue of wide voltage range, as voltage magnitude is not increased, but only shifted. If for example +20/-5 switching levels were desired to be achieved, the initial signal should have 25V peak-to-peak range. It is also notable, that the same effect could be achieved by implementing a conventional Zener clipper with two different Zener voltages.

The most straightforward way to ensure sufficient voltage range to cover high turn-on and negative turn-off voltage is to select a PWM-controller with high operation voltage capability, for example the previously stated 25V. This approach is easy as it does not introduce any added circuitry to design. Also, some controller manufacturers add an option for both positive and negative supply to drive components on negative

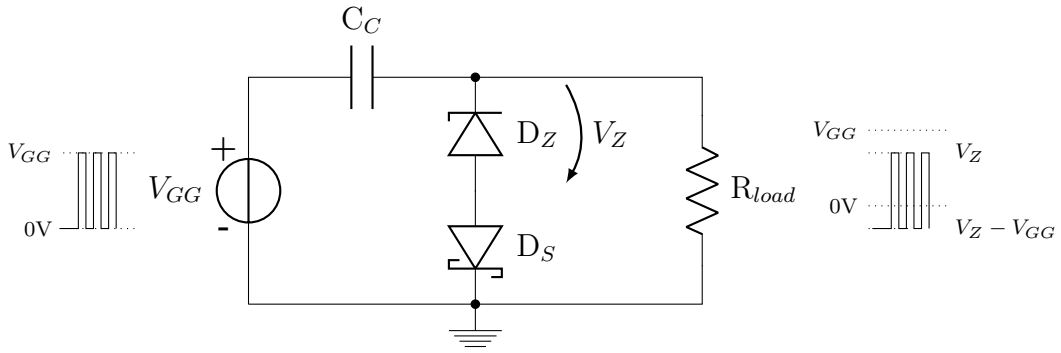


Figure 18: Negative voltage clamper with an additional Zener diode $D_Z$ to set voltage boundaries for positive and negative.

voltage [52]. If controllers with these capabilities can not be found or are otherwise undesirable for application in question, the amplitude can be boosted up with isolation transformer or specified requirements can be loosened on both ends. Newer generations of SiC MOSFETs already have less strict switching voltage demands, which by its behalf ease up on the required voltage range [53]. It also has to be noted, that power device manufacturers often develop their own gate drive circuits, that reach the requirement specifications (for example [54], [55]).

### 4.2.4 Loss Minimization

On loss minimization, the main focus should be kept on conduction and switching losses, due to their significance compared to other circuit losses in gate driver. Conduction losses depend on $R_{DS(on)}$, which depends on the amplitude of gate voltage, as stated in Section 4.1. On-resistance decreases as the gate voltage is increased from conduction boundary to the desired amount, at around 18-20V. Increasing amplitude further than that does not bring any additional benefits considering conduction losses, and often the specified maximum gate voltage is around 25V [42].

Minimization of switching losses contains a bit more aspects to consider compared to conduction losses. As stated in Section 3.2.3 according to Equation (19), lost energy at switching instant is equal to the overlap of channel voltage and current. Lost energy at turn-off depends on gate resistance and off-voltage, whereas at turn-on it only depends on gate resistance. Therefore, $E_{off}$ can be minimized by lowering $R_G$ and using negative turn-off voltage, and $E_{on}$ simply by reduction of $R_G$. However, gain derived from $R_G$ reduction on turn-on transient is less distinct. Negative turn-off voltage can decrease $E_{off}$ up to 40 %, if turn-off voltage is reduced from 0 to -5 V. However, it has no impact on turn-on energy losses [42].

Driver itself also possesses a driving loss, consisting of positive and negative driving voltage ($V_{GG}$ and $V_{EE}$), gate charge ($Q_G$) and switching frequency ($f_s$) in the following manner:

$$E_{drive} = (V_{GG} - V_{EE})Q_G f_s \tag{26}$$

if negative turn-off voltage $V_{EE}$ is not utilized, this term reduces to zero. However, since driving losses usually take up a small fraction of total circuit and device losses (usually at just a few $\mu$J), they can be perceived insignificant [39].

### 4.2.5 Active Clamping

Active clamping was originally developed for efficiently demagnetizing a transformer of a forward converter [56], but the term can be further extended to refer to an active component, such as a transistor, being utilized as a clamping circuit. Usually this technique is used in power converter circuits to minimize switching losses with zero-voltage switching (ZVS) [57], but the same general idea is easy to implement to gate drive circuits. There, a transistor can be set between MOSFETs gate and source to actively provide a low impedance path between the terminals as the device is turned off, thus ensuring zero voltage turn-off. This circuit is conventionally known as an active Miller clamp [58], since it is often utilized in half-bridge topologies to reduce the effect of the Miller current $I_{GD}$ originated undesirable device turn-on [41].

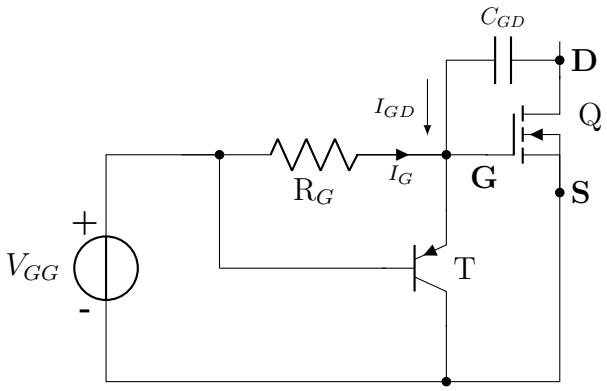


Figure 19: General pnp-type BJT utilized as an active Miller clamp between MOSFETs gate and source terminals.

An example of a bipolar pnp-transistor being used as a clamping circuit is presented in Figure 19. The transistor is self-driven, indicating that there is no external control circuit or source for clamping it. The base of the transistor simply follows the gate drive signal, disabling the channel in case of high state and enabling it at a low state. It is notable, that BJTs are controlled by their base current, rather than gate voltage respectively to MOSFET [50], so part of $I_G$ is used to disable transistor channel with this circuit. Additional resistors may be added to the circuit to ensure that the transistor operates only on saturation and cutoff regions [50].

Relevant benefits of active clamping include energy savings through ZVS as well as verified low turn-off voltage, with minor additional design efforts. Potential drawbacks include specific timing requirements to ensure sufficient delay during clamping as well as additional parasitics, that are introduced to the circuitry through added transistors. Timing requirements are more strict in a case, where separate control for clamping is implemented [57]. Finally, it has to be mentioned, that

active solutions always introduce new failure mechanisms to gate driving circuitry, so simplicity is an asset on gate drive circuit design [12].

### 4.2.6 Example Solutions

This subsection depicts a few examples of complete gate drive circuit solutions found on literature, which have been proven to be functional by prototypes. For a two-switch flyback topology, the following preliminary requirements were defined: isolation has to be utilized with a pulse transformer rather than optical isolation, and the circuit has to be expandable for two simultaneous switches, meaning that circuits intended to be used within bridge topologies were neglected. Many of the presented solutions contain one or more previously illustrated building blocks to fit requirement specifications.

A considerable aspect of overall example solutions is, that there are already quite a few different evaluation board -type drivers available by common power MOSFET manufacturers, that are ready to be utilized for power converters. However, the finished products are often remarkably expensive and intended to be used on bridge-type configurations or modular SiC MOSFET packs rather than discrete devices [59]–[62]. Therefore, their use is either not possible or worthwhile in industrial applications.

First, a simple version of a magnetically isolated gate drive circuit specially designed to fit the requirements of SiC MOSFET is evaluated [63]. The circuit is depicted in Figure 20, and it consists of a bipolar totem-pole, coupling capacitors, isolation transformer, Zener clipper, and a bypass resistor. Bypass resistor $R_{GS}$ commonly used to provide a safe path for excess energy to flow, in this case if Zener voltage $V_{Z1}$ is not reached.

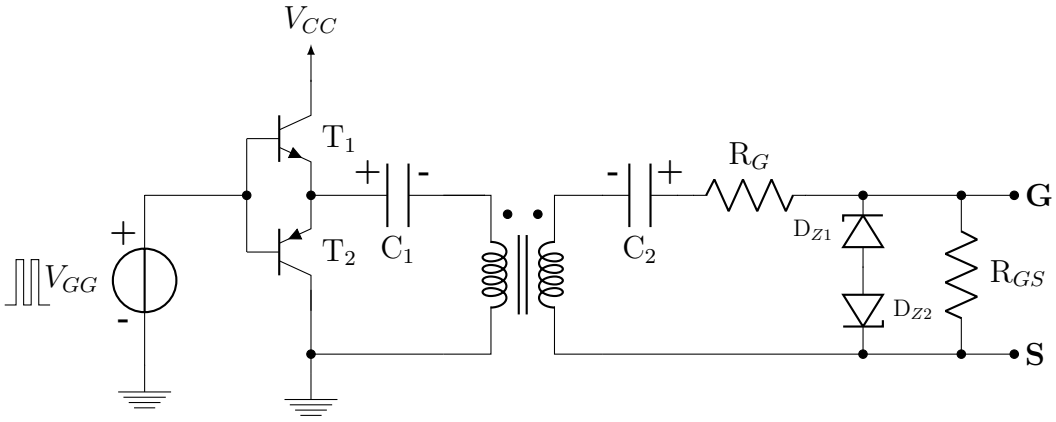


Figure 20: Example of simple magnetically isolated gate drive circuit.

With this solution, there was an initial need to improve driving current capability with a totem pole. The transformer is magnetized with a positive signal fluctuating between $V_{CC}$ and circuit ground and reset by coupling capacitors $C_1$ and $C_2$. By implementing a capacitor in both primary and secondary sides of the pulse transformer, voltage offset as well as gate voltage variation from the duty cycle (Section 4.2.2) are

removed. Then positive and negative voltage amplitudes are regulated with a Zener clipper [63].

The second example resembles the first one, the major difference being that the totem-pole is implemented on the secondary side of the isolation transformer [64]. The complete circuit is shown in Figure 21.

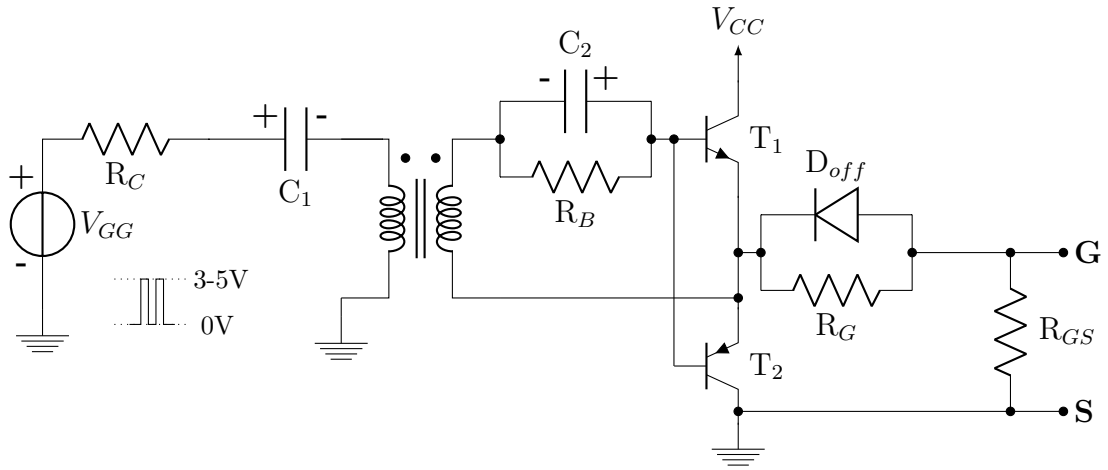


Figure 21: Example of another approach for isolated gate driver.

The example consists of a damping resistor $R_C$ and coupling capacitor $C_1$ on transformer primary, as well as a base resistor $R_B$, speed-up (coupling) capacitor $C_2$, bipolar totem-pole, gate resistor $R_G$, turn-off diode $D_{off}$ and a bypass resistor $R_{GS}$ on secondary. This circuit utilizes low amplitude pulses to the pulse transformer, and the amplitude and current are amplified on the transformer secondary by the totem-pole circuit. The speed-up capacitor on the secondary side is connected in parallel with a totem-pole base resistor to decrease the propagation delay of the driving signal. Diode $D_{off}$ is added in parallel with the gate resistor to ensure rapid turn-off speed for the switch, similarly to resistor selection [64].

From the application point of view, the circuit possesses some major disadvantages. First of all, if the example would be expanded to include two secondaries, voltage supplies for $V_{CC}$ should be isolated from each other. Two secondaries would also be more complicated designs compared to the first example, and therefore prone to differences in delay and overall performance.

The third example considered (Figure 22) is designed to fit the requirements of a dual-switch forward converter [9]. Converter type resembles a lot a two-switch flyback from the gate driving point of view, as two switches are simultaneously controlled with identical gate signals.

The circuit consists of many previously mentioned building blocks (from left to right in Figure 22): a bipolar totem-pole, capacitor coupling, isolation transformer with two identical secondaries, turn-on and -off gate resistance selection, pnp-transistor as an active clamping component, gate to source bypass capacitor and negative voltage clamper circuit. In the figure, $V_{EE}$ is the negative operating voltage, of which absolute value equals $V_{CC}$.

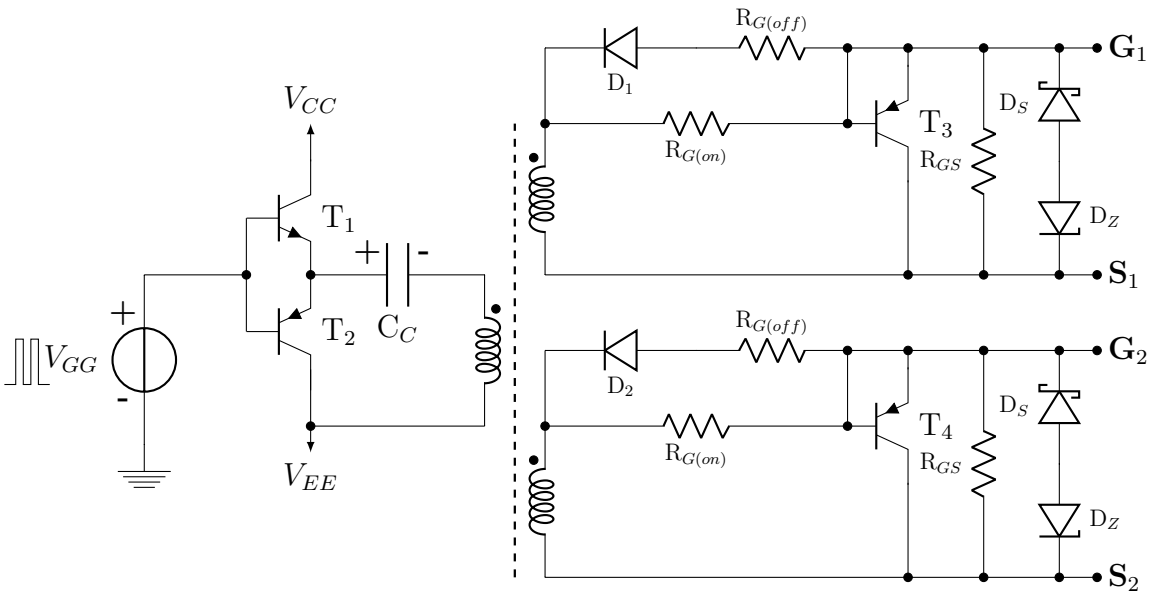


Figure 22: Example gate drive circuit designed for dual-switch forward converter.

Totem-pole first increases available current capacity for PWM-signal $V_{CC}$, waveform of which is fed to transformer primary at an amplitude of ±20V ($V_{CC}$ to $V_{EE}$). If the turns ratio of the pulse transformer is 1:1:1, that voltage amplitude is also available on transformer secondaries. When gate pulse is at high state +20V, pnp-transistors are functioning at the cutoff region, and the same voltage amplitude is transferred to MOSFETs gates. When a gate pulse is at its low state at -20V, transistors $T_3$ and $T_4$ are conducting, and negative voltage clampers clamp the gate-source voltage to equal $V_{EE} + V_Z$. Turn-off voltage can be set to desired negative value via Zener diodes, for example by setting turn-off to be -5V, which is common for SiC MOSFETs [9]. The negative voltage clamper circuit is constructed in reverse compared to an example in Figure 18, due to the negative polarity of $V_{EE}$.

The final circuit example considered (Figure 23) is perhaps the most interesting on the thesis point of view because it is based on a commonly used power converter circuit. This driver circuit is derived from a model of two interleaving forward converters, with parallel secondaries through diodes, instead of output filtering inductors as in conventional forward converter [65]. In this driver circuit, parallel converters are being switched on a complementary manner, meaning that only one gate signal is at high state at a time. This approach enables total duty cycles between 0-100%, as a single forward converter is capable of only a 50% duty cycle due to the need for transformer reset [65].

Generally, forward converter transformer consists of a primary, secondary, and magnetization reset windings. Magnetization reset winding has reversed polarity compared to primary and secondary, and it is utilized for eliminating the excess core flux in the transformer during every switching cycle. As switch $Q_1$ or $Q_2$ is conducting, current flows from $V_{CC}$ through the corresponding transformer primary, being also transmitted to the secondary side. As the other switch is not conducting,

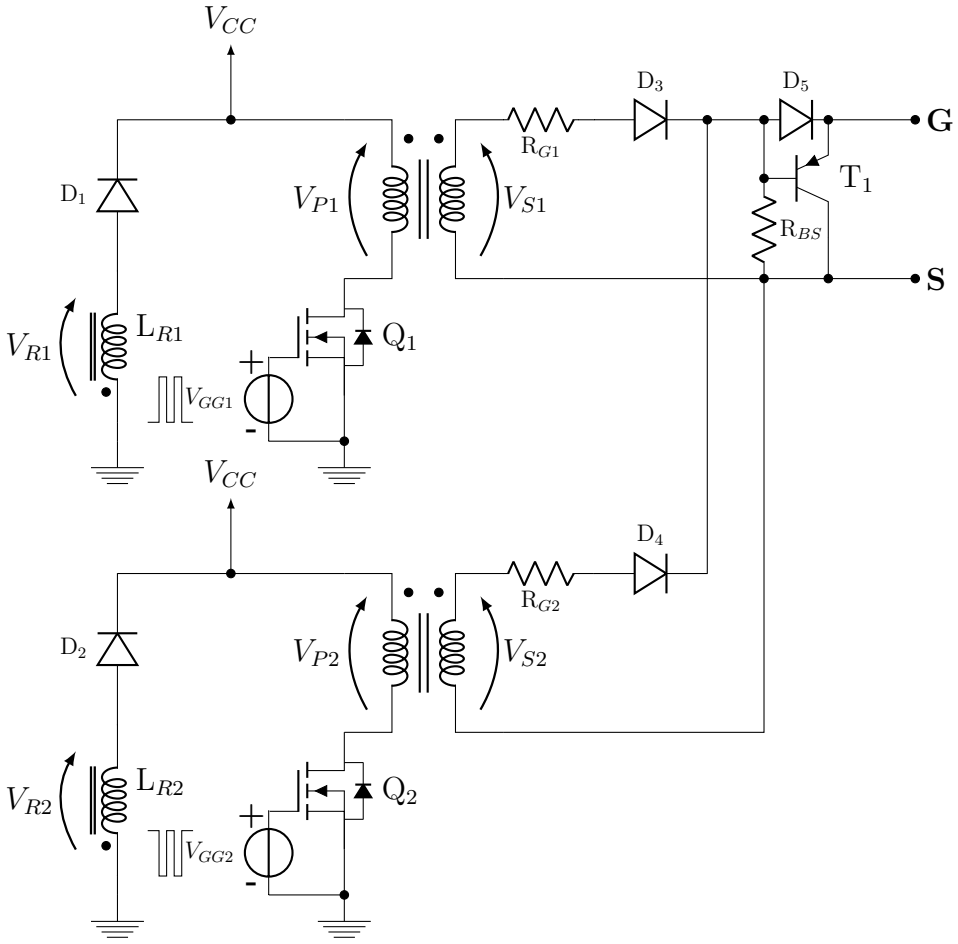


Figure 23: Interleaving dual-forward converter-based gate drive circuit.

excess core energy of the corresponding transformer is clamped back to operating voltage supply from the reset winding ($L_{R1}$ or $L_{R2}$) through a demagnetization diode ($D_1$ or $D_2$) [4], [65].

The complete circuit with its two forward type transformers is shown in Figure 23. Resistors $R_{G1}$ and $R_{G2}$ on transformer secondaries function as gate resistors for the power MOSFET. Diodes $D_4$ and $D_5$ force the secondary current flow towards converter output. Diode $D_5$ blocks energy return, pnp-type BJT $T_1$ functions as an active clamper, and resistor $R_{BS}$ provides the BJT base current a path to MOSFET source potential [65].

As this circuit is aimed to be used at high switching frequencies, parasitic resonant effects from power MOSFETs may cause unwanted false triggering for control switches $Q_1$ and $Q_2$. Therefore, an external circuitry for damping the resonance effect and thus preventing false triggering may have to be considered [65].

## 4.3 Proposed Concept

The gate driver concept proposed in this thesis resembles a dual-output version of a conventional forward converter, presented in Figure 24. The converter is controlled via switch Q, similarly to flyback. Magnetization reset winding $L_R$ is wound around the same core as primary and secondary windings of the transformer, but the orientation of the winding is reversed compared to the transformer [4].

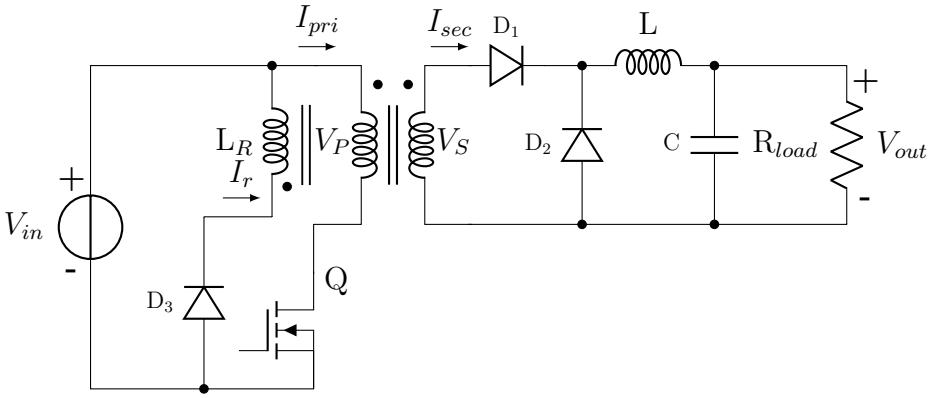


Figure 24: Conventional forward converter.

Switching the transistor Q on causes the current to flow through the primary winding. The current flow during transistors on-time causes a magnetic flux to build up in the transformer core, during which diode $D_3$ is reverse biased so no current flows through $L_R$. Simultaneously, $D_2$ is reverse biased, so secondary current $I_{sec}$ flows through inductor L towards converter load [4], [5]. As switch Q turned off, core energy stored in the transformer flows out from reset winding $L_R$. For preventing core saturation, the core has to be completely demagnetized before turning the switch on again [4], [5]. Relevant waveforms of the forward converter operation are presented in Figure 25.

In the proposed forward converter-based gate drive concept, isolation is achieved by a standard pulse transformer. However, the demagnetization demand is fulfilled by a Schottky diode rather than including a reset winding. The second difference to the conventional forward converter is the secondary inductor being replaced by a diode, similarly to the last example in Section 4.2.6. The main switch Q is utilized in the proposal with a standard low-power n-channel MOSFET, the gate of which is supplied directly from the output of a PWM-controller.

Forward converter-based gate drive concept was selected for its demagnetization properties. Demagnetization gets rid of the unwanted duty cycle dependent voltage offset found on capacitor coupling, addressed on Section 4.2.2.

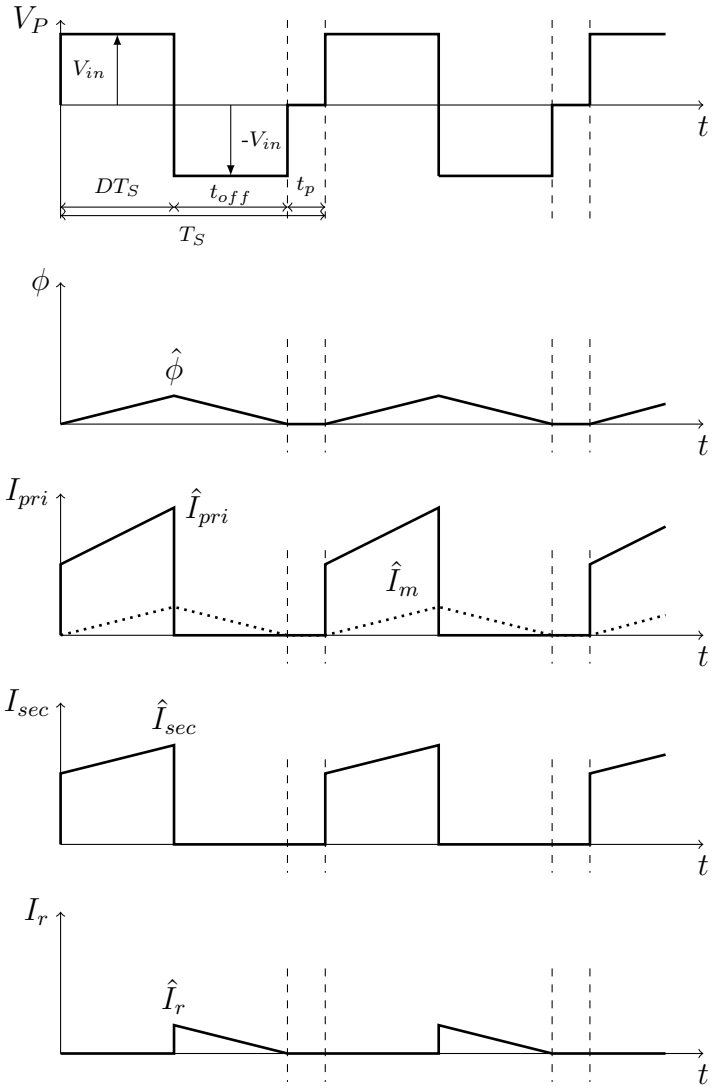


Figure 25: Primary voltage $V_P$, core flux $\phi$, magnetizing current $I_m$ as well as primary $I_{pri}$, secondary $I_{sec}$ and reset winding current $I_r$ waveforms for conventional forward converter.

### 4.3.1 Structure and Working Principle

On the proposed concept (Figure 26), the primary side of the transformer consists of a PWM-controller, MOSFET, gate resistor, capacitor, two Schottky diodes, and a Zener diode. As the transformer is a typical pulse transformer, forward converter core reset is taken into account using a voltage clamper consisting of Schottky diodes $D_{S1}$ and $D_{S2}$, and optional Zener $D_Z$ to free-wheel core energy back to the controller supply storage capacitor C. Both the pulse transformer and MOSFET $Q_{GD}$ are supplied directly from the controller output, so the amplitude of transmitted gate pulses is predictable and well known. Diode $D_{S1}$ between circuit ground potential and controller output also catches the undesired negative voltage transients, which

by default should not occur. The transformer secondary contains two diodes, a gate and bypass resistors, as well as a pnp-type BJT for active clamping. Secondaries are similar to the last example in Section 4.2.6, with the difference of being separated from each other and connected to the same transformer primary.

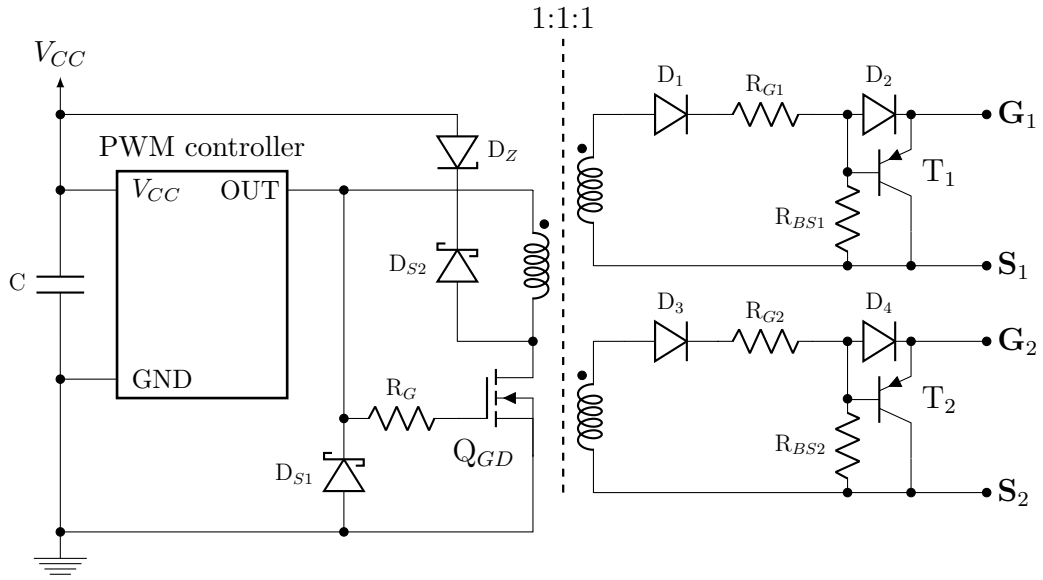


Figure 26: Proposed forward converter-based gate drive circuit.

The working principle of the driver resembles that of a forward converter. As the channel of MOSFET $Q_{GD}$ is conducting, current flows through the primary winding and device channel to ground. As it is not conducting, core energy can be reset through the free-wheeling clamp diodes $D_{S1}$ and $D_{S2}$, and $D_Z$ to $V_{CC}$. The gate voltage signal from controller output is directly transmitted from primary to secondaries, where it is rectified and fed to main MOSFETs gates. If the primary gate pulse is at a low state, gate potentials of the main MOSFETs are clamped to source potentials by $T_1$ and $T_2$ to ensure low impedance path, and therefore zero voltage.

Some simplifying preliminary assumptions can be made before analysing the performance of the proposed circuit. First, the amplitude of $V_{CC}$ is regulated and monitored with external circuitry before supplying it to the controller, so it is initially assumed constant and reliable. Also, the internal voltage losses in the controller are low, the transformer windings are perceived to be perfectly coupled, and forward voltage drop of secondary diodes is low. These issues need to be later addressed in more detail in evaluating the complete power converter circuit and its gate drive circuitry as a whole.

The concept is expected to deliver zero to +18V output to flybacks' main MOSFETs. It may seem inconsistent towards driver design not to include negative turn-off voltage, but as component manufacturers do not require it and one of the key interests of the thesis was examining the sufficiency of different voltage levels for both turn-on and -off, zero voltage is set as a starting point for circuit design. The evaluation of the turn-off voltage decision can be discussed after the circuit simulations.

Forward converter-based gate driver design is viable, due to its well-known functionality and predictable nature. As the gate driver does not require high power levels, the design process is quite forgiving as well. Also, the available duty cycle from the forward converter (0-50% due to reset requirement) is sufficient for fulfilling DCM flyback operation. However, the concept possesses some potential problems that can be identified straight away. First, the controller output should be able to provide sufficient gate current to both transformer primary and gate of $Q_{GD}$. Second, issues of potential false triggering may have to be addressed, discussed in the last example of Section 4.2.6 and further on [65]. As negative voltage switching is not applied to the preliminary model, a sufficient margin between power MOSFET threshold voltage and turn-off voltage must additionally be revised and secured.

# 5 Gate Driver Design

This section depicts the process of composing the previously proposed gate drive circuit. Requirements for different components and their configuration are addressed from a functional power converter point of view. Furthermore, additional building blocks of the gate drive circuit are identified. These building blocks are utilized for reliable and predictable gate driver operation, where control signal requirements are identified according to special demands set by SiC MOSFETs.

Alongside the bare gate driver circuit, the design process takes into account the control of a power converter discussed in Section 2.5, as its functionality is integrated to PWM-controller, which is one of the building blocks of the gate driver. A block diagram of different sections and their relation to each other is depicted below in Figure 27. Building blocks and components defined in this section include the main MOSFETs, PWM-controller, pulse transformer, regulator, and Undervoltage-Lockout (UVLO) circuitry.

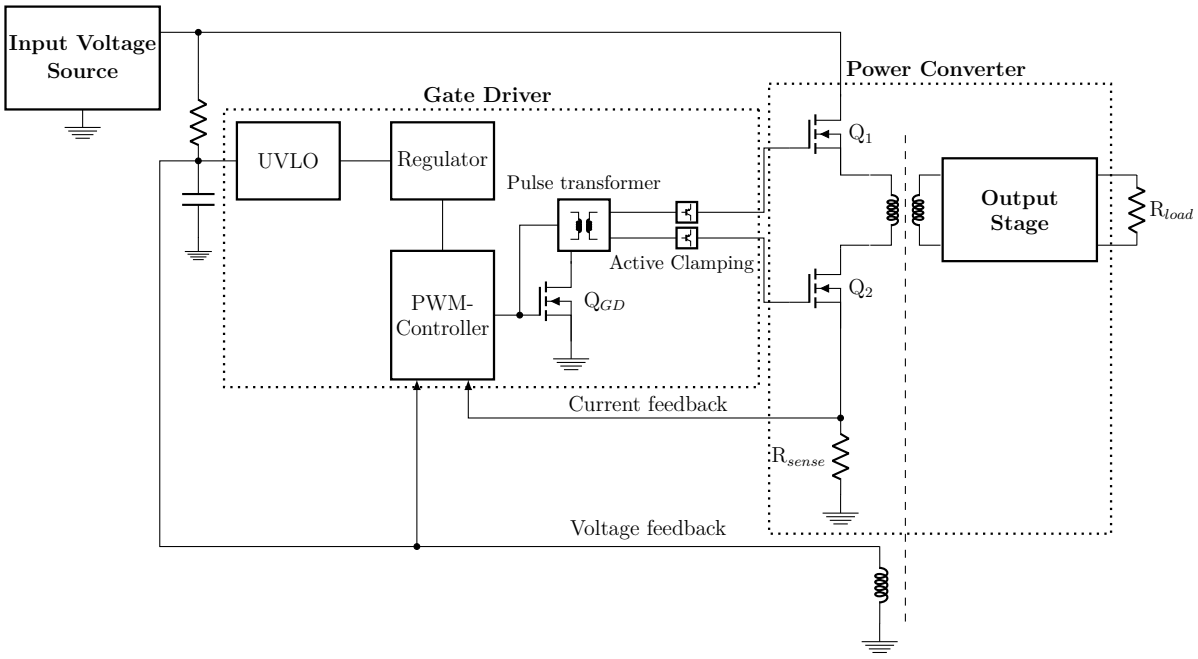


Figure 27: Block diagram of gate drive circuit and power converter.

In addition, the power converter model has some initial, application-specific requirements, which are gathered to Table 1. These preliminary requirements contain operational voltage limits, converter switching frequency, and maximum output characteristics of the converter. They have been set before the beginning of the design process to act as final objective values for the converter design.

Table 1: Preliminary requirements for the power converter.

| | |
|---|---|
| Min. $V_{in}$ | 567V |
| Max. $V_{in}$ | 1200V |
| $f_s$ | 50kHz |
| $V_{out}$ | 24V |
| $I_{out}$ | 8A |

## 5.1 Component Specification

After identifying all necessary segments of the gate driver and power converter, different components to fulfill them must be specified. This section states the selection of different component types, their values, justification of their use, and if necessary, their configuration processes.

### 5.1.1 Power MOSFETs

Power MOSFETs ($Q_1$ and $Q_2$ in Figure 27) are the main component to be addressed, while the rest of the circuit is based on their attributes. Initially, two n-channel power MOSFETs were selected, Component A and Component B. They have similar blocking voltage capabilities and current ratings, but their advised turn-on and -off voltages differ. Component A is recommended to be switched at +20/-5V while Component B at +18/0V. While switching both of them off at zero volts, the difference between preferable negative voltage and zero voltage turn-off can be evaluated.

### 5.1.2 PWM-Controller

The PWM-controller circuit selected for this application is LT1244 from Analog Devices [66]. The controller is a high-speed current mode pulse-width-modulator, with a maximum supply voltage of 25V. Under current mode control, the controller measures the transformer primary current and accordingly manipulates the PWM-output duty cycle, to regulate the power converter output. The basic operation of the control mode is presented in Section 2.5.2. Figure 28 depicts all components to be configured around the PWM-controller to achieve a stable operation of the power converter.

There are three aspects to consider while setting up the controller circuit: Setting a constant switching frequency and maximum duty cycle to desired values, as well as defining current and voltage feedbacks according to desired peak-current and output voltage.

According to the device datasheet [66], switching frequency and maximum duty cycle are determined by implementing a simple RC-circuit between the internal reference voltage pin of the component (Pin 8), oscillator frequency determination

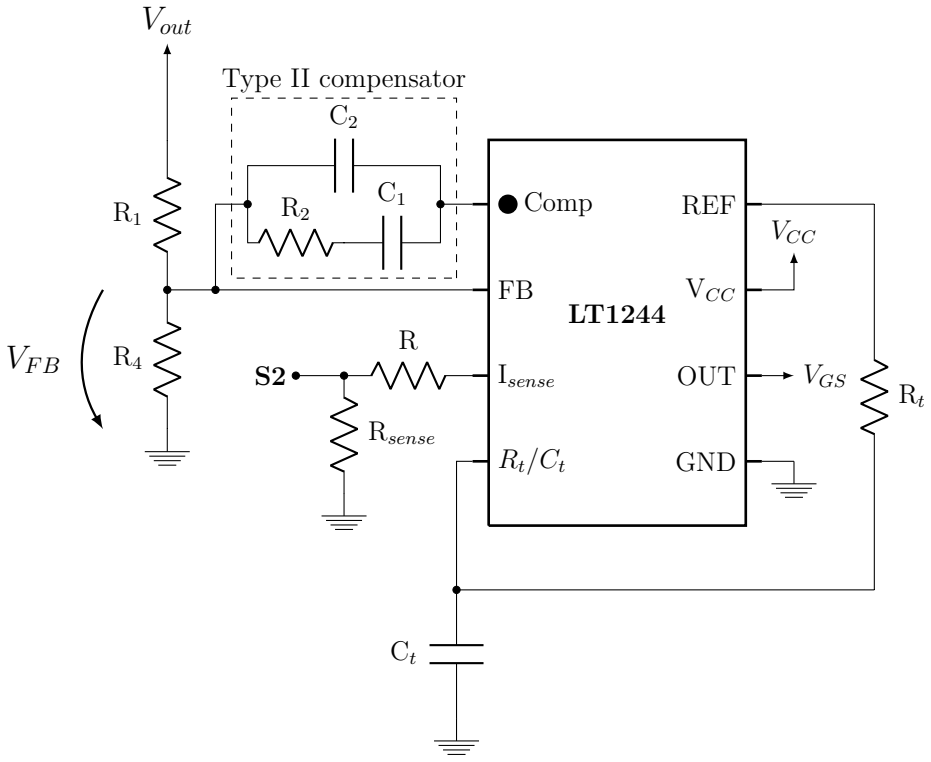


Figure 28: Controller configuration.

pin ($R_t/C_t$, Pin 4) and circuit ground. Resistors ($R_t$) and capacitors ($C_t$) values are defined according to equations found on the datasheet. For oscillator period applies:

$$T_S = t_r + t_d = 0.58 \cdot R_t C_t + \frac{3.46 \cdot R_t C_t}{(0.0164) R_t - 11.73} \tag{27}$$

Translating to switching frequency by taking the inverse of oscillation period: $f_s = \frac{1}{T_S}$. Maximum duty cycle is defined by:

$$D_{max} = \frac{t_r}{T_S} \tag{28}$$

The values of the switching frequency and duty cycle are selected according to the electrical characteristics of the utilized circuit. In this case they are: $f_s = 50$kHz and $D_{max} = 0.48$. The selected controller also limits the maximum achievable duty cycle to below 0.5, which is convenient for DCM flyback operation.

Voltage feedback is defined between compensation (Pin 1) and voltage feedback (Pin 2) pins, by implementing a compensator network to internal error amplifier of the circuit. The input voltage to a feedback pin is taken from power converter output and scaled down according to target output value with a voltage divider. The internal reference point of the error amplifier is 2.5V, so values for resistors are chosen in such manner, that target output voltage value evokes that amount to

feedback pin. Basically:

$$V_{FB} = R_4 \frac{V_{out}}{R_1 + R_4} \tag{29}$$

where $V_{out}$ is the desired converter output voltage and $V_{FB}$ set to equal error amplifier reference value, in this case 2.5V.

Compensator refers to a circuit utilized to counteract gains and phases on a feedback loop, and they are commonly used to make the overall feedback system more stable by modifying their transfer functions [67]. The chosen compensator type for this application is Type II-compensator, which consists of serial RC-circuit in parallel with a capacitor. The circuit is connected between the input and output of the error amplifier, and it flattens the feedback gain and improves phase response in the mid-frequency range. Therefore, it is most commonly utilized for current-mode control for converters operating in DCM [67].

The value of peak-current is set by a sensing resistor between lower MOSFET source and circuit ground $R_{sense}$. The resulted voltage on source potential is proportional to the current flowing through primary inductor [66]. The amount of this voltage is monitored by the current sense pin (Pin 3) on LT1244, which compares the voltage over the sensing resistor to an internal reference value [66].

### 5.1.3 Pulse Transformer

Another crucial component of the gate driver circuit is the pulse transformer. The selection of primary inductance, core type, and turns ratio should be carefully considered, as they affect whole circuit operation. Within the thesis scope, magnetizing inductance is the most crucial component, as it is a defining factor in the simulations. However, to retrieve a realistic value for that, it is reasonable to go through the whole practical design process.

The practical transformer design is an iterative process, where multiple different quantities need to be taken into account, as they are strongly dependent on each other. The process begins with a definition of turns ratio. Generally, a pulse transformer turns ratio of one is desired, as it is easier and more straightforward to utilize. In this thesis, that value is used as a starting point, and boosting options are later addressed if necessary.

The second step of the process is defining the transformer core type. The commonly used core material is a high permeability ferrite, for maximizing the magnetizing inductance and minimize the required current [46]. There are multiple different core types suitable for this purpose, so the selection is not necessarily optimal at first try. If the selected core is later found to be insufficient, the design process can be restarted from here [46].

After core selection, the number of turns for primary winding needs to be determined by making sure, that the core does not saturate. This is evaluated by a boundary condition [46], [68]:

$$B_s \mathrm{N}_P A_e > V_{in} D_{max} T_S \tag{30}$$

where $B_s$ is the core saturation flux density dependent on core material, often set to $B_s$=150mT, $\mathrm{N}_P$ the number of primary turns, $A_e$ the cross-sectional area of core, $V_{in}$ the primary input voltage, $D_{max}$ the worst-case duty cycle and $T_S$ the duration of switching period. Equation (30) is derived in Appendix A.

Practical transformers also have imperfect characteristics, that have to be accounted for during their design process. Compared to an ideal transformer, core permeability is not infinite, and core material suffers from losses. Due to permeability, a magnetizing current is needed for establishing a flux within the core [69]. Magnetizing inductance $L_m$ is used for representing the core magnetization phenomenon and can be generally thought of as inductance seen on transformer primary [4]. In this thesis, magnetic inductance is carefully considered, as it is the most crucial pulse transformer parameter in simulations. Generally, the equation for magnetization inductance can be written to be:

$$L_m = \frac{\mu_r \mu_0 A_e \mathrm{N}_P^2}{l_e} \tag{31}$$

where $L_m$ is the magnetizing inductance, $\mu_r$, and $\mu_0$ the permeability of magnetic material and vacuum respectively, $\mathrm{N}_P$ the number of primary turns, $A_e$ the cross-sectional core area and $l_e$ the length of the magnetic path. Equation is also derived in Appendix A.

After defining the magnetizing inductance, transformer primary and secondary currents as well as their root-mean-square (RMS) values are addressed. They affect the selection of winding size, and winding losses. Primary current consists of two components, the magnetization current and reflected secondary currents:

$$I_{pri} = I_m + I_{sec}\frac{\mathrm{N}_S}{\mathrm{N}_P} \tag{32}$$

where $I_m$ is the magnetizing current, $I_{sec}$ the secondary current, $\mathrm{N}_P$ number of primary turns, and $\mathrm{N}_S$ number of secondary turns. For a transformer having two identical secondaries with the same number of turns, Equation (32) can be rewritten as:

$$I_m + \left(\frac{\mathrm{N}_{S1}}{\mathrm{N}_P} I_{S1} + \frac{\mathrm{N}_{S2}}{\mathrm{N}_P} I_{S2}\right) = I_m + \frac{\mathrm{N}_S}{\mathrm{N}_P}(I_{S1} + I_{S2}) \tag{33}$$

where $I_{S1}$ and $I_{S2}$ are the individual secondary currents, and $\mathrm{N}_{S1}$=$\mathrm{N}_{S2}$=$\mathrm{N}_S$ the number of secondary turns. Magnetizing current is calculated from voltage over an inductor (Equation (2)) by utilizing magnetizing inductance, and it reduces to:

$$I_m = \frac{V_{in} D T_S}{L_m} \tag{34}$$

The peak value of magnetizing current can be retrieved when the duty cycle is at its maximum value of $D_{max}$.

Transformer secondary currents $I_{S1}$ and $I_{S2}$ can be approximated according to peak values of MOSFET gate currents, defined on Section 4.2.1 by Equation (23).

There is some additional current flowing to the base of the clamping BJT, which adds up to the secondary current $I_{sec}$, but it is neglected.

Peak gate current is defined by MOSFETs gate charge and required transition time to charge up the gate. Maximum transition time $t_{tr,max}$ is defined in this context according to component datasheet values, by adding the rise time and turn-on delay together. By also retrieving the total gate charge of components, maximum secondary currents can be determined for different components (Table 2).

Table 2: Component characteristics and gate current.

| | $Q_G$ | $t_{tr,max}$ | $\hat{I}_G$ |
|---|---|---|---|
| Component A | 13nC | 16.5ns | 0.79A |
| Component B | 14nC | 37ns | 0.38A |

Now, as maximum transformer secondary currents are known, the peak of the reflected current component can be calculated. Secondaries are perceived to be approximately identical and equally loaded, therefore:

$$\frac{\mathrm{N}_S}{\mathrm{N}_P}(\hat{I}_{S1} + \hat{I}_{S2}) \approx 2\frac{\mathrm{N}_S}{\mathrm{N}_P}\hat{I}_G \tag{35}$$

so the reflected current depends on turns ratio and component-specific peak gate current. Turns ratio dependence has to be accounted for if one to one turns ratio is perceived insufficient during testing.

Now, as the peak currents for both the magnetizing current and reflected currents are known, different transformer winding types can be evaluated. For the windings, the RMS-value of current defines their requirements, so initially the waveforms of primary and secondary currents should be known to compose them. The primary current consists of previously defined components, magnetizing current and reflected secondary currents. The waveform of the magnetizing current is similar to one presented in Figure 25, so its component to primary is a simple sawtooth wave fluctuating between zero and $\hat{I}_m$. During the turn-off period, reducing magnetizing current flows through demagnetization diodes and Zener ($\mathrm{D}_{S1}$, $\mathrm{D}_{S2}$ and $\mathrm{D}_Z$ in Figure 26) instead of the primary winding, so its magnitude is not accounted here.

As previously stated, transformer secondary currents are approximated as MOSFETs gate currents, that charge up the gates during turn-on. Their waveforms for turn-on and turn-off are sketched on Figures 12 and 13 according to information found on [29], [39], and can be viewed as narrow triangles, where peak value is reached at the instant of pulse turn-on (Figure 29). The duration of the gate current transient is equal to maximum transition time $t_{tr,max}$, and maximum amplitude equals previously defined peak values of $\hat{I}_G$. It is notable, that secondary currents are individually accounted for when considering secondary winding specifications, but the combined effect is taken into account on the primary side according to Equation (35).

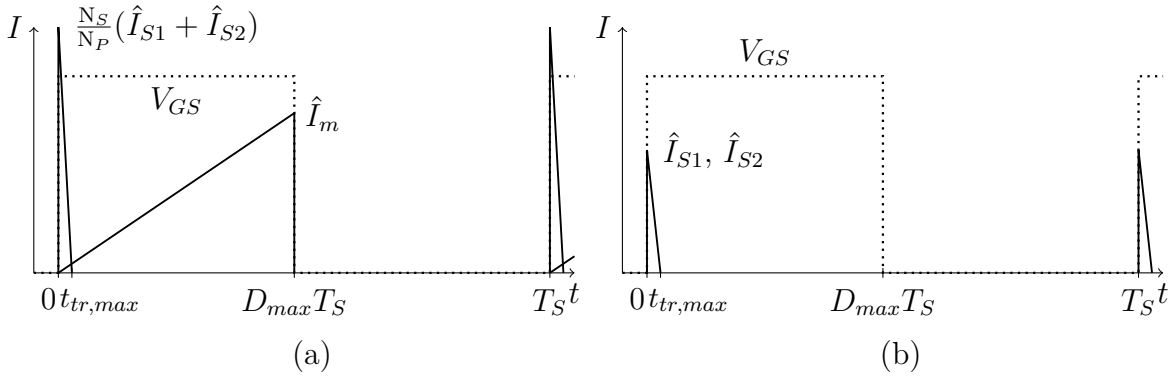


Figure 29: Illustration of the pulse transformer currents for (a) primary (b) secondary.

According to Figure 29, RMS-values for transformer magnetizing current and secondary current can be calculated similarly to sawtooth wave:

$$I_{m,RMS} = \hat{I}_m \sqrt{\frac{DT_S}{3T_S}} = \hat{I}_m \sqrt{\frac{D}{3}} \tag{36}$$

$$I_{sec,RMS} = I_{S1,RMS} = I_{S2,RMS} = \hat{I}_G \sqrt{\frac{t_{tr,max}}{3T_S}} \tag{37}$$

Accounting all primary RMS-current components together, the total current requirement for transformer primary can be attained:

$$I_{pri,RMS} = \sqrt{(I_{m,RMS})^2 + \left(2\left(\frac{N_S}{N_P}\right)^2 (I_{sec,RMS})^2\right)} \tag{38}$$

After calculating the RMS-currents, the next issue to consider is the winding size. First, it has to be made sure that all of the turns fit within the transformer winding window and then decided, how the winding is carried out. This allows the selection of winding wire gauge and type, enabling the evaluation of winding losses.

Then, transformer losses can be estimated. There are two major contributors to these losses, winding losses from the resistance of copper windings and core losses due to hysteresis in magnetic cores [5].

The amount of winding losses depends on copper volumes relation to total winding volume, thus taking into account the width of the insulation layer [5]. Constant used for depicting this value is known as copper fill factor $k_{Cu}$. As windings are perceived to be round, long cylinders, their volume relation can be calculated as [5]:

$$k_{Cu} = \frac{V_{Cu}}{V_w} = \frac{A_{Cu} l_w}{A_w l_w} = \frac{A_{Cu}}{A_w} \tag{39}$$

$V_{Cu}$ and $V_w$ are volumes of copper wire and total winding respectively, $l_w$ the length of the winding, $A_{Cu}$ the cross-sectional area of copper winding and $A_w$ the total area

of winding, including the isolation layer. Winding losses per volume are generally given by [5]:

$$P_w = k_{Cu}\rho_{Cu}(J_{rms})^2 \tag{40}$$

where $\rho_{Cu}$ is the electrical resistivity of copper and $J_{rms} = I_{rms}/A_{Cu}$ current density in the copper winding [5]. The unit of $P_w$ reduces to (W/m$^3$), so the total volume of the copper still has to be calculated in order to retrieve the losses. In this context, three winding layers consisting of the same number of turns, are perceived to be exactly on top of each other, causing the winding loop area to grow the amount winding diameter to each direction. Therefore, based on geometry, the length of the copper winding for a rectangular-shaped core increases by eight times the winding diameter per turn for each winding layer, if the layers are superposed. For three layers, consisting of one primary and two secondaries, winding lengths will approximately be:

$$l_{w1} = Nl_N \tag{41}$$

$$l_{w2} = N(l_N + 8d_w) \tag{42}$$

$$l_{w3} = N(l_N + 16d_w) \tag{43}$$

where $l_N$ is the length of one turn (from the datasheet of transformer yoke and core) and $d_w$ is the diameter of winding with insulation. By multiplying each length with copper area $A_{Cu}$, the approximation of each winding volume is attained. Then, the total winding losses are:

$$P_{w,tot} = \sum_{n=1}^{3} P_{w,n}V_{Cu,n} = A_{Cu}(P_{w1}l_{w1} + P_{w2}l_{w2} + P_{w3}l_{w3}) \tag{44}$$

Core loss occurs, as all magnetic cores suffer from hysteresis effect. As the core is magnetized, the amount of magnetic flux density $B$ and magnetic field intensity $H$ depend on current as well as initial conditions of $B$ and $H$. Their relation ($B$-$H$ curve) within the core is non-linear, as the transition between maximum and minimum values due to alternating current follow different paths during core magnetization. After magnetization is completed, the curve depicts a lagging phenomenon, called hysteresis, as flux density lags behind magnetic field intensity. Hysteresis forms a loop between boundary conditions of a $B$-$H$ curve, which represents the work done on the material by the applied field. Work is dissipated as heat within the core, referring to hysteresis loss. It is dependent on switching frequency as well as core material and volume, and can be evaluated with a modelling equation giving the core loss per volume unit [5], [69]:

$$P_{core} = k(f_s)(\Delta B)^n \tag{45}$$

where $k$ and $n$ are material specific constants, $f_s$ is the switching frequency and $\Delta B$ is the change in flux density. It can be calculated as:

$$\Delta B = \frac{V_{in} D_{max} T_S}{2 \mathrm{N}_P A_e} \tag{46}$$

Instead of material-specific constants $k$ and $n$, a graph may be given on the core datasheet, which can be similarly used for defining the core loss for specific core volume and switching frequency. Both constants depend on core ferromagnetic material and can be empirically determined [5], [69]. Value of $n$ usually varies between 1.5 and 2.5 [69].

If losses are not found to be satisfactory, core type as well as the number of turns might have to be reselected to minimize them. Otherwise, the next step of the transformer design process can be considered.

After loss estimations, leakage inductance ($L_{leak}$) of the transformer is determined. Fundamentally, leakage flux refers to the amount of magnetic flux, that is lost in the transformer due to imperfect coupling in such manner, that the flux does not completely link to primary or secondary windings [4], [5]. Transformers for high-frequency applications are often designed for minimizing $L_{leak}$, as it may cause overvoltage transients at switch turn-off [5]. Amount of leakage inductance is defined according to the volume integration, which refers to volume of the total winding [5]:

$$\frac{1}{2} L_{leak} (I_m)^2 = \frac{1}{2} \int_V \mu_0 H^2 dV \tag{47}$$

where $H$ represents the magnetic field and $\mu_0$ the permeability of free space. Equation (47) reduces according to geometry and characteristics of selected core type. For a rectangular-shaped core it can be approximated as [5]:

$$L_{leak} \approx \frac{\mu_0 (\mathrm{N}_P)^2 l_A b_c}{3 p^2 h_w} \tag{48}$$

where $l_A$ is the average length of a single turn (here $l_A = l_N + 8 d_w$, from Equation (42)), $b_c$ the width of the winding window (for three layers of wires, three times the winding diameter), $p$ the number of interfaces between winding sections (for three layers, $p$=2), and $h_w$ the height of the core.

Finally, the maximum amount of stored energy in the core is addressed, as in the proposed circuit it will be dissipated on the Zener diode ($\mathrm{D}_Z$ in Figure 26) during each demagnetization period. Magnetizing energy can be defined as [4]:

$$E_m = \frac{1}{2} L_m I_m^2 \tag{49}$$

It is also notable, that this amount of energy has to be dissipated within one demagnetization period, thus giving the average power requirement for the component:

$$P_{ave} = \frac{E_m}{(1 - D) T_S} \tag{50}$$

After all previous steps of the design process, a prototype would preferably be assembled, making it possible to measure frequency response and then test the transformer in a circuit to determine its efficiency and thermal characteristics [68]. However, within the thesis scope the design process stops here and attained parameters for magnetization inductance and other characteristics are utilized on simulations. The whole process is depicted here in order to verify, that the magnetizing inductance for the selected core is applicable for the proposed circuit. Example of the design process yielded the following characteristics for the transformer:

Table 3: Transformer properties for selected core [70], [71].

| Parameter | Quantity |
|---|---|
| Core type | EFD20/10/7 |
| Number of turns | 38 |
| Magnetizing inductance | 1.73mH |
| Primary RMS-current (max) | 44mA |
| Secondary RMS-current (max) | 13.1mA |
| Winding type | 29AWG |
| Winding losses | 0.6mW |
| Maximum core flux | 73.34mT |
| Core losses | 36.5mW |
| Leakage inductance | 0.49uH |
| Zener dissipation | 0.83W |

### 5.1.4 Auxiliary Voltage Regulator

To make sure that the amplitude of gate pulses remains predictable and stable on all instants, a linear regulator is added to the gate drive circuitry. The regulator supplies the operating voltage to the controller, which is used for further supplying the pulse transformer. As voltage is set to a constant value, the supply voltage should remain stable at all times.

The selected component is LT317A from Linear Technology / Analog Devices [72], as it possesses high output current capabilities with adjustable output voltage. It is a simple three-terminal voltage regulator, where the desired output voltage is set by utilizing voltage division with two resistors between output and adjust pins, and circuit ground.

Selected amplitude for regulator output supplying the controller is 18.5V. This value was selected so that the maximum supply voltage of the controller would not be exceeded. Also, as controller's voltage output is limited to 18V, and little to no internal voltage drop occurs, the selected value was perceived to be sufficient.

### 5.1.5 Undervoltage-Lockout Solutions

Undervoltage-lockout (UVLO) is a function used to disable a device if a supply voltage reduces below a specified operational limit. It is generally needed, as many

circuits require a certain minimum operation voltage to guarantee their correct functionality [73]. Many integrated circuits include function by default, but it can be implemented externally as well. A common manner to do so is with a comparator circuit, set to supervise the operational voltage limit and disable the circuit or its supply as the operational limit is reached, for example by using a transistor from comparator output [22].

Typically, UVLO-circuits are designed to include some degree of hysteresis. This means, that the start-up and shutdown voltage limits intentionally differ from each other. Hysteresis is added, because when a device is turned on, it draws current, often causing the supply voltage to drop. Without hysteresis the start-up voltage would drop immediately below the specified limit, turning the device off again [73]. On the selected controller (LT1244), the aforementioned UVLO hysteresis boundaries are 16V for start-up and 10V for shutdown [66].

In this thesis, UVLO-function is utilized as the final structural block of the gate drive circuit to limit the minimum amplitude of gate pulses of MOSFETs. This is desirable for ensuring, that the MOSFETs are never switched partially on or off. Especially the aforementioned voltage drop situation is problematic during start-up and requires a prominent amount of focus. There are unlimited possibilities for implementing the functionality, but in this context, two different solutions are compared to a solution without any external UVLO-circuit, shown in Figure 30. Proposed circuits form three different solutions, where Solution 1 does not feature external UVLO-circuitry, and Solutions 2 and 3 include different UVLO-variations.

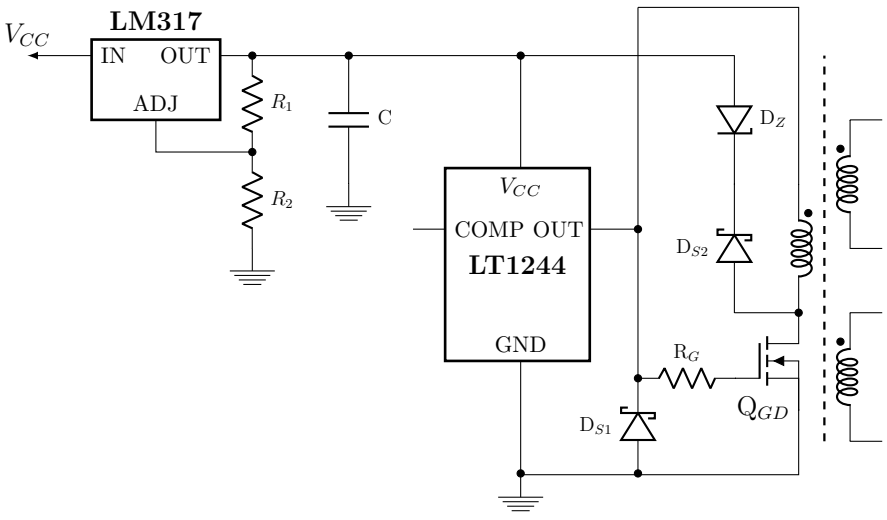


Figure 30: Solution 1. Primary side of the gate driver concept, utilizing the auxiliary voltage regulator. There is no external UVLO-circuitry implemented.

If external UVLO is not implemented, internal UVLO limits of the selected controller apply. This corresponds to a situation, where the first pulses are released when the supply voltage $V_{CC}$ is 16V. Correspondingly, if $V_{CC}$ reduces to 10V, pulses are cut-off. Therefore, the minimum gate voltage requirement for SiC MOSFETs, 18V, is often not met.

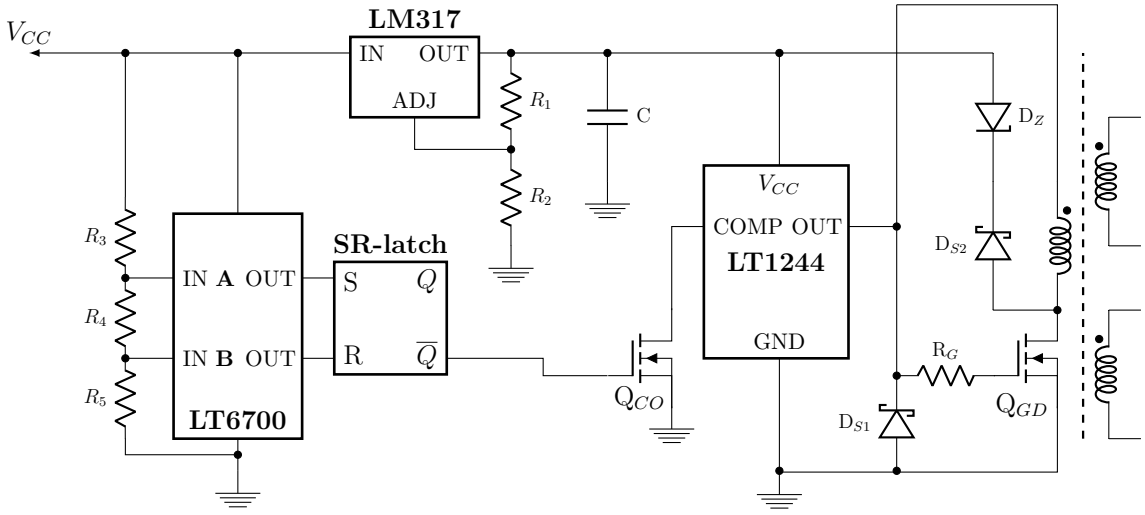


Figure 31: Solution 2. Dual-comparator LT6700 creates start-up and shutdown boundaries, which are utilized by controlling $Q_{CO}$ through a SR-latch circuit.

The first circuit with UVLO-implementation (Solution 2 in Figure 31) utilizes a few components, such as a dual comparator circuit (LT6700HV from Linear Technology [74]), set-reset (SR) latch (flip-flop) -circuit and a simple MOSFET transistor. The fundamental concept is based on monitoring the input voltage to the regulator and disabling the controller if the voltage is not within an acceptable operational window. Monitoring is implemented, by setting the boundary conditions for start-up and shutdown voltage to dual-comparator circuits inputs, with respect to the internal reference voltage. The comparator's output signals are then fed to the SR-latch circuit, which is capable of storing information within internal transistor states, according to its input values [69]. As a start-up boundary is reached, the SR-latch output signal $Q$ is switched from low to a high state and inverse $\overline{Q}$ from high to low, enabling the controller. Accordingly, as shutdown boundary is reached, inverse $\overline{Q}$ is switched from low to high, disabling the controller. Thus, the use of SR-latch also possesses an opportunity of using the inverse signal of logical states, as it has two outputs which are always in opposite states [69].

Enable and disable functions are fulfilled by controlling a small n-channel MOSFET, an enabler MOSFET ($Q_{CO}$), connected between controllers COMP-pin and circuit ground. By default, the inverse of logical SR-latch output signal $\overline{Q}$ is connected to the gate of the MOSFET, thus grounding the COMP-pin if adequate start-up voltage has not been reached. While COMP-pin is grounded, the controller may be powered up, but no gate pulses are transmitted forward. As the voltage window is reached, the MOSFETs gate signal is terminated and gate pulses are released.

The solution creates an UVLO-circuit with adjustable boundaries and hysteresis. However, as controller circuit powers up when the supply voltage exceeds its internal start-up limit, it consumes current on this standby mode, even though it does not release any gate pulses forward.

The next solution (Solution 3 in Figure 32) attempts to eliminate the inconvenience of standby current consumption. The general idea behind it is similar to the other

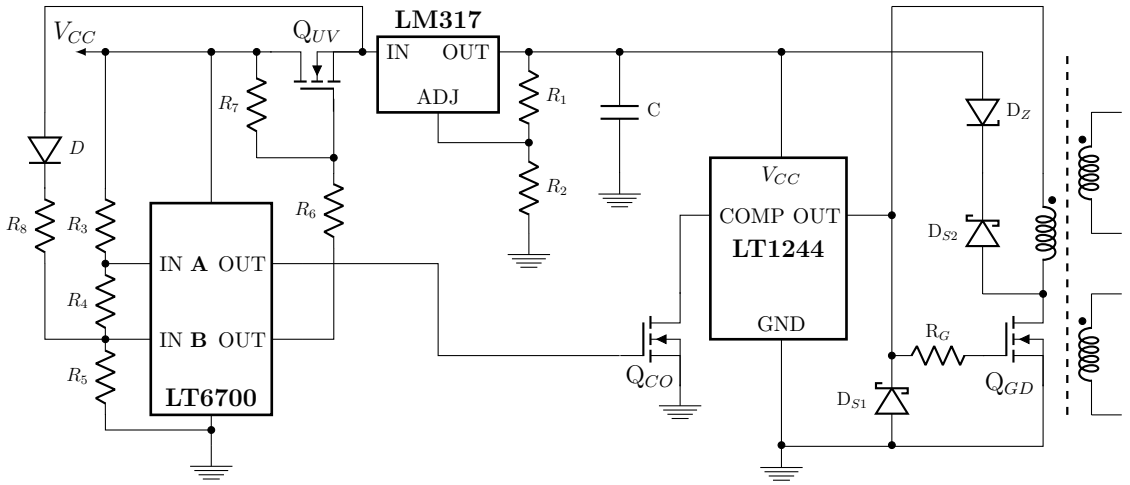


Figure 32: Solution 3. MOSFET $Q_{UV}$ is set to disable the supply, if voltage boundaries set for $V_{CC}$ are not fulfilled.

UVLO-solution, but the SR-latch is eliminated, and instead the supply voltage to the regulator ($V_{CC}$) is cut-off using a voltage supervision MOSFET ($Q_{UV}$). The MOSFET functions as a gateway of supply voltage: as defined start-up voltage is reached it starts to conduct. Similarly, if supply voltage reduces below shutdown voltage, it stops conducting. In addition to supply voltage monitoring, another comparator output is used to control the MOSFET $Q_{CO}$, connected between the COMP-pin of the controller and circuit ground similar to the first solution. Supervision ensures, that the gate pulses are terminated after the supply voltage is cut-off, as there is some energy stored in a capacitor connected to controller operation voltage potential. The capacitor cannot be removed, as it keeps the operating voltage steady and reduces voltage ripple.

Connected to the voltage supervision MOSFETs ($Q_{UV}$) source potential is a diode, which feeds the voltage back to comparator input. Feedback is required, as otherwise the supervision MOSFET would not remain in a conductive state after reaching start-up boundary voltage. As in the previous solution, also in this one the amount of hysteresis, as well as voltage boundaries can be freely defined.

## 5.2 Simulations

Simulations were carried out using the LTSpice simulator tool provided by Linear Technology / Analog Devices Corporation. Simulation models were based on the building blocks identified and profoundly characterized in Section 5.1. Models consisted of both the power converter section, as well as the discussed gate driver proposal, featuring different UVLO-solutions.

Specific component models for SiC MOSFETs A and B were composed to LTSpice with information found on the component datasheets. Addressed quantities included for example component on-resistance $R_{DS(on)}$, threshold voltage $V_{th}$, internal gate resistance $R_G$, and parasitic capacitances ($C_{DS}$ and $C_{GS}$). Models were based on

the switch-model of LTSpice and created according to information found on [75]. Differences in their characteristics are presented in Table 4.

Table 4: List of defined simulation parameters for SiC MOSFET models.

| Parameter | **Component A** | **Component B** |
|---|---|---|
| On-resistance ($R_{DS(on)}$) | 1Ω | 1.15Ω |
| Threshold voltage ($V_{th}$) | 2.6V | 2.8V |
| Gate resistance ($R_G$) | 24.8Ω | 64Ω |
| Drain-source capacitance ($C_{DS}$) | 11pF | 10pF |
| Gate-source capacitance ($C_{GS}$) | 189pF | 176pF |

Composed MOSFET models were utilized in a two-switch flyback converter, with attributes corresponding to Table 1. In addition, PWM-controller, pulse transformer and regulator were implemented to the model according to Section 5.1.

Flyback converter sub-circuit and secondary side of the gate transformer were kept identical between all solution models, and potential needs for modifications are discussed after retrieving the simulation results. By keeping the framework constant, differences between the proposed solutions can be identified, and evaluation remains comparable.

### 5.2.1 Evaluation Criteria

Simulation results were evaluated in terms of three quantities, gate voltage on-state voltage level, its variation at different operation points, and gate off-state voltage level. First of all, due to SiC MOSFETs high on-state gate voltage requirement presented in Section 3.3, voltage amplitude was monitored at power converter start-up, steady-state operation, and shutdown. Therefore, an acceptable minimum limit for amplitude had to be defined for the simulations.

The definition begins from the effect of low amplitude: Low amplitude gate pulses increase internal channel resistance ($R_{DS(on)}$), thus increasing conduction losses. On-resistance produces a voltage drop over the device channel, which depends on the gate voltage amplitude. If the voltage drop and channel current are known, component power dissipation can be evaluated. Characteristics differ for selected components but required information is given on device datasheets. Therefore, a compromise can be found by examining power dissipation estimates for different gate voltages.

In Table 5, total component power dissipation $P_D$ is approximated for selected MOSFETs at room temperature. Converter start-up instant is used as a reference when the maximum value of current flows through the MOSFETs. Third and sixth column scale the value of power dissipation compared to the optimal gate voltage case, depicting how much $P_D$ increases as $V_{GS}$ reduces.

From Table 5, an acceptable worst-case limit was selected to be 16V. The selection indicates the absolute minimum amount of $V_{GS}$ at MOSFETs gate during on-state, while previously defined 18V remains a target value for steady-state converter

Table 5: Component power dissipation for different gate voltages.

| **Component A** | | | **Component B** | | |
|---|---|---|---|---|---|
| $V_{GS}$ [V] | $P_D$ [W] | % | $V_{GS}$ [V] | $P_D$ [W] | % |
| 20 | 14 | 100 | 20 | 14.4 | 100 |
| 18 | 17.5 | 125 | 18 | 17.2 | 119.5 |
| 16 | 21 | 150 | 16 | 21.4 | 148.8 |
| 14 | 28 | 200 | 14 | 45.5 | 317.1 |
| 12 | 70 | 500 | 12 | - | - |

operation. Selected limit ensures, that worst-case power dissipation is at most 150% of steady-state operation.

The second criterion is the consistency of voltage amplitude between the simulated time instants, or the variation of on-state voltage between operating points. Fundamentally, the amplitude values should differ as little as possible, but the solution types are prone to some extent of variation between steady-state and shutdown for example. Since the lower boundary of the gate amplitude was set to 16V and the aim of operation to 18V, a variation boundary of ±2V was selected for evaluation. However, as the effect of this quantity does not determine the safe operation of a converter, the main concern towards converter operation is emphasized in the other two criteria.

The third quantity evaluated during simulations was how well the off-state voltage remains at zero. Aspect is crucial, as threshold voltages of SiC MOSFETs are generally low, and even unstable on high temperatures (Section 3.3). According to device datasheets, nominal threshold voltages for selected components differ from 2.4V to 2.8V, but with 150°C junction temperature, they may decrease down to 1.4V and 1.6V respectively.

Due to high variation on the threshold voltage, turn-off voltage should remain exactly at zero, to achieve at least a little margin between the worst-case conduction boundary and turn-off voltage. If the active clamping functions properly, the turn-off voltage should have no problems to remain at zero volts.

The three aforementioned evaluation criteria were perceived as sufficient in evaluating the device operation. Additionally, appropriate power converter operation was ensured during testing, referring to requirements presented in Table 1 being met at all times.

# 6 Simulation Results

This section depicts the results derived from simulations for different solutions, supply voltages, components, and time instants. Additionally, it discusses some of the solution specific advantages and disadvantages, as well as evaluates the evolution potential of each proposed solution. Results for each of the proposed solutions are presented in Table 6.

Table 6: Simulation results.

| **Solution 1:** | | **Min. Gate Voltage** | | |
|---|---|---|---|---|
| Component | Supply [V] | Start-up [V] | Steady-state [V] | Shutdown [V] |
| A | 567 | 14.2 | 16.8 | 8.7 |
| A | 1200 | 12.3$^{(1)}$ | 16.5 | 8.7 |
| B | 567 | 14.2 | 16.8 | 8.7 |
| B | 1200 | 12.3$^{(1)}$ | 16.5 | 8.7 |
| **Solution 2:** | | **Min. Gate Voltage** | | |
| Component | Supply [V] | Start-up [V] | Steady-state [V] | Shutdown [V] |
| A | 567 | 16.5 | 16.5 | 14.9 |
| A | 1200 | 16.5 | 16.5 | 14.9 |
| B | 567 | 16.5 | 16.5 | 14.9 |
| B | 1200 | 16.5 | 16.5 | 14.9 |
| **Solution 3:** | | **Min. Gate Voltage** | | |
| Component | Supply [V] | Start-up [V] | Steady-state [V] | Shutdown [V] |
| A | 567 | 16.5 | 16.5 | 14.8 |
| A | 1200 | 16.5 | 16.6 | 14.8 |
| B | 567 | 16.5 | 16.5 | 14.8 |
| B | 1200 | 16.5 | 16.5 | 14.8 |

## 6.1 Solution 1

The first gate driver solution does not include an Undervoltage-lockout implementation, so turn-on and turn-off limits are solely set by the internal limits of the PWM-controller (Figure 30). This leads to issues especially during turn-off transients, as controllers internal UVLO-limits are 16V at start-up, and 10V at shutdown. As seen in Table 6, during start-up and shutdown the gate pulses are below these limit values, due to voltage drop caused by the controller, pulse transformer, and secondary diodes.

With a 1200V supply, second and third gate pulses reduced surprisingly low. The phenomenon is visible on all instants with 1200V supply, marked with $^{(1)}$ in Table 6. The maximum supply voltage corresponds to the lowest duty cycle, so narrow pulses were expected, but phenomena cannot be explained comprehensively with a low duty cycle. The waveform of the occasion is depicted in Figure 33 for the first solution.

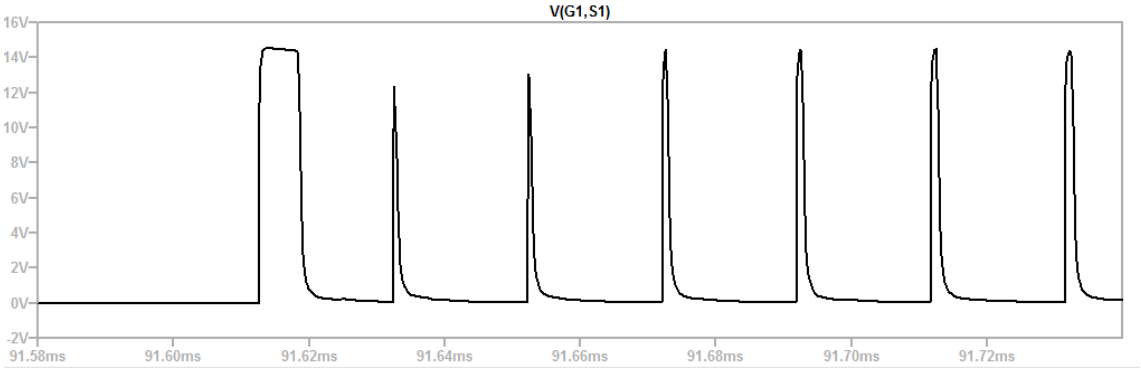


Figure 33: First few gate pulses with 1200V supply [(1)] (Solution 1).

The situation is problematic, as during a start-up the power converter fundamentally operates on CCM, therefore the current through the MOSFETs is at its maximum. Also, according to power dissipation criteria defined in Section 5.2.1, such low gate pulses can not be accepted. In addition, the phenomenon was quite common, as it occurs at every start-up with a high supply voltage. The problem was first traced to the controller output, indicating that it was generated within the controller. The hypothesis was founded on the fact, that a similar gate pulse with insufficient amplitude (13.8V) was detected directly on the controller output. Also, replacing the PWM-controller got rid of the problem.

However, the root cause for the problem was not found within the controller, but rather from the combination of the controller's output capabilities, the gate resistor of $Q_{GD}$, and the selection of MOSFET $Q_{GD}$ model. The width of the gate pulse released by the controller was so narrow, that the MOSFETs gate could not be charged during that time period, causing the voltage amplitude to eventually be insufficient. The phenomenon can be avoided with careful selection of MOSFET $Q_{GD}$ and its gate resistor.

Based on simulations, there is no clear difference in behaviour between Components A and B. This can be perceived as positive, since components seem to be coincident with each other, thus enabling the use of either in potential physical application.

According to the expectations, the first solution does not fit the required demands for SiC MOSFETs. The worst case is found during shutdown, where gate voltage amplitude reduces dangerously low, even below 9V. However, the third quantity to be monitored, off-state voltage, remained stable at zero volts all the time. This indicates, that active clamping on transformer secondary functions as specified.

## 6.2 Solution 2

The general model of the second solution is depicted in Figure 31, and the working principle is discussed in Section 5.1.5. The solution features an UVLO-circuit implemented for monitoring the gate voltage amplitudes and disabling the gate signal if the amplitude is too low. In addition, for this solution the MOSFET on the gate

driver proposal, $Q_{GD}$, was replaced with a model containing a smaller gate charge. The selection got rid of the undesirable start-up issue marked with (1) in Table 6 and depicted in Figure 33, thus improving the worst-case start-up amplitude.

However, the derived results indicate that specified requirements could not be met. This is due to secondary diodes forward voltage drops, that decrease the driver output voltage from 18V to around 16.5-17V at steady state. The controller output is internally clamped to 18V [66], so increasing controller $V_{CC}$ and therefore output pulse amplitude does not fix the problem. Hence, either the secondary diodes should be removed, another PWM-controller should be selected, or a boosting pulse transformer is needed.

As removing diodes would compromise the basic forward converter-based gate driver operation, it is not a viable improvement for the circuit. Additionally, many of the commercial PWM-controllers feature maximum voltage output capabilities similar or inferior to the selected LT1244. Therefore, the best option to improve the circuit is to implement a boosting transformer. It can be done simply by adding a few turns to both of the transformer secondaries, thus achieving a higher voltage output.

On a positive note, the results indicate that especially shutdown voltage amplitude was raised near to its acceptable level. Moreover, differences between measured time instants were significantly reduced altogether. This indicates, that UVLO-function implementation was successful, and its basic idea is viable for voltage amplitude supervision on a gate drive circuit. Additionally, with just slight circuit modifications, requirement specification could be met. Moreover, the turn-off voltage remained stable and low, similar to the original solution. However, despite the promising solutions, the standby current consumption issue described in Section 5.1.5 still remains.

## 6.3 Solution 3

The third solution is viewed as a whole in Figure 32, and Section 5.1.5. Its advantage compared to the second solution is the supply voltage supervision MOSFET $Q_{UV}$, used to cut-off the voltage supply $V_{CC}$ to the regulator, and further to the controller. The advantage reduces the amount of standby current consumption on both the regulator as well as the PWM-controller. The rest of the solution is similar to the first one, including the same enabler MOSFET-solution ($Q_{CO}$) to remove undesired gate pulses.

The solution shares the same problem with definitive gate voltage value as the previous solutions, as diode forward voltage drop decreases the final voltage amplitude. Nevertheless, derived results are very similar to the second solution in terms of amplitude, differences between time instants, and turn-off voltage level. Therefore, adequate means for further circuit evolution is provided.

Since the potential solutions do not fulfill the evaluation criteria for minimum gate voltage amplitude or steady-state operation, an improved circuit model is composed.

## 6.4 Solution 4

The fourth solution features the same UVLO-circuit utilized for the third solution, but the pulse transformer turns ratio is increased. An increase is carried out by adding four turns to both of the transformer secondaries, providing a boosting ratio of $\frac{N_S}{N_P} = \frac{43}{38}$=1.13. The ratio was selected to be as low as possible, since it affects the pulse transformer characteristics, as described in Section 5.1.3. Also, the ratio was simulated without going through the pulse transformer design process again. Additionally, if results would not be adequately improved, the ratio increase could be reconsidered. Simulation results are presented in Table 7.

Table 7: Simulation results for the improved solution with increased secondary turns.

| **Solution 4:** | | **Min. Gate Voltage** | | |
|---|---|---|---|---|
| Component | Supply [V] | Start-up [V] | Steady-state [V] | Shutdown [V] |
| A | 567 | 18.8 | 18.8 | 16.8 |
| A | 1200 | 18.8 | 18.8 | 16.8 |
| B | 567 | 18.8 | 18.7 | 16.8 |
| B | 1200 | 18.7 | 18.7 | 16.8 |

As simulation results in Table 7 indicate, an increased number of secondary turns combined with UVLO-functionality of the third solution yields acceptable results. Boosting action raises the entire voltage amplitude accordingly, for all time instants. Otherwise, the circuit functions as it did before.

However, additional issue considering the shutdown instant was discovered. It is very rare but may reduce the amplitude of the last gate pulse below the specified value. It was discovered on one of the last simulation rounds and is depicted in Figure 34. Grey waveform depicts the gate signal of the enabler MOSFET $Q_{CO}$, and the black waveform the gate signal of the main MOSFETs.

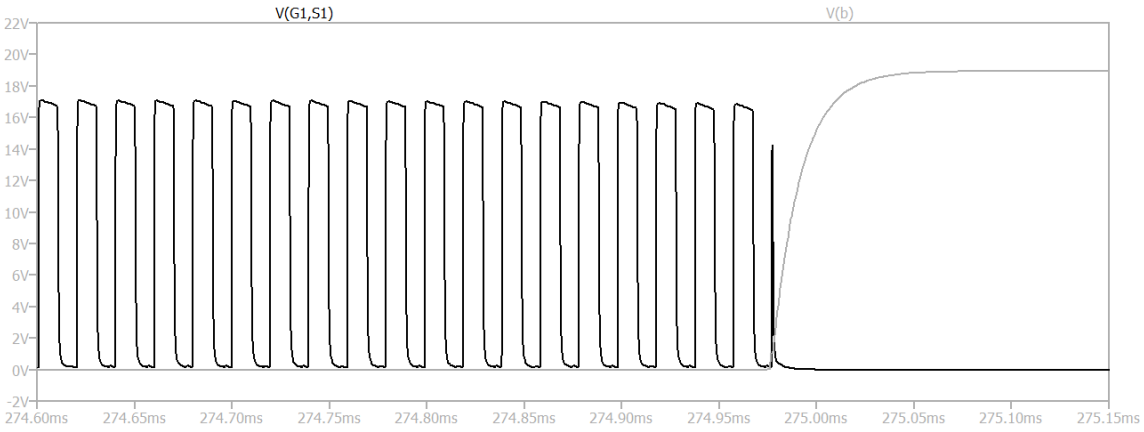


Figure 34: Poorly terminated last pulse during shutdown (Solution 4).

The problem occurs, if a gate voltage of $Q_{CO}$ is supplied when a pulse is released by the controller. Released pulse is cut-off in the middle of its rise time, so when the

pulse is terminated by $Q_{CO}$, it falls short from its nominal value. For comparison, a normal shutdown occasion is presented in Figure 35.

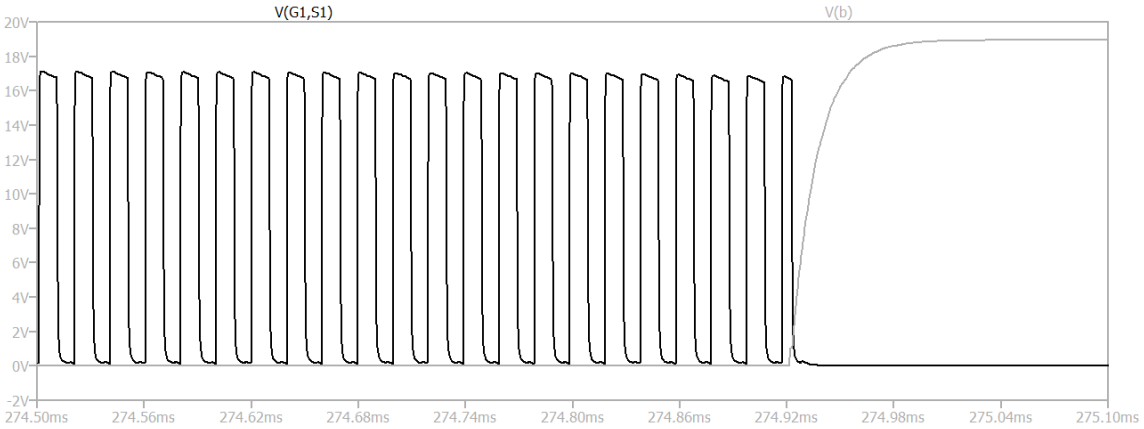


Figure 35: Normally terminated last pulse during shutdown (Solution 4).

Considering the rarity and occurrence instant of the pulse, and that the converter is shutting down there is practically little to no current flowing through the MOSFET, so the power dissipation remains low. Besides, the timing between released pulse and $Q_{CO}$ gate pulse must be within just some nanoseconds from each other for the phenomena to occur. However, identifying this phenomenon was valuable during the simulation process, so that it can be accounted for in the future. The phenomenon is most likely possible on both Solutions 2 and 3 as well since their pulse disabling is fulfilled the same way.

All in all, the fourth and improved solution fulfills all requirements for gate voltage amplitude and off-voltage stability and can be perceived as a potential candidate for further development. With this circuit solution, all requirements for a SiC MOSFET-based two-switch flyback converter can be met.

# 7 Conclusions

In this thesis, a forward converter-based gate driver circuit was proposed to be utilized in a SiC MOSFET-based two-switch flyback converter. The type of the gate drive circuit was selected due to its demagnetization properties, which can be used instead of capacitor coupling, which generates a duty ratio dependent voltage offset. In addition, the basic operation of a forward converter is well-known and predictable.

To the proposed concept, a few additional building blocks were added for fulfilling the voltage requirements set by the SiC MOSFETs. These building blocks included a constant frequency PWM-controller, a voltage regulator, active clamping, and an Undervoltage-lockout circuit. They were implemented to make sure, that the defined minimum criteria considering MOSFETs gate voltage would always be achieved, including converter start-up, shutdown, and steady-state operation.

The proposed concept was evaluated via circuit simulations, by using the LTSpice simulator tool. The differences between the building blocks induced three potential solutions, that could be simulated and compared with each other. Additionally, two different SiC MOSFET models were composed to be tested in these solutions.

The results derived from the simulations indicated the potential of the proposed gate drive concept, but also justified the use, as well as underlined the necessity of Undervoltage-lockout implementation. Demand for it was clear, as the bare forward converter-based concept was found not to be an adequate solution for fulfilling all demands set by the SiC MOSFETs.

Also, one problem considering the switching waveforms was identified. The problem occurred during shutdown and was later found to be rare and insignificant. It occurred, if the enabler MOSFET ($Q_{CO}$) received a disable signal some nanoseconds before the controller is about to release a gate pulse. The delay between the two signals could cause the gate pulse to be disabled during its rise time, thus leading to a poorly terminated gate pulse with insufficient voltage amplitude. However, during a shutdown, the amount of current flowing through the MOSFETs is zero or near zero. Therefore, the resulted heat dissipation was negligible.

The initial results indicated, that the defined minimum requirement could not be achieved with a pulse transformer with a one-to-one turns ratio, so a boosting version of the transformer was required. Requirement induced composition of an improved solution, which provided promising results by surpassing all of the defined expectations. However, it was notable that the previously mentioned problems could not be eliminated. The boosting turns ratio simply increased the worst-case voltage amplitudes to acceptable levels at all time instants.

Simulations also indicated, that the differences between the two selected SiC MOSFETs were minor, so the proposed concept would be functional with either of them. Also, the worst-case voltage amplitudes between varying time instants were found to be sufficiently consistent with each other.

Undoubtedly, there is still room for improvement. The main potential in further circuit development is affiliated with component selection and overall optimization. Additionally, some alternative circuit building blocks could be implemented to the proposed concept, but they are not speculated in this context. Components that

could be reselected include the linear regulator and the additional MOSFETs ($Q_{GD}$, $Q_{CO}$, and $Q_{UV}$) as well as their gate resistors.

The selected linear regulator functioned as specified, but a model with lower losses and reduced voltage drop could be considered. Additionally, the capacitor placed on the regulator output should preferably be scaled down. With the current solution, a large capacitor is required for keeping the regulator output voltage stable.

Also, during the design process, added MOSFETs and their gate resistors were completely ignored, even though their accurate selection could have greatly improved the gate driver functionality. Their characteristics affect overall current consumption and rise times of different control signals, that are utilized in the UVLO-circuitry. The importance of their effect was realized when investigating the origin of an initial start-up issue. The problem occurred due to hastily selected MOSFET model, which induced a few low-amplitude pulses during start-up. Therefore, both the selection of utilized MOSFETs as well as their gate resistors should have been more carefully addressed. Besides, overall circuit optimization could have always been developed further in terms of efficiency, general functionality, reliability, and cost-efficiency.

Other aspects to consider include the reliability of derived results, justification of their evaluation criteria, and potential weaknesses of the simulator tool as well as component models. The derived simulation results were consistent between different solutions, and values were almost as expected. Also, the simulated waveforms for a forward converter-based proposal matched nearly exactly with textbook waveforms, indicating that the functionality was correct.

The evaluation criteria and chosen gate voltage amplitude could have differed from selections. For the purpose of the simulations, the evaluation criteria covered all necessary segments and were perceived to be versatile and sufficiently strict for a comfortable assessment of the overall operation. However, the selected amplitude limits cause a slight degree of concern, especially during turn-off. Even though the results indicated that the active clamping was functional, negative turn-off voltage would have been needed, if the off-state voltage would not have been stable. Nevertheless, the initial selection of 0/18V switching was adequate for both components during simulations, indicating that the application could be functional in the real world. However, for verifying the functionality, the switching amplitudes should be carefully tested with a prototype.

The last aspect to consider is the simulator tool itself, and how authentically the tool and its circuit models depict the real world. Generally, LTSpice has been widely used for a long time and found to be a convenient tool for the industry as well as education. The integrated circuit models found within the program library, which were mostly utilized during the simulations, can fundamentally be found functional and reliable. However, the generated switch models possess some risks compared to internal circuit models, found within the program. Moreover, internal simulation algorithms do not reveal which of the model parameters are taken into account and which are neglected. Nevertheless, these issues are consistent between the different solution proposals, so that at least they can be compared to each other quite reliably.

For future considerations, the most important duty would be to build a functional prototype of the proposed circuit. The prototype would confirm the simulation

results, and therefore expose a lot of important information about the strengths and weaknesses of the solutions. The prototype would also help in determining the superiority of the solutions, as either of the proposed UVLO-solutions could be selected for further development. The prototype would also help more efficiently in evaluating the current consumption, reliability, size, and overall cost. Additionally, the prototyping process would potentially reveal supplementary improvement requirements, that cannot be found on simulation results. These requirements include, for instance, the possible need for negative turn-off voltage.

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# A Derivation of Transformer Equations

This section derives the equations for magnetizing inductance as well as saturation boundary conditions for both an inductor with ferrite core and a transformer.

Magnetizing inductance derivation starts from definitions of magnetic flux $\Phi$, flux linkage $\lambda$ and inductance $L$:

$$\Phi = BA \tag{A1}$$

$$\lambda = \mathrm{N}\Phi \tag{A2}$$

$$L = \frac{\lambda}{I} \tag{A3}$$

Magnitude of magnetic flux inside the inductor core is defined as:

$$B = \mu H \tag{A4}$$

where $H$ is the electric field, defined as:

$$H = \frac{NI}{l} \tag{A5}$$

where $I$ is the current flowing through the inductor. Permeability $\mu$ in Equation (A4) is defined as a product of vacuum permeability and relative permeability $\mu = \mu_0\mu_r$, latter of which is defined as:

$$\mu_r = \frac{\mu_c}{1 + \mu_c \frac{l_g}{l}} \tag{A6}$$

where $\mu_c$ is core permeability and $l_g$ length of air gap. By taking into account previous definitions, inductance can be defined as:

$$L = \frac{\mathrm{N}\Phi}{I} = \frac{NBA}{I} = \frac{N\mu HA}{I} = \frac{N\mu A}{\frac{Hl}{N}} = \frac{N^2\mu A}{l} \tag{A7}$$

where the magnetization inductance for an inductor is written as:

$$L_m = \frac{\mu_r\mu_0 A_e N^2}{l} \tag{A8}$$

where $\mu$ is permeability, $N$ number of turns, $A_e$ core cross-sectional area and $l$ length of the magnetic path.

Definition of the boundary condition for an inductor begins by searching maximum value for $H$ as a function of peak primary current $\hat{I}_{pri}$:

$$H_{max} = \frac{N\hat{I}_{pri}}{l} \tag{A9}$$

then correspondingly for $B_{max}$:

$$B_{max} = \mu H_{max} = \mu \frac{N\hat{I}_{pri}}{l} = \mu \frac{N\hat{I}_{pri}}{l} L \frac{1}{L} = \mu \frac{N\hat{I}_{pri}}{l} L \frac{l}{\mu N^2 A_e} = \frac{L\hat{I}_{pri}}{NA_e} \tag{A10}$$

So boundary condition for core saturation is retrieved as:

$$B_s N A_e > L\hat{I}_{pri} \tag{A11}$$

Similarly for a transformer, starting from voltage across an inductor:

$$v(t) = L\frac{di}{dt} \tag{A12}$$

By taking into account the constant input voltage $V_{in}$, which is applied for maximum amount of time $D_{max}T_S$. Equation (A12) can be rewritten as:

$$V_{in} = L\frac{di}{D_{max}T_S} \tag{A13}$$

and further:

$$V_{in}D_{max}T_S = L\hat{I}_{pri} \tag{A14}$$

By taking into account the boundary condition for inductance (Equation (A11)), we can conclude for a transformer:

$$B_s N A_e > V_{in}D_{max}T_S \tag{A15}$$

where $N$ equals primary turns $\mathrm{N}_P$.