HELSINKI UNIVERSITY OF TECHNOLOGY
Engineering Physics and Mathematics

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Improving the performance of a single-electron turnstile

Master's thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Technology.

Espoo, November 30, 2009

Supervisor: Prof. Matti Kaivola
Instructors: Prof. Jukka Pekola and Dr. Antti Manninen

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ABSTRACT OF MASTER'S THESIS

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Abstract:

The creation of accurate electrical current by transferring electrons sequentially from one island to another with well known frequency has been pursued by many research groups internationally for two decades. It has been demonstrated that currents, with a relative uncertainty in the 10^{-8} range, can be produced at picoampere level. However, a comparison against other electrical quantum standards would require a two orders of magnitude higher output current. The consistency check between the quantum standards is crucial for a redefinition to take place in the SI unit system. To date, it has not been possible to increase the current without losing the high accuracy.

In this thesis, the performance improvements of the so-called SINIS turnstile are studied. It is a relatively simple device but yet its potential accuracy is high according to a theoretical analysis. The two features have been obtained by combining the useful properties of superconductors and normal metals. The simplicity of the device makes it possible to parallelize these devices as is experimentally demonstrated in this thesis by operating ten devices simultaneously. This yields a current exceeding 100 pA, sufficient for the comparison.

Although the theoretical analysis predicts low error rates in the $10^{-7} - 10^{-8}$ range for the turnstile, in experiments, the accuracy has been limited to 10^{-4} or above due to an unknown leakage process. This leakage can be phenomenologically explained by extra states in the superconducting gap which ideally should have no electronic states present. Yet, the true origin of these states is not known. In the second part of this thesis, a study of the leakage is done. The theoretical analysis shows both analytically and numerically that the electromagnetic environment can produce similar features as the phenomenological model. In addition, it is experimentally shown that one can suppress the leakage by an order of magnitude in the turnstiles by screening out the effect of the environment. This is a strong evidence that the leakages at this level arise from electromagnetic environment.

The main implication of the thesis is that the hybrid turnstile is most likely to succeed in having a higher output current but still retain the high accuracy. As an outcome of this thesis, it can be estimated that in its present form, the turnstile can reach a current of at least 100 pA with a relative accuracy of at least 10^{-5}.

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Tiivistelmä:

Tarkan sähkövirran tuottaminen siirtämällä elektroneja yksitellen alueesta toiseen tunnetulla taajuudella on ollut monen kansainvälisen tutkimusryhmän tavoite kahden vuosikymmenen ajan. On osoitettu, että virtoja, joiden suhteellinen tarkkuus on 10^{-8} alueella, voidaan tuottaa pikoampeeritasolla. Vertailumittaus muiden sähkösuureiden kvanttinormaaleihin vaatisi kuitenkin noin sata kertaa korkeampia lähtövirtoja. Kyseisen vertailun antama yhdenmukaisuus on erittäin tärkeää SI-yksikköjärjestelmän uudelleenmäärittelyn kannalta. Tähän mennessä ei ole kuitenkaan ollut mahdollista kasvattaa virtaa menettämättä korkeaa tarkkuutta.

Tässä työssä on tutkittu suorituskyvyn parannuksia niin sanotussa SINIS-kääntöportissa. Se on rakenteeltaan yksinkertainen laite, mikä mahdollistaa laitteiden rinnakkaistamisen. Lisäksi teoreettisen analyysin perusteella sillä on mahdollista saavuttaa suuri tarkkuus. Nämä kaksi tarvittavaa piirrettä on saatu yhdistämällä suprajohteiden ja normaalimetallien ominaisuuksia. Tässä työssä on kokeellisesti osoitettu, että kymmentä laitetta voidaan käyttää samanaikaisesti rinnakkain. Näin saadaan virtataso, joka on yli 100 pA ja riittää siten vertailun suorittamiseen.

Vaikka teoreettinen analyysi ennustaa suhteellisen virheen olevan tasolla $10^{-7} - 10^{-8}$, havaitaan kokeissa 10^{-4} tai suurempia suhteellisia virheitä johtuen tuntemattomasta vuotoprosessista. Tämä vuoto voidaan selittää fenomenologisesti suprajohteiden epäideaalisella tilatiheydellä. Ilmiön todelliselle alkuperälle on esitetty monia teorioita. Tämän työn toisessa osiossa tutkitaan tätä vuotoa. Teoreettisen analyysin perusteella nähdään sekä analyyttisesti että numeerisesti, että kyseinen ilmiö voi aiheutua sähkömagneettisesta ympäristöstä. Lisäksi on kokeellisesti osoitettu, että vuotoa voidaan pienentää vähintään tekijällä kymmenen, kun sähkömagneettisen ympäristön vaikutus suodatetaan pois. Tämä viittaa siihen, että kyseisellä tarkkuustasolla vuoto aiheutuu ympäristöstä eikä ole suprajohteen tai itse liitoksen ominaisuus.

Tämän työn tärkein tulos on, että SINIS-kääntöportti näyttäisi olevan potentiaalinen laite, jossa korkea tarkkuus ja korkea lähtövirta voidaan yhdistää. Diplomityön tuloksista voidaan arvioida, että nykyisen kaltaisella kääntöportilla päästään vähintään 100 pA:n virtaan 10^{-5} suhteellisella tarkkuudella.

Sivumäärä: 50	Avainsanat: Sähkövirran kvanttinormaali, SINIS kääntöportti

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Contents

Chapter 1

Introduction

1.1 Quantum metrological triangle

Quantum mechanics has provided predictions and explanations to many fascinating new phenomena. Some of these phenomena can be used to measure physical quantities with extremely high precision. Voltage and resistance are two examples of quantities whose units are routinely realized with quantum mechanical effects [1, 2]. The unit of resistance can be realized with quantum Hall effect which relates voltage and current to each other via fundamental constants of nature, while the unit of voltage can be obtained from a known frequency with the Josephson effect. In this way, the units of electrical quantities can be expressed in terms of two fundamental physical constants, Planck's constant h and the charge of electron e as illustrated in Fig. 1.1.

However, one of the links in Fig. 1.1 between voltage, current and frequency, is still too weak [3]. It is the relation between current and frequency which can be realized by transferring electrons one by one. Electron pumps have been actively studied for this purpose, but no one has yet realized this link at high enough current levels and compared it to the other two effects with high precision. The realization of all these ratios together is crucially important because it will provide a consistency check for the two fundamental physical constants h and e using three independent quantum phenomena. This consistency would then allow moving towards the redefinition of the SI system of units in a more precise way with fundamental physical constants. Perhaps one day even kilogram can be defined with the help of these electrical quantities instead of the artefact which is currently in use. This could be done by comparing mechanical energy and forces to electrical ones in a watt-balance [4]. On the other hand, if the results do not agree, there must exist a physical phenomenon, perhaps a new one, responsible for this, and this result would be at least as important as the consistency.

One of the main reasons why this experiment has not been done yet is that the signals obtainable from quantum phenomena have rather low levels when compared to the noise power level in a typical measurement setup. To get accurate results in the noisy environment one would need too long averaging times in practice. The averaging time can be reduced either by increasing the signal or by carefully excluding any excessive noise sources. Typically one needs

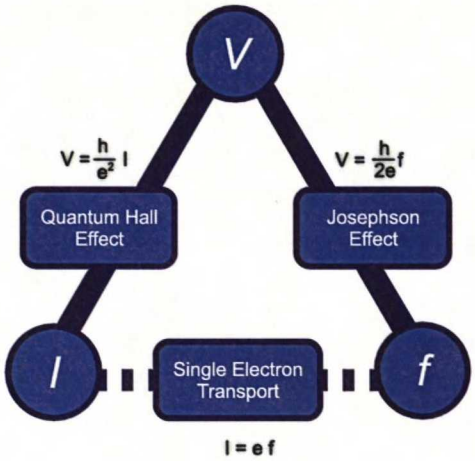

Figure 1.1: The quantum metrologial triangle connects voltage V, current I and frequency f through three different quantum mechanical phenomena and provides an independent verification for two different physical constants of nature, Planck's constant h and the elementary charge e.

both of these improvements to accomplish a precise measurement.

In the most optimal case, only Johnson-Nyquist noise [5, 6] is present. It arises from the resistance R used in the experiment and causes current fluctuations through the resistance with a uniform power spectral density $S_I(f) = 4k_BT/R$. Here k_B is the Bolzmann's constant and T the temperature of the resistor. If the relative accuracy $\delta I/I$ has to be below a certain limit, the required averaging time τ is given by

$$\tau \geq \frac{4k_BT}{RI^2\left(\delta I/I\right)^2}. \tag{1.1}$$

With a $^3\mathrm{He} - {}^4\mathrm{He}$ dilution refrigerator one can perform measurements at temperature $T = 100$ mK. It has been estimated that a resistor with a traceable resistance of the order of $R = 1$ MΩ can be used in the experiments [7, 8]. The quantum metrological triangle has to be closed with higher accuracy than that of the present SI-unit definitions of electrical units. In other words one should aim at a relative uncertainty of $\delta I/I = 10^{-7}$. This implies that with current $I = 100$ pA one needs to average for 15 h which is still within reasonable time scales from the experimental point of view. However, we notice from Eq. (1.1) that if an order of magnitude lower current is used or if one needs an order of magnitude higher precision, the averaging time grows by a factor of 100. This means that one has to average over two months which starts to be impractical.

In this thesis, it is experimentally shown that the recently discovered hybrid SINIS turnstile [9] can produce quantized output currents exceeding 100 pA by using ten parallel devices without compromising the accuracy. Moreover, the origin of the leakage limiting the relative accuracy to 10^{-4} in earlier measurements, has been discovered and methods to suppress it are demonstrated. Therefore, as an outcome of this work, the current pump is very close to fulfilling the strict requirements which the quantum metrological triangle experiment

sets.

As many other devices for pumping electrons have been suggested and demonstrated, the next section is devoted to giving a short description of these other main candidates. Then, in Chapter 2, the theory relevant to this work is presented. It consists of a brief description on how the operation of the device and most of the error mechanisms can be explained by sequential tunneling. Moreover, it is shown that the electric environment of the device can explain a phenomenological model, which was originally introduced for life-time broadening in superconductors [10, 11]. Chapter 3 is devoted to the parallelization of the devices. It consists of a description of the sample fabrication and the measurements which were used to determine device uniformity and the stability of the offset charges. Also a parasitic coupling, pronounced in parallel devices, was observed to degrade the operation. Fortunately, this coupling can be suppressed, which is also demonstrated. In Chapter 4, experimental evidence of the origin of leakage from environmental fluctuations is presented. As an outcome, the leakage determining the relative accuracy is suppressed to the 10^{-6} range where the present measurement capabilities are limiting the observation of further improvements. Finally in Chapter 5, the conclusions of this thesis are summarized.

1.2 Various approaches for pumping electrons

Single charge tunneling in normal metallic devices has been studied extensively far over two decades [12]. The operation of most of such devices is based on small metallic regions, so-called islands. At low temperatures the addition of a single electron to an island requires more energy than what thermally can be supplied. In this limit, the transport of single electrons can be controlled. The electrons are transported to and from the island through tunnel junctions, which are weak links allowing electrons to hop between the metallic regions by quantum-mechanical tunneling. The operation of these junctions is based on the overlap of electron wave functions between the two regions, which couples the two electron systems and produces tunneling.

With an array of two or more islands in series one can make an electron pump where electrons are carried from island to island one by one. To the present day, these devices have produced the most accurate transport of electrons. With a seven-junction pump, the relative error in the number of transported electrons has been only $2 \cdot 10^{-8}$ and the average hold time of electrons in a trap has been 600 s [13]. This device has been used to realize the unit of capacitance with an uncertainty of $3 \cdot 10^{-7}$ [14]. However, as the operation of the pump requires time for relaxation of the charge distribution in each step of the transport, the operation frequency is limited to 10 MHz yielding a current of the order of 1 pA only. This is not sufficient for the closure of the quantum metrological triangle. Furthermore, this type of pumps require as many RF signals as there are islands and therefore the parallelization would be a laborious task.

To overcome the requirement of having more than one RF signal, a turnstile device was proposed two decades ago [15]. The idea in this device is to inject an electron from one lead to a middle island in the first half of the cycle and push it out to another lead during the next half. A bias voltage is needed to set the preferred direction of tunneling, which poses some extra electrons

to leak through. With normal metals one has to use extra series junctions to obtain hysteretic behaviour, which suppresses unwanted electron tunneling during the cycle. The inclusion of these extra islands slows down the device and one needs to tune the inevitable offset charges of many islands to obtain the highest accuracy with this type of a pump. In this thesis, a turnstile device is also used. The difference is that instead of the extra junctions and gates used originally, the novel hybrid turnstile uses properties of a superconductor, namely the absence of electron states in the superconducting gap, to obtain hysteresis. This yields only a minor improvement in the speed, but more importantly, one needs to compensate the offset charges of only a single island, and the superconductor suppresses the harmful cotunneling of many electrons.

The current of a single turnstile device is still limited to the 10 pA range [16, 17]. To obtain even higher currents from a single device, many different ideas have been proposed. Pumps based on semiconductors have been proposed and tested [18–21]. Using semiconductors, one can construct similar devices as with metals. By applying a voltage near a doped semiconductor, one can change the potential of the system locally. Hence, a tunnel barrier can be formed by applying a large enough negative voltage. The advantage of this type of a barrier is that one can tune it by changing the voltage. This implies that in practice one could decrease the tunneling resistance of a barrier when tunneling is preferred and increase it when tunneling is not wanted. In principle, this could lead to faster and more accurate devices. However, the drawbacks of semiconducting devices lie in the same features as the advantages. As semiconductors are so tunable, it is hard to control and predict precisely all the processes in the devices. However, the semiconducting devices are still relatively simple, which, in principle, should make them feasible for parallel operation [21]. At best, a single semiconducting device has been operated either at $f = 3.4$ GHz or with a relative accuracy of 10^{-4} at low frequencies [22]. The combination of these two is still to be reached.

Even more exotic devices have been proposed to overcome the difficulties mentioned above. One of the approaches is to use surface acoustic waves (SAW) and let electrons to ride through a quantum dot or wire along with the moving energy minimum created by the SAW [23]. This approach creates a convenient way to obtain pumping at 3 GHz but the accuracy has been limited to 10^{-3} in the experiments so far. Another class of devices uses the properties of superconductivity to obtain pumping operation. One of these devices is a sluice type Cooper-pair pump, where two SQUIDs make valves for Cooper pairs and a small island with a gate electrode acts as a piston [24–26]. These devices can provide currents at a nanoampere level but the accuracy is still quite moderate. A direct current to frequency conversion taking place in a circuit consisting of Josephson junctions was proposed in Ref. [27] and electron counting in Ref. [28]. A mechanical shuttle capable of transporting electrons has also been suggested to suppress the leakages, as vacuum would be used as an insulator in the cycle [29]. The experimental data of pumping is still lacking with the shuttles. Finally, the so-called quantum phase slip (QPS) devices should be mentioned [30]. If one could build a system which is an exact dual of the Josephson junctions, it should be able to provide current plateaus similar to voltage plateaus obtained by Josephson junctions which are used in primary voltage standards in many metrology institutes. However, experimental evidence of such a dualism in RF-driven experiments has not been shown yet.

Chapter 2

Tunneling in small NIS-junctions

When two conductive metals are brought to close proximity but are still separated by a thin isolating layer, a tunnel junction is formed with finite probability for electrons to pass through it. This arises because the wavefunctions decay exponentially over the insulating barrier, and with thin enough barriers, the wavefunctions can overlap and hence have a coupling which produces the current. In this thesis, we concentrate on junctions between normal and superconducting metals which are called NIS[1]-junctions for short. First in this chapter, we will characterize the current through these junctions under an ideal voltage source and describe Coulomb blockade, which is a phenomenon unique to small structures. Then we continue by explaining the operation principle and various error mechanisms of a hybrid turnstile. Finally, we discuss how electromagnetic environment influences leakage through a junction.

2.1 Charge and heat transport by tunneling

Tunneling rates through a barrier can be calculated from the first order perturbation theory with the Fermi's golden rule approximation [31]. When using this approximation one has to make the basic assumption of perturbation theory, i.e., that the coupling between the leads is weak. One typically also uses the continuum limit, where different discrete eigenstates of the unpertubed system are approximated with a continuous spectrum of states. This approximation is valid as long as the number of free charge carriers is large as is the case in metals. In addition to these approximations, we also assume in the first part of this chapter that the energy δE obtained in transition is fixed. This energy is typically caused by a voltage across the junction, i.e., $\delta E = eV$. In very small junctions, the charging energy also contributes to this energy. The effect of the charging energy is described in Sect. 2.2 and the assumption of fixed energy change is relaxed in Sect. 2.6, where the influence of the environment is introduced.

With the assumptions mentioned above, in the case of a NIS-junction, we

[1]Normal metal - Insulator - Superconductor

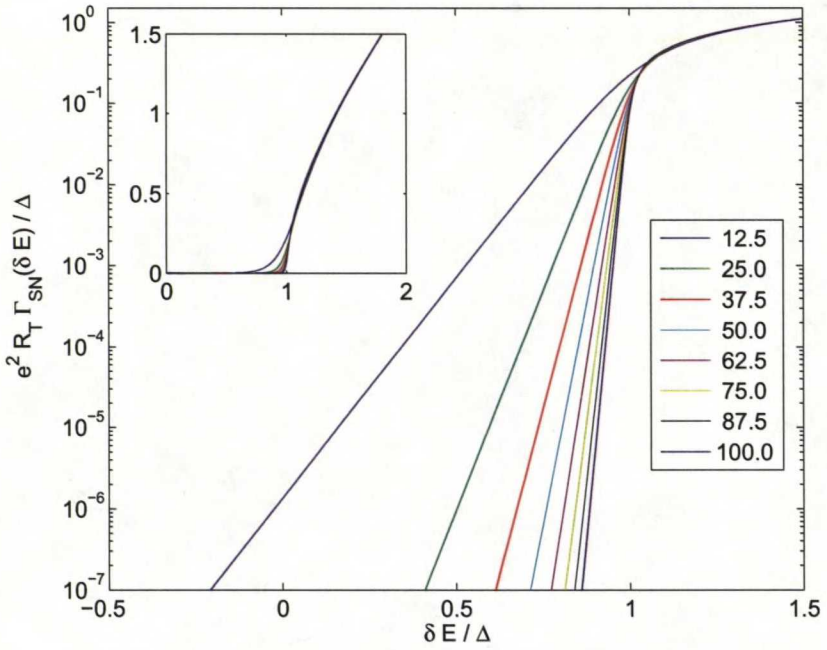

Figure 2.1: Tunneling rates in a NIS junction calculated from Eq. (2.1). The legend shows $\Delta/(k_B T_N)$, which is varied between the curves. For aluminium, $\Delta/(k_B T_N) = 25$ corresponds to $T_N \approx 100$ mK, which is a typical value obtained with dilution refrigeration methods. The inset shows a plot in linear scale from which one sees that above the threshold, $\delta E \geq \Delta$, the current is insensive to temperature. With low values, the rates are determined by an exponentially small number of thermally exited electrons in a normal metal as is seen from the main panel. The curves are relatively insensitive to variations in the temperature of the superconductor T_S. The temperature of the superconductor was taken to be such that $\Delta/(k_B T_S) = 25$. In this case, the relative amount of thermally exited quasiparticles compared to the number of quasiparticles participating in the transport in the superconductor is of the order of $\exp(-\Delta/k_B T_S) = 10^{-11}$.

get the transition rate for tunneling from a superconductor to normal metal as

$$\Gamma_{SN}(\delta E) = \frac{1}{e^2 R_T} \int_{-\infty}^{\infty} n_S(E) f_S(E)(1 - f_N(E + \delta E))dE, \qquad (2.1)$$

where δE is the energy obtained by an electron in transition, R_T is a parameter called the tunneling resistance, $n_S(E) = \frac{E}{\sqrt{E^2-\Delta^2}}$ is the BCS density of states of a superconductor with an energy gap Δ [32], $f_S(E) = \frac{1}{1+e^{-\beta_s E}}$ is the Fermi function of the superconductor where $\beta_S = 1/k_B T_S$ with T_S the temperature of the superconductor. Similarly $f_N(E)$ is the energy distribution for a normal metal. The tunneling rates at various normal metal temperatures T_N are shown in Fig. 2.1. A typical feature is that the rate becomes large only when $|\delta E| > \Delta$. This is due to the absence of electron states in a superconductor with $|E| < \Delta$

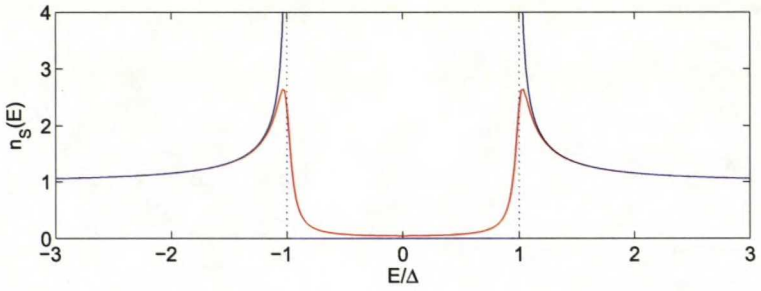

Figure 2.2: Ideal BCS density of states $n_S(E)$ in superconductor shown as solid blue line. Ideally there are no states present with $|E| < \Delta$. Red curve shows a phenomenological Dynes type density of states calculated with Eq. (2.15) and $\gamma = 0.05$. This has typically been used to model features in experiments.

which can be seen from the density of states $n_S(E)$ presented in Fig. 2.2. For tunneling from a normal metal to a superconductor we have

$$\Gamma_{NS}(\delta E) = \frac{1}{e^2 R_T} \int_{-\infty}^{\infty} n_S(E)(1 - f_S(E)) f_N(E + \delta E) dE. \tag{2.2}$$

The symmetries $f(-E) = 1 - f(E)$ and $n_S(-E) = n_S(E)$ with Eqs. (2.1) and (2.2) yield the relation $\Gamma_{NS}(\delta E) = \Gamma_{SN}(-\delta E)$. Hence, reversal of the bias, i.e., $\delta E = eV \hookrightarrow \delta E = -eV$ gives an equal rate but in the opposite direction.

Equations (2.1) and (2.2) give a very intuitive result for the tunneling rates. Let us for example consider the different factors in the integrand of Eq. (2.1). The factor $n_s(E) f_s(E)$ corresponds to the number of occupied states at energy E in the superconductor which the electron tunnels from. Similarly, the factor $1 - f_n(E + \delta E)$ corresponds to the vacant states which the electron can enter to. When summing over all possible energies E, we end up with Eq. (2.1). The prefactor of the integral describes the magnitude of the coupling, where the tunneling resistance R_T is a scale factor for the tunneling rate. It is linearly dependent on the area of the junction, on the electron densities of both sides, and on the transmission probability. From Eqs. (2.1) and (2.2) one can also see that this parameter corresponds to the asymptotic resistance observed at large voltages as the approximation $n_S(E) \approx 1$ is valid for $|\delta E| \gg \Delta$. Hence, it is a parameter that can be easily determined experimentally. For a scematic presentation of the tunneling rates see for example Ref. [33].

Similarly to the tunneling rates in Eqs. (2.1) and (2.2), we can also derive equations for the heat fluxes $\dot{Q}$ applied to either the superconductor or the normal metal from the junction. For the normal metal, we obtain

$$\dot{Q}_{SN}(\delta E) = \frac{1}{e^2 R_T} \int_{-\infty}^{\infty} (E + \delta E)\, n_S(E) f_S(E)(1 - f_N(E + \delta E)) dE \tag{2.3}$$

for tunneling from the superconductor to the normal metal, and

$$\dot{Q}_{NS}(\delta E) = \frac{1}{e^2 R_T} \int_{-\infty}^{\infty} (E + \delta E)\, n_S(E)(1 - f_S(E)) f_N(E + \delta E) dE \tag{2.4}$$

for tunneling from the normal metal to the superconductor. Equations (2.3) and (2.4) can be easily understood as deposition or extraction of particles either

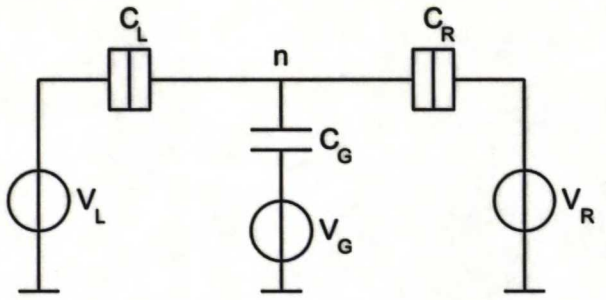

Figure 2.3: Single electron transistor consists of two tunnel junctions with capacitances C_L and C_R which are biased with voltages V_L and V_R respectively. In addition, there is coupling to the island via a gate capacitance C_G for controlling the tunneling rates with voltage V_G. The number of excess electrons in the island is n.

above or below the Fermi energy. If particles are deposited to below the Fermi energy or extracted from above, cooling will occur. The opposite processes produce heating. With NIS junctions one can have either heating or cooling of the normal metal depending on the energy change δE and temperatures T_N and T_S [34]. For calculating the heat flux for the superconductor, one has to use E instead of $(E + \delta E)$ as the deposited energy in the integrands of Eqs. (2.3) and (2.4). This leads to non-equal heat fluxes on the different sides which can be explained by Joule heating.

The heat fluxes in Eqs. (2.3) and (2.4) are important if the conductor is thermally isolated. In this case the temperature can be different from the base temperature of the experiment. With small structures at low temperatures this is typically the case as electron-phonon coupling is relatively weak and limits the thermal conduction [34, 35]. The energy transport rate from electrons to phonons can be calculated analytically [36] and is given by

$$P = \Sigma\Omega(T_e^5 - T_p^5), \tag{2.5}$$

where Σ is a material parameter, Ω the volume of the electron system, T_e the electron temperature and T_p the temperature of the phonon system. This is typically the bottleneck for heat conduction in small structures and hence other thermal resistances can be neglected as is done in this thesis by assuming that the phonon temperature is equal to the bath temperature and the temperature of the superconducting leads. It has also been assumed that the distribution functions of the electrons will obtain the Fermi-function form. This is the quasi-equilibrium limit, which might not be valid if a significant amount of transport takes place in the system [37, 38]. However, this subject is not yet well understood.

2.2 Charging energy

With small enough junctions and low enough temperatures, the discreteness of charge plays a major role in the determination of tunneling processes. In other words, the charging energy caused by the transfer of one electron in the

system becomes observable. This energy cost can prevent the transition across a junction. The phenomenon is called Coulomb blockade. One of the simplest systems where the effect can be observed is a single electron transistor (SET), which is shown schematically in Fig. 2.3. In this device we have a small island which is connected via tunnel junctions to two leads. The leads are used for applying a bias voltage across the device. In addition, it contains a capacitively coupled gate for controlling the charge transport.

Let us now calculate the energy needed by an electron to tunnel. For the electrical potential V_{island} and total charge ne of the island we can write equations

$$\begin{aligned} V_{island} &= V_i - \frac{Q_i}{C_i} \\ ne &= \textstyle\sum_i Q_i \end{aligned} \tag{2.6}$$

where $i = R, L, G$ corresponds to one of the source or gate branches having charge Q_i in the capacitor C_i. The free energy of the system is given by

$$E_{ch} = \sum_i \frac{Q_i^2}{2C_i} - \sum_i Q_i V_i. \tag{2.7}$$

Here the first sum corresponds to the energy stored in the capacitors. In addition, in the second sum the energies obtained from the voltage sources are taken into account. In other words, we are dealing with an open system where electrons can be supplied or extracted by the voltage sources. Hence, the proper free energy is the Gibbs free energy [39] which is what we have in Eq. (2.7).

Instead of considering energy as a function of the charges Q_i, it is more instructive to use Eqs. (2.6) to express it as a function of the voltages V_i and the island charge number n instead. The voltages can be considered as fixed control parameters when tunneling takes place between different charge states n. In addition, we are only interested in the energy difference which arises when n changes by one. Therefore we can neglect in Eq. (2.7) terms that do not depend on n, and after simplification we get

$$E_{ch} = E_c \left(n - n_g\right)^2, \tag{2.8}$$

where $n_g = \sum_i \frac{C_i V_i}{e}$ and $E_c = \frac{e^2}{2C}$ with $C = \sum_i C_i$. Further on, from Eq. (2.8) we can calculate the energy difference E_{ch}^+ (E_{ch}^-) required for transferring one electron into (out from) the island

$$E_{ch}^{\pm} = \pm 2E_c \left(n - n_g \pm 1/2\right). \tag{2.9}$$

The energy E_c is called the charging energy since it corresponds to the maximal energy which is needed when the system goes from the ground state to the first exited state.

The offset charge of the island, n_g, is used to shift the energy minimum of the system. This is depicted in Fig. 2.4 where the two extreme cases called gate open, or degenerate state, and gate closed state are shown. In the gate open case, n_g is set half way between two charge states so that these states are degenerate in energy. Therefore, in this case no energy penalty has to be paid when transiting between the states and that is the reason for calling it gate open. In the other extremum, n_g is set exactly to integer value. In this case the energy required is maximized to a value E_c and hence this is called

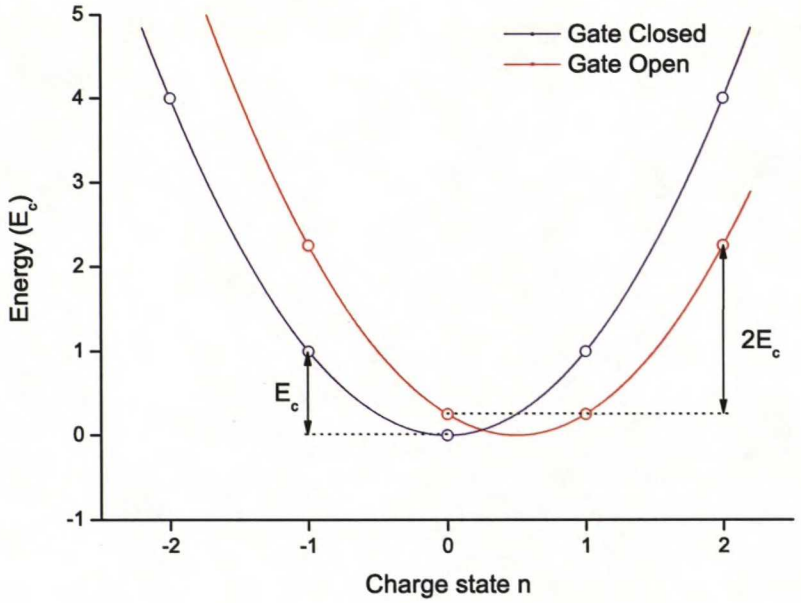

Figure 2.4: Charging energy in the cases of gate closed ($n_g = 0$) and gate open ($n_g = 0.5$). In the gate open case the energies for $n = 0$ and $n = 1$ are equal. Therefore, no energy penalty is required when moving between these states. The transitions to $n = -1$ or $n = 2$ require an energy of $2E_c$. With closed gate, only one state is at minimun energy and the energy penalty for the transition is maximized to E_c.

gate closed. The definition of n_g implies that the gate voltage V_G and the bias voltages V_L and V_R contribute to n_g. However if the transistor is symmetrical, i.e. $C_L = C_R$, and it is symmetrically biased, i.e. $V_R = -V_L$, the contribution from biasing vanishes. Therefore n_g is often also called the gate charge as it is typically controlled with the gate voltage V_G.

Equation (2.9) describes the energy change when the charge state of the island is changed without taking tunneling into account. If we consider tunneling from either the left or right bias line, we must also take into account the fact that one additional electron is transferred from or to the corresponding source in addition to the offset charges of Eq. (2.7) to compensate for the tunneled electron. Therefore, the total energy change when tunneling either from (upper sign) or to (lower sign) the island through the junction $i = L, R$ is given by

$$E_i^{\pm} = E_i^{\pm}(n) = \pm 2E_c\,(n \pm 1/2 - n_g) \pm eV_i. \tag{2.10}$$

2.3 Master equation

From Eq. (2.10) we see that the energy obtained in transition is different for different charge states. Therefore, one has to construct a way to analyse the

transitions between all different charge states. The way to do this is to describe the system with a master equation as was originally done in the so-called orthodox theory [40, 41]. By using the master equation, one loses coherence which is typical for a quantum mechanical system. However, in metals, the coherent features do not play a role in such large structures and the assumption is justified. The evolution of the probability $P(n,t)$ to find the system at charge state n at time t is given by

$$\frac{dP(n,t)}{dt} = \Gamma_{n,n}P(n,t) + \Gamma_{n-1,n}P(n-1,t) + \Gamma_{n+1,n}P(n+1,t), \qquad (2.11)$$

where $\Gamma_{m,n}$ is the transition matrix element which corresponds to the transition rate for moving from charge state m to n for $m \neq n$ and the transtition rate for moving out from state m for $m = n$. The first term in Eq. (2.11) corresponds to moving out from state n and the last two correspond to moving from state $n-1$ or $n+1$ to n, respectively. Here sequential tunneling is assumed, i.e., the charge state can change only by one when tunneling takes place. With the rates in NIS-junctions presented in Eqs. (2.1) and (2.2), the matrix elements are given by

$$\begin{aligned} \Gamma_{n-1,n} &= \Gamma_{SN}(E_L^+(n-1)) + \Gamma_{SN}(E_R^+(n-1)) \\ \Gamma_{n+1,n} &= \Gamma_{NS}(E_L^-(n+1)) + \Gamma_{NS}(E_R^-(n+1)) \\ \Gamma_{n,n} &= -(\Gamma_{n,n-1} + \Gamma_{n,n+1}). \end{aligned} \qquad (2.12)$$

It is straightforward to take into account higher order tunneling in these equations by adding more terms for a larger change of n. For example, Andreev reflection changes the state from n to $n \pm 2$ [16]. Preliminary simulation results with these second order processes are presented in Chapter 4.3 in order to explain some non-trivial features in the measured current.

Typically, electrical current through one of the leads is the experimentally observed quantity. Following the ideas of a master equation, the average current through the left junction is given by

$$I = e\sum_n (\Gamma_{LI}(n) - \Gamma_{IL}(n))P(n,t), \qquad (2.13)$$

where $\Gamma_{LI}(n)$ is the transition rate from the left lead to the island and $\Gamma_{IL}(n)$ vice versa. With sequential tunneling, these are given by $\Gamma_{LI}(n) = \Gamma_{SN}(E_L^+(n))$ and $\Gamma_{IL}(n) = \Gamma_{NS}(E_L^-(n))$ and for higher order tunneling, one has to add corresponding terms with the correct charge. Similarly, the average heat flux to the island can be written as

$$\dot{Q} = \sum_{i=L,R}\sum_n (\dot{Q}_{iI}(n) - \dot{Q}_{Ii}(n))P(n,t). \qquad (2.14)$$

2.4 Operation principle of a SINIS turnstile

A SINIS turnstile is a single electron transistor with NIS junctions [9]. The operation can be understood by considering the thresholds for tunneling. From Eq. (2.10) combined with Eqs. (2.1) and (2.2) we get for tunneling into the island the requirement $-2E_c(n+1/2-n_g) \pm eV_b/2 \geq \Delta$, and for tunneling out from the

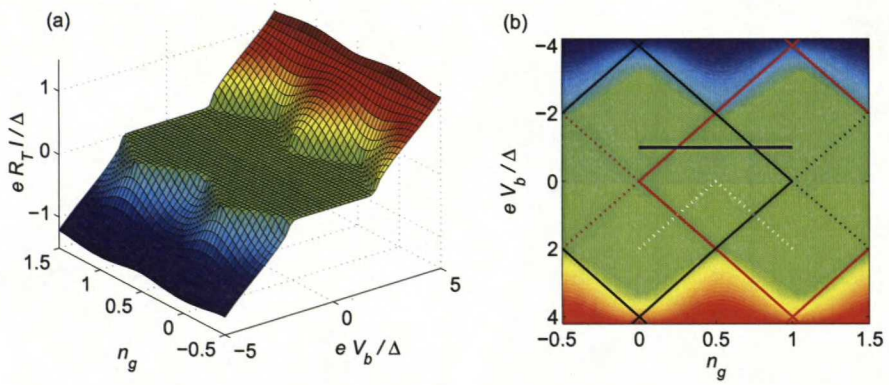

Figure 2.5: DC current-voltage characteristics of a SINIS turnstile. In (a) the current I obtained from numerical calculations is plotted as a function of bias voltage V_b and gate offset n_g. The superconducting gap suppresses the current up to $V_b = 2\Delta/e$. In addition, the Coulomb blockade provides additional suppression which is maximal at the gate closed state and minimal at the gate open state. In (b) the energy thresholds for different single electron tunneling events are plotted for states $n = 0, 1$ as black and red lines respectively. One threshold from both of the neighbouring states has to be overcome for DC current to flow. Therefore, the boxes consisting of solid lines show the stable regions for these two charge states. However, an electron can be transferred in the subgap region by changing the gate offset. One electron at a time can be brought into the island or out from it by moving the gate offset n_g over the edge of the stability region of the corresponding charge state. By moving back and forth along the solid blue line, one electron is taken from one of the bias leads and another one is deposited to the other lead. By repeating this cycle at a frequency f, a current $I = ef$ is generated. If the bias voltage V_b is varied during the pumping cycle according to the dotted white line, thermal errors will be minimized, sub-gap leakage will be avoided and higher pumping frequencies will be obtained [42]. Such a cycle has not yet been realized in experiments.

island $2E_c(n-1/2-n_g) \pm eV_b/2 \geq \Delta$. Here the total bias voltage is $V_b = V_L - V_R$ and the non-symmetrical part of the bias is included to n_g. The upper (lower) sign corresponds to the junction on the side of positive (negative) bias voltage. Compared to a SET consisting of normal metal, in the case of superconducting leads, one has to overcome the extra energy of the superconducting gap Δ. In the current-voltage curves, this feature opens up a region $|V_b| < 2\Delta/e$ with ideally no current. This is shown in the numerical simulations presented in Fig. 2.5. In Fig. 2.5 (b), the thresholds for the states $n = 0$ and $n = 1$ are shown as black and red lines, respectively, superimposed on the experimental stability diagram. The area inside the solid black (red) box shows a region where the charge state $n = 0$ ($n = 1$) is stable. Pumping of one electron in a cycle is possible by moving n_g back and forth along the solid blue line. By doing so, the thresholds of tunneling into the island from the negative side of bias and out from the positive side are crossed sequentially. Always when a tunneling event has occurred, the thresholds change as n changes. This causes the system

to prevent additional tunneling of electrons. Figure 2.6 presents a numerical simulation with a sinusoidal gate drive. It can be seen that during the first part of the cycle, the system goes from $n = 0$ to $n = 1$ by taking an electron from one lead and then, during the second part of the cycle, from $n = 1$ to $n = 0$ by extracting an electron to the other lead. Many electrons can be pumped within one cycle by increasing the RF amplitude and changing n_g by more than one.

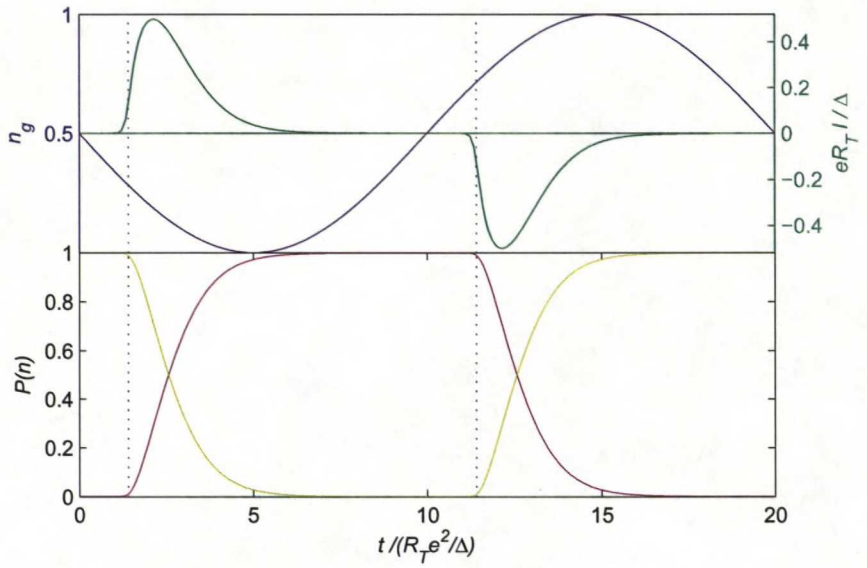

Figure 2.6: Principle of single charge transport in SINIS turnstile. In the upper inset, the alternating gate charge number n_g is shown as solid blue line as a function of time t. The thresholds for tunneling out through the right junction and tunneling in through the left junction are exceeded at time instances shown as dotted vertical lines. The currents I through these junctions are shown as solid green lines. When the tunneling threshold is crossed, the tunneling rate through that junction increases and one electron is transported. In the lower inset, the probabilities $P(n)$ of finding the island with charge state $n = 0$ (magenta) and $n = 1$ (yellow) during the cycle are plotted. The current I and the probabilities $P(n)$ obtained from the master equation represent statistical averages. The tunneling process itself is assumed to be infinitely fast [43].

2.5 Accuracy of a SINIS turnstile

There are many possible mechanisms that can generate errors to the pumped current. Some of these phenomena depend on the pumping frequency while others are frequency independent and can be considered as DC properties of the device. Many of the phenomena can be described within the sequential tunneling approximation such as effects arising from too high temperature. Also missed tunneling, backtunneling and parasitic coupling to the leads, all discussed below, can generally be understood within this approximation. The ultimate limitation to the pumping accuracy is considered to be set by higher order

tunneling processes leading to a relative accuracy of 10^{-8} at best [16]. However, in typical experiments, there is leakage in the gap of the superconductor which depends linearly on the bias voltage. This typically limits the relative accuracy to 10^{-4}. The leakage can be modelled with a phenomenological model of the density of states in the superconductor, but the true origin of this kind of behaviour has been unclear. In this section we describe the different error sources in pumping and also describe the model of the sub-gap leakage. In the next section, we demonstrate theoretically that a significant contribution of the leakage comes from the electromagnetic environment of the turnstile. This model is supported by the experiments presented in Chapter 4.

2.5.1 Frequency independent errors

Here we present errors of the turnstile that do not depend on the pumping frequency. First, we consider thermal errors caused by electrons which lie above the Fermi energy due to thermal exitation. Some of these electrons can tunnel even if the threshold is not exceeded as can be seen from Fig. 2.1 at $\delta E < 1$. This can cause either tunneling of an extra electron through the island or backtunneling of an electron against the bias voltage. The tunneling of extra electrons is pronounced with a high bias voltage while the backtunneling is more probable with low bias voltages. The rates for forward and backward tunneling can be estimated easily from the sequential tunneling model [9]. For the gate open state the former one is given by $\exp(-eV_b/(2k_BT_N))$. Correspondingly, the backtunneling is largest at the turning point of n_g where one is closest to the threshold of backtunneling. If pumping is done so that this extremum point lies half way between the forward and backward tunneling thresholds, the maximum relative rate for backtunneling is given by $\exp(-(\Delta - eV_b/2)/(k_BT_N))$. Minimizing these errors yields $eV_b = \Delta$. At this bias point, the two errors are of the order $\exp(-\Delta/(2k_BT_N))$. This corresponds to the tunneling rate at energy change $\delta E/\Delta = 0.5$ in Fig. 2.1. For aluminium, which we use as the superconductor, $\Delta/k_B = 2.3$ K. To get the error rate below 10^{-8} one should have $T_N \lesssim 50$ mK. This is obtainable with dilution refrigerators. However, as thermal coupling from electrons to the phonon environment is weak at low temperatures according to Eq. (2.5), one should take care that the island is not heated too much during the pumping. By using a varying bias as shown in Fig. 2.5 (b) (dotted white line), one obtains thermal errors of the order $\exp(-\Delta/(k_BT_N))$ corresponding to the tunneling rate at energy change $\delta E/\Delta = 0$ in Fig. 2.1. In other words, the temperature can be sligthly higher: $T_N \lesssim 100$ mK. Even by optimizing the gate drive with a constant bias so that not too much time is spent near the gate open state or the backtunneling limit, the error rate can be decreased close to this optimal case. For example, a sine wave or square wave with proper amplitude is sufficient.

By lowering the temperature, thermal errors can be suppressed to arbitarily low values. It has been shown theoretically that the ultimate accuracy is then limited by the higher order processes [16], namely the Andreev reflection and Cooper-pair - electron cotunneling. Andreev reflection can be suppressed during the pumping cycle if $E_c > \Delta$ as presented in Fig. 2.7. In this regime, the turnstile can be influenced by the Cooper-pair - electron cotunneling which is allowed for any turnstile parameters. This limits the current quantization accuracy to 10^{-8} with realistic parameter values.

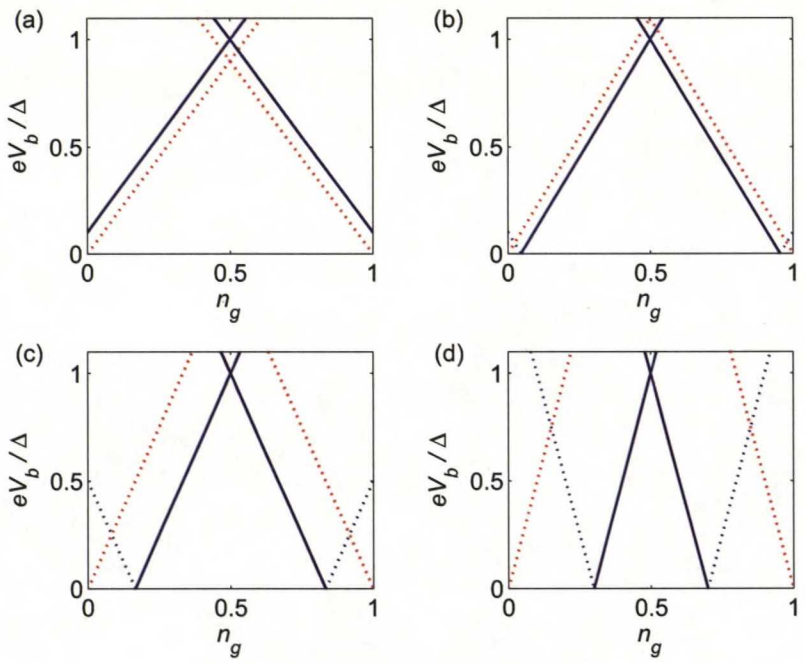

Figure 2.7: Thresholds for normal tunneling and Andreev reflection. Solid blue lines are the thresholds needed for pumping one electron in a cycle. The dashed blue lines are backtunneling thresholds and the dashed red lines denote Andreev reflection thresholds. The charging energy E_c is varied between the panels. In (a) $E_c/\Delta = 0.9$, (b) $E_c/\Delta = 1.1$, (c) $E_c/\Delta = 1.5$ and (d) $E_c/\Delta = 2.5$. With $E_c < \Delta$, one always exceeds the Andreev threshold before exceeding the normal tunneling threshold as can be seen from panel (a). Therefore in this case, Andreev reflection cannot be avoided. At $eV_b = \Delta/2$ the Andreev threshold is more limiting for the gate charge amplitude if $E_c < 2\Delta$ as in panel (c). Above that, the backtunneling threshold limits the amplitude as can be seen from panel (d). However, the Andreev threshold limit can be reached by having a varying bias voltage.

In addition to the errors mentioned above, there is an additional leakage source present in the experiments. In the DC current-voltage curves of the turnstile, this leakage can be seen as essentially a linear slope in the gap region. Correspondingly, the pumping plateaus show slopes of similar magnitude. Typically, this subgap leakage has a conductance which is $10^3 - 10^4$ times smaller than the tunneling conductance $1/R_T$ of the sample. This limits the accuracy of the current plateau to the same order of magnitude.

The leakage, which is approximately ohmic, can be described phenomenologically by the so-called Dynes model, which was originally developed to describe pair-breaking in superconductors [10, 11] but the origin of this type of noise has been unclear until to date [44]. According to the Dynes model, the ideal density of states of a BCS superconductor [32] is replaced by a broadened density of

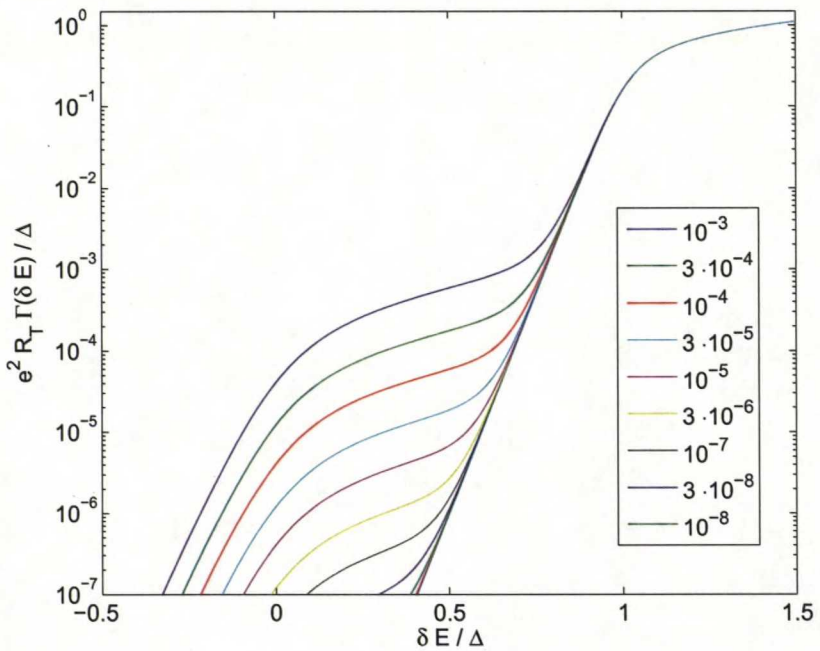

Figure 2.8: The tunneling rates $\Gamma(\delta E)$ as a function of the energy change δE when the phenomenological Dynes model is used. The parameter γ determining the number of sub-gap states present is varied between the curves according to the values in the legend. The normal metal and the superconductor are assumed to be at a temperature corresponding to $\Delta/(k_B T_i) = 25, i = N, S$. The tunneling rate can be considered to consist roughly of NIN-type tunneling with a threshold at $\delta E/\Delta = 0$ and NIS type tunneling with a threshold at $\delta E/\Delta = 1$. Below the thresholds, the rates are suppressed exponentially as the number of thermally exited electrons which are able to overcome the energy cost becomes smaller.

states

$$n_s(E) = \left| \mathrm{Re}\left(\frac{E/\Delta + i\gamma}{\sqrt{(E/\Delta + i\gamma)^2 - 1}} \right) \right|, \tag{2.15}$$

where i is the imaginary unit and one typically has $\gamma = 10^{-4}$ for thin aluminium films. This gives linear leakage in the subgap region with the conductance ratio γ between the zero-bias conductance and $1/R_T$, and therefore it fits well to the experiments and has been used in a variety of simulations to account for the observations. The linear leakage arises from a non-zero density of states with energies $|E| < \Delta$ which can be seen from Fig. 2.2. The tunneling rates $\Gamma(\delta E)$ calculated with the phenomenological density of states of Eq. (2.15) are presented in Fig. 2.8. The values of the legend denote different values of γ. With small γ, the rate is equal to that in Fig. 2.1. As γ becomes larger, approximately linear tunneling rate with respect to δE of the order of $\gamma\Delta/(e^2 R_T)$ is present when $\delta E/\Delta$ is between 0 and 1. Above threshold ($\delta E/\Delta > 1$) similar rates are

obtained as with the ideal model ($\gamma = 0$). With negative energies, the Dynes model predicts exponentially small tunneling rates. The relatively large leakage present for $\delta E/\Delta$ between 0 and 1 is most likely limiting the accuracy of our turnstiles. In Sect. 2.6 we show both analytically and numerically, how the electromagnetic environment induces this kind of an effective density of states. Further on, in the experimental part of this work, we present a verification that this leakage can be suppressed down to the $\gamma = 10^{-6}$ range, with obvious implications for the performance of the turnstile.

2.5.2 Frequency dependent errors

Above we discussed low frequency regime, but let us now turn into the influence of higher pumping frequency. Generally there is maximum operation frequency of the device for a given accuracy level. One of the errors occurs when electron tunneling is missed during a pumping cycle. This happens if the system does not have enough time to relax between the two adjacent charge states at the turnover point of n_g. Let us consider the case where only one electron is pumped during the cycle as this is the most prominent method for accurate pumping. Let us use square wave drive, as it is the simplest to analyse and yields the highest operation frequency. By assuming $T = 0$, the transition rate (2.1) or (2.2) gives

$$\Gamma(\delta E) = \frac{\sqrt{\delta E^2 - \Delta^2}}{e^2 R_T}, \tag{2.16}$$

if $|\delta E| \geq \Delta$. Otherwise the rate is zero. If we assume that the device is operated at constant bias, the frequency independent error sources described in Sect. 2.5.1 imply that one should use a value $V_b = \Delta/e$ to minimize thermal errors. Additionally, the amplitude of the RF drive has to be limited to prevent errors occuring from either backtunneling or higher order effects [16, 17]. The corresponding thresholds are plotted to Fig. 2.7. Backtunneling limits the gate amplitude to $n_g \leq 3\Delta/4E_c + 1/2$ and Andreev reflection to $n_g \leq 1 - \Delta/4E_c$ at $eV_b/\Delta = 1$. This implies that with $E_c < 2\Delta$, the Andreev threshold is more limiting, and from Eq. (2.16) and (2.10) the rate at the threshold is given by

$$\Gamma = \frac{1}{R_T C}\sqrt{1 - (\Delta/E_c)^2}. \tag{2.17}$$

For $E_c \geq 2\Delta$, backtunneling becomes more limiting and the rate at this threshold is

$$\Gamma = \frac{\Delta}{e^2 R_T}\sqrt{3}. \tag{2.18}$$

From Eq. (2.17), we see that the tunneling rate can be increased by decreasing the capacitance C of the junctions up to $E_c \approx 2\Delta$. With $E_c > 2\Delta$, the backtunneling saturates the rate with respect to C to the value given by Eq. (2.18) and higher charging energy does not increase pumping speed [17].

Using a square wave drive, one can easily solve the master equation with fixed tunneling rate and estimate the errors produced. From the exponentially decaying solution, one obtains the probability to miss an electron as $p_{miss} = \exp(-\Gamma/(2f))$, where f is the drive frequency. This implies that current for one turnstile is limited to $I = -e\Gamma/(2\ln(p_{miss}))$. For aluminium based device this means that the maximum current is limited to 20 pA with the backtunneling

limited rate of Eq. (2.18) and tunneling resistance $R_T \approx 400$ kΩ if we aim at suppressing higher order tunneling processes down to $p_{miss} = 10^{-8}$ [16].

The best way to pump electrons would be to use varying bias during the pumping cycle (see Figs. 2.5 and 2.7). The most ideal way for the cycle would be to have it parallel to the non-wanted processes and perpendicular to the wanted ones as shown in Fig. 2.5 (b) and suggested by M. Gustafsson [42]. This enables one to reach R_TC time constant limited maximum frequency also for $E_c > 2\Delta$ because the threshold of Andreev reflection can always be reached. In addition, the sub-gap leakage which is largest at gate open state would be suppressed as the voltage is lowered in this region. However, the practical realization of this type of pumping is somewhat more complex as one needs frequency $2f$ for the bias line when the actual pumping frequency is f. This requires another RF signal to the device or a rectification of the RF gate signal and tuning of the ratio which is coupled to the device. One should also note that an uncontrolled variation in bias voltage creates problems if the turnstile enters the backtunneling region with too low bias or goes to the conducting state with too high bias. In this work, it was experimentally observed that the RF gate signal can couple to the bias leads, and cause errors as will be described in Sect. 3.5.

It has been analysed theoretically and demonstrated by experiments that the normal metallic island in a SINIS system can be cooled with RF gate signal if the driving frequency is low enough, whereas too high frequency leads to heating [35, 45]. The cooling suggests that self-heating is not a major concern with proper operation regime of the device. However, the heating of the island at higher pumping amplitudes limits the maximum operation frequency of a turnstile as it gives rise to thermal errors. For this reason, the varying bias voltage will probably not make higher operation frequencies possible in practice but the the method may be useful in suppressing leakages.

One more thing that has to be taken into account when maximum operation frequency of a turnstile is considered, is that the pumping signal should not have frequency components with $f > h/\Delta$. Otherwise there will be generation of exitations into the superconductor which is likely to yield errors. This condition is easily satisfied as for aluminium the condition gives $f < 50$ GHz which is always satisfied, if the other limiting conditions for frequency are followed.

2.6 Influence from the environment

In the analysis above, a NIS-junction was considered to be ideally biased with a voltage source. However, typically there is always a finite impedance $Z(\omega)$ between the biasing source and the junction. For a linear circuit this implies that the effective bias voltage at the junction is different from the voltage at the source and there may be e.g. resistive losses in between. However, for tunnel junctions this picture is not sufficient. One fundamental physical phenomenon arising from the environment is that one cannot assume the bias source to provide fixed amount of energy to electrons which tunnel but, instead, the electrical environment can either absorb or emit energy. In this section it is shown how the environment yields an effective density of states which coincides with the Dynes model presented in Sect. 2.5.1. The analytical calculation was originally carried out by J. P. Pekola [46].

2.6.1 Energy exchange in low resistance environment

Similarly as for normal metal junctions [31], a perturbation theory calculation which takes environment into account leads to a rate

$$\Gamma_{SN}(\delta E) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} n_S(E')f_S(E')(1-f_N(E+\delta E))P(E-E')dEdE' \quad (2.19)$$

for tunneling from superconductor to normal metal. A similar generalization of Eq. (2.2) applies to opposite direction. Here $P(E)$ is a function determined by the environment and it can be interpreted as probability to receive energy E from the environment. Generally it is given by

$$P(E) = \frac{1}{2\pi\hbar}\int_{-\infty}^{\infty} \exp\left(J(t) + \frac{i}{\hbar}Et\right)dt \quad (2.20)$$

with

$$J(t) = 2\int_0^{\infty}\frac{d\omega}{\omega}\frac{\mathrm{Re}Z(\omega)}{R_K}\left[\coth\left(\frac{\beta\hbar\omega}{2}\right)(\cos\omega t - 1) - i\sin\omega t\right]. \quad (2.21)$$

Here i is the imaginary unit, $R_K = h/e^2$ and $\beta = (k_BT)^{-1}$ where T is the temperature of the environment. For resistive environment with the junction capacitance included, $\mathrm{Re}\ Z(\omega) = R/(1+(\omega RC)^2)$. With contour integrals and residue theorem, one can calculate the integral of Eq. (2.21) with this environment. The result is given by

$$J(t) = \frac{\rho}{2}[\cot B(1-e^{-|\tau|}) - \frac{|\tau|}{B} - 2\sum_{n=1}^{\infty}\frac{1-e^{-n\pi|\tau|/B}}{n\pi(1-(n\pi/B)^2)} - i\ \mathrm{sign}\,(\tau)\,(1-e^{-|\tau|})], \quad (2.22)$$

where $\rho = 2\pi R/R_K$, $\tau = t/(RC)$ and $B = \hbar/(2k_BTRC)$. According to Eq. (2.20), for $\rho \ll 1$, the linear term in τ starts affecting $P(E)$ when $\rho\,|\tau|\,/(2B) \sim 1$. As the exponential functions in Eq. (2.22) are always smaller than one, similar condition is never met and we can neglect them if $B > 1$. The condition $B > 1$ is relaxed in Sect. 2.6.3. With these approximations we have

$$J(t) = \frac{\rho}{2}\left[\alpha - \frac{|\tau|}{B} - i\ \mathrm{sign}\,(\tau)\right], \quad (2.23)$$

where α is a constant and can be fixed later by normalization of $P(E)$. By integrating Eq. (2.20) with $J(t)$ from Eq. (2.23) we get

$$P(E) = \frac{1}{\pi}e^{-\rho\alpha/2}\frac{(\rho k_BT)\cos(\rho/2) + E\sin(\rho/2)}{(\rho k_BT)^2 + E^2}. \quad (2.24)$$

The normalization $\int_{-\infty}^{\infty}P(E)dE = 1$ yields $e^{-\rho\alpha/2} = 1/\cos(\rho/2)$. Therefore Eq. (2.24) can be written as

$$P(E) = \frac{1}{\pi}\frac{(\rho k_BT) + E\tan(\rho/2)}{(\rho k_BT)^2 + E^2}. \quad (2.25)$$

With $\rho \ll 1$ this is essentially a Lorentzian distribution with HWHM of $s = \rho k_BT$. In this case, the odd part $E\tan(\rho/2)$ in Eq. (2.25), which provides

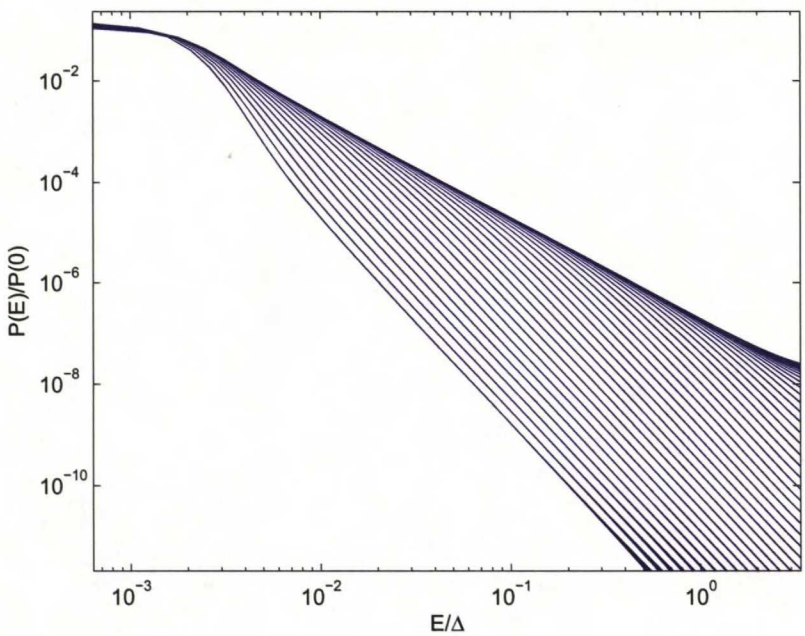

Figure 2.9: Shape of $P(E)$ with RC-environment and low resistance. The fixed parameters are $\rho = 10^{-4}$, $s/\Delta = 10^{-3}$. The capacitance C is varied between the curves. In the uppermost curve it is given by $RC\Delta/\hbar = 10^{-2}$ corresponding to Lorentzian function. The lowermost curve has the largest capacitance $RC\Delta/\hbar = 10^3$. In this case the tail of Lorentzian is strongly suppressed yielding lower leakages to the I-V curves.

detailed balance condition up to first order, can be neglected for $E < k_B T/2$. This condition has to be fullfilled up to energies $E \sim \Delta$ for describing the subgap region entirely. This implies that we must have environment temperature $T \gtrsim \Delta/k_B$. For aluminium this means $T \gtrsim 2.3$ K, which is by an order of magnitude higher than the bath temperature of the experiments and sets severe limitations on the validity of the pursued model under experimental conditions. In other words, the assumption is valid if the noise comes from a source at higher temperatures. The results presented here are still preliminary and subject to further analysis.

2.6.2 Effective density of states in tunneling rates

In the case of general environment ($P(E) \neq \delta(E)$), the tunneling rate of Eq. (2.1) has to be replaced by Eq. (2.19) and similarly for Eq. (2.2). If $f_S(E')$ does not change around the peak of $P(E-E')$, we may approximate $f_s(E') \approx f_s(E)$ and Eq. (2.19) can be written in the form

$$\Gamma(\delta E) = \frac{1}{e^2 R_T} \int_{-\infty}^{\infty} n_{s,eff}(E) f_s(E)(1 - f_n(E + \delta E))dE, \tag{2.26}$$

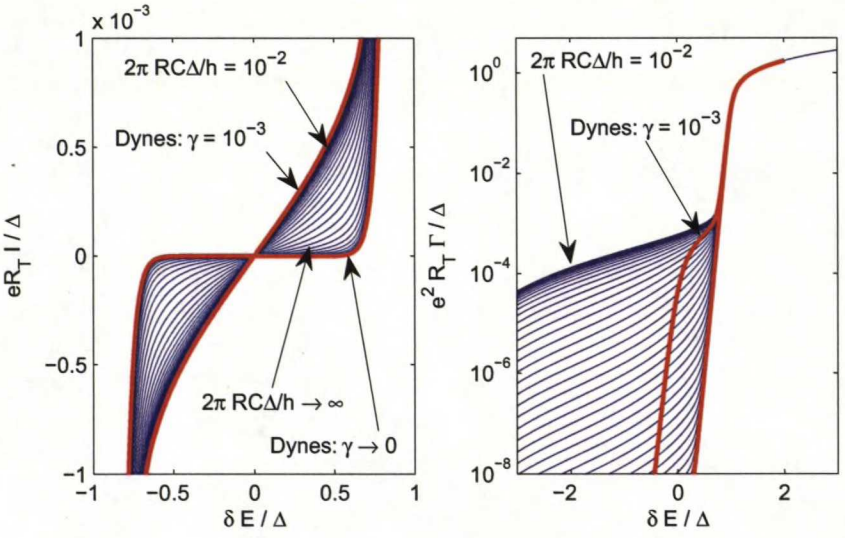

Figure 2.10: Comparison of current I and tunneling rates Γ obtained either with $P(E)$ calculations in RC-environment (blue) or with Dynes model (red). The parameters for $P(E)$ calculations are $\rho = 10^{-4}$, $s/\Delta = 10^{-3}$ and capacitance is varied in the range $RC\Delta/\hbar = 10^{-2} - 10^{3}$. The I-V curves in small capacitance regime coincide with the calculation made with Dynes model with $\gamma = 10^{-3}$ showing similar leakage as predicted by Eq. (2.28). On the other hand, the current in high capacitance case coincides to Dynes model with $\gamma \to 0$. Although the I-V curves match quantitatively, the same is not true for tunneling rates even qualitatively with negative energies δE. For Dynes model, the tunneling rate is exponentially suppressed but for $P(E)$ calculation the scaling is $\Gamma \propto (\delta E)^{-1}$ due to the slowly decaying tail of the Lorentzian.

where

$$n_{s,eff}(E) = \int_{-\infty}^{\infty} n_s(E')P(E - E')dE'. \tag{2.27}$$

Eq. (2.26) is identical to (2.1) but with effective density of states given by Eq. (2.27). With Eq. (2.25), neglecting the odd part, one obtains from Eq. (2.27)

$$n_{S,eff}(E) = \left| \mathrm{Re} \frac{E + is}{\sqrt{(E + is)^2 - \Delta^2}} \right|, \tag{2.28}$$

where $s = \rho k_B T$. This result can be obtained by making inverse Fourier transformation to Eq. (2.27) and using the fact that Lorentzian lineshape (i.e. $P(E)$) is the real part of the Fourier transform of $e^{-st}H(t)$, where $H(t)$ is the Heaviside function. Eq. (2.28) is obtained by making again the Fourier transformation and using the frequency translation rule. Eq. (2.28) coincides exactly to the Dynes model of the density of states shown in Eq. (2.15) with $\gamma = s/\Delta = \rho k_B T/\Delta$. With $R = 0.1\ \Omega$ and $T = 10$ K we get $\gamma = 10^{-4}$ for aluminium. This matches to the sub-gap leakages observed in experiments. Therefore our calculation demonstrates that the Dynes model can result from environment fluctuations and is not a property of the junction itself.

2.6.3 Deviations from the Dynes model

The validity of approximations made in Sections 2.6.1 and 2.6.2 was studied with numerical simulations. The simulations were made for $s/\Delta = 10^{-3}$, which generates similar leakage as what has been observed in measurements without ground planes. The results are presented in Figs. 2.9, 2.10 and 2.11. Figure 2.9 presents $P(E)$ for different capacitance values C. For small C, $P(E)$ is independent of C. When C increases enough, approximation $B > 1$ is not any more satisfied, and increasing capacitance starts to suppress $P(E)$. In this case one has to take into account the first term in Eq. (2.22). For $C \to \infty$, $\cot B = 1/B$ and one can use a short time expansion to get $J(t) = 0$ which gives correctly $P(E) = \delta(E)$. The tunneling rates Γ and resulting currents I for single NIS junction are presented in Fig. 2.10 for different capacitance values as blue lines. Correspondingly, the results for Dynes model with $\gamma = 10^{-3}$ and $\gamma \to 0$ are shown. From there, we see that the Dynes model and resistive environment (see Eq. (2.28)) behave similarly as far as currents are considered. Also in Fig. 2.11, the slope $I/\delta E$ at different bias values δE is presented with different capacitances. From there, we see that the leakage is roughly linear up to a certain bias voltage, where the leakage saturates to a value determined by thermal exitations.

From the tunneling rates in Fig. 2.10, we see that the Dynes model and $P(E)$ calculations do not match at all values of δE. With $\delta E > 0$, the two models match while at $\delta E < 0$ there is a large discrepancy. With negative energies, Dynes model will lead to exponentially small tunneling rates. This should be especially the case in single electron transistors at gate closed state, where current is vanishingly small. The resistive environment, however, produces a weaker dependence. With large δE tunneling rate follows $\Gamma \propto (\delta E)^{-1}$. This is caused by the long tail of the Lorentzian shaped $P(E)$. Assumption $f_s(E') \approx f_s(E)$ is justified for positive δE when one expects high transition rates, but for negative energies that should provide low rates, the approximation is not valid. In the latter case, a significant contribution to the integral of Eq. (2.19) is obtained when $f_S(E')$ is below Fermi energy and essentially yields an integral over a Lorentzian tail. The main implication of this finding is that one cannot solely trust to the current suppression provided by ideal Coulomb blockade in the presence of electromagnetic environment. It predicts that an exponentially small currents can be obtained in blockade. However, at RC-environment, the Coulomb blockade yields only a small suppression if the environment is at high temperature. However, the resistive model used here may not describe all the details of the transport perfectly: it is an oversimplification. Typically, the Coulomb blockade suppresses currents by at least few orders of magnitude, but still, the extremely low leakage at negative energies, which is not in the reach of DC experiments, the rates are expected to be higher than those given by the Dynes model. However, the current - voltage curves of a single NIS-junction are indistinguishable between the Dynes model and the resistive environment as is seen from Fig. 2.10.

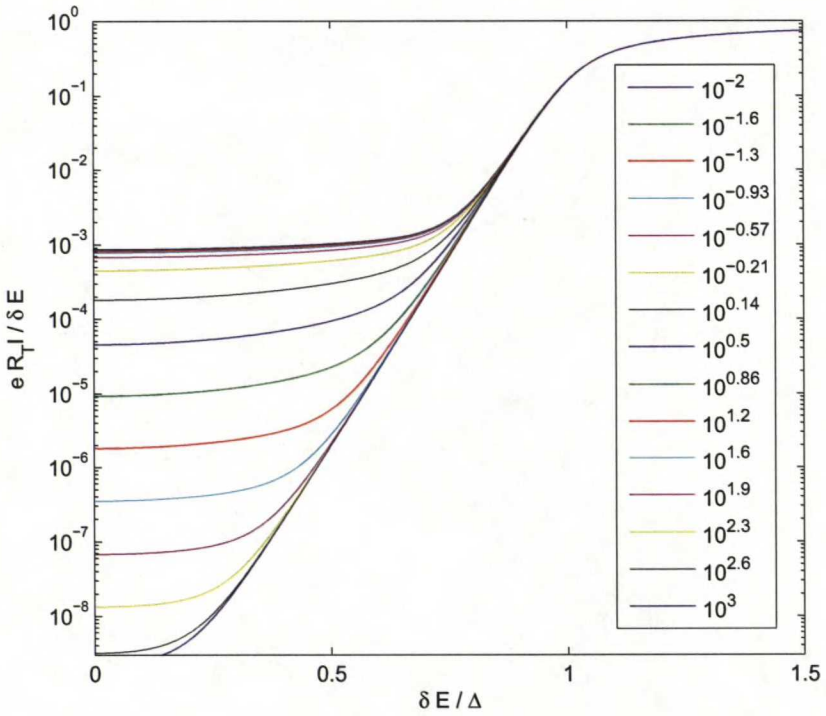

Figure 2.11: Influence of the capacitor to the sub-gap leakage. The slope $I/\delta E$ is plotted as a function of δE. The different capacitance values $RC\Delta/\hbar$ are shown in the legend. The electromagnetic environment yields approximately linear leakage valid up to the regime where thermal errors saturate the slope.

Chapter 3

Parallel turnstiles

At the first glance, parallel operation of multiple turnstiles seems like a straigthforward thing to do. There are, however, two concerns that have to be considered while operating multiple devices. First, the uniformity of device parameters has to be at high enough level. Typically the requirements for some parameters are stricter than for others. For a SINIS turnstile, the parameters determining thresholds have to be more uniform than the tunneling resistances as will be described in Sect. 3.2. Moreover, it is shown that the requirements for uniformity are met by the already fabricated and measured samples and therefore this will not hinder the parallelization.

Secondly, for a device based on charging effects, the stability of background charges is of major importance. These charges should not vary too much during the experiments so that the operation is not disturbed. As the number of parallel devices increases, one also has increasing number of offset charges to compensate. Therefore the offset charge instability sets constraints to the maximum number of parallel devices as will be described in Sect. 3.4.

Finally, in Sect. 3.5 the coupling of RF pumping signal to biasing leads is analysed. This can cause limitations to the maximum pumping frequency and it can limit the pumping accuracy as the bias voltage can decrease to too low values, or increase into the conducting regime of the turnstile. The effects from the bias coupling arise especially with parallel turnstiles as the degrading effect requires asymmetric coupling to different sides of the bias lines. With the increasing circuit complexity of parallel devices, these asymmetries are easily generated. The main results of this Thesis on parallelization are also reported in Ref. [47].

3.1 Sample fabrication and cooling

The samples used in this work were fabricated by electron beam lithography. It is a standard method for making structures with size below the capabilities of optical lithography. Two most common variants are the two-layer process shown in Fig. 3.1 and the three-layer process with one additional resist layer improving the resolution of the two-layer process.

In the two-layer process, copolymer and polymethylmetacrylate (PMMA) resist layers are first made on top of an oxidized silicon wafer. Individual layers

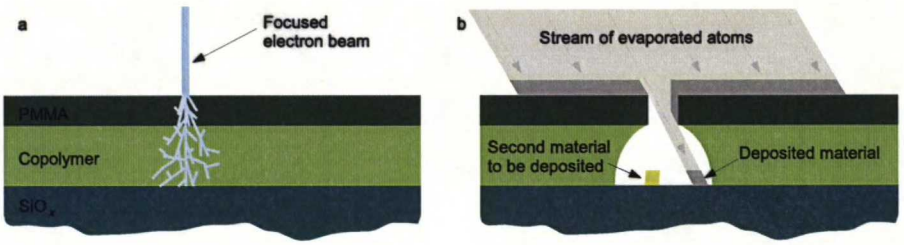

Figure 3.1: Principle of two-layer electron beam lithography. In (a) focused electron beam is used to write the structures to the PMMA-copolymer resist. After development, a cave shown in (b) is formed into the copolymer layer and a sharper mask into the PMMA layer. A stream of atoms is then deposited from different angles to create operational overlapping structures. After this step, a lift-off removes the resist layers and the extra materials attached to them, and the structures as shown in Fig. 3.2 are obtained.

are formed with the spin-coat technique by pouring few milliliters of diluted resist on top of the wafer and then spinning the wafer to obtain uniform resist layer with typical thickness of $100-1000$ nm. After spinning, the wafer is baked to remove the solvent and after baking, one can repeat the procedure to make the next layer. The parameters used were 40 s at 4000 rpm for copolymer and 40 s at 2500 rpm for PMMA. The baking lasted for a few minutes at 170 °C.

After resist spinning, the patterns were written with a focused electron beam as shown in Fig. 3.1 (a). As the high-energy electrons hit the resist layers, they break bonds of the polymer. These broken polymer chains can then be removed with a solvent. This procedure is called development and the used solvent is called developer. The contrast of electron exposure is lower in copolymer than in PMMA and hence one is able to remove higher amount of resist from the copolymer layer than from the PMMA layer. Therefore a wider cave-like opening is formed under the sharper opening in PMMA layer as shown in Fig. 3.1 (b). The developer used was MIBK:IPA solution (1:3 W/W) and typical development time was 30 s.

After development, the structures are formed by depositing metal atoms through the openings from different angles. This was done by an electron-beam evaporator, where metal is heated and, with the energy obtained from the electron-beam, shooted towards the wafer as shown in Fig. 3.1 (b). First, aluminium was deposited to create the superconducting parts. Then, the tunnel junctions were formed by oxidizing aluminium with O_2 and finally normal metal (AuPd) was deposited at a different angle to create normal metal parts. Typical parameters were: $30-70$ nm film with deposition rate $1-10$ Å/s and pressure $P < 10^{-6}$ mbar. After deposition, the resist and extra metal on top of it were removed in a lift-off process. Acetone at 50 °C was used as the solvent and after removal of the resist, rinsing was done with isopropanol.

The difference in the three-layer process is that there is an additional germanium layer between the polymer layers. This makes it possible to do lithography with higher resolution as the pattern is written only to the thin PMMA layer. Next, this pattern is developed similarly as expained above. After this, the pattern is transferred to the germanium by reactive ion etching in CF_4 gas. The

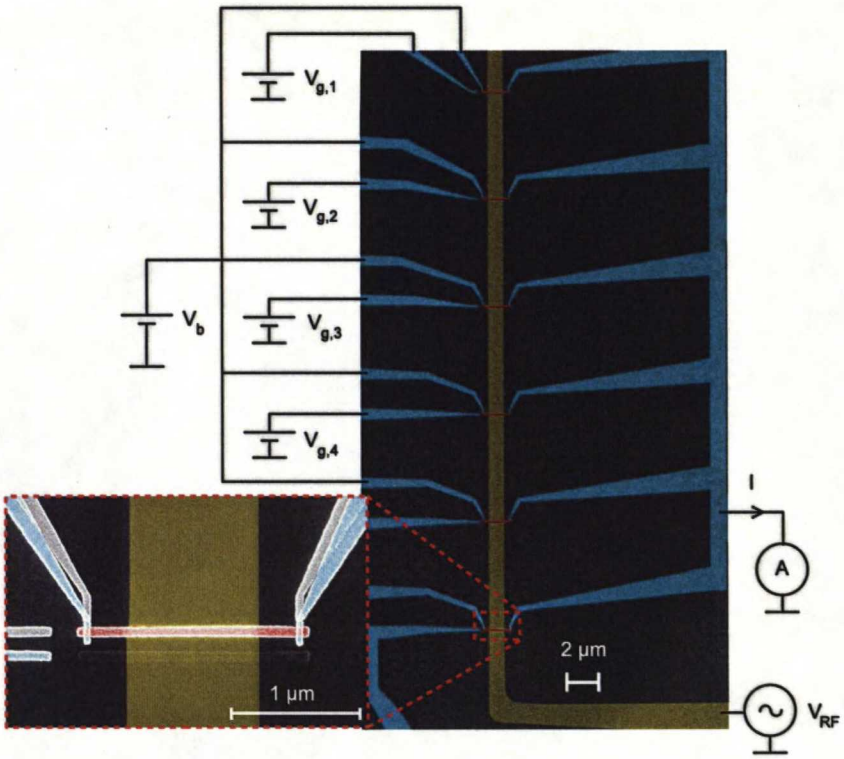

Figure 3.2: A scanning electron micrograph of a sample with six parallel turnstiles. Different structures are colored for clarity. A buried RF gate (yellow structure) is on top of the oxidized Si substrate. It is isolated from the other structures with a SiO_x layer made with spin-on glass technique. Turnstiles, with blue superconducting leads and red normal metal islands, are on top of this layer.

undercut under Ge mask is finally formed by etching of the bottom copolymer with oxygen in the electron-cyclotron-resonance (ECR) machine and deposition is done similarly as above. For the samples used in the final measurements of parallel turnstiles both two and three-layer processes were used. A scanning electron micrograph of one of the samples is shown in Fig. 3.2.

The bias voltage and RF gate voltage can be common for all the parallel turnstiles. In addition, each turnstile needs an individual DC gate for compensating the inevitable offset charges which are generally different for different devices. As the common biasing lines and RF gate cannot be fitted into one plane, a buried RF gate was fabricated underneath the turnstiles as shown in Fig. 3.2. This choice makes it also possible to design the coupling from RF gate to islands with lower parameter scatter.

The chips were fabricated at NEC by Dr. Yuri Pashkin. The process was started by making contact pads to a 3.6 mm x 3.6 mm chip with standard photolithography process. The pads are located at the edges of the chip with the leads stretching to the chip center leaving a square-shaped 80 μm x 80 μm area free for fine structures. Then, in this area, a 3 nm / 20 nm thick Ti/Au

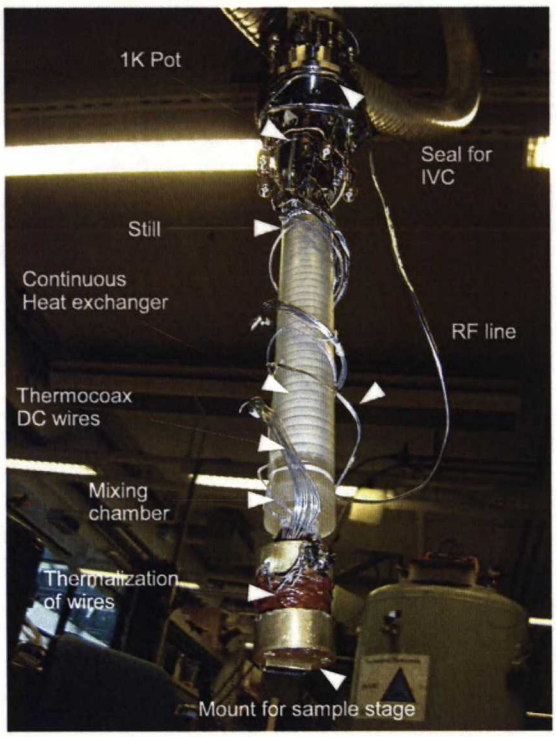

Figure 3.3: A plastic dilution refrigerator used for performing the low temperature measuremets of the thesis. The still, mixing chamber and one continuous heat exchanger are all combined to one plastic part. 1 K pot is used to condense the incoming ^{3}He by evaporating ^{4}He obtained from the liquid He-bath where the cryostat is held. The ^{3}He is obtained from a condensing line coming from the room temperature. Then liquid ^{3}He is transported through the line lying inside the heat exchanger to the mixing chamber. In the mixing chamber, the liquid is diluted to produce cooling. After dilution, the journey of ^{3}He continues through the heat exhanger towards the hotter parts of the cryostat, and on its way it cools the incoming liquid. In the still, ^{3}He is evaporated by using a room temperature pump returning the ^{3}He gas back to the condensing line.

RF gate, shown in yellow in Fig. 3.2, was deposited through a conventional soft mask resist formed with the two-layer electron beam lithography process. The RF gate was connected to one of the leads and covered in the next step by a patterned spin-on glass layer to isolate it from the turnstiles made above the RF gate. Finally, SINIS type turnstiles were fabricated using two-angle deposition through a suspended mask created in a Ge layer using the three-layer electron-beam process. Deposition of the superconducting leads (Al, blue in Fig. 3.2) and normal metal islands (Au/Pd, red colored island and non-colored extra shadows in Fig. 3.2) was done in Micronova using an e-gun evaporator with an oxidation step in between, immediately before the low temperature measurements.

The low temperature measurements were made with a dilution refrigerator capable to obtain temperatures below 100 mK at the mixing chamber. The cryostat is shown in Fig. 3.3. The main parts of the cryostat and the circulation

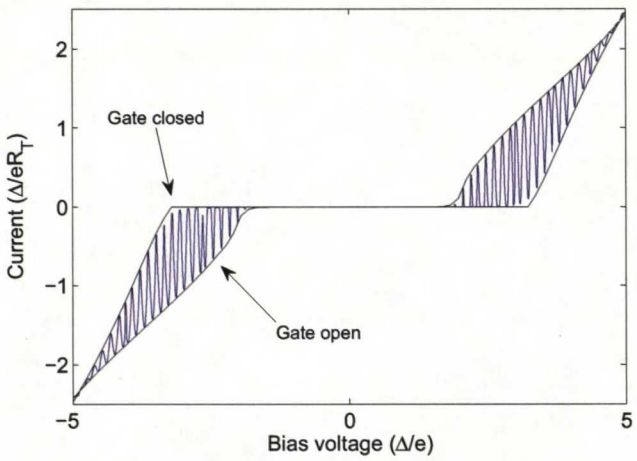

Figure 3.4: Current-voltage characteristics of a typical turnstile. The gate offset n_g is swept over a few periods of the island charge back and forth so that the measured solid blue curve reaches both extreme cases of gate open and gate closed repeatedly. The solid black curves show the simulations for these extreme cases within the sequential tunneling approximation. The bath temperature used in simulations was 100 mK but the results are insensitive to it on this scale. The effect of tunneling into the electronic temperature of the normal metal island was taken into account according to Eqs. (2.5) - (2.4) and assuming that phonon temperature T_p is equal to the bath temperature. The value used for the material dependent parameter $\Sigma = 4 \cdot 10^9$ WK^{-5}m^{-3} is consistent with the values obtained for the same Au-Pd alloy in earlier experiments [35, 37]. The island volume was used as a fit parameter and deviated 20 % from the expected value, which is typical to such a small structures. The varying electron temperature of the island narrows the gate modulation as the increased temperature at gate closed state produces larger currents above the gap.

of ^{3}He are explained in the caption. For a thorough description of dilution refrigerators see Ref. [48]. The cryostat contains 12 DC lines which are filtered with thermocoax-lines. For RF signal, an attenuator at 4 K with nominal value ranging between $20 - 40$ dB was used. The line going from the 1 K pot to the sample stage is a superconducting coaxial line and produces only a minimal amount of heat load to the base temperature.

3.2 Device uniformity

The most crucial requirement for parallelization is the device uniformity. Typically the uniformity is much better between devices made at the same time on the same chip than between single devices on separate chips. This feature is even used for making very sophisticated and outperforming applications such as current mirrors in integrated circuits. In the case of SINIS turnstiles, the tunneling thresholds described in Sect. 2.4 should not be too different from each other. To study this uniformity, four turnstiles on one chip, similar to those

Table 3.1: The parameters of the four turnstiles A-D. R_T and C_{RF} are estimated from the measurement data with uncertainty of 1 %. Δ and E_c/Δ are fitted with the help of numerical simulations to within 2 % precision.

	R_T (kΩ)	Δ (μV)	E_c/Δ	C_{RF} (aF)	$V_{r,m}$ (mV)
A	490	213	1.03	25.3	3.82
B	580	214	1.10	23.5	3.60
C	610	214	1.10	24.7	3.83
D	742	215	1.16	23.4	4.12
Variation	20 %	0.5 %	6 %	4 %	7 %

shown in Fig. 3.2, were measured independently. The DC current-voltage characteristics of one of the turnstiles is shown in Fig. 3.4. The gate offset n_g was swept back and forth so that both extreme cases of gate open and gate closed were obtained from the envelope of the results. (Compare to minimum and maximum current with respect to n_g in Fig. 2.5.) Correspondingly, simulations with sequential tunneling approximation were carried for both of the cases according to the equations described in Chapter 2. The simulation curves, shown as black solid lines in Fig. 3.4, match well to the measurements. The device parameters Δ and E_c shown in Table 3.1 were obtained from the fitting of the simulations to within 2 % accuracy and R_T to within 1 %. In addition, the coupling capacitance of the common RF gate to each of the islands was determined by connecting a DC voltage to the gate line and measuring change δV required for one modulation period in the turnstile current at a fixed bias voltage. Then the coupling capacitance is given by $C_{RF} = e/\delta V$. This parameter is also shown in Table 3.1.

The parameters determining the thresholds, explained in Sect. 2.4, are Δ, E_c, and C_{RF}. The superconducting gap is very similar for each of the turnstiles since it is a material dependent parameter. For aluminium it also depends sligthly on the thickness of the film but as the films for the turnstiles are evaporated at the same time, the variation of Δ is negligible. As small islands are needed for these devices, the charging energy E_c and coupling capacitance C_{RF} have somewhat higher variation. These variations will make the plateau narrower in parallel operation of the turnstiles. According to numerical simulations, the flat plateau region is smaller by 0.1 in terms of gate charge number n_g. This is tolerable if the metrologically flat part of the plateau is substantialy wider than this. The maximum width of a plateau as a function of gate charge is 1 e at $T = 0$, $\gamma = 0$ and $f \ll \Delta/(e^2 R_T)$ without higher order tunneling.

3.3 Experimental realization of parallel pumping

After the characterization of individual pumps, the bias lines of turnstiles were connected together and parallel pumping presented in Fig. 3.5 was measured. Here we have changed the DC gate states of one (Fig. 3.5 (a)), two (b), three (c) and four (d) devices simultaneously while keeping others at gate open. The turnstiles working around gate open will contribute one electron per cycle each

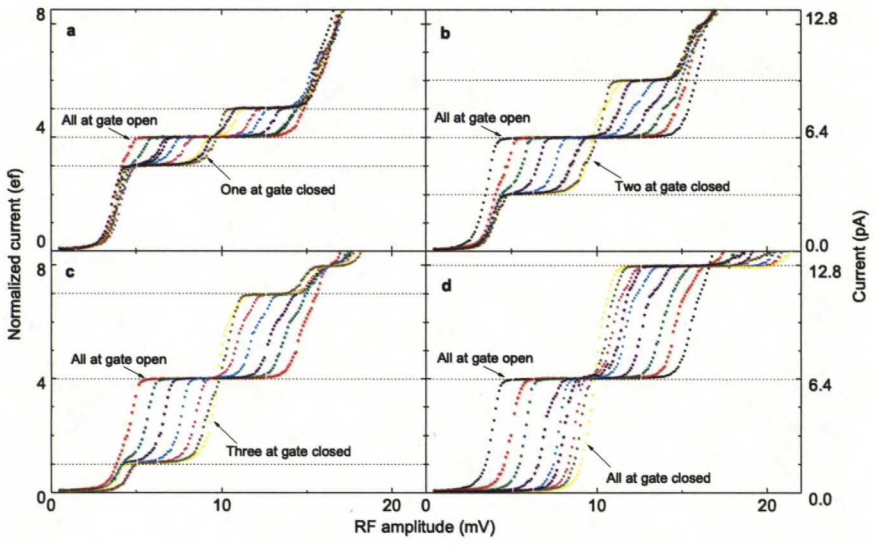

Figure 3.5: Parallel pumping of four turnstiles at $f = 10$ MHz. From (a) to (d), the DC gate charge of one to four devices is tuned between gate open and gate closed states, respectively, while the rest of the turnstiles are kept at gate open. This yields plateaus where 4 or $4 \pm N$ electrons are pumped in each cycle where N is the number of tuned devices. The case $N = 4$ shows pumping curves similar to those of a single turnstile but with four times higher current. The slope on the plateau where all the devices are pumping one electron is 2 pA/V per turnstile with respect to RF amplitude. The slopes for single turnstiles were similar up to the accuracy of the measurements limited by the drift of the current amplifier to the 10 fA level. The bias voltage was set to 200 μV during the measurements.

to the current and the turnstiles working around gate closed will provide either zero or two electrons in a cycle depending on the RF amplitude. Thus we obtain current plateaus where the number of electrons transported within one cycle varies between zero and eight. This measurement demonstrates that we can fully control the DC gate states of each device. Next, to demonstrate the reproducibility and robustness, ten turnstiles were operated similarly by a single RF drive. Two chips were used from different batches, with six turnstiles on one chip and four on the other. All ten devices were bonded to one common bias line. No preliminary characterisation of individual devices was made. The results for different bias voltages are shown in Fig. 3.6. This setup yields 104.1 pA at the first plateau with a pumping frequency of 65 MHz, which demonstrates a current level large enough for closing the quantum metrological triangle [49]. In the present experiment, the number of parallel devices was limited by the number of DC lines available in the cryostat.

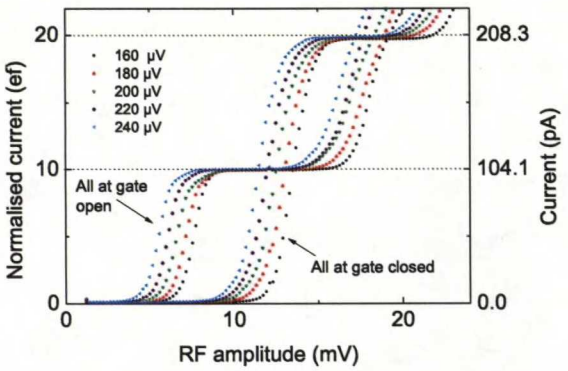

Figure 3.6: Ten turnstiles working at $f = 65$ MHz. DC gate charges of all turnstiles are set either to open or to closed state. The current at the first plateau is approximately 104.1 pA. The insensitivity to the bias voltage is also shown: the numbers in the panel indicate bias voltage values.

3.4 Stability of offset charges

In practise, the number of devices which can be operated in parallel simultaneously is determined by the offset charge stability. The strategy of a pumping experiment is to first set the DC gate voltage of each turnstile, then perform the pumping measurement and afterwards check the offset charges again. If they are not within the limits, one discards the data. To study the stability of the ten devices, the DC gate modulation was measured as a function of time for each of the turnstiles simultaneously. The time for one cycle was chosen to be 10 minutes which was equal to the time required to measure the data of one trace in Fig. 3.5. The gate stability for the turnstiles is shown in Fig. 3.7. From the data, histograms of the offset charge changes were determined for each of the devices as shown in Fig. 3.8. Moreover, in the inset a histogram for the corresponding maximum change of the ten turnstiles is presented. From this we obtain 73 % probability to get valid data with this measurement setup as described in the figure caption. Additionally, we can estimate the maximum number of turnstiles operable in parallel to be 17 in the present case, which would yield efficiency of 50%. One may improve this by performing the gate offset check faster.

It is also possible that the offset charges drift or jump to the erroneous regime during the pumping but then come back before the re-measurement and then one obtains poor data without noticing. This is a problem arising with a single device, not due to the parallelization and it has not been studied yet so carefully. From the data of Fig. 3.7 one would expect that this feature should be relatively rare as the drift seems to evolve typically to the same direction and jumps are relatively rare. Still, these missed errors migth become crucial when one strives to obtain the highest possible accuracy.

By decreasing the measurement period one could increase the number of

devices as they have less time to collect offset charge. We estimate that the measurement period can be decreased by one or two orders of magnitude. This will allow one to increase the number of parallel devices accordingly. Also different materials or fabrication methods can provide smaller drifts and hence allow larger integration scale. In our devices, typical spectral density of charge noise followed relation $S_q(f) = \alpha^2/f^2$ at the observed frequency range $f = 1\ \mu\text{Hz} - 1$ mHz with $\alpha = 10^{-6}\ e\sqrt{\text{Hz}}$. The magnitude is quite similar to previously reported values [50, 51]. Even better performance with no drifts has been observed for metallic single-electron devices previously [52, 53]. That would allow further increase in the number of parallel devices. However, such an improvement is not required for the ten parallel devices presented here.

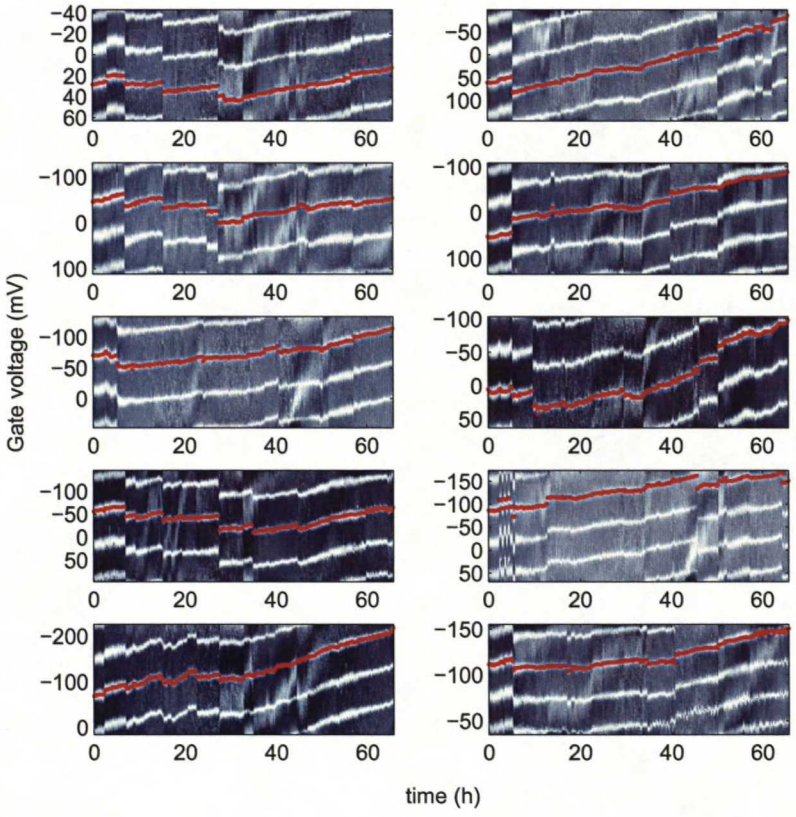

Figure 3.7: Gate modulation of ten turnstiles as a function of time without RF gate drive. The light/dark areas correspond to maximum/minimum current. The red dots show the gate open states which are changing due to variations in the offset charges. The data are obtained as one set within sequential sweeping of the gate voltages of the ten turnstiles. The ten sweeps are then repeated every ten minutes.

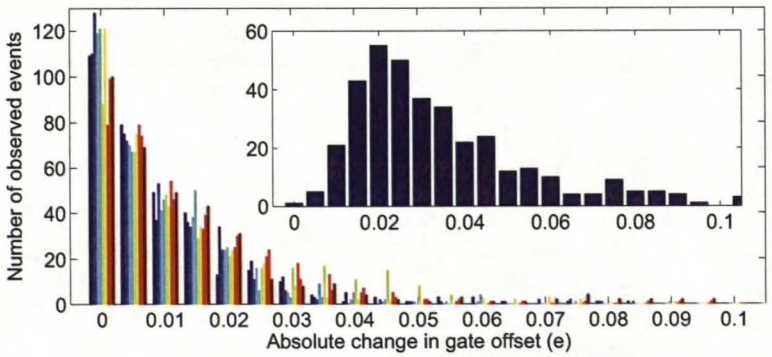

Figure 3.8: A histogram of the changes in the offset charge between sweeping sets repeated at ten-minute intervals. The different colours denote different individual devices. In the inset, a histogram of the largest change in each set is shown. The total number of sweeps per turnstile is 410. Although for individual devices the changes are peaked at zero, for ten turnstiles it is more likely that at least one of the devices has a change of few percent. To obtain an estimate for the maximum number of devices that can operate in parallel, we assume that the offset charge changes are independent as the average correlation coefficient between the devices was 0.12. This gives a lower limit for the probability of having N turnstiles in correct gate states as $p_N = p_1^N$, where p_1 is the probability of having one turnstile in a correct state. The flatness of the theoretical current plateaus is such that with the observed 10 % variation in tunnelling thresholds we can still tolerate 5 % changes in gate offsets. With the measured data, this will lead to $p_1 = 0.96$ and $p_{10} = 0.71$ for the ten parallel devices. This is consistent with the value $p_1^{10} = 0.73$ obtained from the data in the inset of (b). Therefore the requirement for efficiency of $p_N \geq 0.5$ will limit the number of parallel turnstiles to $N = 17$ according to the presented data and measurement time.

3.5 Coupling of the gate signal to bias leads

Parallelization of devices always leads to higher complexity of the design. This might degrade performance of the system. In the case of SINIS turnstiles one faces coupling of the RF gate voltage to the biasing leads. Problems arise when the coupling to the two bias lines is not equal as will be explained below. This is typically the case with parallel devices as the bias lines are not identical on both sides. For example, the sample shown in Fig. 3.2 has one common lead and bonding pad on the right hand side, and individual leads and pads on the other side.

As shown in Fig. 3.9, the coupling to the bias leads arises due to inevitable stray capacitances C_{GL} and C_{GR} between the RF gate and the bias leads and resistances R_{GL} and R_{GR}, which are needed at sample stage for proper thermalization of electrons. A typical value for the resistors is $R_{Gi} = 100\ \Omega, i = L, R$, which is much lower than the tunneling resistance of the turnstile. Therefore we can neglect the effect of the turnstile when we calculate the coupling strength. This assumption implies that we are dealing with a linear circuit and the dif-

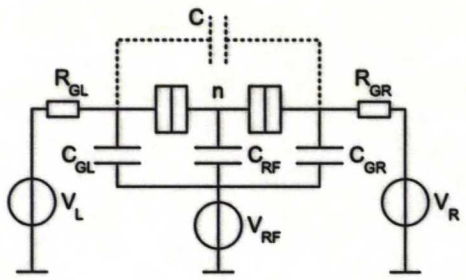

Figure 3.9: Coupling of RF gate voltage V_{RF} to the tunneling lines of the turnstile. The RF gate has inevitable stray capacitance to the bias leads. In addition, resistors are needed in these lines to keep the electrons well thermalized. These impedances build up an $R_{Gi}C_{Gi}$ high-pass filter from which the RF signal can couple to the bias lines. The dotted lines denote the shunt capacitor C that can be used to suppress the coupling.

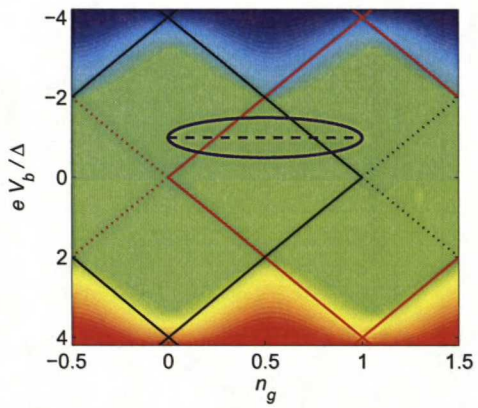

Figure 3.10: The coupling of RF gate voltage to the bias lines of the turnstile causes differences to the pumping cycle of a turnstile. Instead of having a pumping cycle with constant bias voltage V_b shown as dashed blue line, one has ellipsoidal trajectory shown as solid blue line. As RF amplitude is increased, the ellipsoidal trajectory also grows with fixed eccentricity. This will lead to increased backtunneling and ultimately to DC leaks. The eccentricity is linearly proportional to the RF frequency f for weak coupling, as is seen in Eq. (3.2).

ferent frequency components can be calculated separately according to basic circuit analysis. For the DC component we still have the same result as previously since capacitors have no effect and we can neglect the effect of the low resistance elements.

Let us next consider the voltages at pumping frequency. The resistance and capacitance act in this case as an RC high-pass filter between the RF gate drive and bias leads. The voltage at this frequency on either side of the turnstile is given by

$$V_{RF,i}(\omega) = \frac{j\omega R_{Gi}C_{Gi}}{j\omega R_{Gi}C_{Gi}+1}V_{RF}(\omega), \tag{3.1}$$

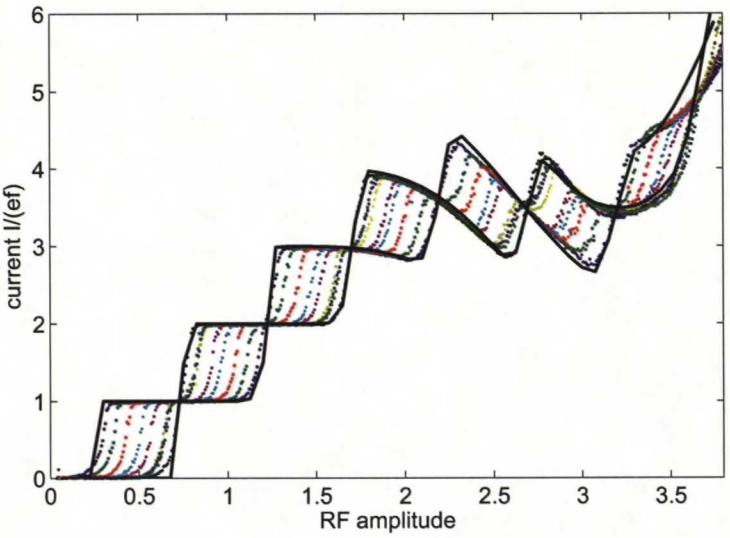

Figure 3.11: The coupling of the RF gate voltage to the bias lines degrades the current plateaus. Dots show pumping with different gate positions for turnstile A of Table 3.1 at $f = 10$ MHz and $V_b = 200$ μV. Solid black lines show simulations of pumping at gate open and closed state. The simulations were done using Eq. (3.2). From the third to the sixth plateau we observe backtunneling due to too low bias during one half of the cycle. With even higher RF amplitudes we see excess current due to operation at conductive region of the SET with too high bias during the other half of the cycle. From the simulations we obtain $\omega RC = 6.1 \cdot 10^{-3}$ as a fitting parameter. The phase change of the RF gate and the DC bias voltage were also used as fitting parameters and the phase change was estimated to be $\pm 0.055 \cdot \pi$ rad. A bias voltage 2 % lower than the nominal value gave the best fit to the data.

where $i = L, R$ refers to the left and to the right side respectively. The common mode part $(V_{RF,R} + V_{RF,L})/2$ of the signal does not affect the operation of the turnstile. This can be considered as a change in RF gate coupling as the potential of the whole turnstile is lifted or lowered by the common mode signal. This part of the signal generates also phase shift into the pumping cycle but the phase shift has no effect on the pumping accuracy.

The differential part $(V_{RF,R} - V_{RF,L})/2$ affects, however, directly the bias voltage V_b during the cycle. To simpilify the analysis, we need to make approximations. The differential signal that couples to the bias voltage should be lower than $\Delta/e \sim 200$ μV for aluminium, as with larger values the operationality of the turnstile is lost. According to Table 3.1, a typical voltage applied to RF gate is much larger, $V_{RF} = e/C_{RF} = 1.6 \cdot 10^{-19}$ C/10 aF = 10 mV. Thus we can assume weak coupling in Eq. (3.1), i.e. $\omega R_{Gi} C_{Gi} \ll 1$. This assumption is also supported by the fact that typical capacitance of a line of length l is $C \sim \epsilon l$. Therefore with $l = 1$ cm and $R = 100$ Ω, we obtain the upper limit of frequency for our system $f \ll (2\pi RC)^{-1} = 10$ GHz. This is well satisfied for the pumping frequencies used. With this assumption, the bias voltage accross the turnstile

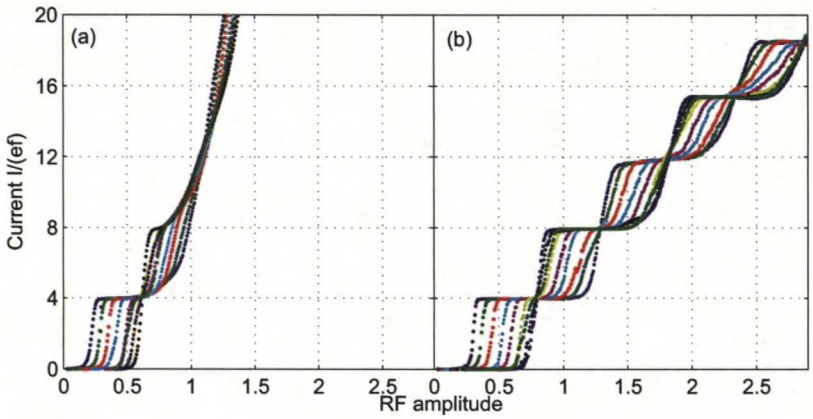

Figure 3.12: In (a) we have four turnstiles with a coupling of RF gate voltage to the bias lines. Pumping frequency is $f = 32$ MHz and bias voltage $V_b = 200$ μV. The coupling degrades the performance so that all the plateaus except the first one vanish. In (b) a capacitor with nominal value of 1 nF was inserted between the bias leads. Therefore the coupling is suppressed and several plateaus can be seen.

can be written as

$$v_b(t) = V_b + \omega RC \cdot V_{RF} \cos(\omega t), \tag{3.2}$$

where $RC = R_{GL}C_{GL} - R_{GR}C_{GR}$ and V_b is the applied DC bias voltage. The implications of the changing bias voltage can easily be seen from the stability diagram of Fig. 3.10. Instead of having an ideal pumping path shown as dashed blue line, we have an ellipsoidal trajectory. As RF amplitude V_{RF} is increased, the ellipsoid grows with fixed aspect ratio. With large enough amplitude, the trajectory will enter the conductive part of the transistor and large DC current is observed. With smaller amplitudes, the main feature of the pumping is that half of the cycle has a low bias voltage which will increase errors caused by backtunneling. Both of these regimes are observed in measurements as shown in Fig. 3.11. The figure contains also simulations within sequential tunneling approximation. From these simulations, the time constant $\tau = RC = 98$ ps is extracted. This verifies that the assumption of weak coupling is valid. Also we see that the coupling capacitances are of the order of $C \sim 0.2$ pF or larger. It can be estimated that structures smaller than 10 μm cannot support so high stray capacitances. Therefore the coupling arises from the pads and the wide leads leading to the smaller structures in our design.

To guarantee accurate operation of the turnstiles, the bias coupling has to be suppressed. Fortunately this is relatively easy to do. By putting a large enough capacitor between the bias lines, one shunts all the high frequency components on the bias voltage (see the dotted lines in Fig. 3.9). To demonstrate this improvement and further to validate the reason for the data obtained in Fig. 3.11, capacitors with nominal value of 1 nF were inserted between the bias lines after observing the coupling. The measurement data with and without the shunting capacitor are shown in Fig. 3.12. We can clearly see that the plateaus have improved after suppressing the coupling. One has to be quite careful when adding

these capacitors as they might be leaky. This DC leakage will add directly to the pumped current and therefore generate errors. In the present case we used ceramic COG capacitors which did not exhibit excess leakage.

Apart from the problems that the coupling to bias lines causes, it also demonstrates that the experimentally obtainable parameters are feasible for having an RF signal in bias lines. In principle, this can be used to obtain RC time constant limited pumping for high charging energy turnstiles according to the discussion of Sect. 2.5.2.

Chapter 4

The origin of leakage in NIS junctions

In Sect. 2.6 we calculated analytically and numerically sub-gap leakage arising from environmental fluctuations and showed that the results coincide with those obtained from the Dynes model. In this Chapter, an experimental study is presented. It verifies two fundamentally important features. First, the external environment is shown to affect the leakage, and second, a method to decrease leakage by an order of magnitude is demonstrated. The study was made by changing the capacitance between the signal lines. The variation was made by introducing a ground plane underneath the structures and comparing the measurements to devices without the ground plane. With high capacitance provided by the ground plane, low leakages are reached as the device becomes voltage biased more ideally. Without the ground plane, the I-V curves are leaky, which can be described by the Dynes model arising from non-ideal biasing.

4.1 Fabricated samples

The samples with ground plane were fabricated so that first a conductive Al ground plane was deposited using a sputterer. The thickness of the ground plane was 100 nm. Then an insulating layer of alumina (Al_2O_3) was made by atomic layer deposition (ALD). In this process 4000 deposition cycles were used, which corresponds to a thickness of 400 nm. The devices were fabricated on top of this insulation layer by standard two layer electron beam lithography as explained in Sect. 3.1. An electron beam micrograph of a SINIS turnstile on top of the ground plane is shown in Fig. 4.1. The fabrication of the ground plane and the insulating layer causes some speckles to the image. This means that the surface is not as smooth as the surface of a bare silicon wafer, but as long as the devices work, the flatness is not an issue.

The first fabricated devices were single-electron SINIS transistors which were used to see whether the ground plane influences the leakage. After that, two sets of single NIS junctions were fabricated so that one set had the ground plane and the other one was without the Al layer but still had the Al_2O_3 layer to yield similar substrate for the devices. The Al_2O_3 layer and all the devices were made in the same deposition batch and the devices were measured in the same

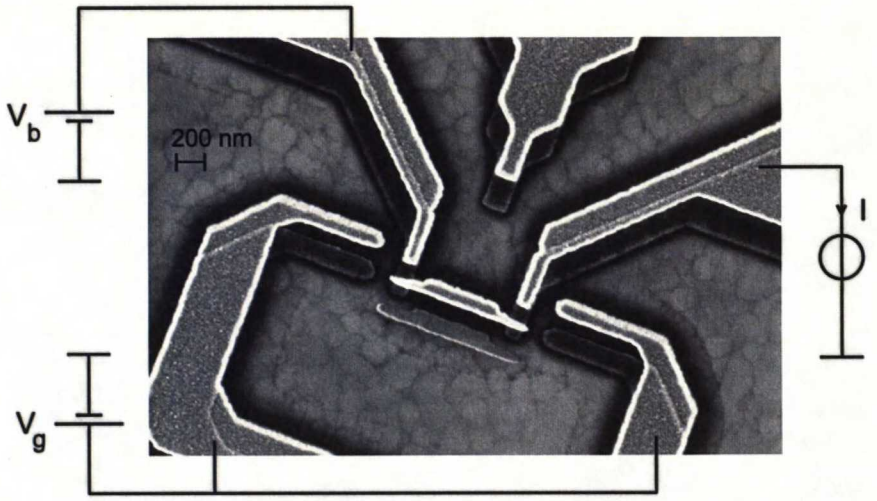

Figure 4.1: A SINIS turnstile fabricated on top of a conducting ground plane. The speckles are caused by the fabrication methods of the ground plane.

cool-down. This minimizes differences which could arise from, e.g., variations in material cleanliness or in the oxidation procedure. In the following section, we present the results of these measurements. Finally, pleriminary results on higher order tunneling processes are presented in Sect. 4.3.

4.2 Suppression of leakage

In Fig. 4.2, an envelope measurement similar to the one shown in Fig. 3.4 is presented in the sub-gap region for a SINIS-turnstile. The device parameters, $E_c = 0.55\Delta$, $R_T = 415$ kΩ and $\Delta/e = 210$ μV, were obtained from a numerical simulation to an envelope measurement at larger scale. The solid red curve denotes the ratio between asymptotic[1] (R_{asymp}) and sub-gap (R_{gap}) resistances $\eta = R_{asymp}/R_{gap} = 2 \cdot 10^{-5}$. For a SINIS turnstile we have $\eta = 2\gamma$ whereas for single junctions $\eta = \gamma$, i.e. the Dynes parameter and the resistance ratio are equal. This difference is because the asymptotic tunneling resistance is twice larger for a SET with two junctions, but as an excess electron tunnels fast away from the island, the sub-gap leakage is limited only by one of the junctions. The value for η estimated here is a conservative upper limit for the residual leakage due to the noise of the envelope measurement. If a straigth line is fitted to the sub-gap region, it yields an order of magnitude smaller slope, but this cannot be considered to be a true measure of the leakage in a NIS junction since Coulomb blockade suppresses the current and one cannot be sure that the gate open state can be extracted from the measurement. Three other samples, two of them from a different fabrication round, showed similar behaviour.

To avoid the the influence of Coulomb blockade, single NIS junctions were fabricated. The results for those junctions are presented in Fig. 4.3. In this experiment, two NIS-junctions on top of a grounded conducting plane (red traces

[1]For turnstile $R_{asymp} = 2R_T$, and for single junction $R_{asymp} = R_T$.

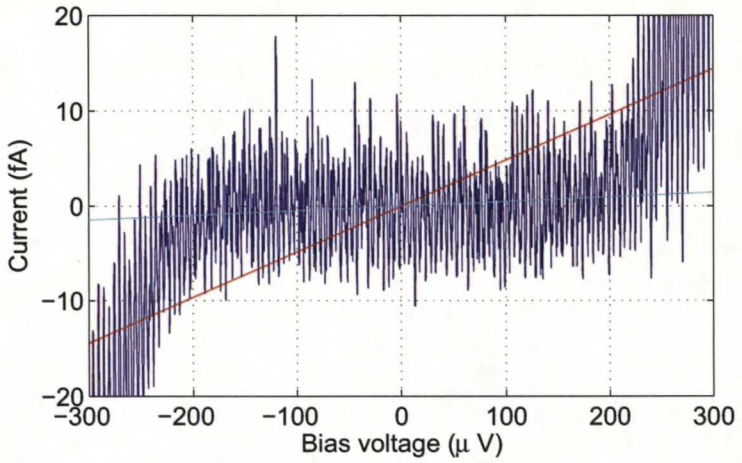

Figure 4.2: Sub-gap leakage of a SINIS turnstile on top of a ground plane. Solid red and cyan lines show resistance ratios $\eta = 2 \cdot 10^{-5}$ and $\eta = 2 \cdot 10^{-6}$ respectively.

Table 4.1: The parameters of the seven measured single NIS-junctions. A and B are on top of bare Al_2O_3, C on top of a floating ground plane, D and E on top of a grounded ground plane and F and G are with plasma oxidized tunnel barriers on top of bare SiO_x.

Sample	A	B	C	D	E	F	G
R_T (kΩ)	740	630	760	590	770	91	130
$\eta\ /10^{-5}$	38	53	2.6	5.4	5.9	50	46

in Fig. 4.3, D and E in Table 4.1), one on top of a floating conducting plane (black trace, C) and two on top of bare alumina (green traces, A and B) were measured in one cool-down. Both alumina and the metal layers were deposited simultaneously for the samples A - E to minimize differences arising from variations in fabrication. In addition, junctions with plasma oxidized barriers and SiO_x substrate without a shielding ground plane were measured (blue traces F and G).

The asymptotic tunneling resistances $R_{asymp} = R_T$ shown in Table 4.1 and ratio $\eta = R_{asymp}/R_{gap}$ of asymptotic and sub-gap resistances were determined. R_{gap} was determined by making a linear fit to bias voltage in the range $V_b = [-100\ \mu\text{V}\ , 100\ \mu\text{V}]$. This is approximately up to half way of the gap and its upper end corresponds to the operation point of a turnstile. From the obtained fits, presented in Table 4.1, we conclude that the ground plane suppresses the leakage by an order of magnitude. This suppression of leakage fits well with the theoretical result presented in Sect. 2.6. We can also compare the capacitances used in the measurement to those from the $P(E)$ theory giving similar performance. For Al_2O_3 the dielectric constant is $\epsilon_r \approx 10$. Therefore, for parallel plate capacitor, we get an estimate $C = \epsilon_r \epsilon_0 A/d \approx 10 \cdot 8.9 \cdot 10^{-12}\text{F/m} \cdot 58\,000\ (\mu\text{m})^2/400\ \text{nm} \approx 10\ \text{pF}$ for the capacitance from the

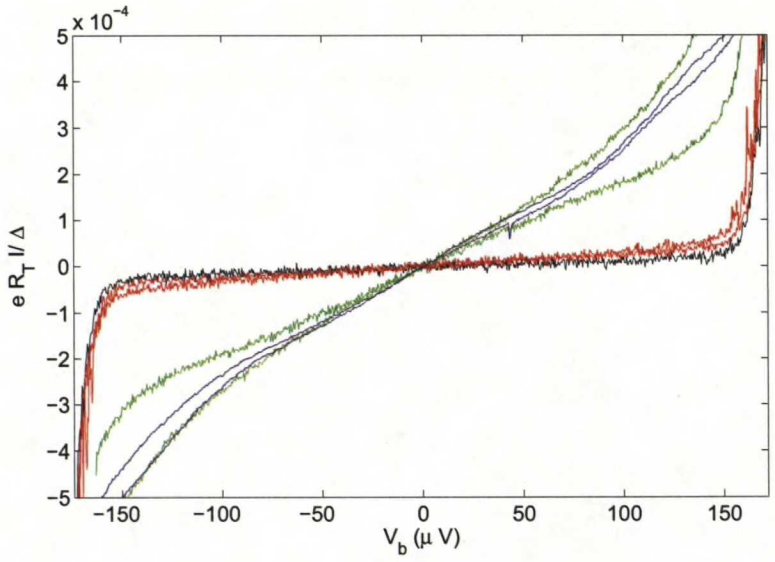

Figure 4.3: Sub-gap leakage of NIS junctions. Two red traces correspond to junctions on top of a ground plane which is connected to cryostat ground. Black trace is with a floating ground plane. Green curves are junctions on top of Al_2O_3 without conductive layer. Blue traces show plasma oxided junctions without ground plane. The superconducting gap Δ, normalizing the y-axis, was assumed to have value $\Delta/e = 200$ μV which is a typical value for Al films of the same thickness.

lead to the ground plane. The area A in this estimate originates mostly from the bonding pad (200 μm x 200 μm). The capacitance between the leads is smaller by a factor of two with floating ground plane due to two capacitors in series while with a grounded ground plane this gives directly the capacicance which shunts the bias line. According to Sect. 2.6, the higher capacitance should yield lower leakage, but according to Table 4.1, measurements show the situation to be vice versa. This can be explained by an additional noise that couples from the grounding route of the conducting plane. When the plane is floating, the system is more isolated and the noise level is lower. It is also worth noting that a floating conductive plane can be problematic for small charge sensitive islands as it increases the cross-coupling. Also the offset charge stability might be affected by the ground connection. Therefore ground connection is probably necessary for single electron transistors.

Finally we can compare the capacitance value provided by the ground plane to the constraint $B \gg 1$ required according to Sect. 2.6.3 to suppress leakage. From this constraint we obtain for leakage $s/\Delta = 10^{-3}$, $C \gg 400$ fF which is satisfied with the used ground plane. Correspondingly for $s/\Delta = 10^{-5}$ we should have $C \gg 4$ pF which is not yet satisfied. We saw residual leakage of the order $s/\Delta = 10^{-5}$ in single junctions and similarly, the turnstiles might have similar leakage present. Therefore the theoretical model predicts the required capacitance level.

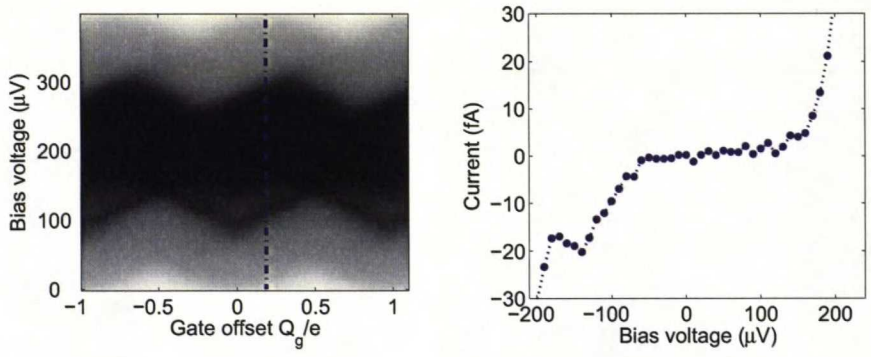

Figure 4.4: A measured stability diagram of a SINIS turnstile with higher order tunneling processes. The dotted line in the stability diagram in the left panel shows the gate offset value used for extracting the I-V curve in right panel. The lack of features in positive bias side is not understood.

4.3 Observation of higher order tunneling processes

If the leakage arising from electromagnetic environment is suppressed, one should be able to observe higher order tunneling processes. According to theoretical calculations, the dominant leakage with low charging energies is Andreev reflection, while with high charging energies these procecesses are suppressed, and electron - Cooper-pair cotunneling becomes the dominant process during electron pumping [16]. The electron - Cooper-pair cotunneling cannot be prevented during a pumping cycle by the choice of the device parameters and it limits the relative pumping accuracy to the 10^{-8} range.

The higher order processes will provide very nontrivial transport features to the SET as is observed in Fig. 4.4 which shows a stability diagram at sub-gap region for a hybrid SET. The device parameters are roughly $R_T \approx 200$ kΩ and $E_c \approx 0.25\Delta$ with $\Delta/e \approx 200$ μV. The device parameters cannot be determined more accurately because no larger scale envelope measurement was done for this device. Due to the low charging energy, it is expected that Andreev reflection might contribute to the current in the gap region. From the measured data it is seen that at half way of the gap, the current increases rapidly contrary to the Dynes model and environment induced leakages. With negative bias, also a drop of current is observed with increasing bias. The location of the drop is gate dependent and periodic. It can be explained by taking into account single electron tunneling and Andreev reflection in a master equation calculation. The results of the calculations are shown in Figs. 4.5 and 4.6. From the stability diagram in Fig. 4.6, one sees a similar drop of current as in the experimental data. Further investigation of current drop in the gate closed state is presented in Fig. 4.5. From (a) one sees that although the tunneling rates for both Andreev reflection and normal tunneling increase, the current suddenly drops. From the probability distribution in (b), one finds out the following explanation: Below the thresholds of single electron tunneling, the Andreev reflection processes determine the current flow. These processes take

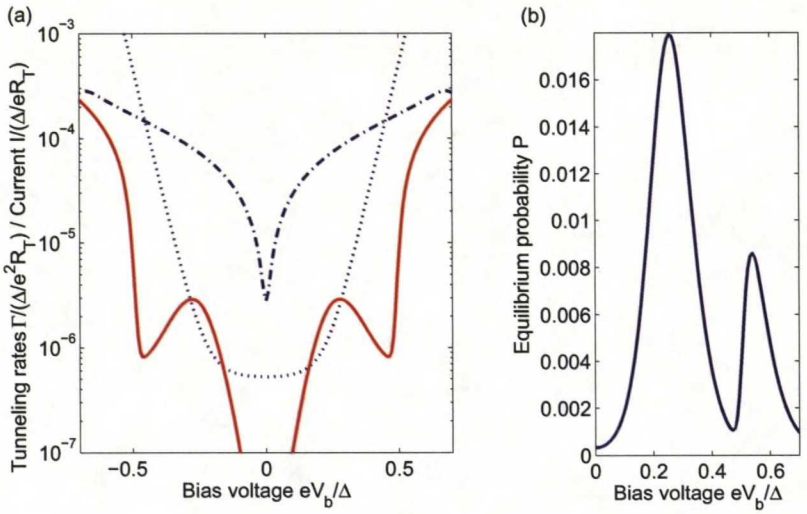

Figure 4.5: In (a) the tunneling rates determining current suppression at gate closed state ($n_g = 0$) are shown. Blue dash dotted line shows rates for Andreev reflection and blue dotted line shows the normal tunneling rate. The current is suppressed when the normal tunneling starts to grow sufficiently. In (b), the probability P for states $N \pm 1$ are shown. The central state N has probability $1 - 2P$ as other states have vanishingly low occupation. The suppression of the current results from the concentration of the probability to state N by normal rates. Andreev reflection is forbidden from this state.

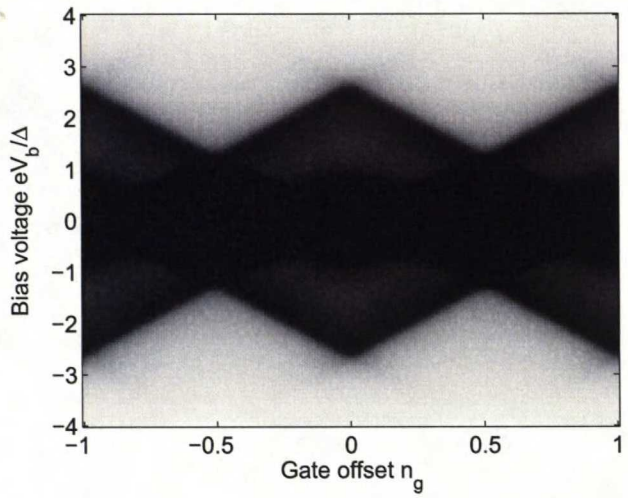

Figure 4.6: Simulated stability diagram with Andreev reflection included in the master equation model described by Eqs. (2.11) and (2.13). The rates for Andreev reflection are obtained from Ref. [16].

place between charge state N and $N \pm 2$. When the single electron tunneling threshold is exceeded, it concentrates the probability distribution to the central state N from which Andreev processes are forbidden and therefore the current decreases although all tunneling rates are monotonically increasing. These features have been observed earlier in the experiments of Ref. [54] but without the asymmetry between positive and negative bias present in Fig. 4.4.

Chapter 5

Summary and conclusions

This thesis was devoted to obtaining performance improvements of a hybrid single-electron turnstile. For a current standard needed in metrology, one should be able to have large enough output current and still retain accurate operation. From the large variety of proposed devices presented in Sect. 1.2 one sees that this is not a trivial task. Extremely high accuracy can be reached at very low currents, but as larger currents are pursued, various problems arise. Therefore, this thesis focused on demonstrating higher currents and the feasibility to improve the accuracy of the device.

In Chapter 2, the theoretical basis of the thesis was presented. The chapter dealt mostly with sequential tunneling taking place in tunnel junctions under ideal bias voltage. The theory and the procedure to take into account the electromagnetic environment has been well established for two decades. However, the link from environmental fluctuations to the phenomenological Dynes pair-breaking model of superconductors is our recent finding. The experimental findings with a ground plane in this thesis support this picture. Also, if we compare the parameters of the experiments to theory, they are in the same range. Therefore we can conclude that the leakages in turnstiles at least in the 10^{-4} range or above arise from environmental fluctuations. It was experimentally shown that for single NIS junctions the leakage can be suppressed at least down to the 10^{-5} range, and similarly for turnstiles. In the case of turnstiles, this provided only an upper limit, as noise in the measurement signal was higher than the leakage. In addition, the theoretical analysis in the Coulomb blockade regime shows that the Dynes model might fail. According to the model, the energy needed for an electron to tunnel should lead to exponentially small tunneling rates as only an exponentially small number of electrons is able to overcome this threshold with thermal exitation. However, the environmental fluctuations do not lead to exponentially small rates at negative energies. This is caused by the relatively slowly decaying tail of the $P(E)$ function. This implies that one cannot trust the Coulomb blockade to be capable of suppressing the tunneling rates exponentially which has appeared as a reasonable approximation to this date.

Another aspect, the maximal output current level, was improved by employing parallel devices. Theoretically it has been calculated that a single SINIS device can produce few tens of picoamperes with a relative uncertainty of 10^{-8} if higher order tunneling determines the accuracy. This current is not yet suf-

ficient for the closure of the so-called quantum metrological triangle, which requires currents of the order of hundred picoamperes. In this thesis it has been demonstrated experimentally that ten devices can be parallelized to produce currents exceeding 100 pA. The parameter variations of four devices were studied. The variation from one device to another in the critical parameters of the charging energy and the coupling capacitance from the RF gate to the island, was 5 % while the superconducting gap had only 0.5 % variation as it depends less on the geometry. The tunneling resistances had somewhat larger variations, about 20 %. However, this parameter is not as crucial to the parallel operation since the largest of the resistances limits the maximum operation frequency. If high accuracy turnstiles can be fabricated, the device parameter variations lead to roughly 0.1 e narrowing of the plateaus in terms of gate charge. This is tolerable if the flat part of the plateau is much wider than this value.

The number of parallel devices was limited in the measurement by the number of DC lines available. More generally, the offset charge instability limits the maximum number of the devices. If there are more devices in parallel, it becomes more and more probable that one of them accumulates too much charge drift during the measurement or induces a charge jump. To characterize this, the drifts of ten turnstiles were measured simultaneously. From the results we calculate that with ten devices and a 10 min measurement time, all of the offset charges stay constant within 5 % limit in 70 % of the cases. If one increases the number of devices from this, the fraction of valid data decreases quite rapidly. However, this could be compensated by a faster measurement which is perfectly feasible.

Finally, coupling from the RF gate line to the bias lines was observed with the parallel samples. This is because in parallel samples, one will end up having more asymmetry in the bias lines, and the asymmetric part of the coupling causes RF-induced variations into the bias voltage. This affects the performance of the device but it can be fixed easily by placing a shunting capacitor accross the biasing lines as was experimentally demonstrated in this thesis. It is also worth noting that by changing the bias in a controlled way during the pumping cycle, one could increase the speed of the device and decrease errors. The practical realization of this method with parallel devices can be complicated.

The main implication of the thesis is that the hybrid turnstile is most likely to succeed in having both high accuracy and high output current. As the outcome of this thesis, it can be estimated that the present turnstile can reach a current exceeding 100 pA with a relative accuracy of better than 10^{-5}.

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