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The advantages of capacitive accelerometers [1], such as zero static bias current and the capability of achieving high sensitivity, are emphasized in ultra-low-power applications. In [1], representing the current state-of-the-art in low-power 3-axis micro-accelerometers, capacitance-to-voltage and A/D conversions were performed separately. In this paper, an ultra-low-power 2nd-order ΔΣ sensor front-end with inherent capacitance-to-digital conversion [2] for a 45dB, respectively. The dynamic latch with zero static power dissipation (Fig. 32.2.2(b)) [5] is used as a comparator.

The prototype was fabricated with a 0.25μm CMOS technology with MIM capacitors. The sensor area of the front-end (Fig. 32.2.6) is 0.49mm². The chip was combined with an external 250μm capacitance-to-voltage and A/D conversions were performed. At the same time, the signal swing at the output of the 1st integrator is reduced, making low-voltage operation easier to achieve. If charge is sourced or sunk from only one side, the system compensates for any offset in the sensor capacitors. The signal boosting and offset compensation can be also used simultaneously.

Because of the low supply voltage, the use of floating switches is not possible without boosting the gate voltages. Therefore, the gate voltage of an NMOS device in a floating transmission gate is increased to 2VDD using charge pumps (Fig. 32.2.2(c)) [6]. To minimize the silicon area, the number of gate-voltage-boosted floating switches was kept as low as possible. Other switches were implemented as single N- or P-MOS devices. The symbol 2x is used to indicate the gate-voltage-boosted switches in Fig. 32.2.1. The area required by the charge pumps is minimized by driving all the switches operating on the same clock phase with a single pump, and by sizing C<<C in each pump.

As the sampling frequency is low, the leakage currents of off-state switches must be minimized in order to prevent signal distortion and temperature-dependent offset. The primary source of leakage is the off-state threshold current which is minimized by using a minimum channel length to increase the threshold voltage whenever there is a voltage drop over an off-state switch. Additionally, the sensor middle electrode DMD was identified as being especially sensitive to leakage currents. To minimize the leakage into this node, a special ultra-low-power 2nd-order ΔΣ modulator is used. The area required by the charge pumps is minimized by driving all the switches operating on the same clock phase with a single pump, and by sizing C<<C in each pump.

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Figure 32.2.1: Schematic of the ΔΣ sensor front-end with an SEM photograph of a 3-axis capacitive micro-accelerometer. (SEM image courtesy of VTI Technologies, Vantaa, Finland)

Figure 32.2.2: Schematics of: (a) a tail-current-boosted Class-AB operational amplifier; (b) a dynamic latch; (c) charge pumps, and (d) an ultra-low-leakage NMOS (left) / PMOS (right) switch.

Figure 32.2.3: Operating principle of (a) signal boosting and (b) offset compensation.

Figure 32.2.4: (a) FFT of measured z-directional data, (b) ±2g acceleration ramps, and (c) an x-directional acceleration pulse.

Figure 32.2.5: Summary of measured performance.

Process 0.25μm CMOS with MIM capacitors
Operating mode With CS and CDS, no signal boosting
Supply voltage 1V
Power dissipation 1.5μW
Sampling frequency per mass 4.096kHz
Noise floor (μg/√Hz) x-axis 917 y-axis 791 z-axis 704
Current consumption / silicon area (μA) (mm²)
- Opamps 0.0358
- Comparator 0.0006
- Charge pumps 1.4μA
- Switches 0.0727
- Clock generator 0.0376
- Capacitors 0.0552
- Wires 0.1181
Total 1.5μA

Please click on paper title to view Visual Supplement.
Figure 32.2.6: Chip micrograph.