Publication V


© 2009 Institute of Electrical and Electronics Engineers (IEEE)

Reprinted, with permission, from IEEE.

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Aalto University’s products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org.

By choosing to view this document, you agree to all provisions of the copyright laws protecting it.
20.3 An Interface for a 300°/s Capacitive 2-Axis Micro-
Gyroscope with Pseudo-CT Readout

Lasse Aaltonen\(^1\), Timo Speelti\(^1\), Mikko Saukoski\(^1,2\), Kari Halonen\(^1\)
\(^1\)Helsinki University of Technology, Espoo, Finland
\(^2\)ELMOS Semiconductor, Dortmund, Germany.

The widespread use of capacitive MEMS vibratory gyroscopes is powerfully driven by low cost [1]; this is partly determined by factors such as die area and the number of necessary external components. Important properties of gyroscopes also include a short start-up time, and resolution that has been recently improved by applying the mode-matching technique [2,3]. However, the electro-mechanical feedback loop for active-mode matching requires additional DSP and chip area, and involves an additional slowly settling loop during the sensor start-up.

The pseudo-continuous-time (CT) secondary (sense) readout technique introduced in this paper is applied to the open-loop secondary readout of a gyroscope operating in the low-pass region. The technique alleviates the issues related to complexity and area as well as the long time constants of the CT readout [4,5] without compromising noise performance or start-up time. The proposed 5.4mW gyroscope interface includes an on-chip HV charge-pump (CP) for excitation and signal detection.

The block diagram of the interface is shown in Fig. 20.3.1. Reliable start-up and clock generation require a CT readout to be used for the drive (primary) loop, although its use can be avoided in the secondary channels. The lossy loop integrator provides the required phase shift, while decreasing the gain at higher frequencies, hence reducing sensitivity to the parasitic resonance modes of the drive resonator. The HPFs provide low-noise gain and remove the offset of preceding blocks; this is also important for the sine-to-square conversion that is required to generate a reference clock for the system. To prevent excess phase noise and glitches in the clock, the noise BW of the amplified primary signal is limited in the integrator before feeding the sine wave to the reference clock generator. In the generator, the signal is led to a comparator through a passive HPF (-3dB @ 200Hz) that removes any remaining offset. The phase shift from the charge-sensitive amplifier (CSA) input to the comparator input can be tuned to 90° with a 1° error over the temperature range. The resulting clock is used as a reference for the fully integrated PLL and as a clock for the amplitude controller, which controls the drive loop dynamics and start-up. During initial start-up, the SC amplitude controller receives few random clock pulses due to the loop DC setting, and amplifies the input signal, \(V_{in}\). The resulting DC control signal maximizes the VGA gain and the drive signal quickly reaches the CP limited level. When the primary signal has increased sufficiently, the signal amplitude settles to the level defined by \(V_{exit}\). In the amplitude controller, filter HPF3, which isolates the SC controller from the CT readout, has feedback MOSFETs that are also used in CSA, HPF1 and HPF2. The additional capacitor \(C_F\) of value 1pF, not present in a primary signal, starts when

\[
\phi_{r1} \text{ goes low. To remove } kT/C \text{ noise at the CSA output, } \phi_{ix}, \text{ which corresponds to the sampling point.}
\]

The prototype is fabricated in a 0.35um HVCMOS technology. The chip (Fig. 20.3.6) area is 7.9mm\(^2\) with an active area of 2.5mm\(^2\). The chip is combined with a 2-axis micro-gyroscope on a PCB and measured using off-chip references. The DC transfer functions from input angular velocity to sensor output, measured at the full input range of \(\pm 300°/s\) and in the temperature range from -10 to 90°C, are shown in Fig. 20.3.3. The noise floors of the sensor, shown in Fig. 20.3.4(a,b), are measured with DC detection of 8.75V, created on-chip using a 2V external \(V_{ref}\). Though the secondary resonators are symmetrical, the quadrature signal levels differ, which affects the interface noise properties. In addition, the compensation cannot fully remove the y-channel quadrature signal, which impairs the linearity and noise performance. The x-channel noise is dominated by the excessive flicker noise of the front-end, and increased by parasitic capacitance on the PCB and cross-coupled drive noise at frequencies above 10Hz. In Fig. 20.3.4(c,d) both channels are shown during start-up. The start-up begins when CP reset is removed, and in 0.4s the secondary channels reach the final zero-rate output (ZRO) with a maximum error of \(\pm 6°/s\).

The ASIC for the 2-axis gyroscope draws 1.8mA from the 3V nominal supply. The proposed pseudo-CT readout technique offers reduced complexity, inherent amplitude detection and chopper stabilization, with minimal noise increase compared with the CT interface. The system parameters and performance are summarized in Fig. 20.3.5.

Acknowledgments:
We thank VTI Technologies for providing the sensor elements and for funding, and the Finnish Funding Agency for Technology and Innovation for funding.

References:
\(\Delta\Sigma\) Closed-Loop Vibratory-Gyroscope Readout Interface with a 0.004°/\sqrt{VHz} Noise Floor over a 50 Hz Band,” ISSCC Dig. Tech. Papers, pp. 580-581, Feb. 2006.
Figure 20.3.1: Block diagram of the interface including an electrical model and schematic drawing of the sensor element, together with more detailed structures of both the CT primary readout and amplitude controller (half of the differential circuit is shown).

Figure 20.3.2: Schematic and used clock signals of the secondary readout channel, which consists of the pseudo-CT readout and the SC notch filters.

Figure 20.3.3: Transfer functions from DC angular velocity to sensor output voltage for both channels at temperatures from -10°C to 90°C in steps of 30°C and 20°C.

Figure 20.3.4: Measured (a) x-channel and (b) y-channel noise floors, and measured (c) x-channel and (d) y-channel outputs during start-up.

Figure 20.3.5: Summary of the measured performance and the open-loop characteristics of the sensor element.