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Via-in-pixel design of truly 2D extendable photodiode detector for medical CT imaging

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Abstract

This paper presents a new design of the silicon-based photodiode detector for medical imaging, especially for the X-ray computed tomography applications. The new structure of the photodiode includes a conventional front-illuminated photodiode and a through wafer interconnection. Moreover, the through wafer interconnection is integrated into the photodiode by being placed inside the active area of the photodiode. This new structure is called via-in-pixel design. Truly 2D photodiode detector can be designed with maximum free space or minimum gap between each two photodiode elements by using the via-in-pixel design. In addition, 2D photodiode detector arrays can be constructed by tiling more edgeless detectors. In the paper, the via-in-pixel photodiodes were demonstrated and the performances were measured. Together with the measurement data, a quasi-3D device simulation was performed to disclose the electrical characteristics of the via-in-pixel photodiode by using Synopsis Advanced TCAD software. The results show that the via-in-pixel design of the photodiode detector can either meet or exceed the medical imaging requirements.

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Keywords: Via-in-pixel design; Computed tomography; Photodiode detector; Through wafer interconnection

1. Introduction

In the X-ray computed tomography (CT) for medical applications, an X-ray source and an array of photodiode detectors are oppositely fixed on a rotating gantry. The X-ray source gives out a fan beam or a cone beam of X-ray. The relative attenuation of the X-rays is recorded by each photodiode element on the detectors when a patient is passing through the imaging system. Thus 2D or 3D images of the interesting object can be reconstructed from continuously collected data by using complex algorithms. 1D detectors have always been used in the system, but image acquisition of the object is very slow. Quasi-2D (multi-slice) detectors with certain limitations are gradually entering the industry [1]. The trend of the modern CT system is to further increase the scanning speed and the image quality.

For a modern spiral CT system [2], the scanning speed can be given by

$$d = \frac{pMS}{t_{\text{rot}}}, \quad (1)$$

where d is the feed speed of the patient, p is the pitch factor of the detector, M is the pixel number (slice number) of the detector along the patient feeding direction, S is the slice width and t_{rot} is the time of one rotation of the gantry. From Eq. (1), the scanning speed can be greatly increased by simply using multi-slice photodiode detector, which means large area detector. For instance, this gives an opportunity to construct cardiac imaging systems capable of completing the whole scan within one breath cycle. Fig. 1 shows a sketch map of the human heart coverage of one detector rotation cycle corresponding to the slice number of the detector arrays. Moreover the resolution of the image is generally known, dependent on the element size. Therefore, high percentage of the sensitive surface coverage of the large

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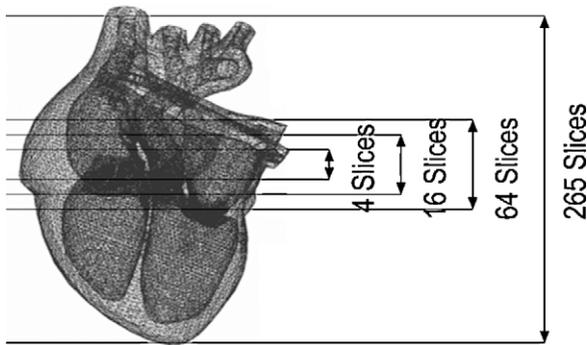


Fig. 1. Sketch map of detector coverage vs. slice number of detector.

area photodiode detector with more elements in 2D is highly demanded by the modern CT industry.

In the conventional CT detector construction, a major limiting factor in providing more detector coverage is the need to read out the signal from the individual photodiode element of the detector through the metal line on the sensitive surface facing the radiation source. The more photodiode elements on the detector, the more space are needed for the readout line. In addition, the associated bonding pads and bonding wires consume a lot of space on the edge of the detector. This prevents the further construction of extended 2D tiled edgeless detector arrays for the imaging systems. These limitations have been discussed in Refs. [3–6], and accordingly two methods have been reported to overcome the problems so far. The first solution is the back-illuminated photodiode (BIP) method [3,4], which has the drawbacks in the fabrication and operation. One drawback is the handling of thin wafers with the thickness typically 100 μm , and the other drawback is the low working bandwidth due to the light current collection by carrier diffusion mode. The second solution is the conventional front-illuminated photodiode (FIP) [7] with a separated through wafer interconnection (TWI) [5,6]. Even though the signal of each photodiode element can be read out directly from the back side of the detector through the TWI, certain space, typically a few hundreds of microns, is still needed for the TWI between each two photodiode elements.

In order to maximize the coverage of sensitive surface and give more flexibility of the photodiode element arrangement, this paper presents an integrated structure of the photodiode with TWI inside the photodiode active area, called the via-in-pixel (VIP) design. Integrating the TWI into the photodiode active area will have certain impacts on the performances of the VIP photodiode. In order to disclose the electrical characteristics of the whole structure, especially the behavior of the PN-junction area next to the TWI, a powerful quasi-3D device simulation software is used to simulate the operation of the demonstrated photodiode under non-illuminated conditions. Furthermore, different electrical parameters are measured from the demonstrated samples, and compared to the simulation results.

2. Design and fabrication

The test VIP photodiodes were designed and demonstrated in this paper. The dimension of the photodiode was optimized

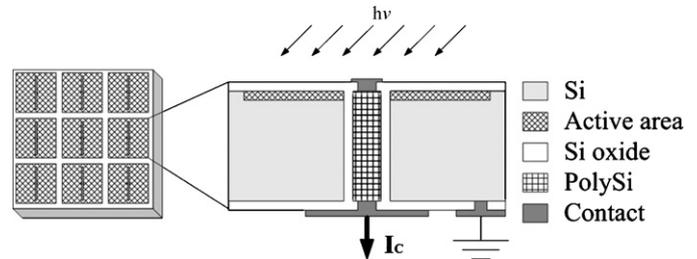


Fig. 2. Detector structure and the cross section of one VIP photodiode element.

for the applications in the medical CT imaging. A typical VIP photodiode detector with 3×3 matrices of photodiode elements and the cross section of the VIP photodiode element can be seen in Fig. 2. The active area of each photodiode element is about 1 mm^2 , and the TWI is inside of the photodiode active area having the dimension of $\phi 50 \mu\text{m}$. The TWI consists of the isolated sidewall and the conductive filling plug. The anode of the photodiode is connected to the top end of the TWI by a vertical metal bar directly on the front surface, and the corresponding contact pad of the anode is connected directly to the bottom end of the TWI on the bottom surface. The silicon substrate serves as the common cathode for each photodiode element with a metal pad connected on the bottom surface as well. The width of the anode metal bar on the front surface is $30 \mu\text{m}$ and the size of the anode contact pad on the bottom surface is about $160 \mu\text{m} \times 160 \mu\text{m}$. It can be seen from the cross section that the incoming light impacts on the front surface of the photodiode, and the photocurrent is collected by the space charge region of the diode junction, then the signal can be read out directly from the bottom through the contact pad. Since the metal bar contact for the anode on the front surface is needed whether the TWI is used or not, the extra active area taken by the TWI from the photodiode active area is negligible, only 0.12% calculated for the 1 mm^2 photodiode active area.

The fabrication of the VIP photodiodes includes two parts. The first part is the processing of TWI by using inductive coupled plasma (ICP) etching, thermal oxide isolation, in situ boron-doped polycrystalline silicon filling and the wafer surface planarization [8]. The ICP etching created a high aspect ratio through wafer via structure on the wafer. Thermally grown silicon dioxide thereafter protected the whole wafer surface including the sidewall of the through wafer vias. Heavily boron-doped polycrystalline silicon was uniformly deposited afterwards by using low-pressure chemical vapor deposition (LPCVD) method, which totally filled the through wafer vias. The planarization of both wafer surfaces was performed by using grinding and chemical mechanical polishing (CMP). Because the wafer with TWIs is fully compatible with the standard silicon processing technologies, basically all the semiconductor processings can be integrated directly onto the pre-processed wafers. This gives great advantages for the productivity. The second part of the fabrication is the photodiode structure. It mainly includes the formation of the PN-junction near the top surface of silicon wafer. Lithography, implantation and annealing were used to form the active area of the photodiode. The contact openings and contact pads on both sides of the TWI were thereafter

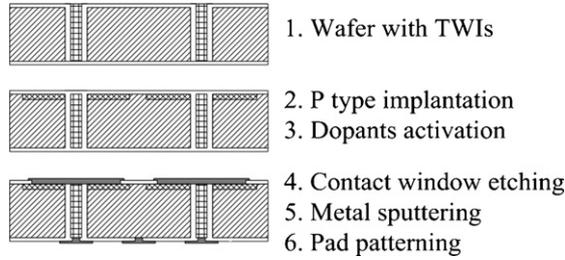


Fig. 3. The processing flow of the VIP photodiode samples.

processed by using the well known wet and dry etching, sputtering and patterning. The rough processing flow can be seen in Fig. 3, where the steps 4–6 shows the cross section from the length direction of the contact metal bar on the front surface. The cross section from the width direction of the contact metal bar can be seen in Fig. 2. In the large area photodiode detectors, the gap between each two photodiode elements is depended on the requirement of the cross talk. Even though this paper only presents a relatively simple way of making photodiodes, there is no limitation of placing more features like usually used guard ring structures and channel stops. The final thickness of the photodiode samples is about 300 μm , it can easily reach 400 μm or even thicker for more robust processing.

3. Measurement results and discussion

The electrical performance of the demonstrated VIP photodiodes was measured within a dark probe station. The measurement results mainly include the leakage current under different bias voltages, series resistance, shunt resistance, breakdown phenomenon and the capacitance of the VIP photodiodes. The measured IV and CV characteristics of the VIP photodiode are also compared with the simulation results. More explanations about the simulation results will be given in the next section. In addition to the measurement under the non-illuminated conditions, the light current result shows the preliminary operation of the VIP photodiode.

3.1. The IV characteristics

The photodiodes are typically optoelectronic PN-junction devices used under a reverse bias. The current generated by the photodiode under reverse bias without light illumination is called the leakage current, and the leakage current presents the background noise in the CT imaging system. The leakage current mainly includes three parts. The first part is the saturated diffusion current [9], and it can be calculated by

$$I_{\text{dc}} = qA_{\text{PN}}n_i \left(\frac{D_e}{N_d L_e} + \frac{D_h}{N_a L_h} \right), \quad (2)$$

where q is the electronic charge, A_{PN} is the PN-junction area, D_e/D_h is the electron/hole diffusion coefficient, L_e/L_h is the electron/hole diffusion length in the quasi-neutral region, n_i is the intrinsic concentration of silicon, N_a/N_d is the doping concentration of acceptor/donor. It can be seen from Eq. (2) that the diffusion current is not related to the bias voltage,

but much depended on the material. The second part is the generation–recombination current [9], and it can be calculated by

$$I_{\text{grc}} = \frac{qA_{\text{PN}}n_i W}{\tau_{\text{g-r}}}, \quad (3)$$

where W is the depletion region width of the PN-junction, $\tau_{\text{g-r}}$ is the carrier generation–recombination lifetime within the depletion region. It can be seen from Eq. (3) that at fixed conditions the variable W is only dependent on the reverse bias voltage V with W proportional to \sqrt{V} . The third part but not the last part is the surface leakage current [10], and it can be calculated by

$$I_{\text{slc}} = \frac{qn_i A_{\text{sur}} S_{\text{sur}}}{2}, \quad (4)$$

where A_{sur} is the PN-junction depletion area on the silicon–oxide interface, S_{sur} is the surface recombination velocity. A_{sur} is not only dependent on the reverse bias voltage, but also dependent on the fixed oxide charge density. In the VIP photodiode, the surface leakage current is generated in two specific locations, which are at the edge of the photodiode and at the sidewall surface of the TWI next to the junction of the photodiode. In general, the saturated diffusion current is negligible compared to the other two parts. There are also auger recombination and high field triggered leakage current, but they are also very small and nearly constant under normal working conditions. Fig. 4 shows the measured IV curve and the simulated IV curves. At the full depletion condition, Eq. (3) gives 13 pA, which corresponds very well the measured value around 4 V. It indicates that the leakage current is dominated by the generation–recombination current over the surface leakage current. Even though the surface recombination velocity is proportional to the damage of the silicon surface on the sidewall of TWI caused by the TWI processes, it is only considered as a minor effect to the total leakage current and S_{sur} should have a small value. At the high voltages, when the electric field begins to reach the breakdown voltage of silicon, the main component of the total leakage current switches to the impact ionization current. It is generated only at high electric field “hot spots” at the outer edge of the photodiode and at the corner areas of TWI next to the PN-junction of the photodiode.

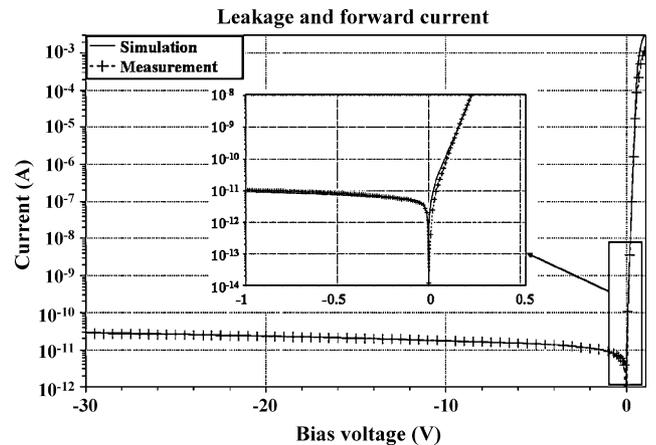


Fig. 4. The measured and simulated leakage current of VIP photodiode.

The breakdown of the conventional photodiode usually happens at the outer corner of the junction edge where there is the highest electrical field. Moreover, the breakdown for a pure TWI without the integrated photodiode is the oxide sidewall breakdown and the breakdown voltage is more than 200 V obtained from our previous report [8]. Since the VIP photodiode is the integration of the conventional photodiode and the TWI, the breakdown may happen at different place with different breakdown voltage. The measured breakdown voltage of the demonstrated VIP photodiode is about 160 V. In order to find where the breakdown is, simulations were performed by using different oxide sidewall thickness of the TWI. The breakdown voltage changes dramatically according to oxide sidewall thickness changes, and the thinner the oxide sidewall thickness the breakdown voltage is smaller. Fig. 5 shows the beginning of the breakdown of the VIP photodiode with the measured and simulated data. The dependence on the oxide sidewall thickness of the TWI gives the clue that the breakdown takes place at the ‘hot spot’ at the corner areas of the TWI next to the PN-junction of the photodiode. In addition, the electrical field of the PN-junction affects the electrical field of the oxide sidewall of the TWI with each other, and all together decreases the breakdown voltage.

The series resistance of the VIP photodiode mainly includes the resistances from TWI, bulk silicon, and the terminal contacts. It can be calculated by using the dynamic current value under the 1 V forward bias condition [5], which gives the average value of 210 Ω . The resistance of TWI holds most of the series resistance of the VIP photodiode. The rest resistance components are negligible with the resistivity of the bulk silicon in milliohm range and the good ohmic contacts. The dark current of the VIP photodiode, which is the current directly measured under the 10 mV reverse bias, is about 1 pA on average. This dark current is well compatible with the dark current from the conventional photodiode without TWI. Based on the gate-controlled diode structure [11], the silicon surface next to the sidewall of the TWI is not depleted with certain positive fixed oxide charge in the sidewall oxide at such low bias voltage. The dark current is mainly from the generation–recombination current as it is in conventional photodiode. Moreover, the n-type autodoping of

the silicon surface next to the TWI sidewall during the oxidation process also helps to postpone the depletion of the silicon surface. The beginning of silicon surface depletion can be seen later in Figs. 9 and 10. The shunt resistance of the VIP photodiode can be easily calculated by using the voltage current ratio under the 10 mV reverse bias, and it gives 10 G Ω on average.

3.2. The CV characteristics

The capacitance of the photodiode together with the series resistance also contributes to the noise of the signal in the data acquisition system. Keeping the capacitance of the photodiode in certain level is required. The total capacitance of the VIP photodiode includes mainly three parts. The first part comes from the PN-junction, and it can be given by

$$C_{PN} = \frac{A_{PN}\epsilon_s}{W}, \quad (5)$$

where ϵ_s is the permittivity of silicon. The second part comes from the TWI it can be evaluated by using MOS structure [12,13], and the calculation at high frequencies can be given by

$$F = \sqrt{\frac{N_d}{n_i}} \sqrt{-(v_s + 1) + e^{v_s} + \left(\frac{n_i}{N_d}\right)^2 e^{-v_s}},$$

$$Q_s = -\text{Sign}(v_s) \frac{kT\epsilon_s F}{q\lambda_i}, \quad V + \frac{Q_f}{C_{ox}} - \psi_{ps} = \frac{Q_s}{C_{ox}} + \frac{kTv_s}{q},$$

$$C_s = \text{sign}(v_s) A_{TWI} \frac{\epsilon_s (e^{v_s} - 1)}{\sqrt{2\lambda_n} \sqrt{-(v_s + 1) + e^{-v_s}}},$$

$$C_{ox} = \frac{\epsilon_{ox} A_{TWI}}{d_{TWI}}, \quad \frac{1}{C_{TWI}} = \frac{1}{C_s} + \frac{1}{C_{ox}} \quad (6)$$

where F is the dimensionless electric field, Q_s is the silicon surface charge density per unit area, $v_s = q\psi_s/kT$ and ψ_s is the band bending potential along the silicon surface, λ_i is the intrinsic Debye length, λ_n is the silicon bulk Debye length, Q_f is the fixed oxide charge density per unit area, ψ_{ps} is the work function difference between the boron-doped polycrystalline silicon and the bulk silicon, A_{TWI} is the sidewall surface area of the TWI, ϵ_{ox} is the permittivity of the silicon dioxide, d_{TWI} is the oxide thickness of the TWI sidewall. Fig. 6 shows the CV curves measured and simulated from a pure TWI at 1 MHz frequency and in the dark condition. It can be seen that the capacitance introduced by the TWI is very small, and the change of the capacitance with the bias voltage sweep is negligible. The third part of the capacitance comes from the contact pad and it can be estimated by using $C_{pad} = \epsilon_{ox} A_{pad}/d_{pad}$, where A_{pad} is the pad area and d_{pad} is the oxide thickness beneath the pad. The fixed oxide charge density is estimated to be $5 \times 10^{10} \text{ cm}^{-2}$ by using the measurement data from the pure TWI structure according to Eq. (6). It can be seen in Fig. 6 that the simulated CV curve moves horizontally with different fixed oxide charge density values. The CV curve with fixed oxide charge density of $5 \times 10^{10} \text{ cm}^{-2}$ fits the measurement data the best. The measured and simulated CV curves from the VIP photodiode are shown in Fig. 7. The capacitance difference between the measurement and simulation is mainly

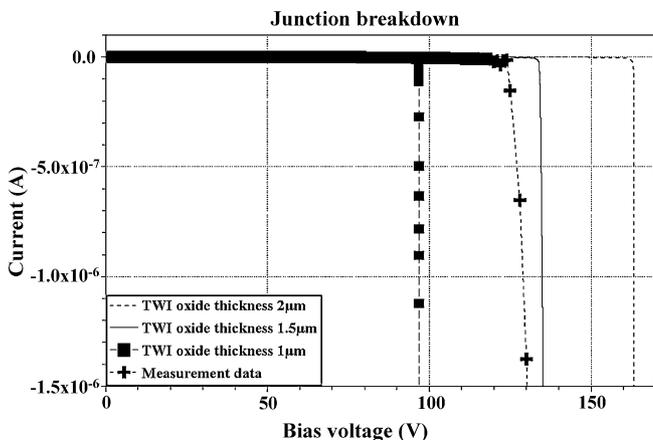


Fig. 5. Measured and simulated junction breakdown leakage current with the sidewall oxide thicknesses of 1, 1.5 and 2 μm .

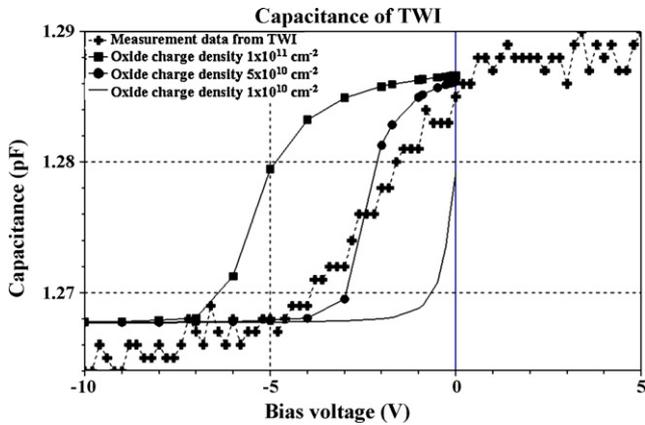


Fig. 6. Measured and simulated TWI capacitances with different fixed oxide charge densities.

due to the missing contact pad for the simulated VIP photodiode device. The VIP photodiode structure for the capacitance simulation can be later seen in Fig. 9.

3.3. The optical characteristics

When a silicon-based photodiode is illuminated by the light having the energy greater than the silicon band-gap energy, the light is absorbed by the semiconductor and the electron–hole pairs are generated. The electrons and holes are separated by the electric field within the depletion region of the PN-junction, and the light current is thereafter read out from the anode of the photodiode. When the VIP photodiode is illuminated by the light, the light current is generated and the measurement results can be seen in Fig. 8. In the CT imaging system, the photodiodes usually work at -10 mV bias voltage, where it gives the maximum current signal.

4. Quasi-3D simulation

Synopsis advanced TCAD quasi-3D simulations, i.e. a 2D simulation carried out in the cylindrical coordinates, of the VIP photodiode were used to model the device opera-

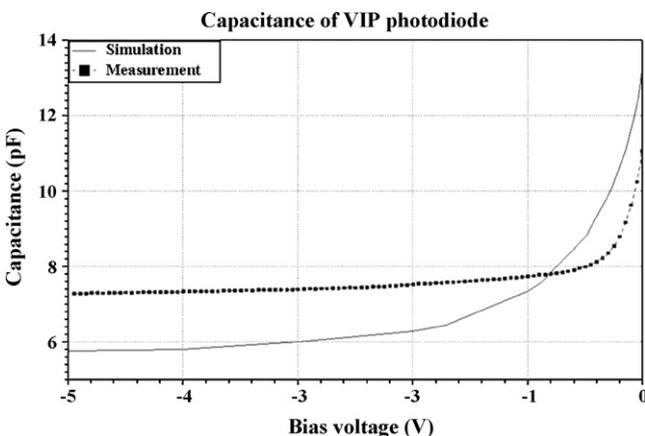


Fig. 7. Measured and simulated capacitances of the VIP photodiode. The simulation does not include the capacitance of the contact pads.

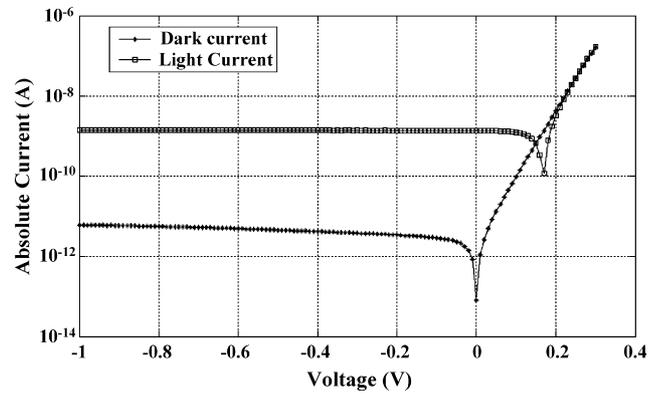


Fig. 8. The light current compared with the dark current measured from the VIP photodiode.

tion, especially the PN-junction area close to the TWI. The free parameters of the simulation, such as the fixed oxide charge density, surface recombination velocity and the carrier generation–recombination lifetime, were obtained from the measurement data of the demonstrated TWI structures and VIP photodiodes.

The simulated 2D structure, shown in Fig. 9(a), has a total thickness of $300\ \mu\text{m}$ with a $25\ \mu\text{m}$ thick high resistive n-type epitaxial layer on top of the conductive n-type silicon bulk. A radius of $25\ \mu\text{m}$ polycrystalline silicon plug with a $1.5\ \mu\text{m}$ thick sidewall oxide was used to define the TWI. To perform the simulation in the cylindrical coordinates the radius of the photodiode was selected such that the total active area of the simulated VIP photodiode matches with the demonstrated VIP photodiode. Thus the active area with radius of $0.564\ \text{mm}$ on the front surface was set to give the total active area of around $1\ \text{mm}^2$. The 2D doping profile of the p-type implantation for the active area was extracted by using synopsis process simulator with a Monte Carlo mode with 200,000 particles. The device simulation grid had in total around 40,000 calculation points and the grid was made denser along all the silicon–oxide interfaces down to around $1\ \text{nm}$ between each two calculation points.

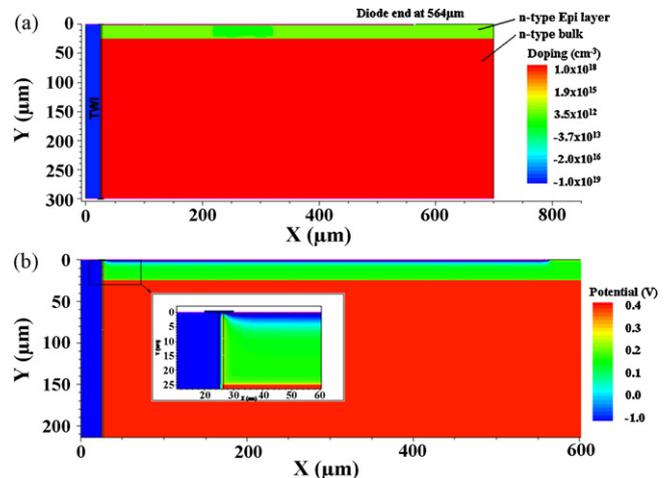


Fig. 9. (a) Doping profile of the structure used in the quasi-3D simulations. The Y-axis at $X=0$ was considered as the axis of rotation. (b) The potential distribution at the common operation condition.

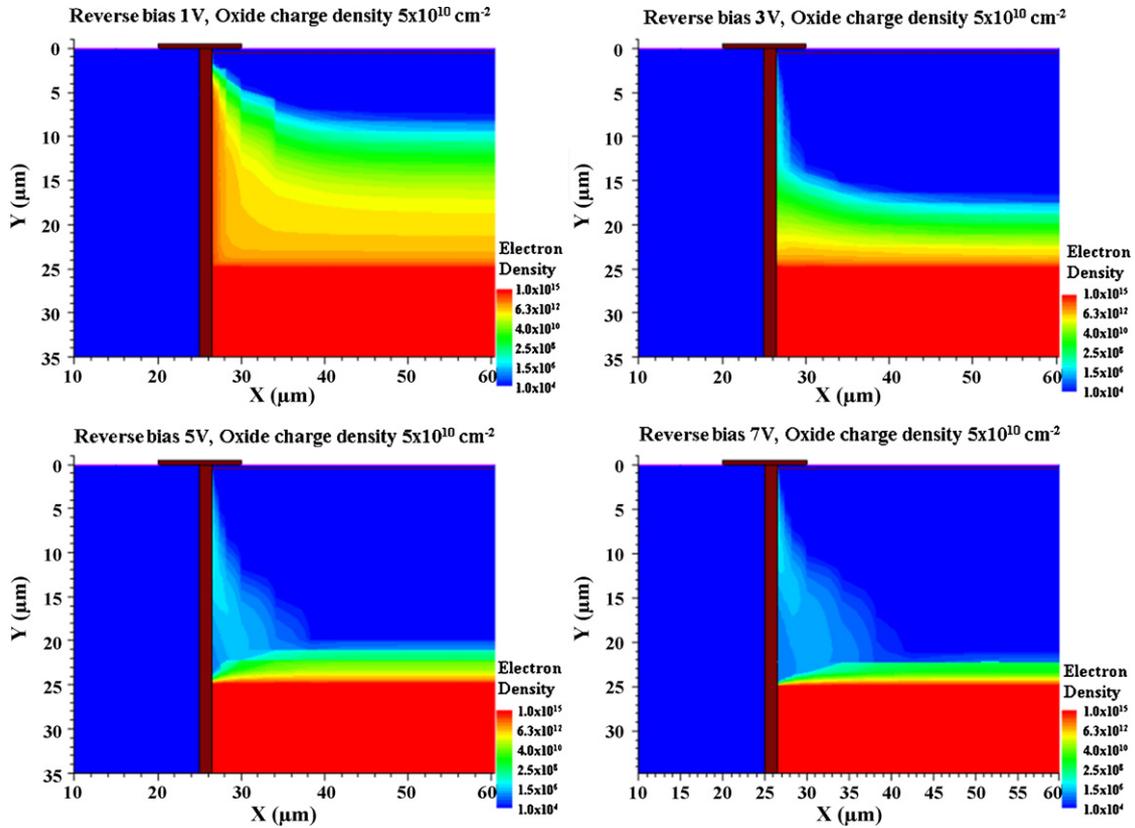


Fig. 10. The depletion of the PN-junction next to the TWI with respect to the electron concentration.

Fig. 9(b) shows the potential distribution of the simulated VIP photodiode at its operation voltage.

The carrier generation–recombination lifetime, τ_{g-r} , was extracted by using Eq. (3). The lifetime of 3 ms was obtained from the measured leakage current value of 13 pA at 4 V reverse bias. As seen in Fig. 10, the high resistive epitaxial layer is fully depleted at 4 V. Moreover, the silicon surface of the epitaxial layer next to the sidewall of the TWI is inverted at 4 V reverse bias as seen in Fig. 6. So, the surface leakage current should have a very small contribution to the measured leakage current.

For the simulated leakage current, S_{sur} , the surface recombination velocity of 3 cm/s was found to give proper behavior of the current up to -30 V, as seen in Fig. 4. The target sidewall oxide thickness of the TWI, 1.5 μm , which is used in the process, has been verified by using the simulations. Fig. 5 shows the breakdown of the measured and simulated VIP photodiode with different oxide thicknesses of the TWI sidewall. The target oxide thickness of 1.5 μm is shown to give approximately correct breakdown voltage behavior. In addition, Fig. 6 has a more profound meaning. It verifies that the sidewall oxide thickness of the TWI has a major impact on the breakdown of the VIP photodiode and implies that the breakdown of the VIP photodiode takes place in the corner of PN-junction next to the TWI.

The fixed oxide charge density of the TWI sidewall, which was used in the simulations for the surface oxide as well, was determined by the individual TWI measurement. The best fitting of the fixed oxide charge density was found to be $5 \times 10^{10} \text{ cm}^{-2}$ from Fig. 6. With the determined fixed oxide charge density,

Table 1

Summary of the key parameters obtained for the simulation

Parameters	Value
Carrier lifetime (ms)	3
Surface recombination velocity (cm/s)	3
Fixed oxide charge density of TWI sidewall (cm^{-2})	5×10^{10}
Fixed oxide charge density of surface oxide (cm^{-2})	5×10^{10}
Oxide thickness of the TWI sidewall (μm)	1.5

the depletion of the region around the TWI with different bias voltages can be seen from Fig. 10. The sharpening of the electron density at the bottom corner of the epitaxial layer next to the TWI is being visualized at 7 V reverse bias. At the reverse bias voltages higher than 30 V, the n-type bulk begins to be depleted from this corner and a region of high electric field is created there. This is a favorable region for the impact ionization current creation and finally the device breakdown happened there prior to the outer edge of the photodiode.

Table 1 summarizes the simulation parameters to correctly describe and understand the behavior of the measured currents and capacitances.

5. Conclusions

The novel VIP design of the photodiode presented in this paper gives a promising solution for truly 2D extendable photodiode detector in medical CT imaging application. The 2D

photodiode detector can be constructed with maximum free space or minimum gap between each two photodiode elements. In addition, more detectors can be tiled together in 2D to have larger detector arrays. IV characteristics, CV characteristics and optical characteristics were measured and discussed from the demonstrated VIP photodiode. Quasi-3D VIP photodiode device was constructed and simulated. The simulation results match the measurement results quite well with proper key parameters obtained. The impact of integrating TWI into the photodiode active area was analyzed by using simulated and measured results. It shows that the effect of the sidewall on the VIP design is negligible under normal operation conditions. The performances and characteristics of the demonstrated VIP photodiodes show that it can meet or exceed the application requirements from the industry.

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Biography

Fan Ji did B.S. from School of Mechanical Engineering and Automation, Beijing University of Aeronautics and Astronautics, Beijing, China, in 2000. M.S. from Department of Precision Instruments, Tsinghua University, Beijing, China, in 2003. Now, the author is working for Detection Technology Inc., Finland, and in the same time being a Ph.D. student of Electrical and Communications Engineering Department, Helsinki University of Technology, Finland. The research area of the author is microelectronic sensors, especially radiation imaging detectors.