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A 12-bit 32 μW Ratio-Independent Algorithmic ADC

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Abstract

This paper describes a ratio-independent algorithmic ADC architecture that requires a single differential amplifier and a comparator. The prototype 12-bit, 41.67 kS/s ADC with an active die area of 0.055 mm^2 is implemented in a 0.13 μm CMOS. The power dissipation is minimized using a dynamically biased operational amplifier. With a 32 μW power dissipation, the ADC achieves 80 dB SFDR and 60 dB SNDR, resulting in a power FOM of 0.9 pJ/conversion. (Keywords: algorithmic ADC, cyclic ADC, ratio-independent, low-power)

Introduction

In various sensor systems, there is a need for ADCs with resolutions ranging from 8 to 12 bits and sample rates under 100 kHz. When the target is to minimize area and power dissipation, an algorithmic or a cyclic converter is an attractive choice [1]. The presented ADC architecture is insensitive to capacitance ratios, amplifier offset, and input parasitics.

Algorithmic Converter

To minimize the ADC silicon area, a ratio-independent architecture is preferred [1]. A traditional ratio-independent algorithmic converter requires two amplifiers and a comparator [1]. To minimize the power dissipation, the number of amplifiers is halved in the presented ratio-independent ADC architecture. The offset and 1/f-noise compensation is done using offset polarity reversing, a similar approach as in [2].

The ADC operation phases are shown in Fig. 1. One bit polarity is resolved in four clock steps. However, three clock step operation is also possible by combining phases 3 and 4, and phases 7 and 8, which leads to increased amplifier loading. In this design, minimizing the current consumption was more important than speed, thus a four clock step approach was chosen to relax the amplifier loading. The total conversion time is $4{\cdot}N = 48$ clock steps, where the number of bits $N = 12$.

Phases 1–4 resolve the most significant bit (MSB) (Fig. 1a) and phases 5–8 are recycled to resolve the rest of the bits (Fig. 1b). Phase 1: The sampled input signal results in charges $C_1(V_{OFF} - V_{IN})$ and C_2V_{OFF} in the respective capacitors. Phase 2: The amplifier output voltage in hold-mode is V_{IN}. Comparator preamplifier offset voltage is stored in capacitor C_C. Phase 3: The polarity of the sampled input voltage is resolved. Phase 4: Voltage V_{IN} is stored in capacitor

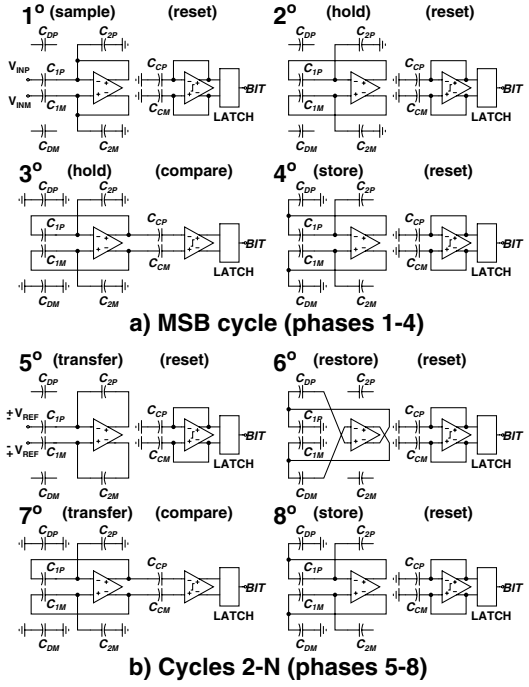

Fig. 1. ADC operation phases.

C_D. Phase 5: The charge $C_1(V_{OFF} - V_{IN})$ stored in capacitor C_1 is transferred to capacitor C_2, resulting in charge $C_2\{V_{OFF} - k[V_{IN} + (-1)^{b(i)}V_{REF}]\}$, where $k = (C_1/C_2)$ and $b(i)$ is the bit from the previous cycle. Phase 6: The voltage $V_{IN} - V_{OFF}$ is stored in capacitor C_1. The polarity of the offset voltage is changed by cross-connecting the differential amplifier inputs and outputs during this step. Comparator preamplifier offset voltage is stored in capacitor C_C. Phase 7: The charge stored in capacitor C_2 is transferred back to capacitor C_1, resulting in output voltage $V_{OUT} = V_{IN}+k(1/k)[V_{IN}+(-1)^{b(i)}V_{REF}] = 2V_{IN}+(-1)^{b(i)}V_{REF}$. Thus, the output voltage is independent of the capacitance ratio k and amplifier offset voltage V_{OFF}. Finally, the polarity of the output voltage is resolved. Phase 8: The output voltage is stored in capacitor C_D for the next cycle. Phases 5–8 are recycled to resolve the desired number of bits. The schematic of the ADC is shown in Fig. 2.

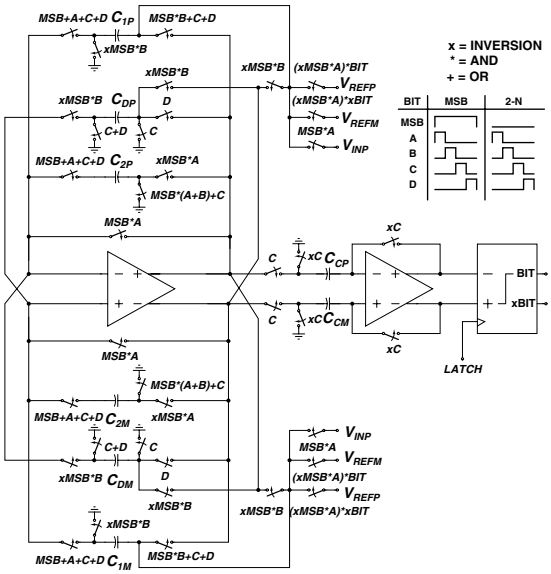

Fig. 2. Algorithmic ADC schematic.

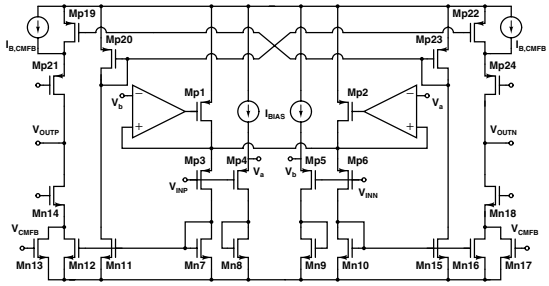

Fig. 3. Schematic of the operational amplifier.

The operational amplifier accounts for a major part of the total current consumption in the converter. To minimize the power dissipation, a tail-current boosted class AB operational amplifier, shown in Fig. 3, is used [3]. With current boosting, the amplifier biasing can be based purely on its small-signal behavior, as the slew-rate is not limited. With critically damped settling, the required minimum gain–bandwidth product (GBW) to ensure sufficient settling accuracy is $GBW = -(\ln E)/(4\pi T)$, where E is the expected settling accuracy and T is the settling time. The input pair formed by Mp3 and Mp6 is operated in weak inversion to maximize the current efficiency g_m/I_D.

Measured Results

The prototype ADC is fabricated in a 0.13 μm CMOS technology. The active chip area is 0.055 mm^2 (Fig. 4), and it draws 18 μA at 41.67 kS/s from a 1.8 V supply. The measured 8192-point FFT plot for a full-scale 18 kHz sinusoidal input signal is shown in Fig. 5. The measured SNDR=60 dB and SFDR=80 dB. The performance is summarized in Table I.

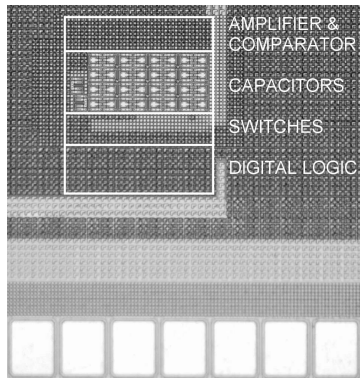

Fig. 4. Chip microphotograph.

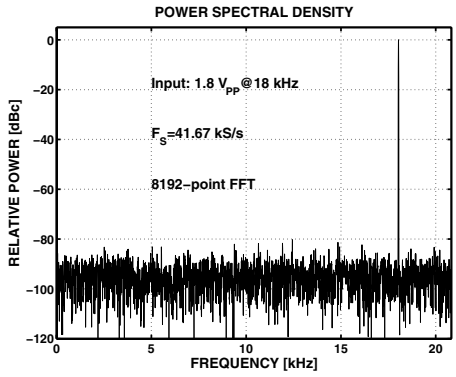

Fig. 5. Measured output spectrum.

TABLE I
PERFORMANCE SUMMARY

Resolution	12 bits
Conversion rate	41.67 kS/s
Process	0.13 μm CMOS
Active area	0.055 mm^2
SNDR/SFDR	60 dB / 80 dB
ENOB	9.7
Power dissipation	32 μW
Power FOM	0.9 pJ/conv

Acknowledgments

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References

[1] P. Li, M. Chin, P. Gray, and R. Castello, "A ratio-independent algorithmic analog-to-digital conversion technique," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 828–836, Dec. 1984.

[2] B. G. Lee, and S. Yan, "A new ratio-independent A/D conversion technique for high-resolution pipeline A/D converters," *Proc. of IEEE ISCAS*, pp. 1960–1963, 2005.

[3] R. Harjani, R. Heineke, and F. Wang, "An integrated low-voltage class AB CMOS OTA," *IEEE J. Solid-State Circuits*, vol. 34, pp. 134–142, Feb. 1999.