A 20 MHz BP-PWM AND BP-DSM CLASS-D PA IN 0.18 μm CMOS

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ABSTRACT

This paper presents a Class-D power amplifier for bandpass pulse width modulated (BP-PWM) and bandpass delta-sigma modulated (BP-DSM) signals at 20 MHz. A 1-bit 6-th order topology is used in the $\Delta\Sigma$-modulator. Integral noise shaping is used in the generation of the bandpass pulse width modulated signal. A two sided pulse width modulation is used with a 6-bit 4th-order noise shaper. The push-pull amplifier part of the Class-D amplifier was fabricated on a 0.18 μm CMOS process and the bandpass filter was composed of a LC ladder network realised with discrete components.

1. INTRODUCTION

Delta-Sigma ($\Delta\Sigma$) modulation and Pulse Width Modulation (PWM) are both widely used in audio application in order to produce high fidelity sound from e.g. data stored on a compact disc [1, 2, 3]. Recently both of these have been researched as methods of digital to analog conversion at higher frequencies including radio frequencies [4, 5, 6, 7]. Class-D power amplifiers and other switching class amplifier have likewise been widely used in audio applications in conjunction with the above-mentioned modulation classes in order to achieve distortionless amplification and high efficiency. It also shares the recent research interest with these [4, 5, 6, 7].

This paper studies both bandpass pulse width modulation and bandpass $\Delta\Sigma$ modulation in combination with an integrated Class-D amplifier operating with an 80 MHz sampling frequency and a signal frequency of 20 MHz.

2. BANDPASS DELTA-SIGMA MODULATION

The $\Delta\Sigma$-modulator topology under study in this paper is a 1-bit tunable sixth-order $\Delta\Sigma$-modulator. The $\Delta\Sigma$-modulator quantises the output to two levels such that most of the quantisation noise power resides outside the signal band. After the $\Delta\Sigma$-modulator an analog band-pass filter removes the out of band quantization noise along with any out-of-band noise and distortion introduced by the one-bit D/A converter.

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The sixth-order noise transfer function (NTF) was designed for a maximum out-of-band gain of 1.7 (4.4 dB) with zeros optimized for minimum in-band noise at an over-sampling ratio of 64. The complete modulator, including word lengths and coefficients, is depicted in Fig. 1. The $\Delta\Sigma$-modulator was tuned to quarter the sampling frequency by adjusting $\cos(\theta_0)$ coefficient in Fig. 1. multiplier of the all-pass network. The $\Delta\Sigma$-modulator has been presented in more detail in [8].

3. BANDPASS PULSE WIDTH MODULATION

In its simplest form pulse width modulation only means that the value of the original digital sample is represented by the width of the (two-level) pulse in the pulse width modulated signal. When the pulse width modulated signal is to be generated digitally as in our case, it would, however, necessitate a sampling frequency difficult to attain with current technologies, in order to achieve desired signal to noise ratio.

The block diagram of the bandpass pulse width modulator used here is shown in Fig. 2. Digital quadrature modulation is employed to upconvert the baseband I and Q signals to a quarter of the clock frequency.

In order to decrease the clock frequency requirement, the time-resolution of the pulse widths must be decreased. And in order to do that without compromising the signal to noise ratio, noiseshaping is needed to move noise from the signal band to the outside of the signal band much the same way as happens with $\Delta\Sigma$-modulation. However, using a basic $\Delta\Sigma$-modulator as noiseshaper we would lose some of the phase information contained in the pulse edges in such a way that the loss causes harmonic distortion and makes it impossible to avoid a very high level f_c - f_1 image (where f_c is the center frequency and f_1 is the signal frequency) from appearing when the signal is upmixed using digital quadrature modulation. Therefore a more sophisticated method of noiseshaping is needed here. Fortunately this kind of method has been presented in prior art [9]. Here we use an integral noise shaping (INS) method presented in [10]. A block diagram of the integral noise shaper is shown in Fig. 3. In the figure N stands for the Nth stage and k_N are coefficients. We used a two-sided pulse width modulator where each side of the pulse is quantized separately with a 6-bit 4th-order noise-shaper.

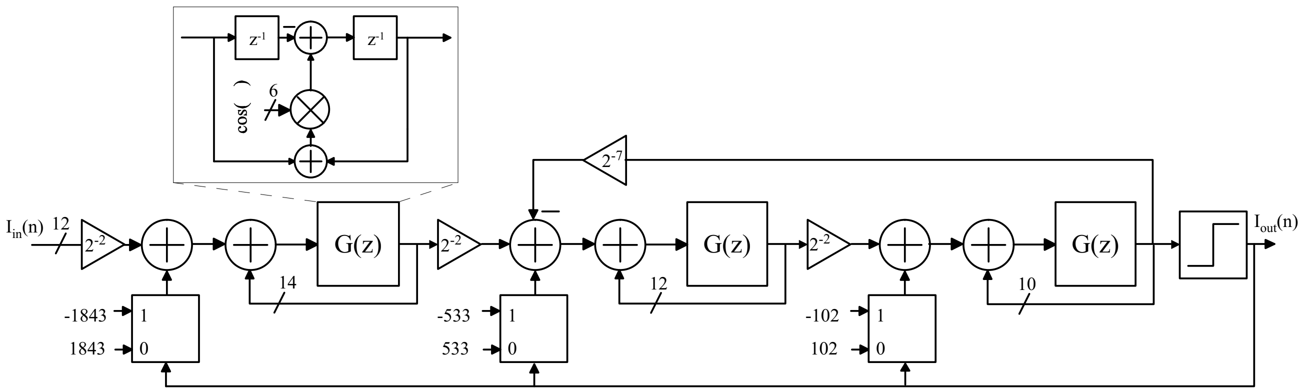

Figure 1. Tunable sixth order modulator

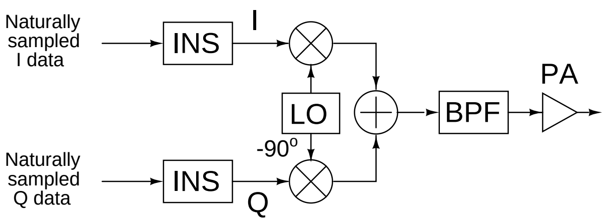

Figure 2. Bandpass pulse width modulation using digital quadrature modulation

4. COMPARISON OF BP-DSM AND BP-PWM

The pulse width modulation must have a quantizer of more than one bit in order to maintain its nature of PWM. A consequence of the use of a multibit quantizer is that the noise notch produced with a noiseshaper is the narrower the more bits the quantizer comprises and therefore it has lower capability of modulating wideband signals than $\Delta\Sigma$-modulation.

In contrast $\Delta\Sigma$-modulation does not necessarily need a more than one-bit quantizer, indeed, our design requires a one-bit quantizer since we use a Class-D power amplifier. However, unlike with PWM, using a multibit quantizer would deepen and widen the notch in the noise floor created by the $\Delta\Sigma$-modulation.

Since the losses in switching mode power amplifiers are (mostly) due to losses related to the switching, it is interesting to compare the switching activity of the two different types of modulators.

We simulated the switching activity with a sine signal of a length of 1 Megasamples such that the signal amplitude was sweeped from 0.19 through 0.63 times the maximum possible input amplitude for the $\Delta\Sigma$-modulator and the signal amplitude of the pulse width modulator was sweeped from 0.19 through 0.88 of the maximum possible input amplitude. These different signal levels were due to the fact that the PWM accepted higher input level still retaining stable operation than the $\Delta\Sigma$-modulator. At the level 0.63 the simulated switching activity of the PWM modulator was 24.9% and that of the the $\Delta\Sigma$-modulator was 24.7% expressed as number of rising transitions per number of samples. In all the simulated range the switching activity of the $\Delta\Sigma$-modulated signal varied between 24.49% and 25.19% and that of the PWM signal between 24.97% and 25.00%. Obviously the differences are not significant. The switching activity varies more with the signal frequency than with the modulation type.

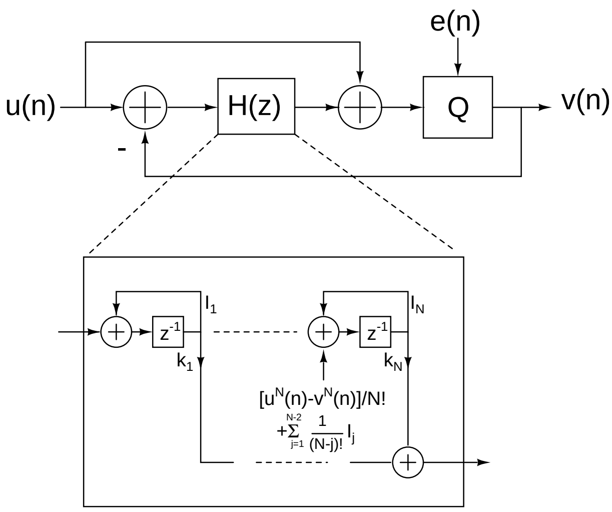

Figure 3. Integral noise shaping block diagram (INS in Fig. 2)

5. DESIGN OF THE CLASS-D POWER AMPLIFIER

A simplified schematic of the Class-D power amplifier is shown in Fig. 4. The power amplifier is composed of a push-pull amplifier i.e. an inverter and a bandpass filter (here an LC ladder).

The push-pull amplifier of the Class-D amplifier was integrated on a single chip using a 0.18 μm silicon CMOS technology. The switches were realised as inverters. Altogether five inverters were cascaded in order to to amplify the low level input signal and in order to decrease the capacitive load of the driving circuitry.

Based on ELDO simulations the widths of the PMOS devices were dimensioned three times the widths of the NMOS devices in order to compensate for differences in

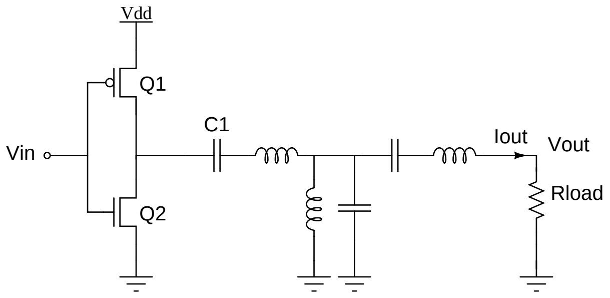

Figure 4. Voltage mode class-D power amplifier

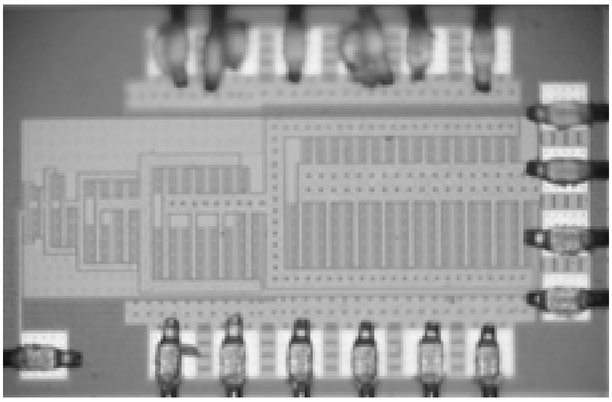

Figure 5. Microphotograph of the push-pull amplifier chip

the mobilities of the charge carriers in the PMOS and NMOS transistors. The lengths were selected equal. Each inverter stage was designed wider than the preceding stage approximately by a factor of e (i.e. base of natural logarithms), minimizing the total delay of the inverter chain.

The layout of the circuit featured six on-chip bonding pads, several stacked metal layers and wide metal wiring to distribute supply voltage efficiently. This is because the circuit draws large transient currents peaking 300 mA from the power supply during switching instants. The chip area is 1.6 mm^2. A microphotograph of the chip is shown is Fig. 5

6. MEASUREMENT RESULTS

The bandpass filter (in Fig. 4) was tuned to a centre frequency of 20 MHz with an insertion loss of 4 dB and 3 dB bandwidth of 3 MHz. Phicomp surface mount multilayer ceramic nickel barrier NP0 capacitors and Coilcraft ceramic core 0805HQ-27NXJBC RF inductors ($Q > 20$) were used. The load impedance in the measurements was 50 Ω.

With a bandpass $\Delta\Sigma$-modulated sine signal at 20 MHz the output power is 17 dBm or 50 mW and the power dissipation is 297 mW (90 mA from a supply of 3.3 V) yielding a drain efficiency of 16.8%. A measured power spectrum with the $\Delta\Sigma$-modulated signal is depicted in Fig. 6. With a bandpass PWM sine signal at 20 MHz the output power is 21 dBm or 126 mW and the power dissipation is 620 mW (188 mA from a supply of 3.3 V) yielding a drain efficiency of 20.3%. A measured power spectrum with the bandpass PWM signal is shown in Fig. 7. The sampling frequency in the measurements was 80 MHz. In both of the above measurements the input power level was maximised.

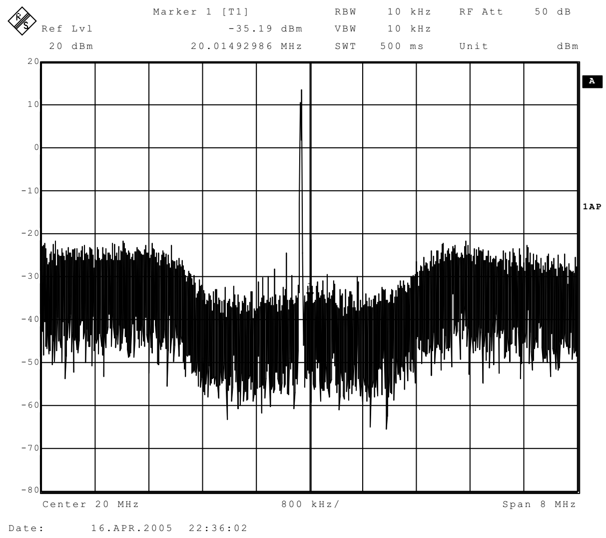

Figure 6. Measured inband spectrum from the Class-D amplifier driven with a bandpass $\Delta\Sigma$-modulated signal

6.1. Analysis of the measurement results

Whilst the measured efficiency is better in this case with a PWM input signal than a $\Delta\Sigma$-modulated input signal, it should be noted, however, that the purpose here is not to establish that using PWM to drive a Class-D power amplifier instead of $\Delta\Sigma$-modulation would result in higher efficiency in a general case.

Furthermore we see that the measured efficiencies of 16.8% and 20.3% fall significantly short of the ideal efficiency of 100% that is attained in simulations with ideal components. In order to explicate what causes the losses, we simulated the circuit with non-idealities using pulse width modulated input signal. The following non-idealities were accounted for: non-ideal transistors, parasitic capacitances on the integrated circuit, inductance in the voltage supply, pads and bonding wires and non-idealities of the bandpass filter such as series resistance and parallel capacitance in an inductor and series inductance of a capacitor. With all the non-idealities accounted for, the simulated efficiency was 25.14%.

With all the non-idealities accounted for, except the parasitic capacitances on the integrated push-pull amplifier, the simulated efficiency was 25.32%

With all the non-idealities accounted for, except for the realistic models for the pads and bonding wires of the power amplifier chip, used in the simulation with all the non-idealities, the simulated efficiency was 25.13%.

With all the non-idealities accounted for, except the inductance of the supply voltage the efficiency was 25.40%

In the simulations above we used as realistic models

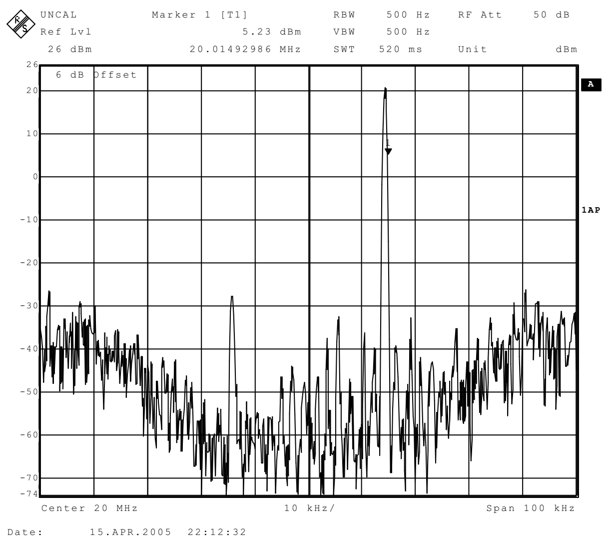

Figure 7. Measured inband spectrum from the Class-D amplifier driven with a BP-PWM signal

for the inductors and capacitors of band-pass filter as were available. The most important non-idealities were the equivalent series resistance of the capacitors and the inductors which were 0.1 Ω and 0.2 Ω respectively for the capacitors and inductors. Simulating the circuit with an ideal bandpass filter but with the all rest of the non-idealities considered, the efficiency was 64.56%. The above simulations indicate that the efficiency is dominated by the losses in the band pass filter.

Whilst the bandpass filter dominates the efficiency it is far from the sole constituent of the infraideal efficiency attained. The secondary source of power loss are the non-idealities within the integrated transistors. In a simulation with all the non-idealities accounted for, the transistor models used were the BSIM3V3 models provided by the process vendor. The aggregate power dissipation within the transistors was 24.36% of the power lost.

The above analysis indicates that the primary source of loss of efficiency are the series resistances of the inductors and capacitors of the bandpass filter and the secondary source of loss of efficiency are the non-idealities within the integrated transistors. The rest of the non-idealities considered in this analysis had only a minor effect on efficiency.

7. CONCLUSIONS

We presented a Class-D amplifier that is driven by bandpass PWM and bandpass $\Delta\Sigma$-modulated signal. The Class-D amplifier comprises an integrated CMOS push-pull amplifier chip and an LC bandpass filter. The efficiencies achieved using these two different input signals were compared experimentally in measurements and the results were 16.8% and 20.3% for the $\Delta\Sigma$-modulated signal and the PWM signal respectively. According to the simulations the infraideal efficiencies are primarily due to the losses in the bandpass filter and secondarily due to the losses within the integrated transistors.

8. REFERENCES

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