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# Free-standing SU-8 microfluidic chips by adhesive bonding and release etching

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## Abstract

Free-standing SU-8 chips with enclosed microchannels and high density of fluidic inlets have been made in a three-layer process which involves SU-8 to SU-8 adhesive bonding and sacrificial etching. With this process we can fabricate microchannels with depths ranging from 10 to 500  $\mu\text{m}$ , channel widths from 10 to 2000  $\mu\text{m}$  and lengths up to 6 cm. The process is optimized with respect to SU-8 glass transition temperature. Thermal stresses and thickness non-uniformities of SU-8 are compensated by novel mask design features, the auxiliary moats. With these process innovations filling of microchannels can be prevented, non-bonded area is minimized and bonding yields are 90% for large-area microfluidic chips. We have released up to 100 mm in diameter sized microfluidic chips completely from carrier wafers. These free-standing SU-8 chips are mechanically strong and show consistent wetting and capillary filling with aqueous fluids. Fluidic inlets were made in SU-8 chips by adding one lithography step, eliminating through-wafer etching or drilling. In our process the inlet size and density is limited by lithography only.

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*Keywords:* SU-8; Microchannel; Microfluidics; Adhesive bonding; Wafer bonding

## 1. Introduction

Microchannels are simple yet essential elements in microfluidic systems. Only in few cases are open, linear channels useful; most often embedded (enclosed) channels with crossings or other more complex geometries are required, and it is usually in those more complex geometries that bonding processes tend to fail. Typical cross-sectional dimensions for microfluidic channels around 50  $\mu\text{m}$  do not pose great fabrication problems; it is the length, which can be over 5 cm for viscosimeters or capillary electrophoresis chips that requires attention.

Fluidic channels have been made in silicon, glass and various polymers. However, many of the unit operations require high voltage, which excludes silicon. Glass microfabrication is generally more cumbersome than polymer processing: wet

etching results in isotropic profile, DRIE is slow and limited in depth, and through-wafer structures are difficult to realize. Bonding of silicon and glass is well established but requires rather high temperature and voltage (300–500 °C, 300–500 V). SU-8 epoxy polymer enables low temperature bonding and high voltage operation. In this work SU-8 channels have been made on top of silicon and glass wafers, and we also demonstrate a release process that results in free-standing SU-8 microfluidic chips, without any supporting wafer.

SU-8 is multifunctional epoxy-based negative photoresist. Its high aspect ratio patterning has been described in many articles [1–4]. Its properties enable fabrication of microchannels with practically any desired dimensions. However, the channel shape is limited to channels with rectangular cross-section and enclosed channels with widely different cross-sectional dimensions are difficult to fabricate. Major drawbacks of SU-8 include difficult removal after curing and its high coefficient of thermal expansion (CTE) compared

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to standard substrate materials. CTE of SU-8 is 52 ppm/°C [5] whereas silicon and glass have values around 3 ppm/°C. This difference causes relatively high stresses to the structures.

In microfluidics SU-8 has been mostly applied as a master for fabrication of microfluidic chips in PDMS [6] even though SU-8 itself is highly suitable for microfluidics because of its good chemical and thermal resistance. Various SU-8 microchannel fabrication processes have been proposed, including direct patterning and lamination [7–12].

Adhesive bonding of SU-8 channels has been done by applying commercially available adhesives [13–15] but in Ref. [16] SU-8 structures were sandwiched between silicon and glass wafers using SU-8 itself as an adhesive. Partially soft baked bonding layer was brought into contact with a patterned wafer. The bonding temperature was 75 °C. After contact between wafers was made, the bonding layer was exposed with UV and the wafer stack was cured on a hot-plate to finish the bonding. In this method the adhesive SU-8 layer was 50 µm thick. In the same article another approach was also presented: channels were patterned after bonding by exposing through the glass wafer. After post exposure bake channels were developed between bonded wafers from the inlets of the microfluidic chip.

Later work has resulted in various modifications of the basic idea outlined in Ref. [16]. In one approach bonding was done by spinning SU-8 on a flexible substrate. Better yield was reported without specific processing conditions or results [15]. In another modification bonding was done below the glass transition temperature, assisted by pressure [17]. Thin layers of SU-8 have also been applied as bonding layers [18,19]. For example in reference [18] a 5 µm of SU-8 was used as an adhesive layer. Bonding of SU-8 without UV-initiation has also been described [20]. Bonding was done in vacuum in a commercial bonder with bonding force of 100 N at a temperature of 90 °C.

Enclosed channels have been reported in the literature but most papers describe fairly simple test structures or limited range of channel dimensions. Our paper explores a much wider range of channel dimensions (both height, width and length), larger variety of channel geometries (crossings, reservoirs and auxiliary structures) and presents solutions to SU-8 channel enclosure. We present results of high-yielding full-wafer bonding in a simple experimental set-up.

In many microfluidic applications identical channel wall properties are emphasized to ensure uniform wetting or surface charging. In this paper we describe a three-layer process where bottom, ceiling and walls are all made of SU-8. We also show how self-supporting all-SU-8 microfluidic chips can be made by sacrificial etching of the carrier wafer. This method enables very high density of fluidic inlets without drilling or through-wafer etching. The released SU-8 microchips successfully passed microfluidic tests with aqueous solutions.

## 2. Methods

Both silicon and glass wafers were used as substrates. Pyrex 7740 glass wafers were from Corning and standard single side polished silicon wafers were from Okmetic. Wafers were 100 mm in diameter and all results reported in this work are for full wafer bonding. SU-8 10, SU-8 50 and SU-8 100 from Microchem Corporation were employed depending on the thickness requirements. SU-8 was used both as a structural material for the channels and also as the adhesive bonding material. Bonding was done in class 10 cleanroom to avoid particle contamination. Process flow for the bonding procedure is shown in Fig. 1.

The bonding process has been described in more detail in Ref. [21] and only a brief outline is given here. Wafer cleaning before bonding was as follows: silicon and glass wafers were given a short hydrofluoric acid (Sioetch 17/02 from Merck) dip (30 s) and DI-water rinse before application of SU-8. Reason for this step was to refresh surface of silicon and Pyrex wafers to improve adhesion of SU-8. After dehydration bake SU-8 was spinned and soft baked on a hot plate in a two-step baking process.

Exposure was done in LOMO EM-5006 mask aligner with doses between 800 and 1500 mJ/cm<sup>2</sup> measured at wavelength of 365 nm. Post exposure bake was done at 95 °C on a hot plate followed by slow cooling back to room temperature. Development was done using propylene glycol methyl ether acetate (PGMEA) in mechanically agitated immersion tank.

Bonding layer of SU-8 was applied on a glass wafer after wafer preparation steps. Adhesive SU-8 layer thickness was varied in our experiments between 50 and 100 µm. Baking times, bonding temperature and exposure of this layer were explored to optimize the bonding process. Bonding was done without dedicated equipment: pressure was applied manually to achieve contact between wafers that were on hot plate. Adhesive SU-8 layer was exposed through the glass wafer and post exposure bake was done to finish bonding by cross-linking across the structural and adhesive SU-8 layers.

Release of three-layer SU-8 chips necessitates sacrifice of the glass wafer, but the silicon wafer can be reused. For the SU-8 removal silicon wafers were thermally oxidized (thickness varied between 100 and 900 nm) before application of first SU-8. HF etch (50%) removed both the glass wafer and the thermal oxide beneath the base SU-8 layer, and SU-8 structure was released. If structures were done between two Pyrex wafers, both of them were sacrificially etched.

## 3. Results and discussion

### 3.1. Optimized bonding process

Bonding with SU-8 after patterning is a tradeoff between two main problems: void formation and filling of the channels by the adhesive SU-8. Temperature during bonding should be low to avoid filling of the channels by the flow of adhesive

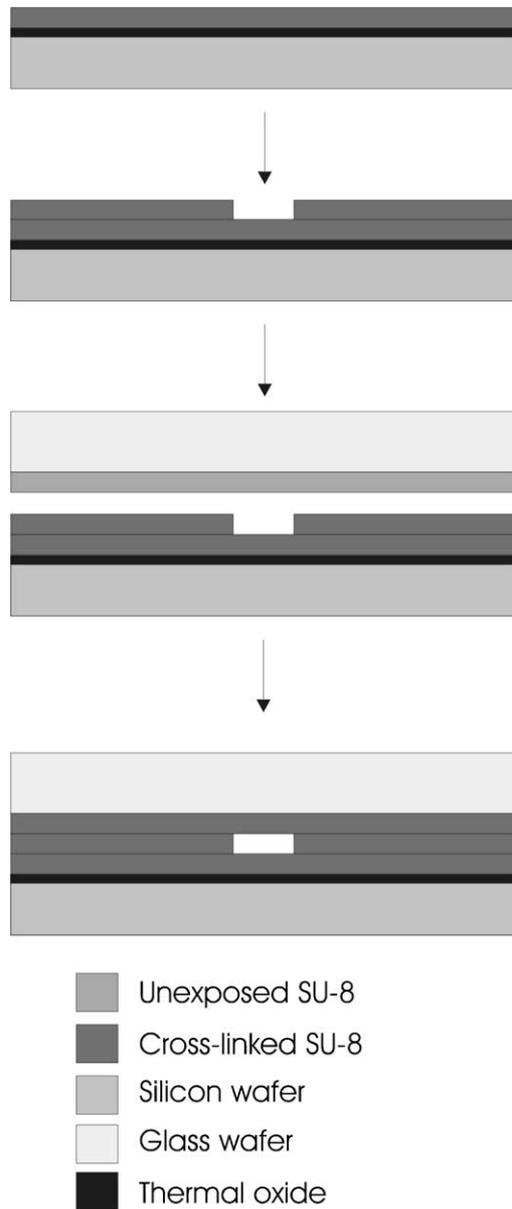


Fig. 1. The process flow for fabrication of closed microchannels. First layer of SU-8 was flood exposed and baked on top of silicon (or glass) wafer (optional thermal oxide layer is used when released SU-8 structures are made). Second layer of SU-8 was exposed and developed. Third layer of SU-8 (bonding layer) was applied on a glass wafer. After partial soft bake wafers were pressed together. Bonding layer was exposed through the glass wafer and bonding was finalized by cross-linking during post exposure bake.

layer SU-8. However, by lowering the bonding temperature, bonding quality suffers and voided area increases significantly. Glass transition temperature of SU-8 (measured as 64 °C in Ref. [22]) is an important parameter because viscosity changes rapidly around this temperature. Blocking of the channels and non-bonded area are defined by the viscosity.

In our experiments we found the bonding temperature of 68 °C to be a good compromise for complete bonding of the wafer with minimized channel filling. Voided area was less than 5% in all our experiments. In the bonding procedure sam-

ples were soft baked on a hot plate keeping the temperature at 65 °C for 15 min to planarize the spun film. Temperature was then ramped up to 95 °C and kept there for 10 min. Wafer was cooled back to 68 °C and wafers were pressed together. After contact was achieved over the whole wafer, adhesive SU-8 layer was exposed through the glass wafer with a dose of 1000 mJ/cm<sup>2</sup>. Post exposure bake of 5 min to ramp the temperature to 95 °C and holding there for 5 min to finish the bonding by cross-linking of SU-8. Both wafers should be heated to the same temperature. This has been found to be essential to avoid deformations in high aspect ratio structures [21].

Pressure can be used to improve bonding. Pressure was applied to the wafers from one edge and continued over whole wafer to eliminate air bubbles (pressure can be applied for example with tweezers). No additional pressure was applied after contact was achieved unlike in Ref. [17]. Neither is an expensive vacuum bonding system [23] needed. Application of pressure by tweezers eliminates non-bonded areas effectively. Reproducibility of pressure application by tweezers has been good in our experiments, if other processing conditions like temperature were under control. However, this simple bonding arrangement leads to poor alignment accuracy compared with commercial vacuum bonding system. This was not a problem in our application because the second wafer was always non-patterned and therefore alignment was non-critical.

Slow cooling ramp of 1 °C/min was required after post exposure bake. In fabrication of three-layer and thick two-layer structures slow cooling is especially important to reduce thermal mismatch stresses in the layers. Cross-sections of two successfully bonded channels are shown in Fig. 2. In Fig. 2(a) a two-layer channel with silicon on the bottom and in Fig. 2(b) a three-layer SU-8 channel are shown.

At 68 °C blocking of channels with height less than 100 μm still remains a problem [21]. Channels are filled during bonding because of thickness non-uniformities of SU-8 layers. When wafers are pressed into contact, any additional SU-8 flows and fills channels. Capillary forces increase this effect. Thickness non-uniformities can be caused, for example, by edge beads, by bubbles after spinning or by soft baking under non-ideal conditions on a hot plate. Extended soft bake above glass transition temperature and moving of the wafer on hot plate planarize SU-8 layers to some extent. However, some thickness non-uniformities remain in layers and they degrade bonding quality. To equalize channel filling, auxiliary moats are required in mask design in addition to optimized bonding process. These are described in Section 3.3.

Bonding at temperatures below 60 °C necessitates pressure to achieve contact. Removal of pressure leads to partial detachment of the wafers because hardened SU-8 does not flow compensating thickness non-uniformities. Bonding also failed if the top wafer was held at 95 °C too long time during soft bake. The amount of solvent should be minimized during soft bake because the remaining solvent reduces cross-linking density and consequently bond strength. Solvent also

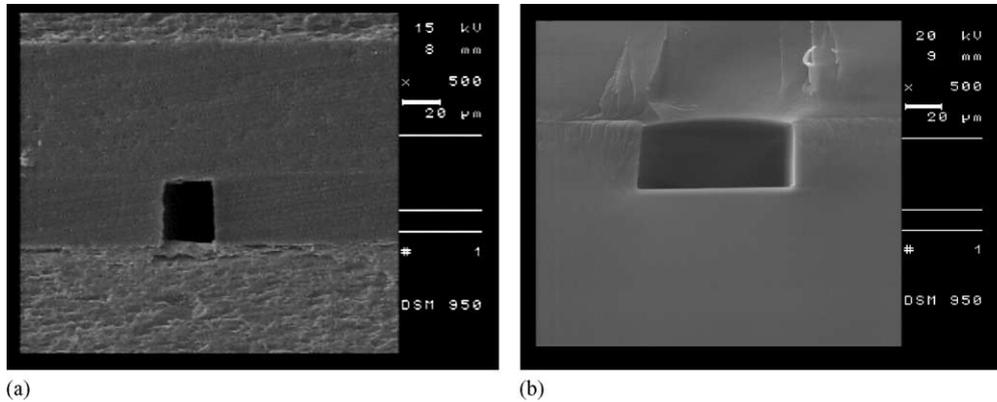


Fig. 2. Bonding after channel formation: (a) two-layer SU-8 channel with silicon on the bottom; (b) three-layer SU-8 channel with SU-8 floor, walls and ceiling.

reduces the viscosity of the adhesive SU-8 layer leading to more pronounced filling of the channels. Furthermore, solvent can later outgas, degrading bonding quality. This was clearly seen when blanket wafers were bonded together.

### 3.2. Comparison to previously published results

In Ref. [16] bonding was done at 75 °C. There was no information about unintended filling of the channels. Neither was void area discussed. No exact values were given for structural layer dimensions studied, but those ranged from 50 μm to few hundreds of micrometers. Bonding of patterned layers was reported to be difficult for feature sizes larger than a few hundred of micrometers. Length of non-blocked channels was not reported.

Pressure-assisted bonding below glass transition temperature of SU-8 has been reported to yield good bonding results [17]. Bonding was done at 48 °C. Channel blocking flow of SU-8 was avoided because of high viscosity of the bonding layer below the glass transition temperature. Therefore, small channels can be sealed with this technique. This method seems suitable for fabrication of laterally small microfluidic devices because of good control of channel filling. Amount of void area was reported to be in the range of 30% having relatively large air escape paths on the wafer. Because of large void area and because of required air escape paths this method is not suitable for fabrication of long separation channels.

The same argument holds for the method where cured SU-8 layers are bonded with commercially available bonder [20]. Only small area bonding was reported. These methods require high pressures or vacuum and therefore also spe-

cial equipment. Our method works with standard cleanroom equipment: only UV-light source and a hot plate are needed. Those are required for all SU-8 processing.

Blocking problem has been reported in the literature also for 5 μm thick adhesive layer and 90 μm high channels [18]. Soft bake was done after the wafers were pressed to contact. Remaining solvent reduces dramatically viscosity of SU-8 and because of this capillary forces can easily draw SU-8 into the channels. If soft bake is done after enclosure, remaining solvent cannot escape because of coverlid and it will probably form bubbles later on at the bonding interface, leading to reduced bonded area. Voided area was not reported in Ref. [18]. Our bonding parameters and results are compared with published results in Table 1. Channel length has not been discussed in previous articles. In our studies we found it to be limiting factor in fabrication of enclosed microfluidic devices. When we tried to reproduce published results, we found that yield of large area devices (e.g. separation channels) can be essentially zero although small area bonding results are good.

### 3.3. Improved mask designs for bonding

In our experiments bonding temperatures above 70 °C resulted in SU-8 flow and complete channel blocking, in accordance with Ref. [17]. We have found that blocking is especially problematic at channel inlets and outlets as well as in places with more complicated geometries like channel crossings.

We have solved the filling problem by application of auxiliary structures. Schematic designs of our auxiliary structures, walls and moats, are shown in Fig. 3. Walls around

Table 1  
Comparison of bonding parameters and results between our studies and other references

Reference	Bonding temperature (°C)	Adhesive thickness (μm)	Channel height (μm)	Channel width (μm)	Channel length	Void fraction
16	75	50	Typically 50–75	NM	NM	NM
17	48	10–50	10	3.6–NM	NM	30%
18	“Soft bake”	5	90	≈100	NM	NM
This work	68	50–100	10–500	10–2000	6 cm	<5%

NM: not mentioned

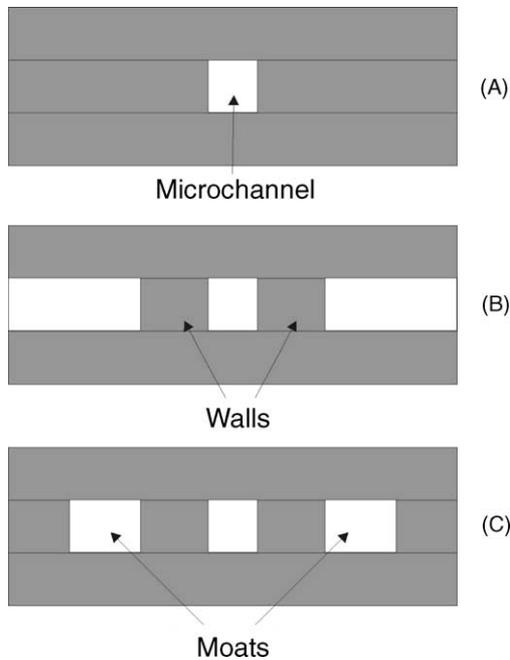


Fig. 3. Cross-sectional views of microchannels: (A) standard channel; (B) channel with walls; (C) channel with moats.

microchannels dramatically reduced filling of the main channels. Problems remain, however, because walls intrude easily into the adhesive SU-8 layer and channel shapes are deformed. Structures surrounded by walls are also mechanically weaker than structures with large area SU-8 around them. This becomes critical for self-supporting SU-8 chips (described in Section 3.4). Because of larger bonding area in moat design, as compared to wall design, moats turned out to be mechanically stronger. These structures can be released completely from the substrates and handled without deformation.

Auxiliary moats clearly improve bonding results. In Fig. 4 the standard channel and moat design channel are shown in top view optical micrograph. Any superfluous adhesive will fill the moats, but the main channels retain their shapes. In

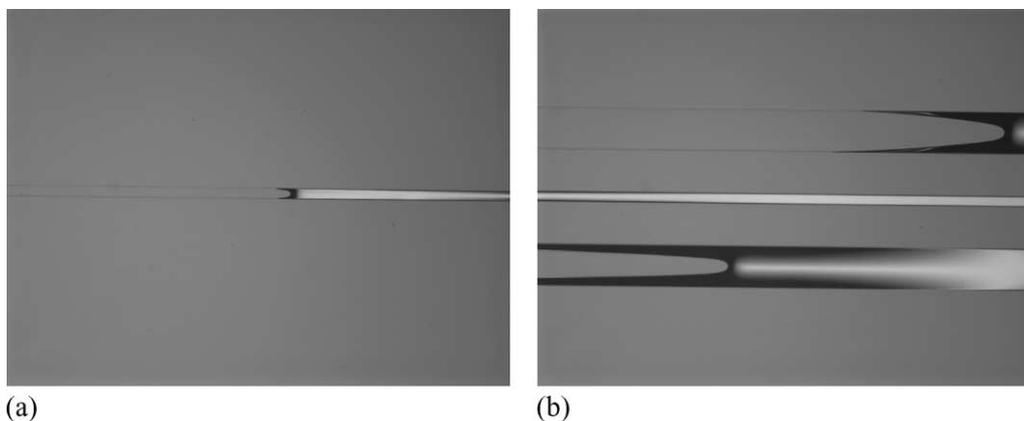


Fig. 4. Top view micrographs of the channels: (a) channel without auxiliary structures is filled with SU-8 during bonding process. (b) With the help of auxiliary structures, channels remained open. Two auxiliary moats were filled with SU-8 but the main channel in the middle was open in the whole length.

Fig. 5 cross-sectional SEM micrographs are shown. Pictures are from the same wafer to ensure identical bonding conditions. If there are thickness irregularities in the adhesive SU-8 layer, moats balance the situation. An arch shaped channel cross-section can form in the case of incomplete filling, as shown for moats in Fig. 5(b). The main channel shape is as designed.

We have found moat width of  $200\ \mu\text{m}$  to be suitable for a wide range of main channel dimensions and SU-8 thicknesses. Distance between moats and the main channel was also  $200\ \mu\text{m}$ . These values resulted in good shape control and mechanical stability. If there are thickness non-uniformities, they do not show up in channel shape. Our bonding method is suitable for enclosing various lateral shapes like large reservoirs. Large area structures also retain their designed shape after bonding.

The effect of auxiliary structures was most clearly seen in channels with heights less than  $100\ \mu\text{m}$ . Channels of these dimensions are usually easily blocked by capillary forces. High stresses enhance channel filling and therefore the beneficial effects of moats were most pronounced with three-layer structures. By improved mask design we have achieved 90% yield for 5 cm long microchannels with cross-sectional dimensions of  $50\ \mu\text{m} \times 50\ \mu\text{m}$ . Without auxiliary structures yield was 10% with identical process.

Large uniform areas of thick SU-8 create high stresses to the wafers. This is caused by difference in thermal expansion coefficient between SU-8 and the substrate. We have divided areas around moats into smaller areas with lines that allow small movement of the SU-8 structures. These stress compensation lines are shown in Fig. 6. The lines are simple and sufficient for the stress compensation on our wafers. Some stress compensation structures have been described in the literature for SU-8 [24,25]. These have been used to improve resistance against cracking, whereas our stress compensation structures are designed to improve bonding.

With methods described above structural layers with thickness between 10 and  $500\ \mu\text{m}$  were successfully bonded. Channels were completely enclosed and channels retained

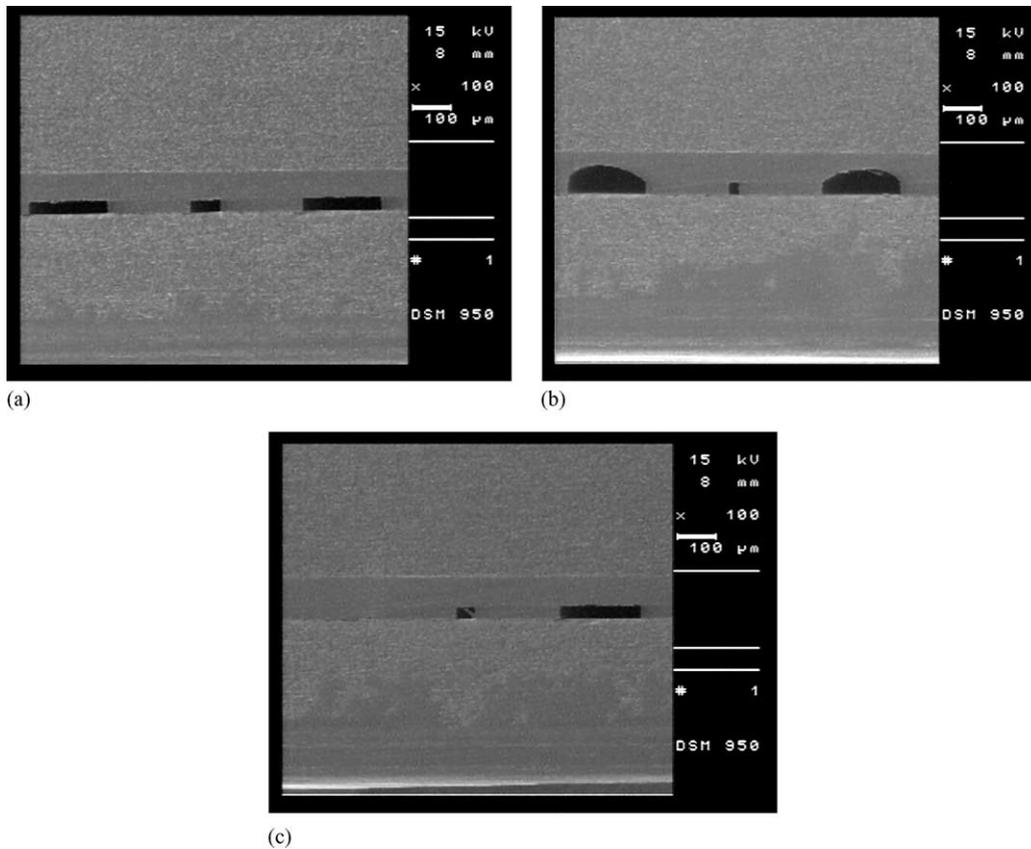


Fig. 5. Cross-sectional SEM images of the channels with moat structures around channels. (a) In most cases both moats and channel are in good condition. If there is in the bonding layer less SU-8 than in the surroundings, moats are bent upward to bonding layer forming arches (b). If there is more SU-8 in the bonding layer than in the surroundings moats are filled with SU-8, but channel remains open. (c) Cross-sectional SEM picture, where another one of the moats is filled. Situations in (b) and (c) are due to non-flatness of SU-8 layers, which is balanced by redistribution of SU-8 during bonding.

their shape over whole 6 cm distance. This limit was only from our mask designs. Longer channels would have been possible with this bonding method. Channels down to 10  $\mu\text{m}$  height can be done by patterning the channels directly on top of Pyrex or silicon wafers with two SU-8 layers (without flood-exposed base SU-8). In the case of three-layer SU-

8 structures channels down to 40  $\mu\text{m}$  in height were fabricated. This limit comes from wafer bowing that result from increased stress in the multilayer system.

#### 3.4. Released SU-8 chips

SU-8 structures were released by sacrificial etching of Pyrex wafer(s) and/or thermal oxide in hydrofluoric acid. Thermal oxide was etched between SU-8 and silicon. During the first 2 h underetching was properly initiated and Pyrex wafer was etched completely away from the top. After 2 h etching the wafers were rinsed quickly in DI-water and dried from top and bottom. In this quick wash, HF remained between the SU-8 and silicon, and lateral etching of the oxide was continued for some hours in dry plastic container. Capillary forces kept the etching proceeding. Etch rate depends on the stress at the SU-8/silicon dioxide interface. Higher stress causes faster etching. In highly stressed wafers 2 h underetching was enough for complete detachment of the full wafer structure, but in some cases etching took 12 h. After releasing, SU-8 structure was rinsed carefully in DI-water.

The released three-layer SU-8 stacks were slightly curved because the thermal mismatch stresses, built in during fabrication. Those cannot be completely relaxed in highly cross-

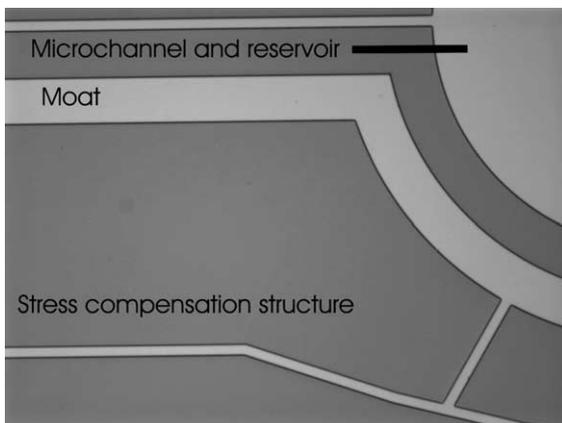


Fig. 6. Channel surrounded by moat. Large SU-8 areas are divided into smaller segments by stress compensation lines. Microfluidic channels 50  $\mu\text{m}$ ; moats 200  $\mu\text{m}$ , reservoir 2000  $\mu\text{m}$  in width.

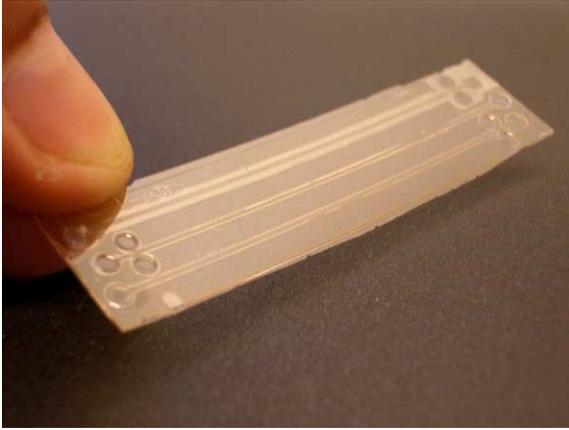


Fig. 7. Released three-layer SU-8 stack with 6 cm long enclosed channels. After releasing chip is cut with scissors to its shape.

linked SU-8. Released SU-8 structure is shown in Fig. 7. If perfectly planar channels are required, the released structure should be pressed against a planar surface or glued to some suitable substrate. However, handling and using of released SU-8 stacks as microfluidic channels was possible without difficulties. SU-8 is mechanically strong but fragile material and therefore full-wafer sized stacks with minimum thickness of  $300\ \mu\text{m}$  were released. Released SU-8 chips can be diced by cutting with a knife or with scissors.

### 3.5. Fluidic inlets in SU-8

Drilling of inlet holes in glass wafers is a difficult task because of glass fragility. Alignment of drilled inlets can also be problematic. In silicon, inlets can be done by wet or dry etching through the wafer more easily, but not completely without problems, either due to shape limitations in wet etching, or low rate in DRIE. Because of this, it is desirable to have the inlets patterned into SU-8. SU-8 inlets can be very close to each other. Shape and alignment of the inlets are accurately defined by lithography and the fabrication process is straightforward. Enclosed microchannels with 2 mm sized fluidic inlets are shown in Fig. 8.

In our approach fluidic inlets are made in the base SU-8 layer. This adds one photomask to the process, but considering the difficulties in other fluidic inlet fabrication methods, this seems to be a reasonable trade-off. The density of fluidic ports is limited by lithographic resolution only. The inlets have to be done as a first step because development of the released SU-8 channel stack is not possible. This is because cross-linking of the SU-8 is cationic polymerization reaction and it is initiated by protons. In strong acid solution the concentration of protons is high compared with normal UV initiated cross-linking. High proton concentration can cross-link the material even in room temperature. This makes the development of the structures exposed to HF impossible.

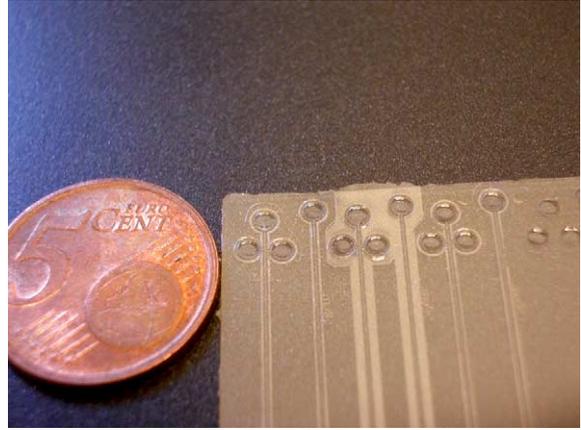


Fig. 8. Closely spaced fluidic inlets in free-standing three-layer SU-8 microchip. Size of the inlets is 2 mm in diameter.

### 3.6. Fluidic tests

Fluidic tests of free-standing SU-8 chips were made with various aqueous solutions: DI-water, tap water, milk and NaCl salt solutions of different concentrations. Liquid was dispensed by pipette into a 2 mm diameter reservoir, and capillary filling of microchannels was observed visually by microscope. We report preliminary fluidic test results with 5 cm long straight channels.

Initial tests showed that salt particles in highly concentrated salt solutions blocked small ( $50\ \mu\text{m} \times 50\ \mu\text{m}$  or smaller) channels easily and therefore made reuse of channels impossible. DI- and tap water were easily pumped away from channels. For salt solutions with salt concentrations less than 16% even the small channels were reusable many times. Milk was difficult to remove from the channels. These channels were not reused.

We also tested open channels made in the two-layer process with SU-8 bottom and walls, without roof. Filling was very erratic. PDMS roof was then attached to cover the open channels. This improved channel filling but did not lead to reproducible results. Enclosed all-SU-8 channels made in our three-layer process, however, exhibited proper wetting and capillary filling, and the channels were consistently filled. The problems in open and PDMS sealed channels were probably due to particle contamination because PDMS covers and fluidic tests were done outside the cleanroom. Three-layer SU-8 chips were enclosed in class 10 cleanroom and therefore particle contamination was avoided. However, fluidic tests were done with the same setup outside cleanroom. Another reason for failure with PDMS cover could be due more hydrophobic nature of PDMS. These aspects of fluidic tests are going to be investigated in the future.

Fluidic test yield of 5 cm long channels was excellent, with erratic chips at wafer periphery only, probably due to SU-8 thickness variation at wafer edges. Fluidic tests point out the importance of having all surfaces of microfluidic channels to be made of the same material.

#### 4. Conclusions

SU-8 has excellent properties for microfluidic applications: it is thermally and chemically stable and mechanically strong enough for self-supporting large area chips. Bonding for channel enclosure can be achieved by avoiding high stresses. This can be accomplished by selection of suitable temperature slightly above SU-8 glass transition temperature, by controlled temperature ramp rates, and aided by auxiliary structures. Microchannels up to 6 cm long with heights between 10 and 500  $\mu\text{m}$  were fabricated successfully. The bonding method we have described here is suitable for enclosing structures with various lateral dimensions on the same wafer with non-bonded area less than 5% in wafer scale.

Three-layer SU-8 chips can be removed from the substrates and those were used as stand-alone microfluidic chips. The simplicity of fluidic inlet fabrication in fully SU-8 chips makes this fabrication scheme very attractive. However, it is essential to fabricate the fluidic inlets in the first SU-8 layer because SU-8 would be polymerized in acidic solutions, and therefore the SU-8 structures must be finished before the release etch process. By application of auxiliary structures described in this article, yield of large area chips was 90%; compared with 10% yield without them, using otherwise identical bonding process. Fluidic tests show promise of reproducible filling and reusability of long microchannel chips.

#### References

- [1] J. Shaw, J. Gelorme, N. LaBianca, W. Conley, S. Holmes, *IBM J. Res. Dev.* 41 (1997) 81–94.
- [2] K. Lee, N. LaBianca, S. Rishton, S. Zohlgharnain, J. Gelorme, J. Shaw, H.-P. Chang, *J. Vac. Sci. Technol. B* 13 (1995) 3012–3016.
- [3] H. Lorenz, M. Despont, P. Vettiger, P. Renaud, *Microsyst. Technol.* 4 (1998) 143–146.
- [4] P. Dentinger, K. Krafcik, K. Simison, R. Janek, J. Hachman, *Microelectron. Eng.* 61/62 (2002) 1001–1007.
- [5] H. Lorenz, M. Laudon, P. Renaud, *Microelectron. Eng.* 41/42 (1998) 371–374.
- [6] D. Duffy, C. McDonald, O. Schueller, G. Whitesides, *Anal. Chem.* 70 (1998) 4974–4984.
- [7] L. Guerin, M. Bossel, M. Demierre, S. Calmes, P. Renaud, *Proceedings of the Transducers'97*, 1997, pp. 1419–1422.
- [8] B. Alderman, C. Mann, D. Steenson, J. Chamberlain, *J. Micromech. Microeng.* 11 (2001) 703–705.
- [9] M. Heuschkel, L. Guérin, B. Buisson, D. Bertrand, P. Renaud, *Sens. Actuat. B* 48 (1998) 356–361.

- [10] P. Renaud, H. van Lintel, M. Heuschkel, L. Guerin, *Proceedings of the  $\mu\text{TAS}$  1998 Symposium*, 1998, pp. 17–22.
- [11] F. Tay, J. van Kan, F. Watt, W. Choong, *J. Micromech. Microeng.* 11 (2001) 27–32.
- [12] F. Tseng, Y. Chuang, W. Lin, *Technical Digest of the 15th IEEE International Conference on Micro Electro Mechanical Structures*, 2002, pp. 69–72.
- [13] E. L'Hostis, P. Michael, G. Fiaccabrino, D. Strike, N. Rooij, M. Koudelka-Hep, *Sens. Actuat. B* 64 (2000) 156–162.
- [14] H. Ayliffe, A. Frazier, R. Rabbit, *J. Microelectromech. Syst.* 8 (1999) 50–57.
- [15] C.-H. Lin, G.-B. Lee, B.-W. Chang, G.-L. Chang, *J. Micromech. Microeng.* 12 (2002) 590–597.
- [16] R. Jackman, T. Floyd, R. Ghodssi, M. Schmidt, K. Jensen, *J. Micromech. Microeng.* 11 (2001) 263–269.
- [17] S. Li, C. Freidhoff, R. Young, R. Ghodssi, *J. Micromech. Microeng.* 13 (2003) 732–738.
- [18] K. Mogensen, J. El-Ali, A. Wolf, J. Kutter, *Appl. Opt.* 42 (2003) 4072–4079.
- [19] L. Cui, T. Zhang, H. Morgan, *J. Micromech. Microeng.* 12 (2002) 7–12.
- [20] C.-T. Pan, H. Yang, S.-C. Shen, M.-C. Chou, H.-P. Chou, *J. Micromech. Microeng.* 12 (2002) 611–615.
- [21] S. Tuomikoski, S. Franssila, *Phys. Scripta T114* (2004) 223–226.
- [22] K. Pfeifer, M. Fink, G. Gruetzner, G. Bleidiessel, H. Schulz, H. Scheer, *Microelectron. Eng.* 57/58 (2001) 381–387.
- [23] F. Niklaus, P. Enoksson, E. Kälvesten, G. Stemme, *J. Micromech. Microeng.* 11 (2001) 100–107.
- [24] H.-K. Chang, Y.-K. Kim, *Sens. Actuat. A* 84 (2000) 342–350.
- [25] V. Seidemann, J. Rabe, M. Feldmann, S. Bütgenbach, *Microsyst. Technol.* 8 (2002) 348–350.

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