PAPER F

# Low-temperature Bonding of Thick-film Polysilicon for MEMS

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# Low-temperature bonding of thick-film polysilicon for MEMS

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## Abstract

Polysilicon thick films have been found to be an irreplaceable option in various sensors and other microelectromechanical system (MEMS)-designs. Polysilicon is also a prospective option for replacing single-crystal silicon in customized silicon-on-insulator-substrates. Due to the nature of polysilicon, bonding for MEMS-purposes has so far concentrated on anodic bonding, which has drawbacks for instance in terms of process duration and thermal load. The objective of this work is to develop low-temperature direct bonding for various polysilicon films. Polysilicon films were grown at varying temperatures and pressures with and without boron doping. The films were polished by chemical-mechanical polishing and cleaned. Surface qualities were studied by atomic-force-microscope before bonding. Wafers were then activated with argon plasma and bonded to oxidized silicon, quartz and glass. Bonding quality was evaluated with scanning-acoustic-microscope, the crack-opening-method and HF-etching. Scanning-electron-microscopy was used to investigate film and interface quality. This development has led to a new kind of polishing process, where several microns of polysilicon are removed still leaving surface direct bondable. This is accomplished by a dedicated and effectively planarizing polishing process. Spontaneous bonding took place and good bonding quality was achieved after annealing at 200°C.

# Introduction

Low-temperature (LT-) direct wafer bonding is known as a potential technology for fabricating silicon-on-insulator (SOI) structures for advanced microsystems and optical devices. It has not, however, been extensively used for wafer-scale-packaging so far, despite of its inherent advantages. As a capping wafer for a silicon-based wafer the thermal match is, of course, ideal over a wide temperature range. The seal is hermetic and outgassing minimal. Alkaline ions, being essential constituents in anodically bondable glasses, are totally avoided [1]. The high applied voltage during bonding which may cause deleterious electrostatic force for devices is not used. The bonding temperature as low as 200°C in direct bonding allows encapsulation of temperature-sensitive devices or use of capping wafers with imperfect thermal match. Furthermore, the process time is shorter than in anodic bonding. The need to encapsulate in high vacuum is common in RF-microelectromechanical systems (RF-MEMS), where the quality factor for oscillating actuators or speed of mechanical switches are improved at reduced pressure. The high vacuum eliminates fluidic friction decreasing the power consumption of the device and at the same time increases the sensitivity to external stimulus. These facts have promoted the present investigation of LT-direct wafer bonding technology.

One of the most important drawbacks in direct bonding is that it requires very good surface finish and total absence of particles in the bonded interface. That is why it is very important to study process cycles resulting in perfect surface polish for bonding. Polycrystalline silicon is a commonly used material in micromachining. Its surface is typically rough due to the microcrystalline structure posing major challenges for the polishing cycle.

We have investigated chemical-mechanical polishing (CMP) processes to efficiently remove the surface roughness that is met after thick film polysilicon growth. Grain boundaries in the polycrystalline structure were found to exhibit preferential etching when processing was

performed with conventional chemicals or processes. This phenomenon was not acceptable during polishing in order to maintain a sufficient level of surface smoothness required by LT-direct bonding [2]. Additionally, the functioning of polysilicon plasma-activation had to be confirmed. The bonding was performed in air or in vacuum. The films were deposited by both with low-pressure chemical-vapour-deposition (LPCVD) and atmospheric-pressure chemical-vapour-deposition (APCVD) growth process. Surface quality was investigated with atomic-force-microscope (AFM), the bonded interface strength was measured with the crack-opening-method and HF-etching test and voids at the bonded interface were studied with scanning-acoustic-microscopy (SAM) [2, 3].

## Experimental

In the experiments, <100> oriented p-type Czochralski grown silicon wafers with a diameter of 100 mm were used. The resistivity of the wafers was 1-50 ohmcm. A thermal wet oxide layer with a thickness of 500 nm was grown at 1050°C on part of the wafers. Polysilicon films were grown with two fundamentally different processes, LPCVD and APCVD. LPCVD-films were grown at 620°C and 680°C followed by an annealing step performed at 1050°C for 1h. The doping level of films was varied from intrinsic to highly boron-doped. APCVD-films were grown at 1100°C with ~$6{,}5*10^{17}$ of in-situ boron doping. Prior to APCVD-process, seed layer of 100nm was grown on all the wafers in 600°C with the LPCVD-process. APCVD-grown films were also annealed subsequently at 1050°C for 15min.

After the film depositions wafers went through a CMP-process carried out with Strasbaugh 6DS-SP two-table polishing system. Polishing was performed as a two-step process where the first step was dedicated for removing most of the high surface roughness and bigger surface defects, and the second one for finishing the surface. Surface quality after the polishing process was then confirmed with AFM in tapping mode (Digital Instruments D3100). After

the polishing and an RCA-1 ($NH_3$:$H_2O_2$:$H_2O$, 70°C) cleaning, the wafers were activated in a reactive ion etcher (Electrotech RIE) using argon plasma. During the plasma exposure the chamber pressure was 150 mTorr with the gas flow set at 30 sccm. The RF power was 150 W. With these parameters the bias voltage of the substrate electrode was 200 V. The duration of the plasma exposure in this study was 30s. After the plasma treatment the wafers were cleaned in deionised water. After cleaning, the wafers were dried in a spin dryer. The wafers were subsequently bonded in a commercially available wafer bonder (Electronic Visions EV801). The bonding was carried out either in air or in vacuum at room temperature. The bonded wafer pairs were annealed for 2 hours at 200°C. After this first annealing step some of the wafers were cut into rectangular slices using a dicing saw. The diced samples were annealed for 2h at 300-400°C. The surface energy of the diced samples was measured in air using the crack-opening-method. The bonded wafer pairs were inspected for interfacial voids using IR transmission imaging and scanning acoustic microscopy (Sonix UHR2000). The surface roughness of the plasma-activated surface was measured with an atomic-force microscope using silicon tips in the tapping mode. As a parallel test for the crack-opening-method an HF-etching test was executed, where samples were first dipped in a 50% HF solution for 10 minutes and subsequently cleaned in deionised water and dried. The etched distance was measured from cross-section samples by using LEO 1560 scanning-electron microscope (SEM) manufactured by Oxford Instruments. Concomitantly, information of the general interface quality was obtained.

## Results and Discussion

Both the LPCVD- and APCVD-films showed maximum film roughness up to 10-15% of the total film thickness. As-deposited film surface topography contained spikes, where sharp tips emerged from surrounding area. This could be seen with both LPCVD- and APCVD-films.

This kind of formation is understandable particularly in case of APCVD-polysilicon due to its strongly columnar structure (see Figure 1). The growth temperatures of the LPCVD-films were kept relatively high (620°C and 680°C) to enable high growth rates. Hence, grains grow preferentially in coarse columnar structure [4]. After the deposition the films were in a relatively high compressive stress which was needed to be relaxed or converted into tensile in order to maintain film stress controllability. The LPCVD-films were annealed after deposition to enlarge crystal size, to improve film quality and to relief stress. Annealing as well as boron-doping were confirmed to slow down the removal rate in CMP. The required removal for smoothening the surface was, however, found to be affected by neither boron-doping nor annealing. This implies that the surface roughness is not affected by doping or annealing. Furthermore, we observed that the retardation effect was significant in very heavily doped LPCVD-poly where boron concentration exceeded $5*10^{18}cm^{-3}$ and was close to its solubility limit at room temperature. We assume that a polishing process is prolonged due to slowed down silicon hydrolytic reaction, where boron in boranes (B-Si) is preferably attacked by hydroxide ions, and the activity of Si-Si hydrolysis is reduced as it has been suggested by *Yang et al.* in the case of single crystal silicon [5]. High decline of the removal rate as a function of annealing temperature and time could be explained by a grain structure consisting of larger grains, in which case the amount of grain boundaries prone to chemical attack by the polishing slurry is reduced. Alternatively, mechanical shear force needed to propagate a crack through a grain could be higher.

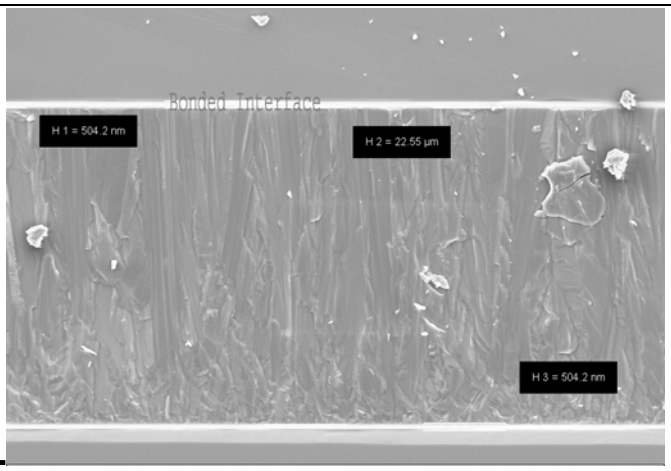


**Figure 1**

The developed CMP-process has been confirmed to be close to an ideal planarization process, where the roughness or tops of patterns are first abraded. This was noted to be exceptionally practical in high-roughness polysilicon polishing, where extreme topographies are commonly found. Hence, the level of necessary material removal is much lower than in a typical polishing process. Figure 2 illustrates the surface smoothening sequence in our polishing process. The development of a suitable CMP-process has achieved a state where local roughness is lowered to a level required for direct bonding as presented in Figure 3. The process uses consumables dedicated for polysilicon smoothening. An initial process removes the major roughness and potential surface defects, and is followed by a finishing step to further enhance the atomic level roughness performance. Typically, removal was kept close to the lowest possible.

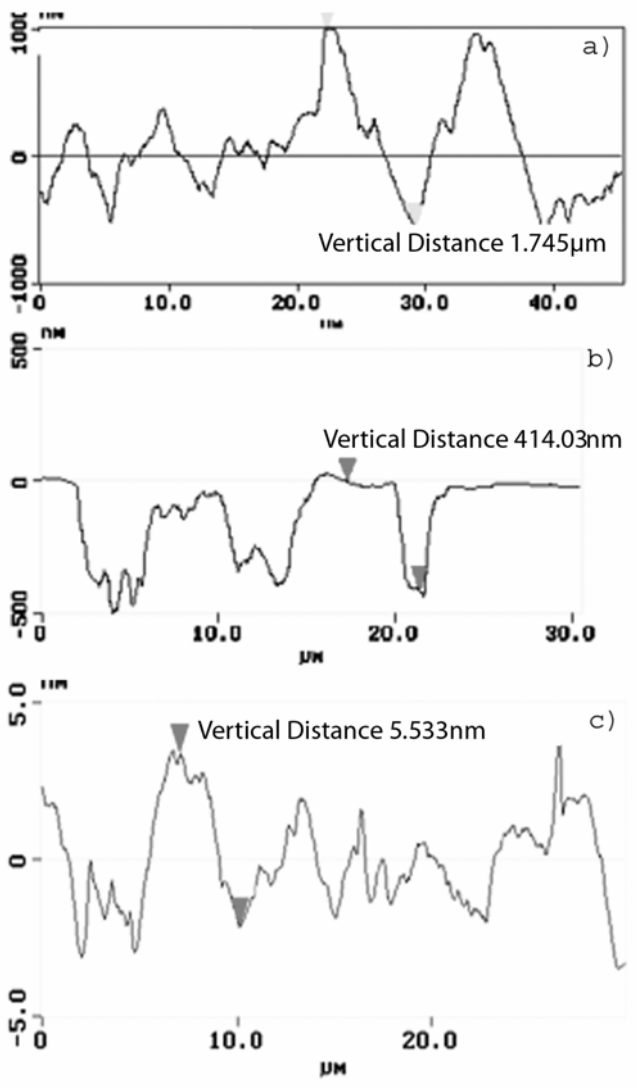


**Figure 2**

**Figure 3**

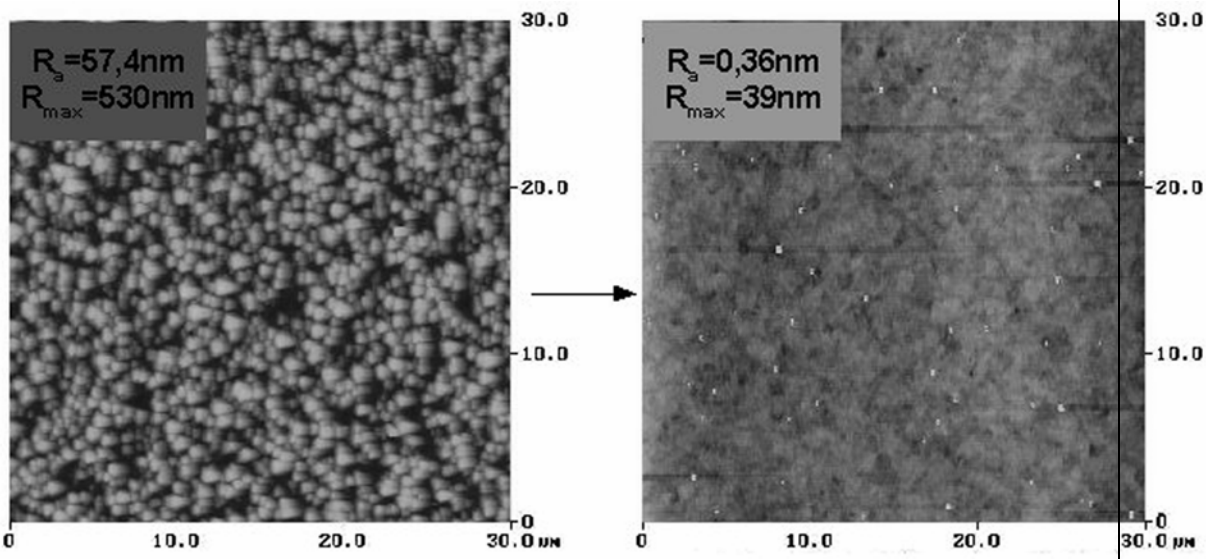

Figure 4 presents a SAM-image taken from a wafer couple where an oxidized silicon wafer with 23µm thick APCVD-grown polysilicon film is bonded to a silicon wafer with 500nm of thermal oxide. The wafer was bonded in vacuum. The visible voids suggest failure in wafer handling in otherwise successful bonding. In general, bonding in air was found to result in slightly higher surface energies than vacuum bonding. This has been also witnessed in case of hydrophilic bonding of Si and $SiO_2$ [6]. According to the results obtained from crack-opening-method measurements, the APCVD-grown films yield bonding strengths higher than those of the LPCVD-films. The HF-etching trials showed systematically higher surface energies corresponding to etch length than crack-opening-method. Figure 5 presents etch lengths of samples annealed at different temperatures. Results for plasma-assisted bonding are published by *Suni et al*. [3].

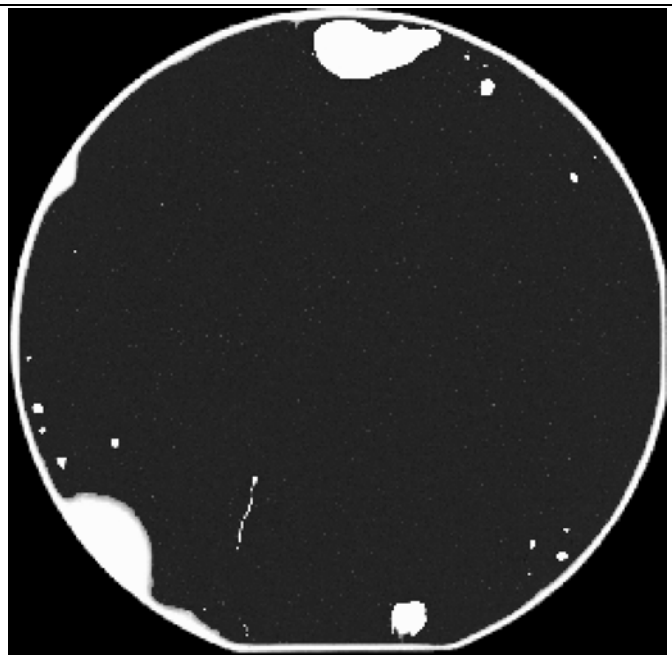

**Figure 4**


**Figure 5**

The surface energy and bonding quality were measured from argon activated and deionised water rinsed samples bonded to thermally oxidized silicon wafers. These samples included both LPCVD- and APCVD-films. The measurement results in Figure 6 show already moderate bond strength after annealing the wafer couples at 200°C for 2 hours.

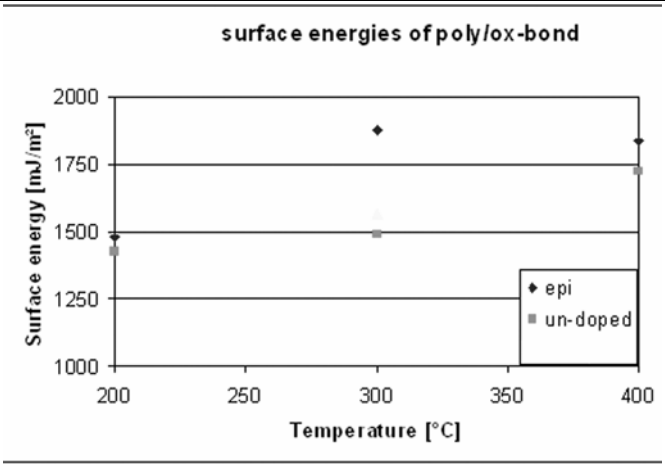


**Figure 6**

Additional experiments were made with bonding varying materials to polysilicon. These studies included quartz (fused silica) and Pyrex glass. Both quartz and Pyrex were treated

with conventional oxide polishing process followed by RCA-1 cleaning and argon plasma-activation with rinsing step. Quartz/APCVD-polysilicon bonding quality was confirmed visually and identified to be uniform with very few visible voids as can be seen in Figure 7.

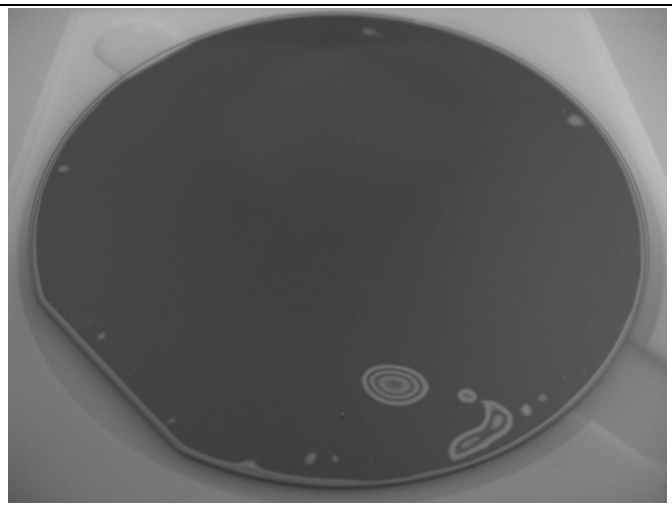

**Figure 7**

## Conclusions

Polysilicon LT-direct bonding as a method for wafer-scale-packaging and vacuum encapsulation has been demonstrated. We have developed a new kind of polishing process, where several microns of polysilicon is removed still leaving the surface direct bondable. This is enabled by a dedicated and effectively planarizing polishing process which allows polishing and LT-direct bonding of patterned wafers as well. The required amount of removal is dictated by the surface roughness of deposited and annealed material. Due to the ideally planarizing process, material removal is close to the roughness amplitude of the deposited and annealed films. Understanding of the polysilicon and the grain boundary behavior under CMP has been greatly improved.

Bonding strengths of around 2000 $mJ/m^2$ and almost void-free interfaces are verifiably achievable. Demonstration of the LT-direct bonding of polysilicon to glass has been done.

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Figure 1. Cross sectional SEM-image of bonded wafer couple Si/LPCVD-polysilicon seed layer/APCVD-polysilicon/Ox/Si.

Figure 2. Line section analysis from an AFM-image taken from a) as-deposited APCVD-polysilicon surface, b)APCVD-polysilicon surface after 100 s polishing and c) the surface after first polishing step when only atomic scale roughness is remaining. Here, no other material loss than peak reduction (ideal planarization) is expected to take place.

Figure 3. LPCVD-polysilicon (thk. 4µm) before and after two-step CMP-process. White dots on the image after CMP are residual abrasive particles.

Figure 4. SAM image of bonded APCVD-grown polysilicon/ox. White areas are voids.

Figure 5. SEM-images of bonded interfaces etched with 50% HF-solution for 10 minutes. Surface energies corresponding to etch propagation lengths are shown with each annealing temperature. The equivalence is taken from [3].

Figure 6. Surface energies of vacuum bonded polysilicon/ox-couples.

Figure 7. A photograph of quartz wafer bonded to a silicon wafer with a polished APCVD-polysilicon film (thickness 23µm).