RF Front-End for Integrated Radar Receivers

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ABSTRACT OF THE
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Beam-steering is used in radars as well as in future communication systems. With increasing transmission bandwidths, implementing beamsteering with time delays instead of phase shifts is beneficial. The main goal of this thesis was to study a concept called the sampling mixer. The concept would permit the creation of receiver front-ends supporting true time delay beam-steering. The sampling mixer concept was studied with circuit simulations and the results support the feasibility of an implementation based on the concept.

Keywords: Beam-steering, Receiver, True Time-Delay

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Keilanmuodostusta voidaan hyödyntää tutkajärjestelmissä, sekä tulevaisuuden matkaviestinjärjestlemissä. Keilanmuodostus voidaan toteuttaa vaihesiirroilla, mutta taajuuksaistojen kasvaessa viiveisiin perustuvalla järjestelmällä saavutetaan etuja. Tämän työn päätavoite oli tutkia näytteistavään alassekoitukseen perustuvaa radiovastaanotinkonseptia, joka mahdollistaisi viiveiden käytön. Konseptia tutkittiin piirisimulaatioilla. Tulokset tukevat konseptin käyttökelpoisuutta.

Avainsanat: Keilanmuodostus, Radiovastaanotin, Aikaviive

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Symbols and abbreviations

Symbols

ϕ	spherical coordinate azimuth angle
θ	spherical coordinate elevation angle
c	speed of light in vacuum
k	Wave number
λ	Wavelength of an electromagnetic wave
T_c	Carrier frequency cycle time
f_c	Carrier frequency / Center frequency
F_s	Sampling rate
N	Sampling factor $\frac{F_c}{F_s}$
Ω	Ohm, unit of electric resistance
k	Boltzmann constant
dB	Decibel
T_t	Track time
T_s	Sampling period
dB	Decibel

Abbreviations

ADC	Analog-to-digital converter
MOS	Metal Oxide Semiconductor (Transistor)
RF	Radio Frequency
IC	Integrated Circuit
BB	Baseband
BW	Bandwidth
NF	Noise Figure
SNR	Signal-to-Noise ratio
FIR	Finite Impulse Response (Filter)

1 Introduction

Beam-steering, pointing the combined radiation of an array of antennas to a desired direction, will be used extensively in future radar and communications applications. In radar applications narrow, rotatable beams are used to locate targets. In communications, beam-steering can be used for spatial multiplexing. This allows multiple users to transmit on a single frequency channel simultaneously, which makes use of the spectrum more effective and can be used to increase data rates.

Phased arrays, arrays or grids of antennas, can been used to enable beam steering [11]. As the name implies they employ phase shifters in the transmit or receive paths to compensate delays caused by different times of flight from target direction to individual antennas. A limitation of this approach is that phase shift equals time delay only at a point frequency. When receiving or transmitting data the signal must have some bandwidth around the carrier frequency. The frequency components closer towards the edge of the transmission band suffer increasingly worse performance. as the transmission bandwidth increases. [9]

The goal for the future is to use increasingly wide communication bandwidths, [2] which makes makes this problem more severe. Wideband phase shifters have been proposed. Creating a perfectly linear phase shifter is difficult. Alternative solution to this problem is to use time delays instead of phase shifts. Delays are the same at all frequencies, so using wide bandwidths does not pose the same problem.

To study the possibilities of implementing time-delay beam-steering, this thesis presents a concept called sampling mixer. It allows the creation of true time delay receivers that can be implemented in CMOS IC. The concept is based on sampling the antenna inputs with down-converting pulses at different times and summing the samples coherently. The concept is enabled by current CMOS technologies that allow the creation of the digital signals that control the sampling at RF frequencies.

An issue related to aliasing of unwanted spectral components on top of the baseband signal in the concept is presented. A compensation circuit that solves the aliasing problem is explained and simulated.

Circuit simulations are also presented for determining the how sampling mixer core parameters are affected by tuning the control signals. The time delay functionality is also demonstrated.

2 Beam-steering

This chapter discusses beam-steering in order to provide background information for requirements for the receiver architecture presented in 3. In this thesis, the term beam-steering refers to electrical beam-steering, which controls the inputs of antennas in an array to steer the direction of reception or transmission. An alternative method to do this would be to physically rotate a narrow-beam antenna. Also, beam-steering arrays are traditionally called phased arrays, but in this thesis they are called arrays. The array term is also not limited to antennas distributed along one dimension, but it also includes antenna arrangements along two or more dimensions.

2.1 Theory of Beam-steering

Beam-steering is a concept that is used for creating and rotating a beam of radiation by combining radiation from multiple antennas in an array. Applications where beam-steering is used include radars, where spatial information of the received signal is used to locate targets, and future communication systems that allow spatial multiplexing [4] [8] to increase spectrum utilisation.

The spatial radiation properties of an antenna array are based on the array geometry. Because the antennas have some distance between them, radiation from each antenna generally has to travel different lengths to reach a target. If we assume that the target for signal transmission or reception is far from the antenna, the radiation can be modelled with a plane wave. Fig. 1 illustrates a plane wave arriving to two antennas. From geometry, we can calculate the difference in distance the wave has to travel to be

$$\Delta d = d\cos(\theta), \tag{1}$$

where d and θ are as in Fig. 1. Because the speed of light is finite, the wave will arrive at the antennas at different times. The time delay is

$$\tau = \frac{d\cos(\theta)}{c}, \tag{2}$$

where c is the speed of light.

Instead of time delays, we can think that the wave comes to the two antennas at the same time but with different phase. The phase shift of the wave can be derived , as

$$\Delta\phi_w = 2\pi f\tau = 2\pi f\frac{d\cos(\theta)}{c} = kd\cos(\theta), \tag{3}$$

where f is the frequency of the incoming wave and k is the wavenumber $k = \frac{2\pi f}{c}$

The phase shift can be compensated by adding phase shifters between the antennas and the transceiver. An alternative method is to add delays or phase shifts to the LO signals going to the transceiver mixers [5].

Because the phase differences caused by the array geometry change with the incident angle, phase shifters only compensate the phases for one direction. The reception or transmit angle is selected with the phase shifters and signals in this

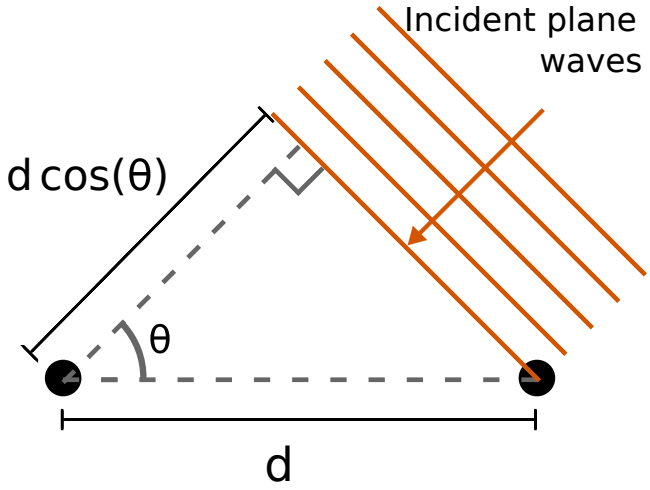


Figure 1: Different travel distances to two antennas (dots)

direction are summed coherently, i.e. in phase. Radiation from or to elsewhere gets summed non-coherently or out-of-phase. The direction where the phase shifters cancel the phase differences caused by the geometry is the direction of maximum gain. There are also directions of zero gain where the phase shifts caused by geometry and shifters add up to 180 degrees, resulting in cancellation. In most cases the phase shifts can be controlled and thus the direction of the beam can be altered.

The way the radiation form the array is summed at any direction can be presented with the array factor (AF), which is a scalar complex function of spherical coordinate angles ϕ and θ. The total radiation pattern of an antenna array consisting of identical elements can be calculated as the product of the radiation pattern of a single element and the AF.

The array factor for an array of N antennas is defined as

$$AF(\theta, \phi) = \sum_{i=0}^{N-1} a_i \times \exp(jk\hat{r_i} \cdot \hat{r}). \tag{4}$$

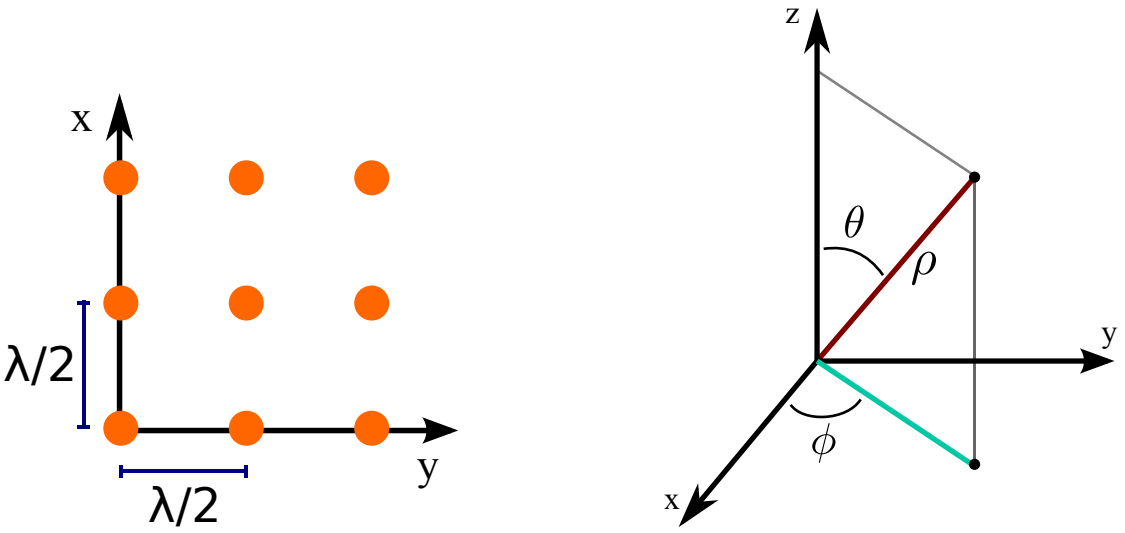
The exponential terms describe the phase shift caused by the array geometry in direction (θ, ϕ) for each antenna. Symbol $\jmath$ is the imaginary unit. $\hat{r_i}$ is the antenna element location and $\hat{r}$ is the unit vector in the direction (θ, ϕ). The phase shifts at each antenna interface, which compensate the phases caused by the array geometry and select the transmission direction, are included in the term a_i, which is a complex factor with amplitude and phase, $a_i = |a_i| \times angle(a_i)$. In a general case, the amplitudes of the signals can also be modified to further shape the array factor and the resulting beam, but, in this thesis amplitudes of a_i are only used for normalizing AF_{max} to 1.

$$|a_i| = \frac{1}{N}. \tag{5}$$

[11]

The following example is used to provide insight on the concept of Array Factor, described by (10). An array setup is shown in Fig. 2a. The antennas are placed

on a grid on the XY-plane with spacing of $\frac{\lambda}{2}$. Fig. 2b shows how the spherical coordinates are defined in relation to the cartesian coordinates. Assuming the plane wave propagation, the distance ρ to the target has no effect on the phase shifts.



(a) (b)

Figure 2: (a) Antennas (dots) on the XY-plane with spacing $\frac{\lambda}{2}$. (b) The spherical coordinates θ and ϕ

Let the element positions be calculated as

$$\hat{r_i} = hd\hat{x} + kd\hat{y}, \tag{6}$$

where $\hat{x}$ and $\hat{y}$ are the unit vectors in directions x and y, and, h and k are indexes of the antennas, so that $h_{max}k_{max} = N$. The unit vector towards direction (θ, ϕ), $\hat{r}$, can be calculated as

$$\hat{r} = sin(\theta)cos(\phi)\hat{x} + sin(\theta)sin(\phi)\hat{y} + cos(\theta)\hat{z} \tag{7}$$

In order to choose a main direction for the beam, the phase shifts a_i are chosen so that they cancel the are selected so that they cancel the phase shifts from the array geometry. The required phase shifts for direction (θ_0, ϕ_0) can be calculated as

$$angle(a_i) = \exp(-jk\hat{r_i} \cdot \hat{r_0}), \tag{8}$$

where $\hat{r_0}$ is

$$\hat{r_0} = sin(\theta_0)cos(\phi_0)\hat{x} + sin(\theta_0)sin(\phi_0)\hat{y} + cos(\theta_0)\hat{z} \tag{9}$$

Substituting (8) to (10) gives an array factor that has its maximum at (θ_0, ϕ_0). The array factor in the main direction is

$$AF(\theta_0, \phi_0) = \sum_{i=0}^{N-1} a_i \times \exp(jk\hat{r_i} \cdot \hat{r_0}) = \sum_{i=0}^{N-1} \frac{1}{N} \exp(-jk\hat{r_i} \cdot \hat{r_0}) \times \exp(jk\hat{r_i} \cdot \hat{r_0}) = 1. \tag{10}$$

Concept of array factor is visualized in Fig. 3 An example of a visualisation of an array factor is presented in Fig. 3. The array consists of 3x3 elements and the beam is directed to $\phi_0 = 0, \theta_0 = \pi/4$. Fig. 3 depicts the amplitude of the AF on a linear scale. It can be observed that the AF is symmetrical in relation to the array. Multiplying the AF with a realistic element radiation pattern would remove the mirror maximum from the resulting combined radiation pattern [11].

The model discussed above has been created in order to gain insight to the beam-steering concept and to provide solution to (4) as time delay values, which can be further utilized in the control of the circuits described in the following chapters.

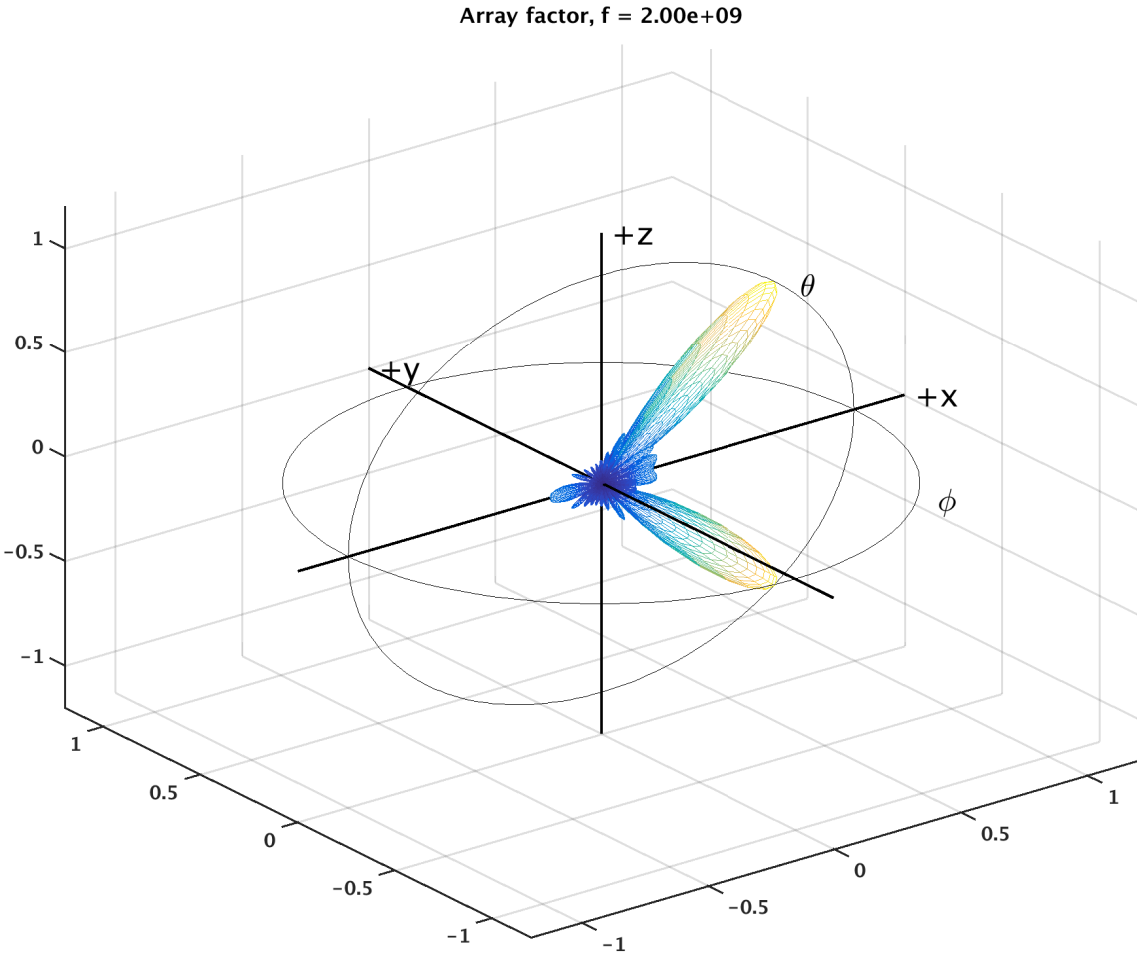


Figure 3: An example AF with 3x3 antenna element

2.2 True Time Delays in Beam-steering

The theory presented in the previous section described how beam-steering can be performed by phase shifters [11]. However, the limitation of beam-steering with phase-shifters can be observed from (3); the phase shift equals time delay only at point frequency f. Therefore, during the data transmission with certain bandwidth,

the signal spectrum is distorted, and, in modern transmission systems there is a trend for increasing wireless communication bandwidths.

Signal components with frequency deviation from selected reception center frequency, for which the phase compensation is defined, suffer from beam squint [1] [9]. The exponential term describing the phase shifts caused by array geometry in (10) is frequency dependent, while a_i is constant. Therefore the direction of the radiated or received beam changes as a function of frequency.

In order to minimize the squint effect,various wide-band phase shifter structures have been proposed, [6] [14]. However, with these methods, the phase shifter can not be made perfectly linear.

A method to completely remove the squint is to use time delays instead of phase shifters. This way, it is possible to consider and compensate the equivalent time delays in (2). The time delays are only defined by the array geometry and beam direction, i.e. they remain constant regardless of frequency.

The frequency dependent phase shifts of the exponential term in (10) can be linked to time delays, by using the relation from (3). We can use (10) and (3) to formulate general With (10) and (3) it is possible to formulate general expression for the relation between phase shifts and time delays in an antenna array. The phase shifts caused by array geometry are included in the exponential term of (10), $\exp(jk\hat{r}_i \cdot \hat{r})$, which corresponds to a phase shift of

$$\Delta\phi_{geometry} = k(\hat{r}_i \cdot \hat{r}). \tag{11}$$

The corresponding time delays are

$$\tau_i = \frac{k(\hat{r}_i \cdot \hat{r})}{2\pi f} = \frac{2\pi(\hat{r}_i \cdot \hat{r})}{2\pi f\lambda} = \frac{f(\hat{r}_i \cdot \hat{r})}{fc} = \frac{\hat{r}_i \cdot \hat{r}}{c}, \tag{12}$$

showing that the time delays are not frequency dependent.

Time delay implementations found in the literature use delay lines to create the delays. The delay lines can be microwave lines [17] or optical cables [18]. Both of these approaches are too large to integrate on silicon.

To address the challenge of creating true time delays, a concept called the sampling mixer is presented in chapter 3.

3 Sampling Mixer

The previous chapter described the benefits of using time delays instead of phase shifts in beam-steering. This chapter introduces a concept called sampling which is mixer suitable for integrated receivers with true time delay capability. Fig. 4 shows a block diagram of a receiver with four antenna inputs. Band-pass filters are used for suppressing signals outside the total operation frequency range of the receiver, and, low-noise-amplifiers (LNA), amplify the received signal and improve the noise performance of the receiver chain [15]. Further design details of LNAs and filters are beyond the scope of this work, as the focus is in the sampling mixer concept and true time delay beam-steering.

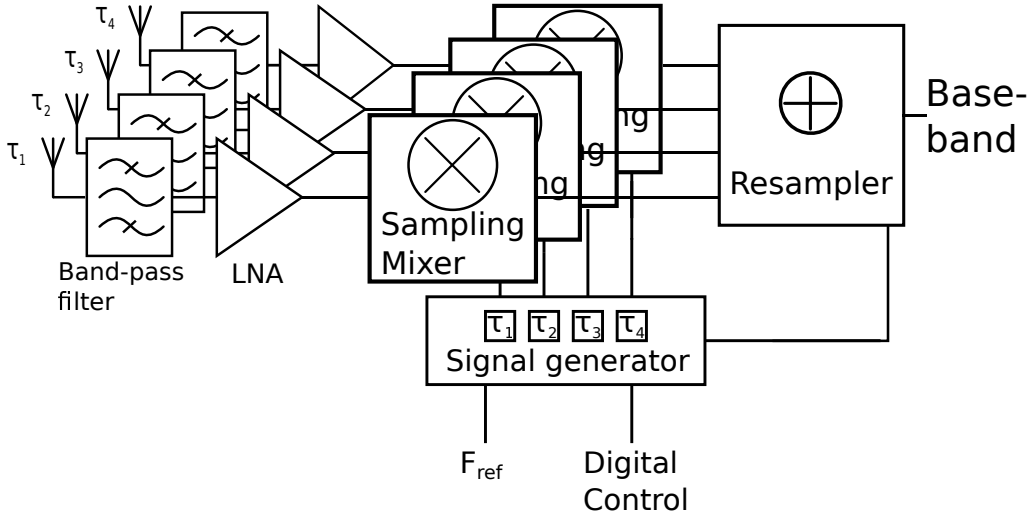


Figure 4: Sampling mixer receiver block diagram

3.1 Concept

The sampling mixer concept is based on sampling the inputs of an antenna array at different times. The different sampling instants are used to cancel the delays in (12) and enabling beam-steering. Fig. 5 shows an example where two antennas, at frequency f_c, have a signal coming to them so that there are delays of $T_c/4$ between each input. When the sampling instants are separated by equal delays, each mixer samples the same part of the sinusoidal input signal.

The samples from each mixer, that are taken at different times, can be aligned in time by re-sampling their sum. The circuit implementations of the summing circuit and the re-sampler are outside the scope of this thesis. It is worth noting that they only have to operate at baseband frequencies, and such circuits are possible. The summing can be done for example with operational amplifiers and samplers have been studied extensively, for example in [3] [10].

Fig. 5 also shows outputs of the mixers and the re-sampler. The re-sampling has to occur before the first mixer samples again. This means that the re-sampling rate

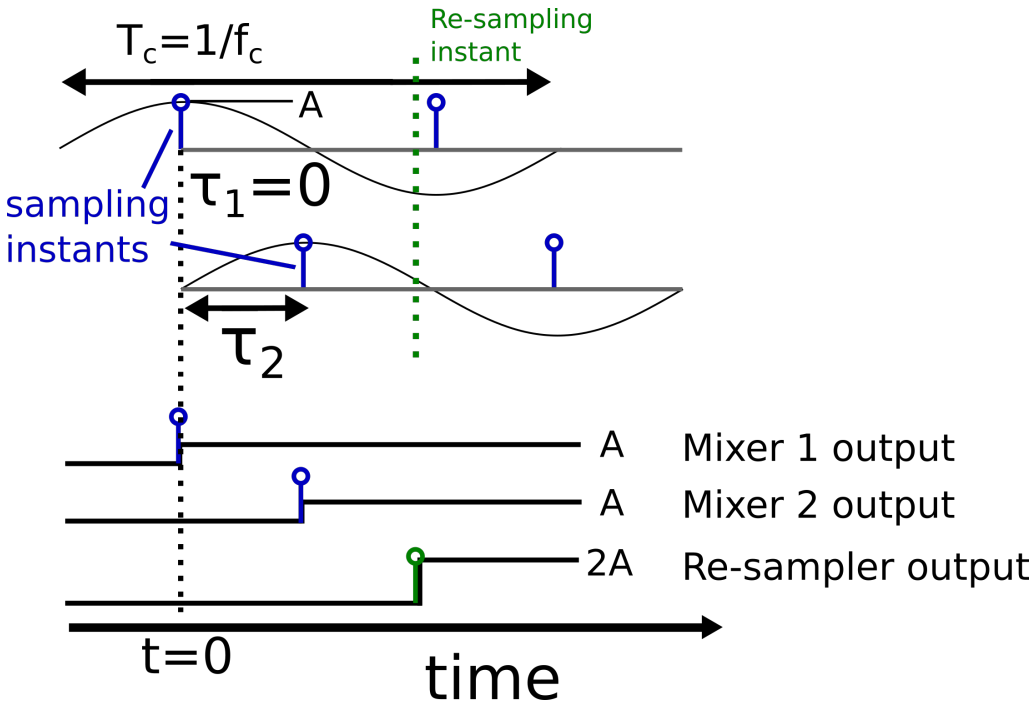


Figure 5: Signal ($f = f_c$) coming to antennas with different delays. Sampling time instants that cancel the delays. Each mixer samples the same part of the input signal. Re-sampling combines and aligns the mixer outputs in time.

is equal to the sampling rate of the individual mixers. This sampling rate defines the maximum delays that can be created with the receiver,

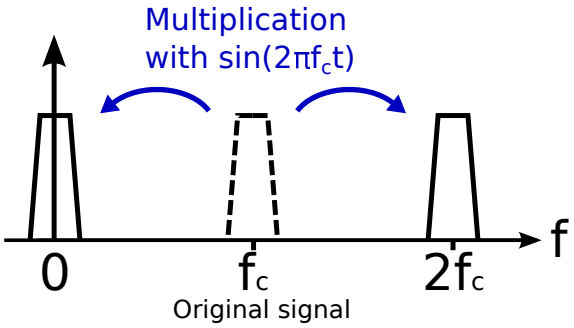
$$\tau_{max} = T_s = \frac{1}{F_s}. \tag{13}$$

Sampling an input with frequency f_c with a sample rate $F_s < 2 * f_c$ would mean violating the Nyquist criterion, which says that, in order to avoid aliasing, the sample rate must be two times higher than the highest frequency component in the input. This means that the delays are limited to $T_c/2$.

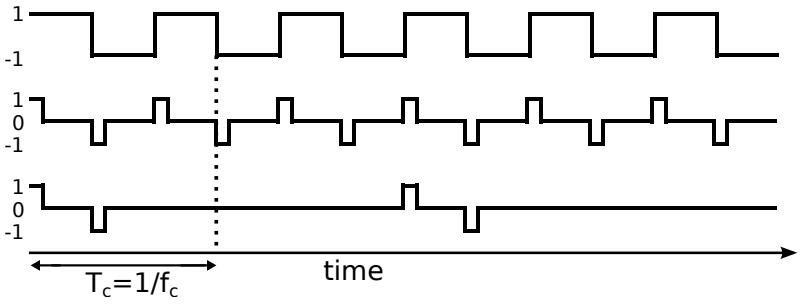
From (2) we can see that, with large arrays and beam-steering angles, the maximum delays needed can be longer than several carrier cycle time periods T_c. This means that our sample rate would need to be much lower than $f_c/2$.

To get around this, the input signal is down-converted to a lower frequency before sampling. Fig. 7 depicts a system which samples a down-converted signal. From signal processing, we know that multiplying an input signal at frequency f_1 with a signal with frequency f_2, splits the input signal to frequencies $f_1 - f_2$ and $f_1 + f_2$. This means that, down-converting a signal from around RF carrier frequency f_c to baseband can be done by multiplying it with a sinusoid also at f_c. In RF engineering, doing these frequency translations is called mixing.

The multiplying signal can also be a square wave between 1 and -1, at frequency f_c. In addition to f_c, the square waves have also higher harmonic frequency components that also down-convert the signal. These components are weaker than the fundamental



(a) Down-converting a frequency band from around f_c to baseband by multiplying with a sinusoid.



(b) Waveforms that can be used for the down-conversion in (a). From top to down: 50% Duty-cycle square wave, 10% Duty-cycle square wave, Pulsed 10% Duty-cycle square wave

Figure 6

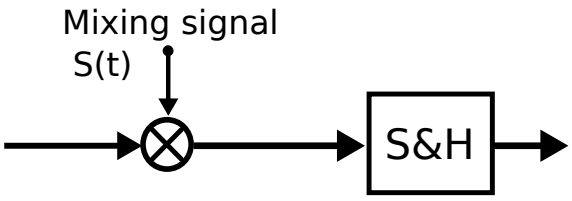


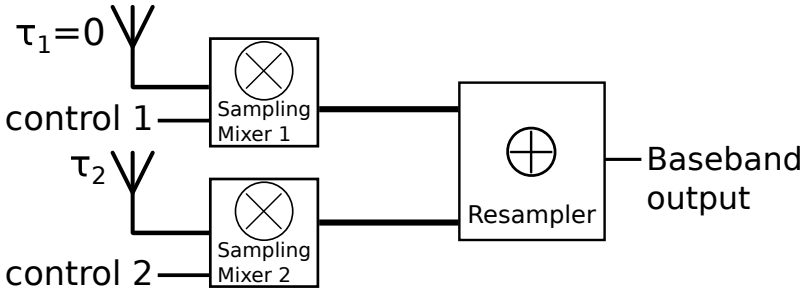
Figure 7: System for down-converting and sampling. The block labelled S&H represents a sample-and-hold circuit.

component but they do down-convert to baseband from multiples of the selected frequency. Depending on the total frequency range of the receiver, the RF filter stages in Fig. 4 can be used to remove components from the harmonic frequencies, so that they don't appear at baseband after the down-conversion. Square wave mixing is used because it is easy to implement with electronic switching, which will be shown in section 3.2.

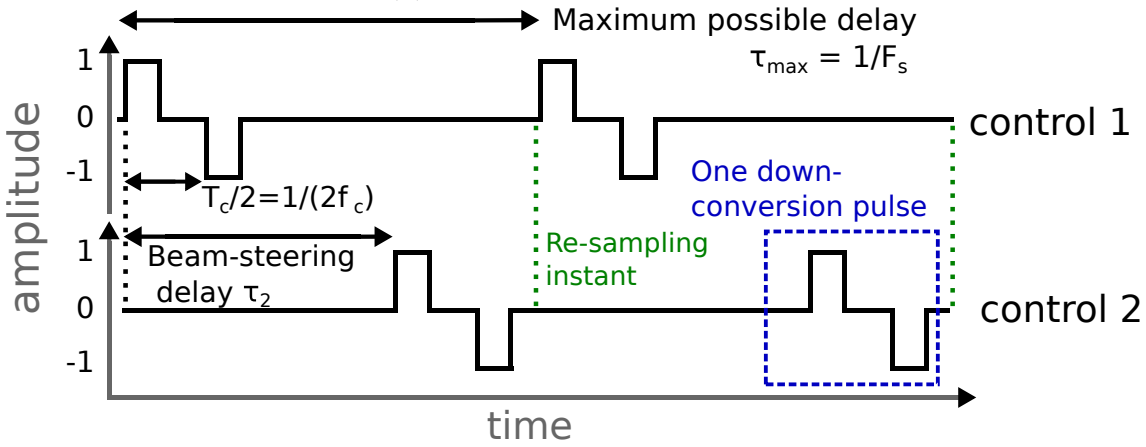
Fig. 6a shows the frequency translation effect of multiplying a signal with a sinusoid. Most importantly for this concept the frequency components that are originally around f_c are moved to the so called baseband, i.e. around frequency $f = 0Hz$. Fig. 6b shows different square wave signals that can be used for down-conversion. The square wave's duty-cycle can be varied without changing the signals

fundamental frequency. The lowest waveform in the Fig. shows a pulsed signal that that is used in the sampling mixer concept to down-convert and sample the input signal at the same time. The digital signal generator circuitry, which generates the down-converting signals for the mixers is outside the scope of this thesis.

Fig. 8 shows the down-converting and sampling signals. When the control signal is 1 the input is connected to the output, and, when it is -1 the input is multiplied by -1 and then connected to the output. While the control signal is 0, the value at the output is held constant, i.e. a sample is saved. It also shows how they are used for compensating the delay τ_2, which is the delay between the incoming signal reaching antennas 1 and 2 of 8a. The pulses of the control signals are the sampling instants of Fig. 5 and both mixers sample the same part of the input signal. Section 3.2 explains how the sample is stored.



(a) A simplified receiver example. The mixers multiply the incoming signal with the control signals. The control signals are described in (b)



(b) The control signals for doing the down-converting and sampling. Maximum possible delays are defined by the inverse of the sampling rate.

Figure 8

Fig. 9 describes the behaviour of an RF signal which is fed to a sampling mixer. The carrier frequency $f_c = 1GHz$ and a transmitted signal component which is a 10 MHz sinusoid signal, up-converted to 1.01 GHz. The first waveform is the RF frequency signal that is received by the mixer. The second wave is the wanted data

signal after down-conversion to baseband. The thicker, discrete time signal shown in the third waveform, is the sampled version of the down-converted signal. The zoomed-in part shows the down-converting and sampling pulse and the time between sampling instants in relation to the RF signal.

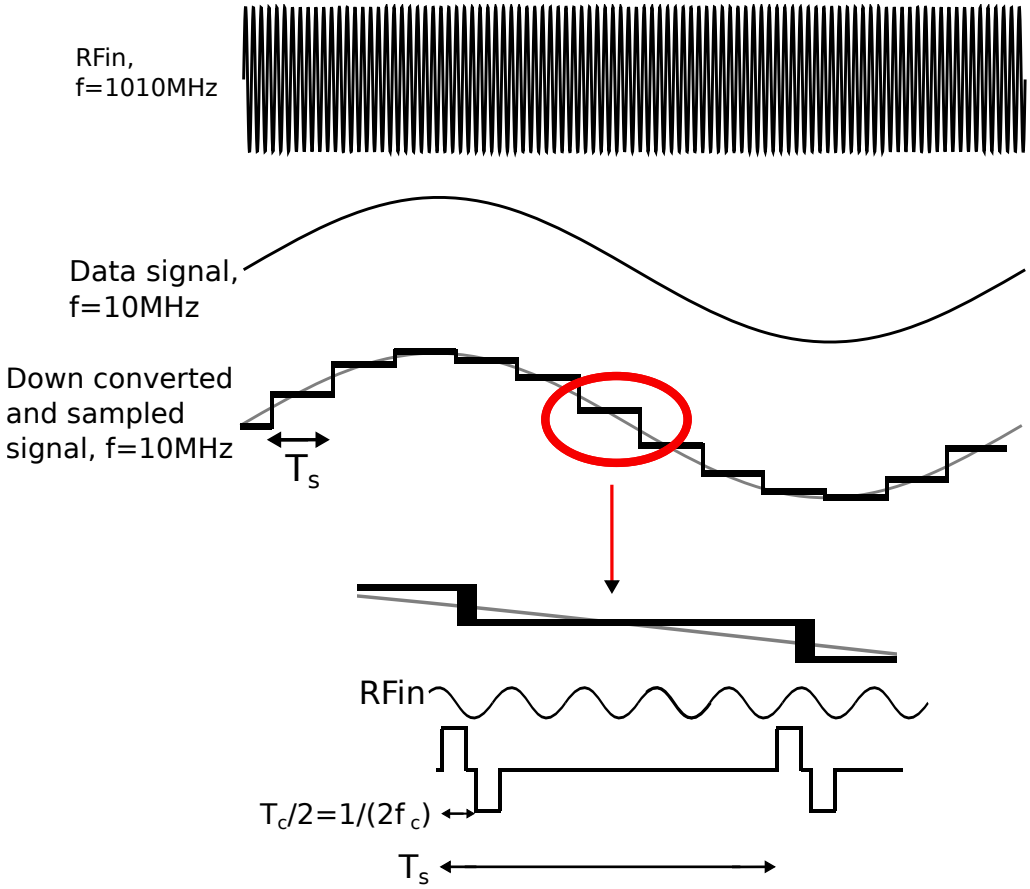


Figure 9: Down-conversion of an RF input signal with the sampling mixer

3.2 Sampling Mixer Core

This section describes the implementation of the sampling mixer core. Based on the previous section, the sampling mixer core down-converts the input signal by multiplying it by 1 and -1, and, stores a sample of the resulting down-converted signal. The circuit model is show in Fig. 10. The mixing operation is done with the passive mixer topology [7]. Multiplying by 1 or -1 is done by changing the polarity of the connection from input to output with the 4 switches, which form 2 pairs. The switches conduct when a voltage is set to their controlling signals. The control signals S_1 and S_{-1} are obtained by splitting the down-converting pulse show in Fig. 8b. The control waveforms are depicted in Fig. 11.

The resistances R_{sw} model the non-zero on resistances of the switches. The capacitor is required for storing the sample. In order to keep the voltage level of the

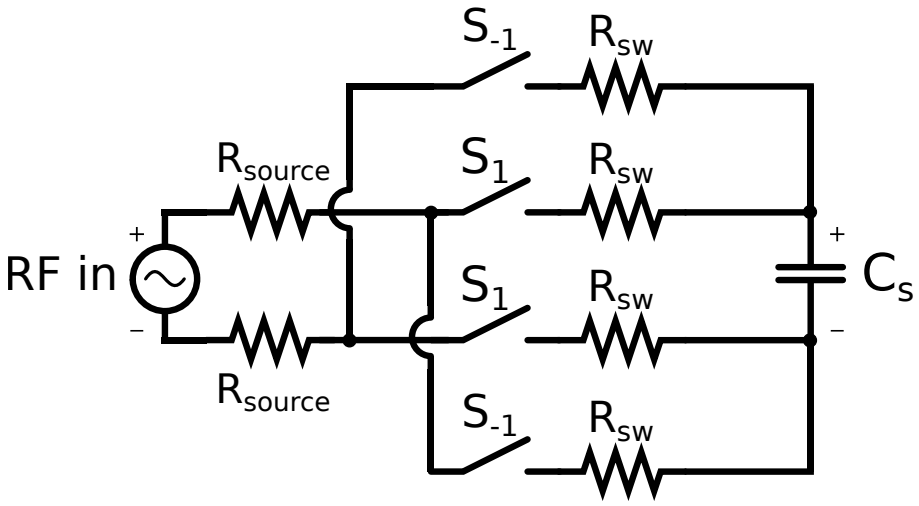


Figure 10: Sampling mixer core. Switching signals S_1 and S_{-1} control the switches.

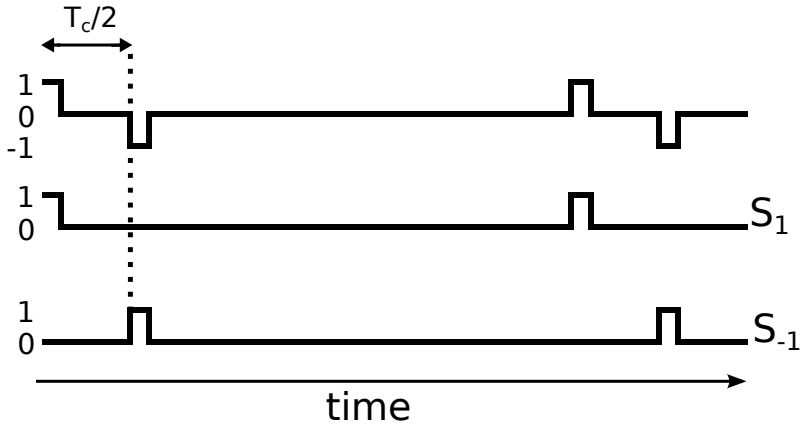


Figure 11: Signals driving the switches of the sampling mixer

capacitor constant when the switches are not conducting, there can be no resistor in parallel with the capacitor in the following stages of the receiver chain.

3.2.1 RC Track-and-Hold Sampler

To analyse the sampling mixer the circuit in Fig. 10, is first considered without the down-conversion capability. Fig. 12 depicts the functional parts of the mixer core, when only the switch S_1 is active. The transfer function of this RC-sampler is now derived.

Track time T_t, in Fig. 12, is the conducting time of the switch, during which the sampler tracks the input through an RC response. T_s is the time interval between samples. Between times T_t and $T_s - T_t$, the sampler holds the output value value at $t = T_t$. The impulse response of the system is shown in Fig. 13. In order to simplify the analysis, the RC-sampler is split into functional blocks. A signal flow graph, which corresponds to circuit and impulse response from figs. 12 and 13, is depicted in Fig. 15. The individual blocks are now described.

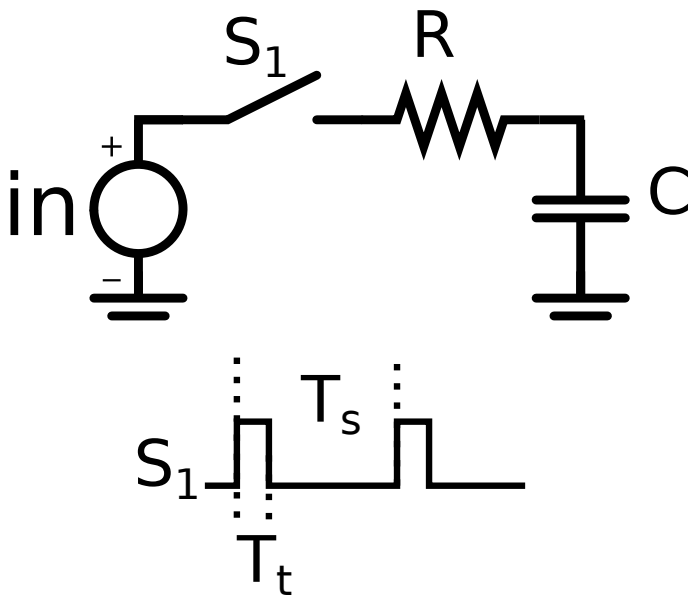


Figure 12: RC Track-and-Hold sampler. Output voltage is defined over the capacitor.

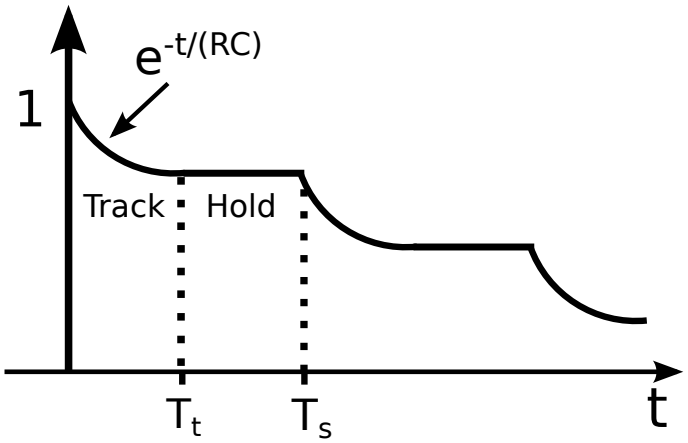


Figure 13: Impulse response of the circuit in Fig. 12

Fig. 14 depicts the impulse response of the track-block, which consists of the same shape repeated every T_s. The repeating response is active, and follows the normal RC-response, during the track period T_t. After T_t its output is zero. The consecutive responses are scaled by a multiple of $e^{\frac{-T_t}{RC}}$. The Laplace transform of the first response pulse is

$$H_{1'}(s) = \int_0^\infty e^{-\frac{T_t}{RC}} e^{st} dt - \int_{T_t}^\infty e^{-\frac{T_t}{RC}} e^{st} dt = \int_0^\infty (\mu(t) - \mu(t - T_t)) e^{-\frac{T_t}{RC}} e^{st} dt$$
$$\int_0^{T_t} e^{-(s+\frac{1}{RC})t} dt = \Big/_0^{T_t} e^{-(s+\frac{1}{RC})t} = \frac{1 - e^{-(s+\frac{1}{RC})T_t}}{s + \frac{1}{RC}} = \frac{1 - e^{-\frac{T_t}{RC}} e^{-sT_t}}{s + \frac{1}{RC}} \tag{14}$$

The track-blocks transfer function repeats $H_{1'}$ every T_s and each repeated response is scaled by a multiple of $e^{-\frac{T_t}{RC}}$.

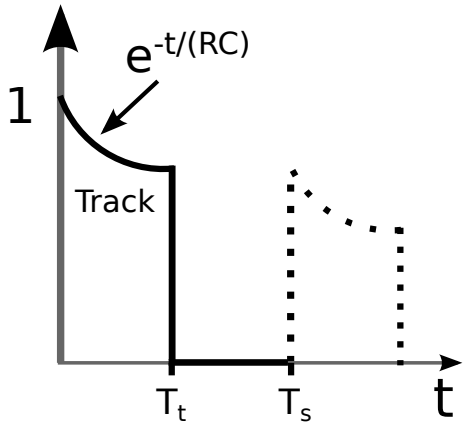


Figure 14: Impulse response of the track block. The part drawn with a solid line is repeated every T_s, scaled with a multiple of $e^{\frac{-T_t}{RC}}$.

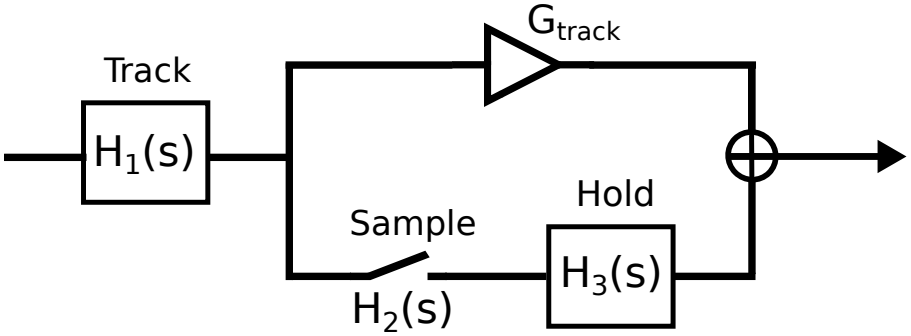


Figure 15: Signal flow graph of the circuit in 12

$$H_1(s) = \sum_{n=\infty}^{\infty} \frac{(1 - e^{-\frac{T_t}{RC}} e^{-sT_t})}{s + \frac{1}{RC}} e^{-\frac{nT_t}{RC}} e^{-nsT_s}. \tag{15}$$

Using the sum of a geometric series

$$\sum_{n=\infty}^{\infty} e^{-\frac{nT_t}{RC}} e^{-nsT_s} = \sum_{n=\infty}^{\infty} e^{-n(\frac{T_t}{RC}+sT_s)} = \frac{1}{1 - \frac{1}{e^{(\frac{T_t}{RC}+sT_s)}}} = \frac{1}{1 - e^{\frac{-T_t}{RC}} e^{-sT_s}} \tag{16}$$

$$H_{1''}(s) = \frac{(1 - e^{-T_t(\frac{1}{RC}+s)})}{(s + \frac{1}{RC})(1 - e^{-\frac{T_t}{RC}} e^{-sT_s})}. \tag{17}$$

The DC gain of the circuit in Fig. 12 is 1 for all $\frac{T_t}{T_s}$. Frequency response $H_{1''}$ is made to match this by scaling it with $1/H_{1''}(0)$.

$$H_{1''}(0) = \frac{(1 - e^{-\frac{T_t}{RC}})}{(\frac{1}{RC})(1 - e^{-\frac{T_t}{RC}})} = RC, \tag{18}$$

which leads to

$$H_1(s) = \frac{1}{RC} \frac{(1 - e^{-T_t(\frac{1}{RC}+s)})}{(s + \frac{1}{RC})(1 - e^{-\frac{T_t}{RC}} e^{-sT_s})}. \tag{19}$$

Transfer function of sampling delayed by T_t is

$$H_2(s) = e^{-sT_t}. \tag{20}$$

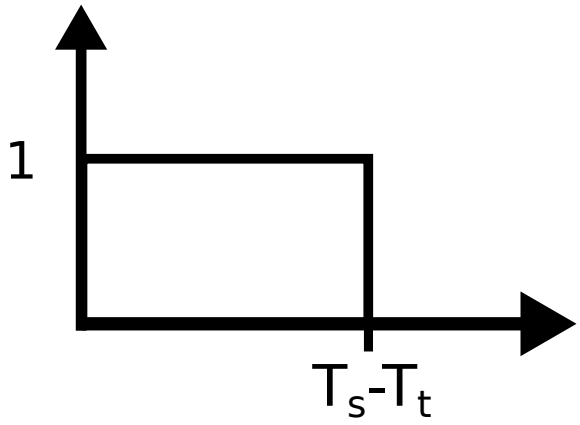


Figure 16: Impulse response of the hold-block.

The hold-block holds the output value of the track-block from $t = T_t$ to $t = T_s$. During T_t its output is zero. Its unscaled transfer function $H_{3'}$ is the Laplace transform of its impulse response, shown in Fig. 16.

$$H_{3'}(s) = \int_0^{T_s - T_t} e^{st} dt = \Big/_0^{T_s - T_t} -\frac{e^{st}}{s} = \frac{1 - e^{-s(T_s - T_t)}}{s} \tag{21}$$

The RC sampler's gain, from Fig. 15, is

$$|H(s)| = |H_1| \left(|H_2||H_{3'}| + G_{track}\right) = |H_1| \left(|H_{3'}| + G_{track}\right), \tag{22}$$

using $|H_2| = 1$. As discussed earlier, the samplers DC gain must be 1. At DC, the gain is

$$|H(0)| = |H_{3'}(0)| + G_{track} = 1 \tag{23}$$

The DC gain of $H_{3'}$ is

$$H_{3'}(0) = \frac{\frac{d(1-e^{-s(T_s-T_t)}}{ds}\Big|_{s=0}}{\frac{d(s)}{ds}\Big|_{s=0}} = T_s - T_t \tag{24}$$

For the case $T_t = 0$, the G_{Track} branch in Fig. 15 is never active and the RC-samplers gain is determined by the hold-block. In this case the hold-blocks DC gain is $H_{3'}(0) = T_s$. In order to set the DC gain to 1, when $T_t = 0$, $H_{3'}$ is scaled by $1/T_s$. The hold-block's transfer function is

$$H_3(s) = \frac{1 - e^{-s(T_s - T_t)}}{sT_s}. \tag{25}$$

In order for $|H_3| + G_{track})$ to be 1 at DC with all T_t, G_{track} is set to

$$|H_3(0)| + G_{track} = 1 \Leftrightarrow \frac{T_s - T_t}{T_s} + G_{track} = 1 \Leftrightarrow G_{track} = \frac{T_t}{T_s}. \tag{26}$$

The frequency response of the RC-sampler, by combining H_1, H_2 and H_3, is

$$\begin{aligned} H_{sampler}(s) &= H_1(G_{track} + H_2 H_{3'}) \\ &= \frac{1}{RC} \frac{(1 - e^{-\frac{T_t}{RC}} e^{-sT_t})}{(s + \frac{1}{RC})(1 - e^{-\frac{T_t}{RC}} e^{-sT_s})} (\frac{T_t}{T_s} + e^{sT_s} \frac{1 - e^{-s(T_s - T_t)}}{sT_s}). \end{aligned} \tag{27}$$

Next, the RC-sampler's bandwidth is considered. Equation (27) shows that for $T_t = T_s$, the sampler's transfer function equals an RC response

$$H(s) = \frac{1}{RC} \frac{1}{s + \frac{1}{RC}}, \tag{28}$$

for which the half power bandwidth is

$$f_{-3dB} = \frac{1}{2\pi RC} = BW_{RC}. \tag{29}$$

Fig. 13, illustrates how the settling time of the circuit is slower compared a normal RC low-pass filter. It was assumed that, as a result of the slower settling, the bandwidth scales with T_t/T_s and the RC-sampler's bandwidth is

$$BW = \frac{T_t}{T_s} BW_{RC}. \tag{30}$$

3.2.2 RC-Sampler with Down-Conversion

The sampling mixer circuit in Fig. 10 does down-conversion, in addition to the track-and-hold sampling presented in the previous section. Fig. 17, depicts a circuit capable of sampling the input with the down-converting signals from Fig. 11. An equivalent signal flow graph is shown in Fig. 18, in which, the down-conversion is done with a separate mixer instead of multiplying the second branch with -1.

The transfer function of Fig.18, without the mixer, is now considered. Because the circuit is linear, inputs 1 and 2, in Fig. 19, can be considered separately. When an impulse is set to input 1 and input 2 is zero, the impulse response follows that shown in Fig. 13, except the capacitor is connected to ground also during S_{-1}. Impulse response of input 2 is identical. Because S_1 and S_{-1} are active for equal lengths, the effect of the second branch, discharging the impulse to ground also during S_{-1}, can be added to (27) by changing

$$H_{RC}(s) = H_{sampler}(s)|_{T_t = 2T_t} \tag{31}$$

The sampling mixer can now be modelled with the block diagram in Fig. 19, in which $H_{tot,RC}$ is

$$\begin{aligned} H_{tot,RC} &= (1 + e^{j\frac{T_c}{2}}) H_{RC}(s) = 2e^{-j\frac{T_c}{4}} (cos(2\pi f \frac{Tc}{4}) H_{RC}(s) \\ &= 2e^{-j\frac{T_c}{4}} (cos(\frac{\pi f}{2f_c}) H_{RC}(s)) \end{aligned} \tag{32}$$

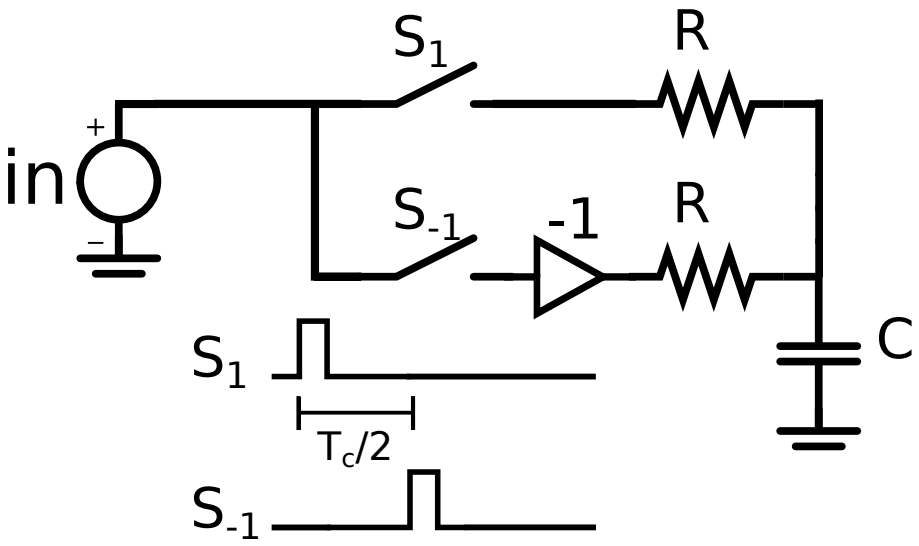


Figure 17: Circuit equivalent to Fig. 3.2

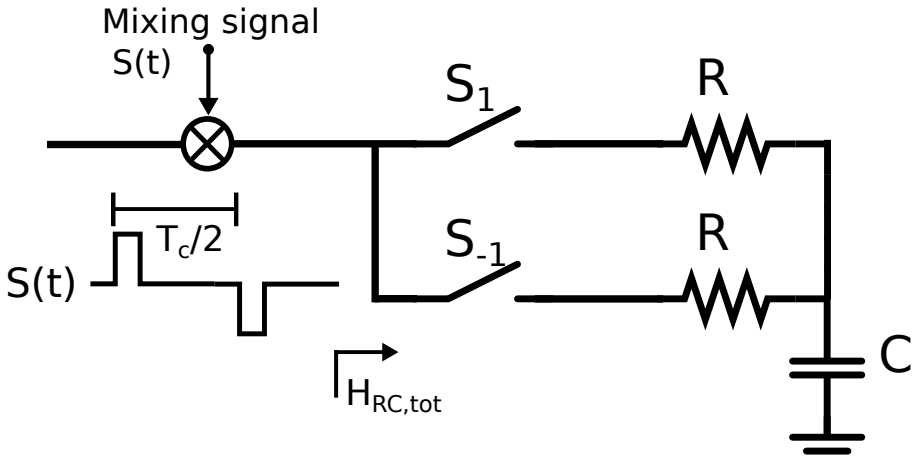


Figure 18: Circuit equivalent to Fig. 17, down-conversion done with a mixer.

Next, the conversion gain of the mixer is considered. The down-converting pulses can be constructed from impulses, shown in Fig. 20. The Fourier transform of an impulse chain repeating every T_s is

$$\sum_n \delta(t - nT_s) \xrightarrow{\mathscr{F}} \sum_n \delta(f - nF_s). \tag{33}$$

The spectrum of the impulses in Fig. 20 is

$$\begin{aligned} S_{imp}(j\omega) &= (1 - e^{-s\frac{T_c}{2}}) \sum_n \delta(f - nF_s) = 2e^{-j\pi\frac{T_c}{2}f} sin(\frac{\pi f T_c}{2}) \\ &= 2e^{\frac{-j\pi f}{2f_c}} sin(\frac{\pi f}{2f_c}) \sum_n \delta(f - nF_s) \end{aligned} \tag{34}$$

The length of the down-conversion pulses is T_t. This is modelled by multiplying $S_{imp}(j\omega)$ with a hold response, which was calculated for hold-time $T_s - T_t$ in 21.

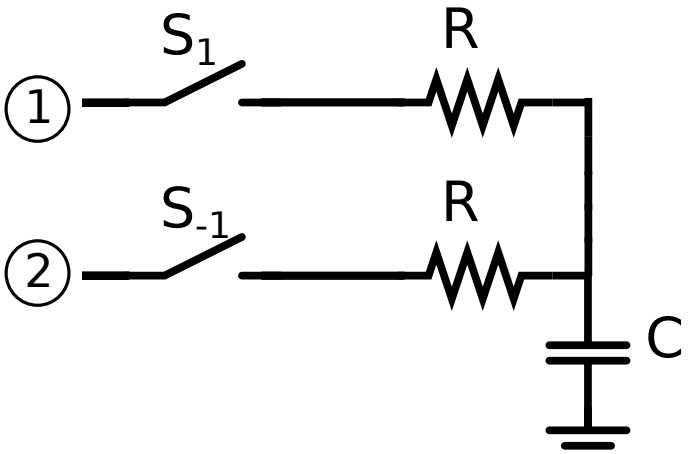


Figure 19: Circuit diagram for $H_{RC,tot}$

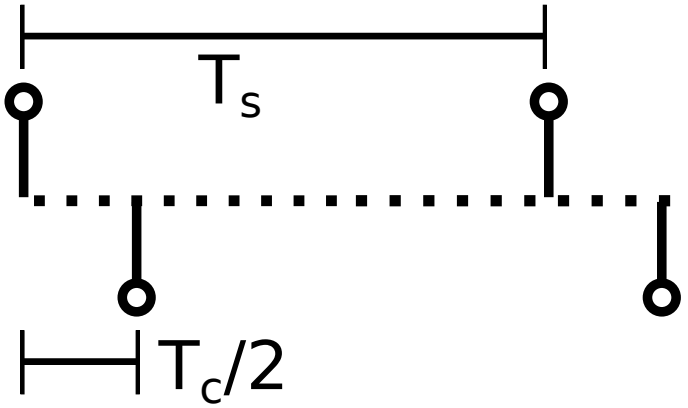


Figure 20: Impulses for modelling the down-converting signal.

With hold-time T_t, the hold response is

$$H_{hold}(j\omega) = \frac{1}{T_t}\frac{1 - e^{-j2\pi T_t f}}{j\omega} = \frac{e^{-j\pi T_t f} sin(\pi T_t f)}{j\pi T_t f}, \tag{35}$$

where the term $\frac{1}{T_t}$ scales the responses DC-gain to 1. The spectrum of the repeating down-converting pulse is

$$S(j\omega) = S_{imp}(j\omega) H_{hold}(j\omega) \tag{36}$$

The amplitude of S_{imp} at $f = f_c$ is 2. This results in a conversion gain of 1 from f_c to DC. The conversion gain is scaled by

$$|H_{hold}(j2\pi f_c| = \frac{sin(\pi \frac{T_t}{T_c})}{\frac{\pi T_t}{T_c}}, \tag{37}$$

which is the total conversion gain of the sampling mixer.

Using (31) and (30), the bandwidth of the sampling mixer is

$$BW = \frac{2T_t}{T_s} BW_{RC}. \tag{38}$$

These equations for the gain and bandwidth of the sampling mixer core are tested in chapter 4.

3.3 Theoretical Limits

This section describes limits for three parameters of the sampling mixer, maximum delays, maximum baseband bandwidth and highest usable down-conversion frequency.

Maximum delays that can be done with a time delay beam-steering system limit the array size and beam-steering angles. If we assume a rectangular antenna array, like in Fig. 2a, we can calculate the maximum distance between two antennas, i.e. the distance between elements in opposite corners of the array.

$$d_{max} = \sqrt{(Hd)^2 + (Kd)^2} = d\sqrt{H^2 + K^2}, \tag{39}$$

where H and K are the number of antennas in X and Y directions, respectively. Now, using (2), the relation between maximum delays, number of antennas, and maximum wanted beam-steering angle from the array normal, θ, is

$$\tau_{max} = \frac{d_{max} cos(\theta_{max})}{c}. \tag{40}$$

The maximum delays that can be done with the sampling mixer are defined by inverse of the sampling rate, as shown in Fig. 8b. The minimum sampling rate, which corresponds to the maximum delay, is limited by the Nyquist criterion. As discussed in section 3.1, the sampling mixer samples the down-converted baseband signal. The sampling rate is limited by the baseband signal bandwidth.

$$F_{s,min} = 2BW_{BB} \tag{41}$$

resulting in

$$\tau_{max} = \frac{1}{F_{s,min}} - \frac{T_c}{2} = \frac{1}{2BW_{BB}} - \frac{T_c}{2}, \tag{42}$$

where the term $\frac{T_c}{2}$ is the minimum length of the down-converting pulse.

The higher bandwidths require higher mixer sample rates, which puts a limit on the length of the delays. Limited delays result in limited array dimensions and beam-steering angles. Because the motivation for using true time delays in beam-steering was to enable the usage of large bandwidths, the upper limits of the bandwidth are now considered.

From (41) we get $BW_{max} = F_s/2$. For the down-conversion to work, the down-converting pulses must be spaced $T_c = 1/f_c$ apart, at minimum. In such a case the down-converting signal resembles the continuous square waves of Fig. 6b, resulting in

$$F_{s,max} = f_c, \tag{43}$$

$$BW_{max} = \frac{f_c}{2}. \tag{44}$$

In practice the bandwidth must be lower, in order to not limit the array geometry and beam-steering too much. Nonetheless, we can see that the sampling mixer allows the usage bandwidths increasing with the center frequency.

The upper limit to f_c, from the point of view of the sampling mixer core, comes from the switching speed of the mixer, Maximum operation frequency is also limited by the digital circuitry which creates the mixer control signals. These limitations are beyond the scope of this thesis.

The slowest switching speed is needed for pulses with 50 % duty-cycle. For signals like this, the time between closing the switches (making it conduct), and opening them, is $T_{cond} = T_c/2$. The smallest conducting time limits f_c by

$$f_{c,max} = \frac{1}{2T_{cond}} \tag{45}$$

If the sampling mixers need to support quadrature modulated data, there are benefits to using a maximum duty-cycle of 25% [12]. This halves the maximum f_c compared to (45).

The circuit model presented in section 3.2 uses ideal switches. For these, there would be no limit for decreasing T_{cond}. In a real IC implementation, the switches would be implemented with transistors. For the signal path, the transistor appears similar to the ideal switch and R_{sw} model from section 3.2. However, the control signals, connected to the transistor gate, see the transistor's parasitic gate capacitance. In order to change the gate voltage, which controls the switch, the parasitic capacitance must be charged or discharged. To make R_{sw} small, the transistor is made wider. This increases the gate capacitance and limits T_{cond}.

In traditional passive mixers, the circuits driving the switches are called LO buffers. They normally consist of a chain of inverters. Inverter chain theory is presented in [16]. To find the minimum conduction time for the switches, the shortest length of a pulse that goes through the chain, while retaining its shape, is considered. If we assume that buffer chains of each switch can be realized without delay mismatches, the time it takes for the pulse to go through does not matter.

The shortest pulse that goes through an inverter is limited by its driving strength and load. For an inverter loaded with the parasitic capacitance of the next inverter in the chain, this reduces to the ratio of their sizes. The transistor widths for minimizing the usable pulse length are

$$W_i = W_0^{iK}, \tag{46}$$

where K is the ratio of 2 consecutive inverters. The number of inverters in the chain are limited by area and power consumption. K is selected such that the last inverter in the chain can drive the load.

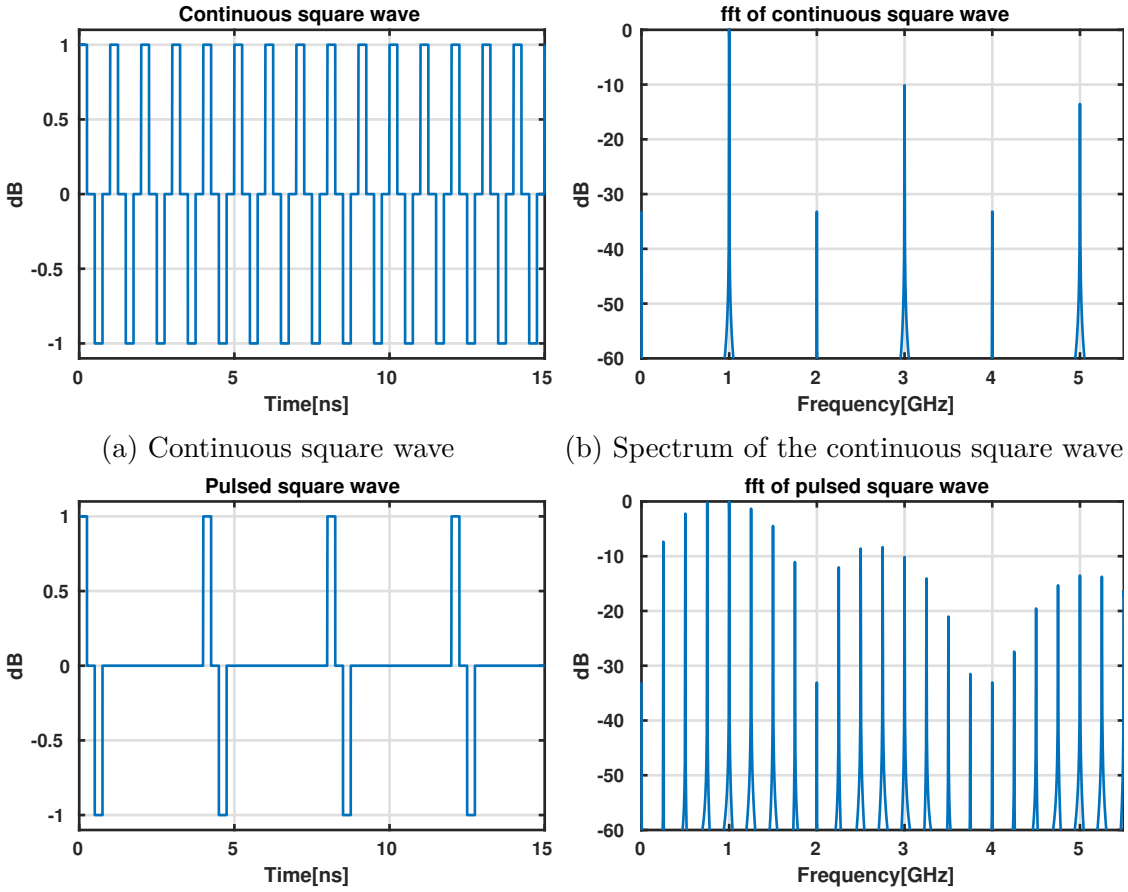
Simulations for determining an estimate for maximum f_c possible with this structure are presented in chapter 4.

3.4 Spectral Aliasing in the Sampling Mixer

This section describes an issue with the sampling mixer related to aliasing of unwanted spectral components on top of the desired baseband signal. A circuit topology for

negating these negative effects is also presented.

Section 3.1 mentioned that signal mixing can be done with square waves instead of pure sinusoids. Square wave type signals are used in the sampling mixer because they are easy to implement with transistor switches. It was also mentioned that the square waves have several spectral components. Fig. 21b shows the Fourier transformed spectrum of a square wave.



(a) Continuous square wave

(b) Spectrum of the continuous square wave

(c) Pulsed square wave

(d) Spectrum of the pulsed square wave

Figure 21

When we use this signal for mixing, we down-convert the input signal from each of the components, as shown in Fig. 6a for a single tone. This means that whatever is at these frequencies in the input is down-converted on top of the wanted baseband signal which originates from around the selected RF frequency f_c. These unwanted spectral components can be divided into signals from other radio transmitters and noise.

Noise that appears in the sampling mixer input is wideband thermal noise from the components that precede the mixer. These include at minimum the antenna, and possibly the LNA and filter show in Fig. 4. Thermal noise in the antenna at any frequency band is

$$V = \sqrt{4RkTBW}, \tag{47}$$

where R is the resistance of the antenna, k is the Boltzmann constant, T is temperature of the antenna in Kelvins and BW is the width of the frequency band.

Resistive components and transistors create wideband thermal noise. This is also the case for the band-pass filter in Fig. 4. The filter can't be used to filter its own thermal noise from outside its pass band. Thus, there is always thermal noise at all frequencies in the sampling mixer inputs. This noise is down-converted to baseband and this increases the receivers noise figure (NF). NF is defined as the degradation of signal-to-noise (SNR) ratio inside a component or a receiver chain. In decibels it is

$$NF = SNR_{in} - SNR_{out}. \tag{48}$$

The thermal noise at the input of the sapling mixer will be down-converted to the baseband from the frequencies of the spectral components of the down-converting signal, thus degrading NF

The sampling mixer utilises pulsed square waves show in Fig. 6b. The spectral content of these signals was analyzed in (49) as

$$S(j\omega) = 2e^{\frac{-j\pi f}{2f_c}} sin(\frac{\pi f}{2f_c}) \sum_n \delta(f - nF_s). \tag{49}$$

When considered without the sum term, the absolute value of $S(j\omega)$ is a function of $sin(\frac{\pi f}{2f_c})$. This has amplitude maxima at frequencies $\{F_c, 3F_c, 5F_c...\}$ and minima at $\{0, 2F_c, 4F_c...\}$. The sum term makes a copy the spectrum every F_s.

For $F_s = F_c$, $S(j\omega)$ is a continuous square wave and its spectrum is shown in Fig. 21b. When $F_s < F_c$, additional components appear in the spectrum. The time domain waveform and spectrum for case $F_s = F_c/4$ are depicted in Fig. 21d. As the sampling mixer multiplies the input with the pulsed square wave frequency components of Fig. 21d, at frequencies other than $f = F_c = 1GHz$, result in down-conversion from these unwanted frequencies.

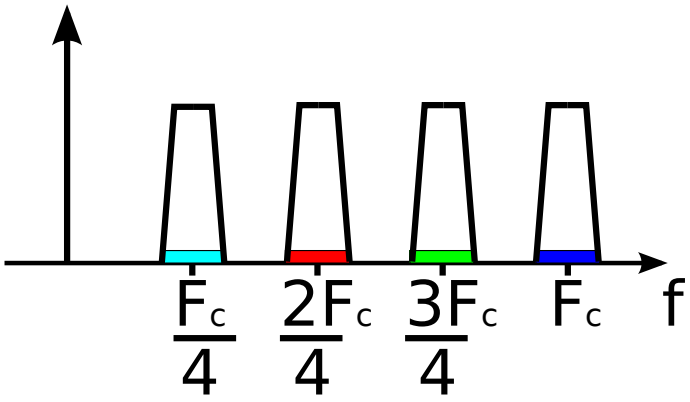


Figure 22: Alias frequencies of H_{RC}.

The issue can also be analyzed with the circuit from Fig. 18 using the transfer function for the ideally down-converted baseband signal:

$$H_{tot,RC} = 2e^{-j\frac{T_c}{4}}(cos(\frac{\pi f}{2f_c})H_{RC}(s)), \tag{50}$$

where $H_{RC}(s)$ is the transfer function of the RC-sampler for the parallel case, of (31). Sampling operation in $H_{RC}(s)$ aliases spectral components from bands with width BW_{RC} centered at every multiple of F_s as illustrated in Fig. 22 for $F_s = F_c/4$. [13]

The term $cos(\frac{\pi f}{2f_c})$ in (50) creates a notch in the frequency response at frequencies $\{F_c, 3F_c, 5F_c...\}$. Fig. 23 depicts the frequency response of $H_{tot,RC}$. The response resembles the spectrum of the pulsed signal of Fig. 21d, with a frequency shift of F_c caused by the ideal mixing of Fig. 18.

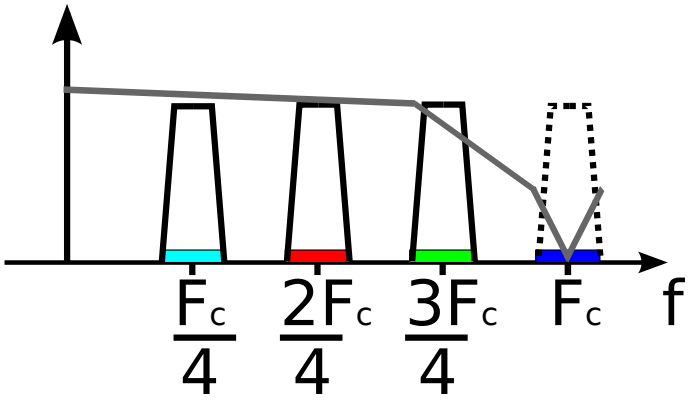


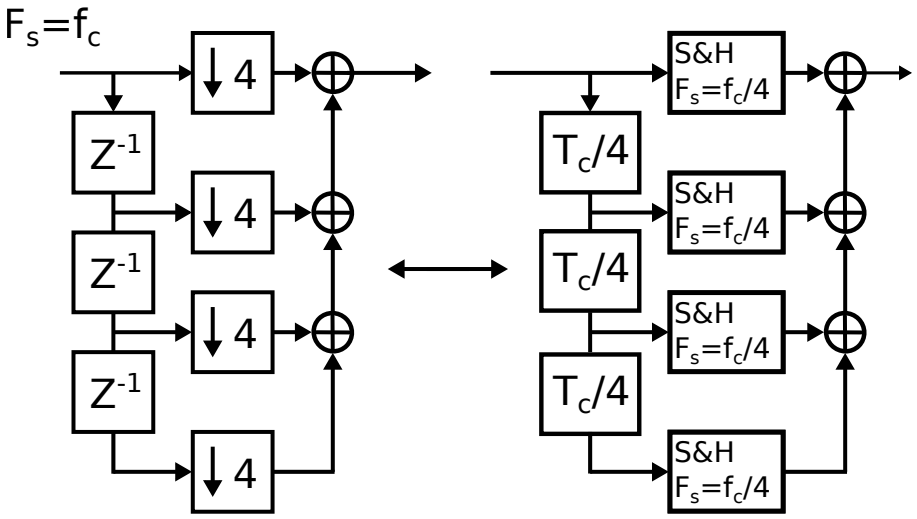
Figure 23: Alias frequencies of $H_{tot,RC}$.

The remaining alias frequencies can be negated by creating additional notches on multiples of F_s below F_c. The effect can be achieved by using a digital polyphase decomposition filter structure, depicted in Fig. 24a [13]. The topology on the right is an equivalent analog version of the same filter, which can be implemented with parallel sampling mixers. In both cases the delays, z^{-1} on the left and $T_c/4$ on the right are one quarter of the sampling period of the output. On the left, the sample rate changes from f_c to $f_c/4$. In the analog version the sample rate is continuous in the input, and $F_s = f_c/4$ after the samplers.

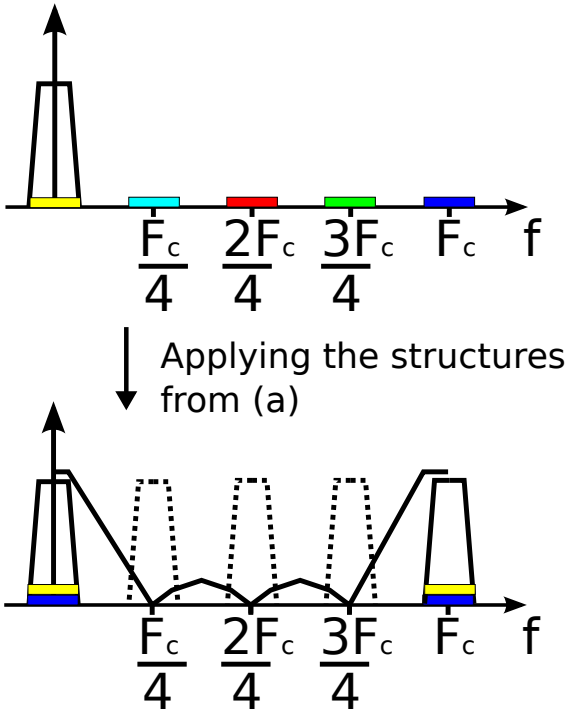
Fig. 24b shows the output spectrum after the input has been sampled with the presented topologies. The frequency notch created with the filter structures is shown as the black line in Fig. 24b. Combining frequency responses of figs. 23 and 24b results in a structure, in which no spectral components below $2F_c$ are aliased on top of the baseband.

Implementing the analog filter structure from Fig. 24b with parallel sampling mixers is now described. For the case of $F_s = f_c/4$, the implementation has 4 sampling mixers in parallel, per antenna. The delay blocks of $T_c/4$ cane be done by delaying the sampling times of the mixers. Because the mixers already support this, no additional hardware is needed for the delays.

Fig. 25 shows the parallel mixers connected to one antenna, an implementation of 24a. The circuit looks more complicated now, but there are no major downsides in having to add more mixers. They are fairly simple and don't consume much chip area. Power consumption stays also acceptable. In this configuration, there are N sampling mixers in parallel, each with a sampling rate of f_c/N. This means that a sampling pulse, one period of a square wave at f_c, needs to be delivered to



(a) Digital polyphase decimation filter (left), and an analog equivalent (right)



(b) Output spectrum of the filter structures of (a). Notches are created in the frequency response.

Figure 24

each mixer every Nth T_c. Activating the switch drivers like this, makes the total power consumed in switch buffering in the aliasing compensated sampling mixer configuration, equal to LO buffering for a traditional passive mixer.

For more than one antenna, the parallel mixers are connected as shown in Fig.

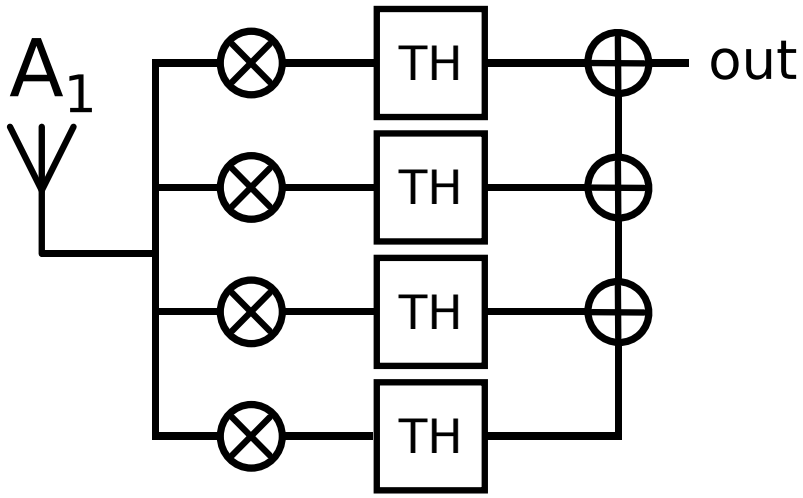


Figure 25: Aliasing compensation setup for 1 antenna. Maximum delay is $4T_c$.

26. The example shows the mixers needed to do the compensation for 4 antennas and maximum delay of $4T_c$. In the figure, each circle with an X inside, represents a sampling mixer core circuit from section 3.2. The other circles are ideal analog summations and the TH blocks are ideal track-and-hold samplers for the re-sampling. The different colors represent the branches from Fig. 24a

The delays between consecutive branches are $T_c/4$, while the delays for each antenna, τ_i come from beam-steering. This means that each mixer samples with delays

$$\tau_{i,k} = \tau_i + \frac{kT_c}{4}, k = [0, 1, 2, 3], \tag{51}$$

where k is the number of the branch. The re-samplers are also not clocked at the same time. They have the same branch delays of $(kT_c)/4$.

Fig. 27 shows the top level block diagram for the receiver with the aliasing compensation.

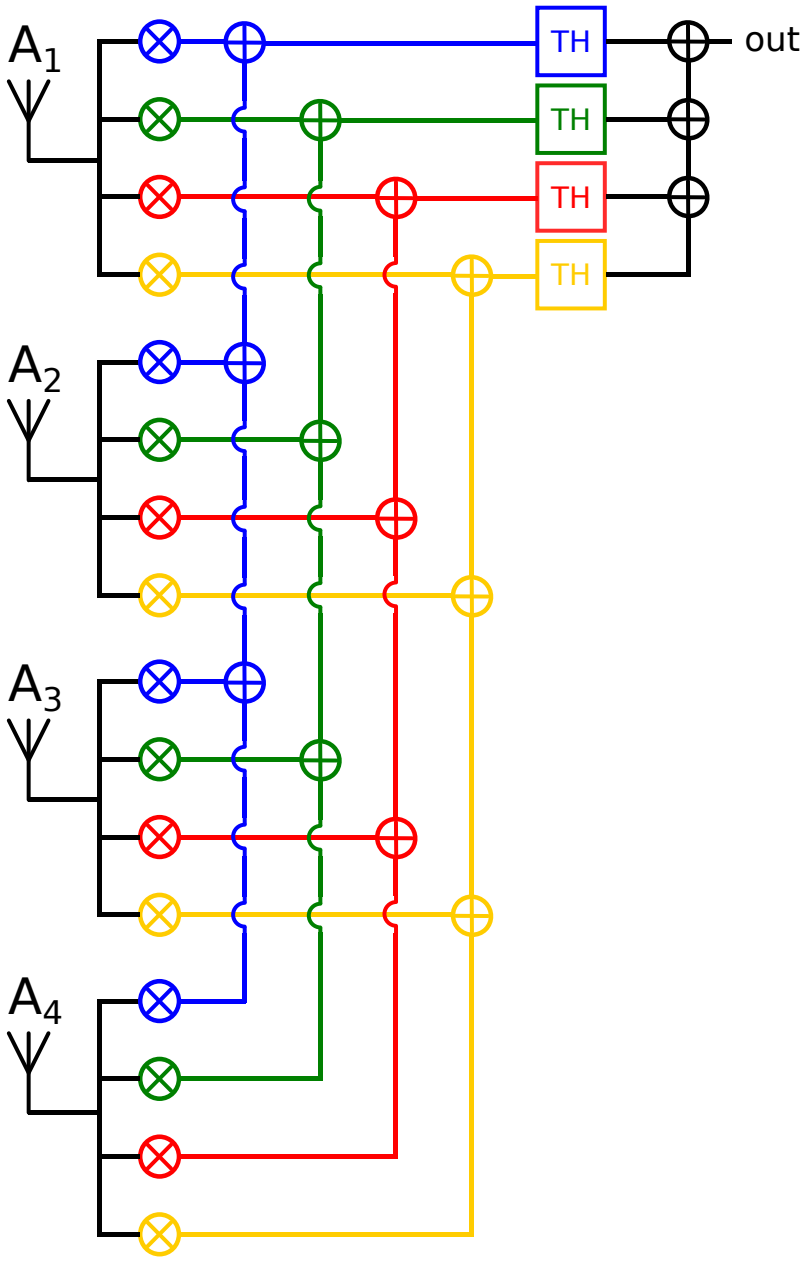


Figure 26: Aliasing compensation setup for 4 antennas and maximum delay of $4T_c$.

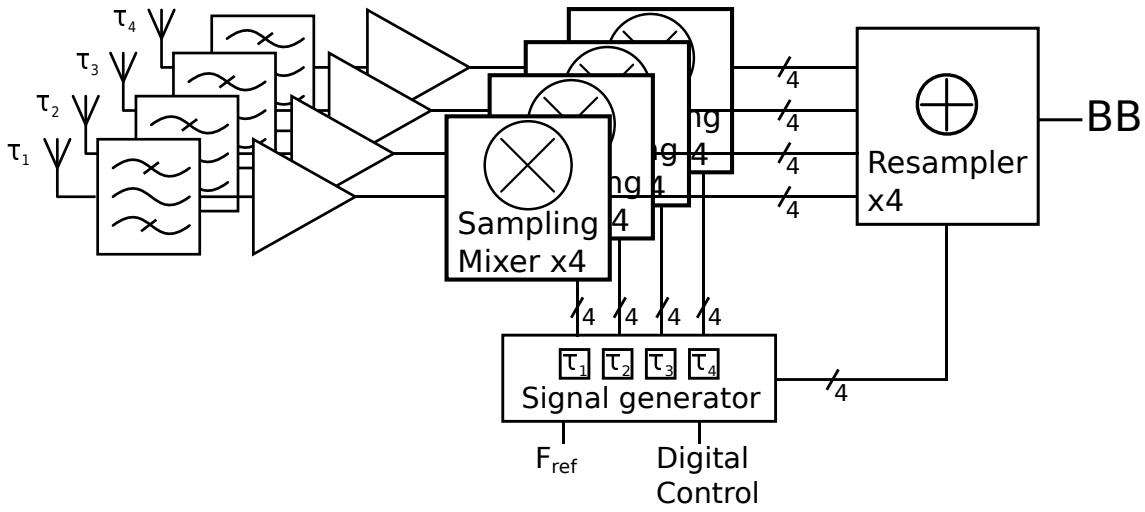


Figure 27: Receiver chain with aliasing compensation

4 Simulation Results

This chapter presents the simulations performed while studying the sampling mixer concept. The aim of the simulations was to verify the the functionality of the receiver concept, and to study the effects of the parameter adjustments. The simulations were done with Mentor Graphics' Eldo simulator.

4.1 Maximum Switching Speed

As describes in section 3.3, the maximum usable f_c with the sampling mixer concept is limited by the switch driver circuit. In order to find an estimate for this limitation, circuit simulations were done for a chain of 20 inverters which had a transistor's gate node as its load. The simulation was done using a 28 nm FD-SOI CMOS library.

The first inverter in the chain is a minimum size inverter and the sizes of the following inverters are scaled according to (46), with K=1.25. The size of the load transistor is, such that it represents a switch switch in Fig. 10 with $R_{sw} = 20\Omega$.

Fig. 28 depicts the chain when its driven with a 20 ps pulse. Simulations showed that this was the shortest length pulse that goes through the chain without distortions in its length. It is concluded that the upper limit of frequency range with the sampling mixer is 25 GHz for a 50 % duty-cycle switching scheme and 12.5 GHz for a 25 % scheme.

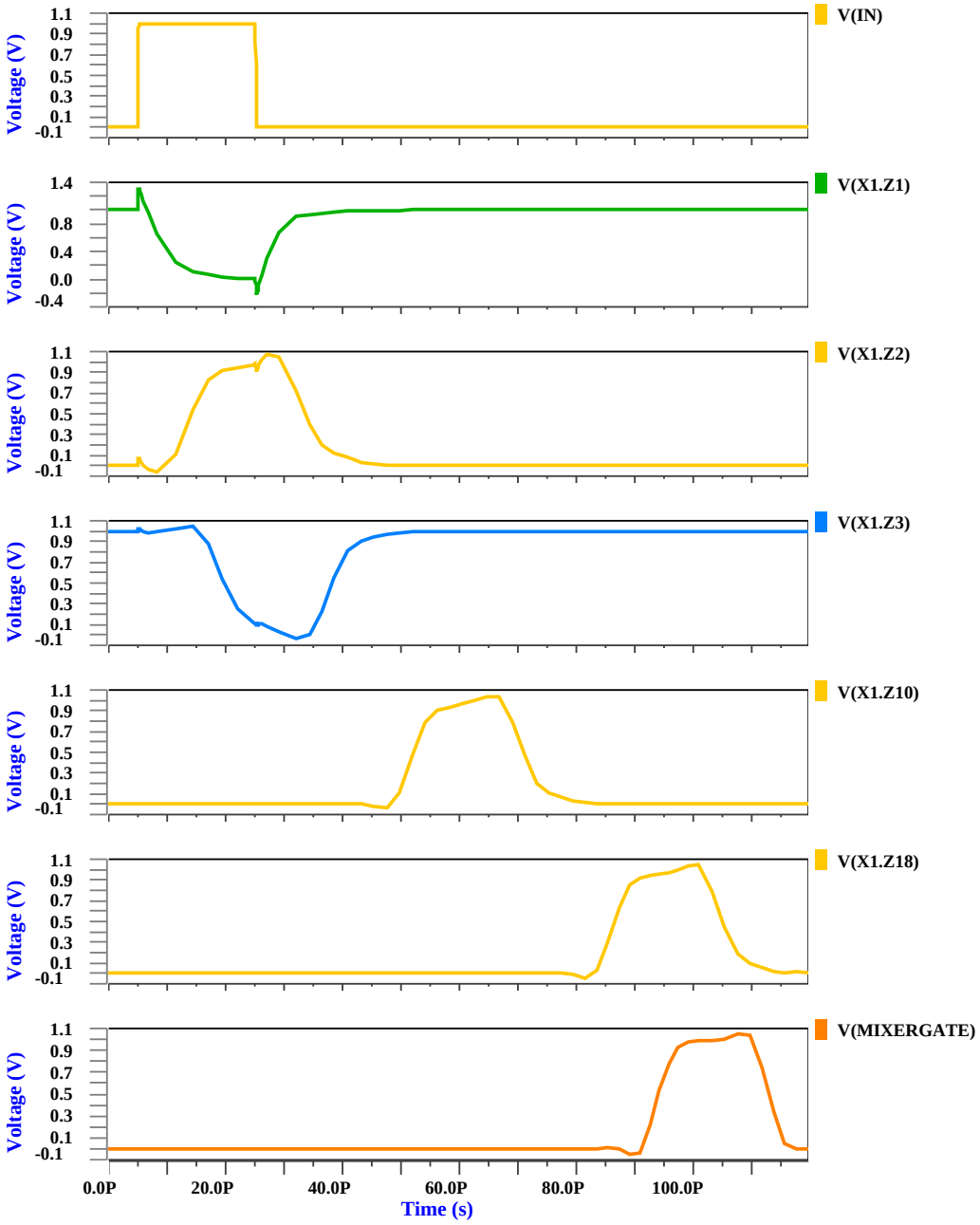


Figure 28: Switch driver simulation.

4.2 Mixer Core Frequency Response

The simulation setup corresponds to the setup presented in Fig. 10. All resistances have a value of 20Ω. The frequency response was measured by comparing the amplitudes of input and output waveforms. This type of frequency response, where the input is at RF frequency and the output at baseband is often called conversion gain. The signal frequencies used in the simulation are as follows. Input tone $f_{in} = 3.01GHz$, down-conversion frequency $f_c = 3GHz$. These give an output frequency of 10 MHz.

The effect of T_t on the gain was presented in (37). This dependency was confirmed by a simulation that compared the gain to T_t. Because the bandwidth is affected by T_t as described in (38), the bandwidth was selected to be 1 GHz: high enough that there is no suppression at the baseband frequency of 10 MHz with the longest T_t. From (29) we get the value of the capacitor to be 1.33 pF.

The results of the simulation are presented in Fig. 29. The blue stems are the simulated gains with different T_t. The orange line shows the theoretical line from (37), for reference. From this result it can be concluded that the equation does represent the effect of the ratio of T_t and T_c on the sampling mixer gain.

The discrepancy in the theory and simulation result at larger T_t/T_c can be explained as follows. The input signal at f_{in} is also up-converted to $f_{in} + f_c$ as explained in section 3.1. With longer T_t the bandwidth of the sampling mixer is larger as expressed in (38). Wider bandwidth means that components at higher frequencies are suppressed less. The output signal is a superposition of the wanted baseband signal and the up-converted signal. Because we simply extract the maximum of the output, the smaller filtering at higher T_ts is visible as increased gain.

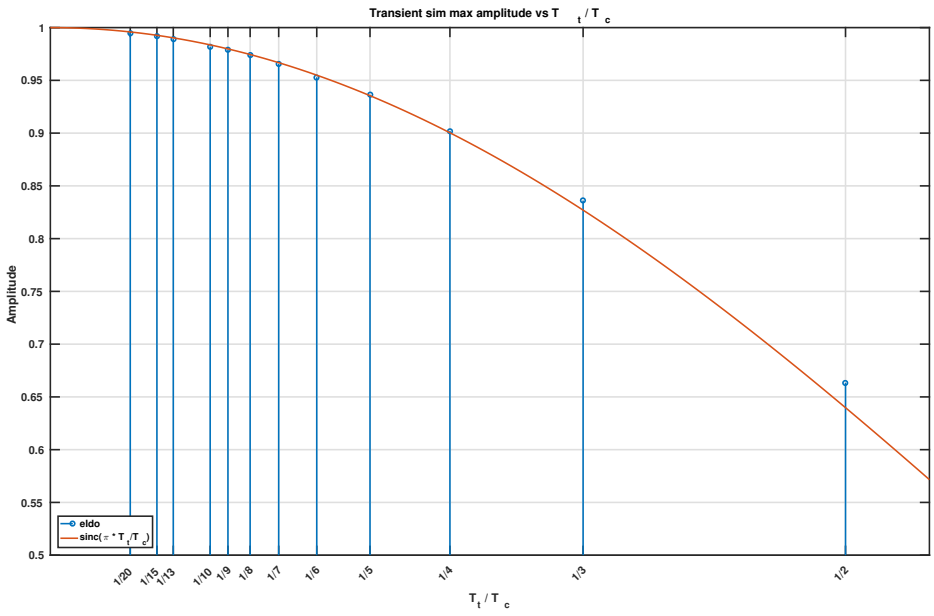


Figure 29: Mixer core gain vs T_t

The effect of the sampling rate factor N, defined as $N = \frac{F_c}{F_s}$, was also studied and found to be negligible. Fig. 30 shows the lack of affect that changing the sampling rate has on the gain of the mixer core. The gain was simulated for three sampling factors $n = 1, n = 5$ and $n = 10$. The case $n = 1$ is equal to driving the mixer with a continuous square wave.

In this simulation, the bandwidth was scaled with N to ensure the output signal is not attenuated by the RC filtering. The bandwidth was scaled by changing the value of the capacitor to be $C = NC_0$.

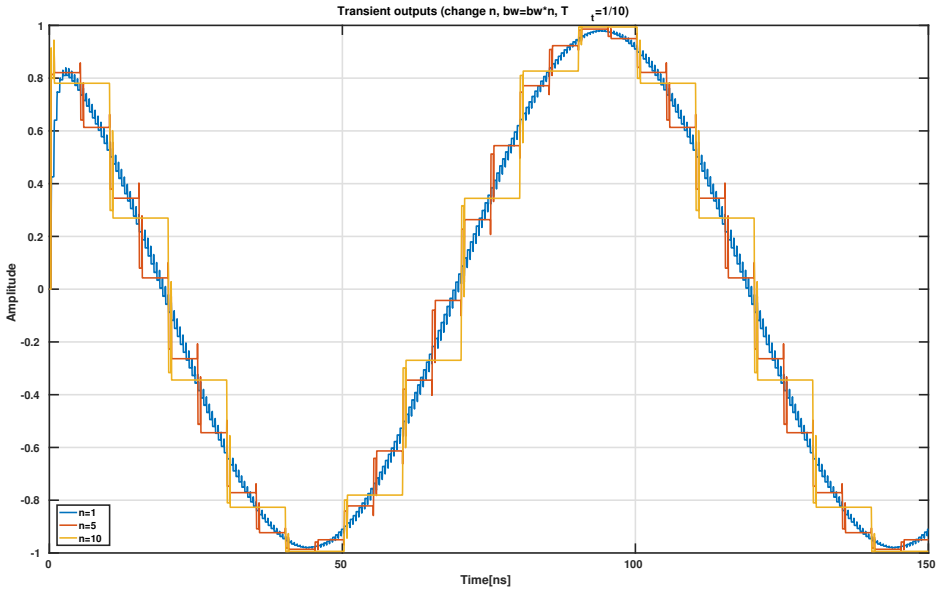


Figure 30: Mixer core gain vs sample rate

4.3 Sampling Mixer Bandwidth

The simulations presented in this section were performed to study the effects of T_t/T_c and the sampling factor N on the bandwidth. As discussed in section 3.2, the bandwidth of the sampling mixer core is defined by the RC response, formed by the switch resistor and the sampling capacitor, and, by the ratio of time that the switches conduct. The simulation setup is similar to the one used in section 4.2 and shown in Fig. 10.

First, the effect of the T_t/T_c relation on the baseband bandwidth of the sampling mixer core is performed by sweeping the offset of the input from the down-conversion/carrier frequency. The input frequency is defined as

$$Fin = f_c + f_{sig}. \tag{52}$$

f_c is set to 3 GHz and the simulation sweeps f_{sig} from 10 MHz to 1 GHz with a resolution of 15 steps per decade.

The bandwidth is determined by finding the -3 dB frequency. In order to do this, the gain of the mixer needs to also be split into two

$$G = G_{TH}G_{lp}, \tag{53}$$

where G_{TH} is the gain caused by the track-and-hold operation (equation (37)) and G_{lp} is the loss from the RC low-pass filter. In (38), the bandwidth of the filter was predicted to depend on the T_t/T_c relation.

This is demonstrated in Fig. 31. Its x-axis is the frequency offset/baseband frequency f_{sig} and the y-axis is the conversion gain in Decibels from frequency $f_{sig}+f_c$ to baseband. The RC -3 dB frequency of equation (29) was set to $f_c/2 = 1.5GHz$.

It is assumed that G_{lp} doesn't affect the total gain at $f_{sig} = 10MHz$. This allows the frequency point, where $G_{lp} = -3dB$ to be calculated as the frequency where

$$G = G_{TH}(f = 10MHz) - 3dB. \tag{54}$$

These -3 dB frequencies were extracted and are compared to theory presented in section 3.2 in table 4.3.

T_t/T_c	-3 dB point from simulations	-3 dB point from (38)
1/2	740 MHz	750 MHz
1/4	437 MHz	375 MHz
1/10	157 MHz	150 MHz

Some of the discrepancies between the simulations and theory visible in the table 4.3 can be explained by the limited number of frequency points in the simulation, and overall, it can be concluded that the simulations do follow the theory.

Another simulation was performed to study the dependency of the bandwidth on the sample rate, described by the sampling factor N. In this simulation, $T_t/T_c = 1/10$, but otherwise it's similar to the previous bandwidth simulation. The results are shown in Fig. 32.

For the selected parameters G_{TH} is approximately -0.1 dB. Because N doesn't affect gain, it is sufficient to find the frequency where the total gain drops to -3.1 dB for each case. The fact that there is already noticeable filtering for the case $N = 10$ at 10 MHz doesn't need to be considered, as was the case in the previous simulation. The extracted frequencies are in table 4.3. These results also follow (38).

N	-3 dB point from simulations	-3 dB point from (38)
1	303 MHz	400 MHz
2	155 MHz	150 MHz
5	62 MHz	60 MHz
10	32 MHz	30 MHz

The unexpected behavior of the curves $N = 5$ and $N = 10$ at high frequencies is caused by the input frequency increasing over the Nyquist limit. For example, in the $N = 10$ case, the sampling rate is $f_c/10 = 300MHz$ which should be two times higher than the down-converted signal. The first data point that shows the gain increasing is at a frequency of over $200MHz > 300/2MHz$.

In conclusion, the bandwidth of the sampling mixer consists of an RC low-pass response, with the -3 dB frequency scaled as predicted by (38).

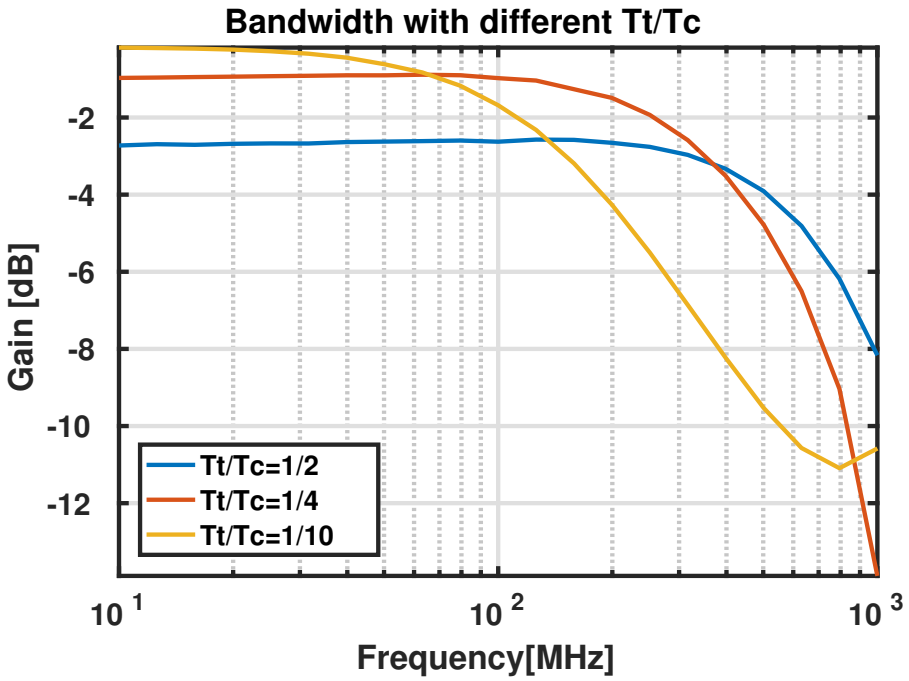


Figure 31: Bandwidth versus T_t/T_c

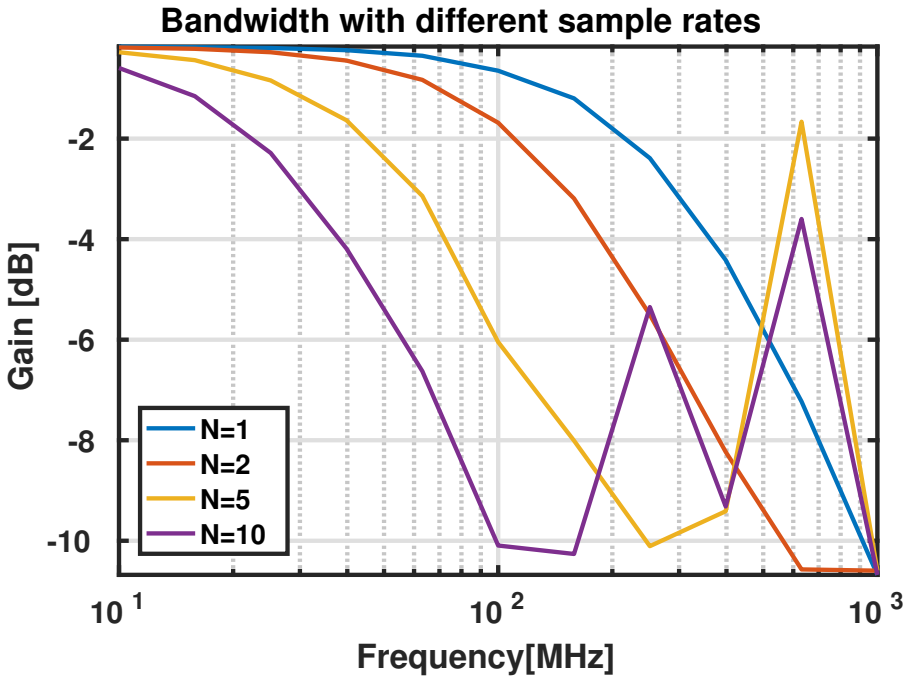


Figure 32: Bandwidth versus sampling factor N

4.4 System Demonstration Simulations

The previous simulations were carried out for a single sampling mixer core. This section demonstrates the operation of a receiver chain built from multiple cores. The simulation setup, shown in Fig. 33, consists of 4 sampling mixers, whose outputs are connected to an analog summation and a re-sampler at the output of the sum. Eldo macro models for analog sum and track-and-hold sampling were used.

The first simulation in Fig. 34 shows how the receiver can be used to combine pulses coming to the inputs of different mixers with delays of over $T_c = 1/1GHz = 1ns$ between them. A pulse with amplitude 0.5 V arrives to the first mixer at time $t = 0$ and the following mixers receive the same pulse after consecutive delays of 1 ns. The re-sampler output shows the sum of these pulses after the re-sampling time at $t = 4.9ns$. Similarly the next set of 1 V pulses is summed at the output. It can be seen that the signals with the delays are summed coherently, as expected.

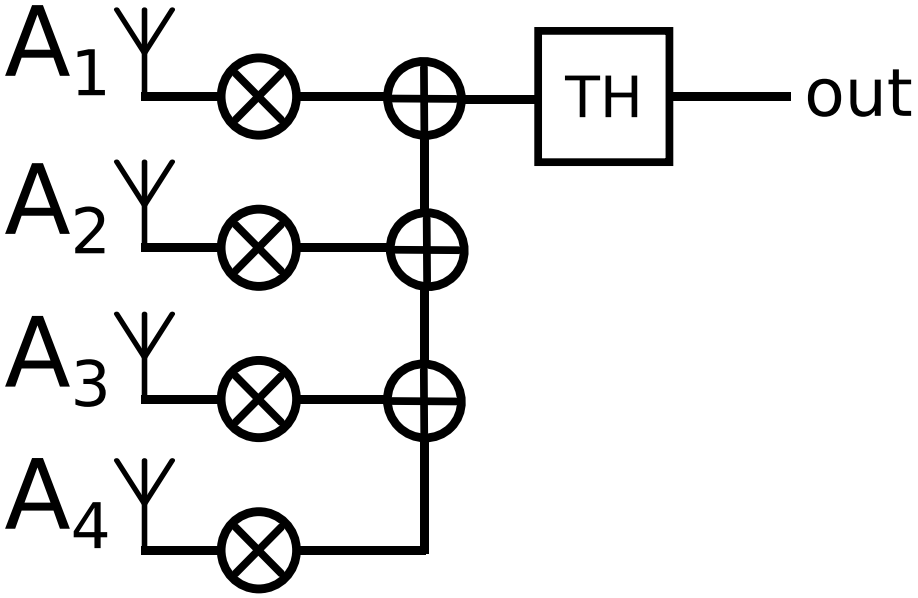


Figure 33: Receiver setup for 4 antennas.

The next simulation was carried out to demonstrate how the signal propagates through the receiver chain. The simulation setup consists of two sampling mixers: it is identical to Fig. 33, but with only 2 antennas and mixers. The antennas have an input signal with amplitude 0.5 at $f_{in} = 3.01GHz$ and the selected down-conversion frequency is $f_c = 3GHz$. The second input is delayed by $3T_c$. The signal at mixer outputs should be at 10 MHz and the combined re-sampler output should have an amplitude of 1.

Fig. 35 depicts waveforms at the inputs of the mixers, the mixer outputs, the control signals for their switches, the analog summation of the mixer output, the re-sampler output and it's control signal. The figure shows how the mixer and re-sampler control signals are timed with respect to the input signal. Fig. 36 shows the simulation with a longer time scale. From this, it can be seen that the mixer and

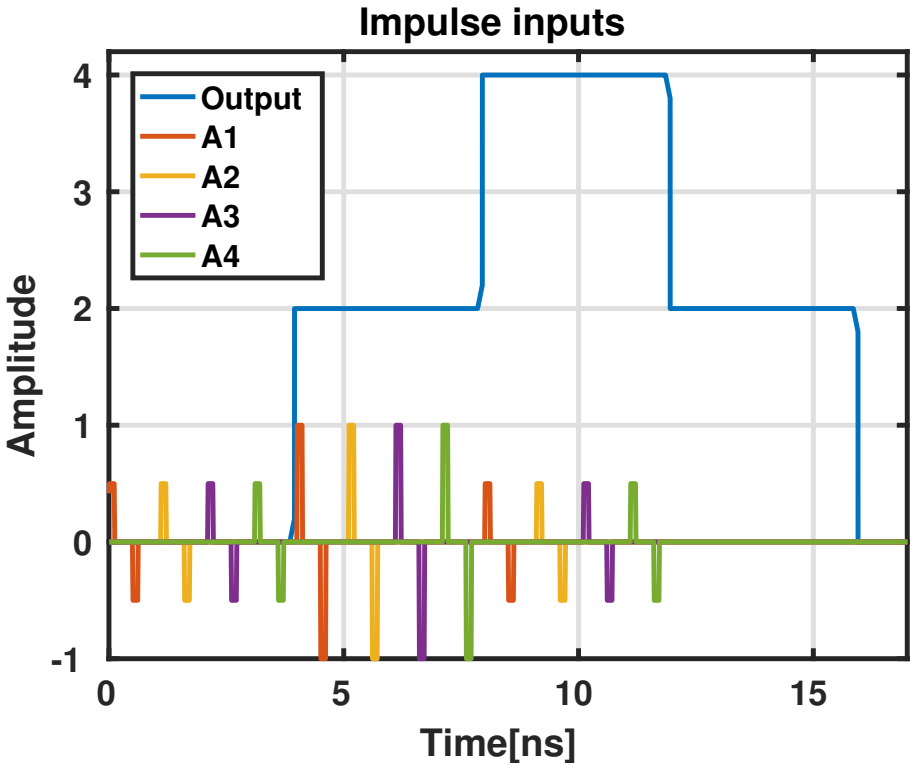


Figure 34: Coherent summation of delayed inputs.

re-sampler outputs are at the wanted frequency and the re-sampler output amplitude is close to 1.

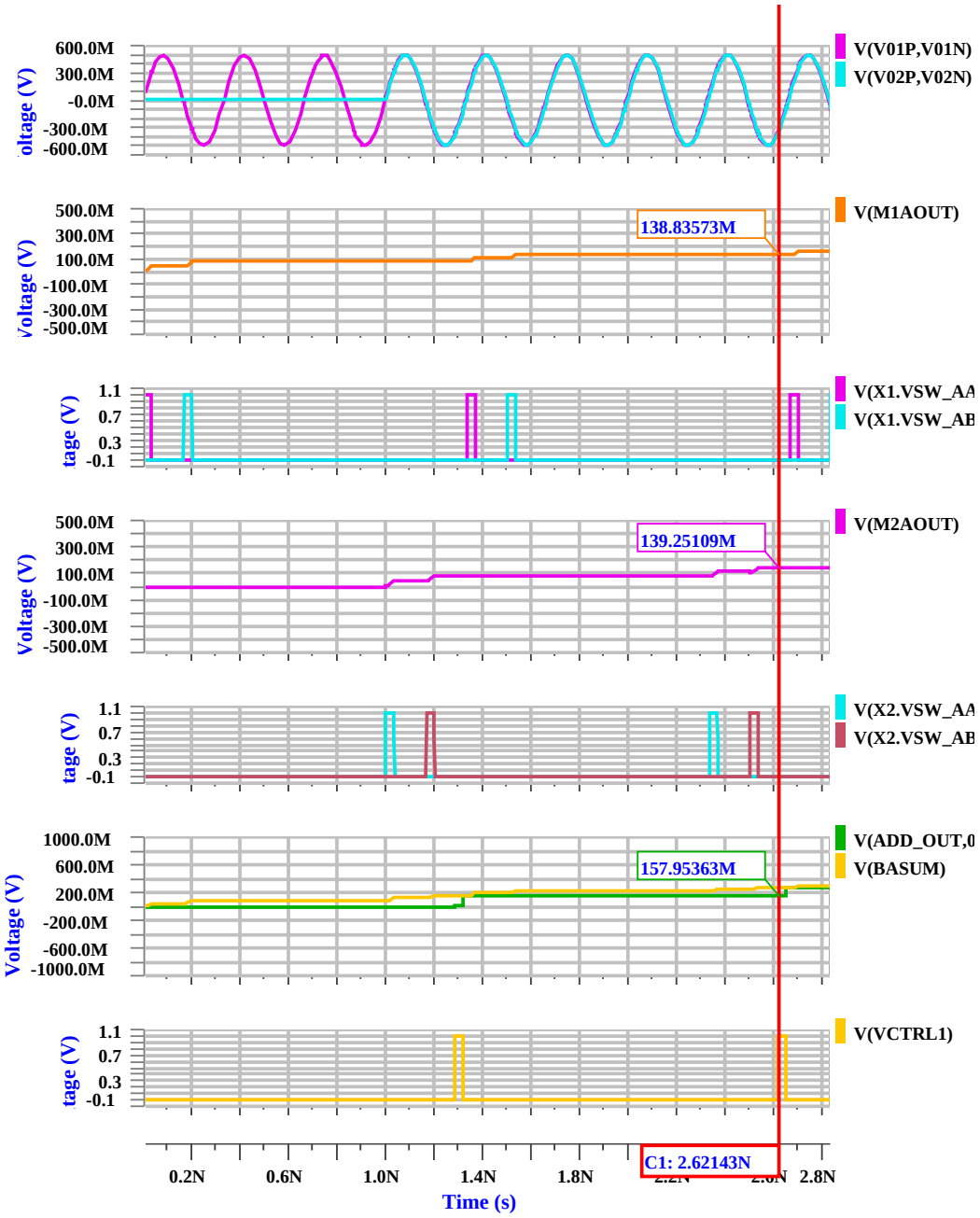


Figure 35: Simulation for demonstrating the operation of a sampling mixer receiver. The waveforms plots are, from top to bottom, as follows. 1: Input signals of the antennas. 2: Mixer 1 output. 3: Mixer 1 control signals. 4: Mixer 2 output. 5: Mixer 2 control signals. 6: Analog sum of the mixer outputs (yellow) and re-sampler output (green). 7: Re-sampler control signal.

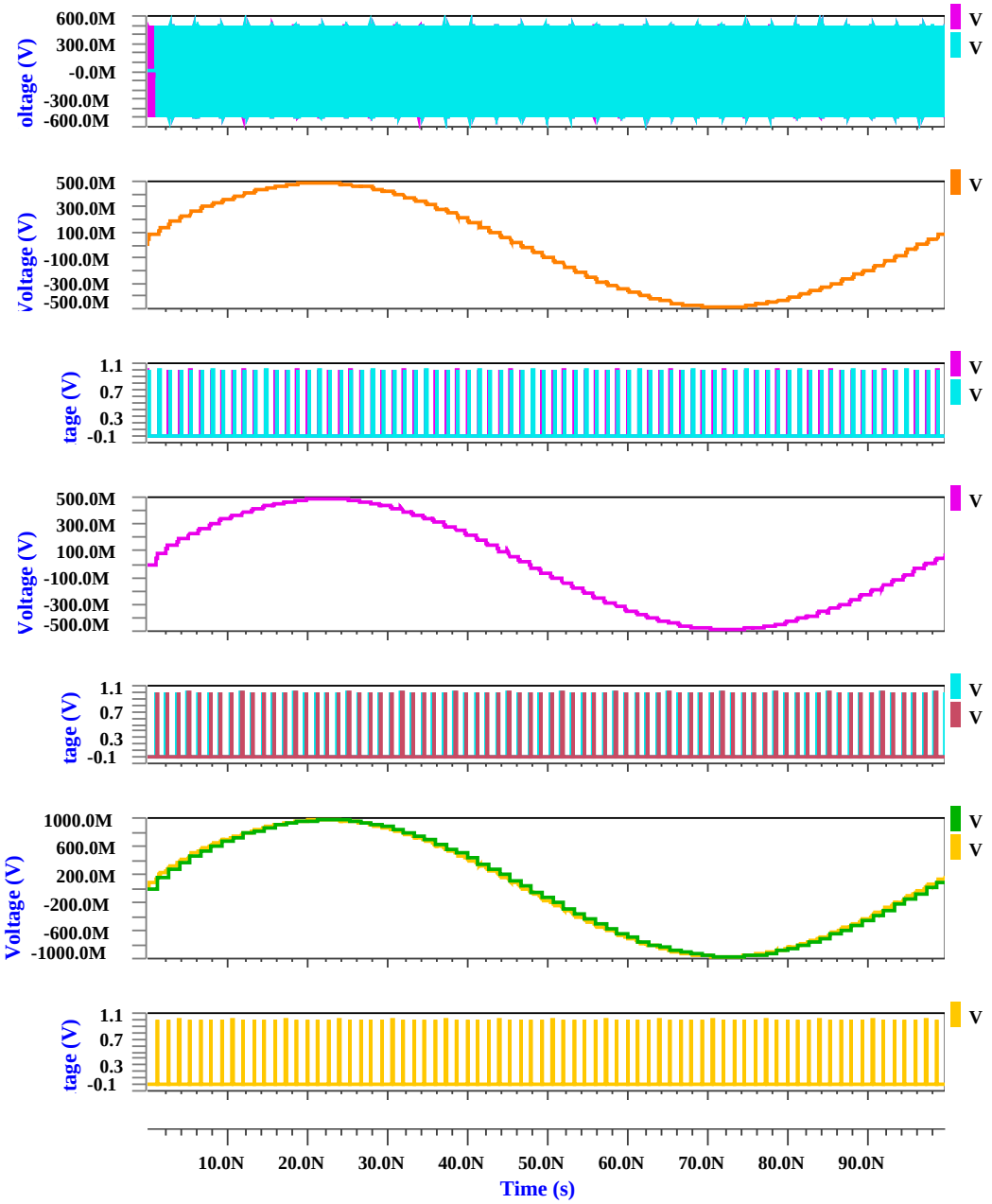


Figure 36: Zoomed out view of Fig. 35

4.5 Aliasing

In this section, the problem with spectral components from unwanted frequencies being down-converted to baseband, and the proposed compensation circuit are studied.

The conversion gain of one mixer from various frequencies is shown in Fig. 37. The simulation setup is the circuit from Fig. 10. As in section 4.3, the input frequency is divided into $Fin = f_c + f_{sig}$. The carrier frequency is swept from 1 GHz to 9 GHz . However, in this simulation the down-conversion frequency doesn't follow f_c. It remains at 3 GHz. So, we have an input signal with 10 MHz offset from the frequencies show on the x-axis. The y-axis shows the conversion gain from the input frequency. The sampling rate was $f_c/4$.

The simulation effectively reveals the aliasing problem, which must be circumvented in order to avoid severe degradation of the receiver noise figure. The frequencies which have down-conversion gain correspond to what was predicted for the pulsed mixing signal in Fig. 21.

To study the compensation circuit, the circuit from Fig. 26 was used to re-run the previous simulation. The result is similar to mixing with a continuous square wave. There is down-conversion from the fundamental frequency and the 3rd harmonic. It was concluded that the compensation circuit does work.

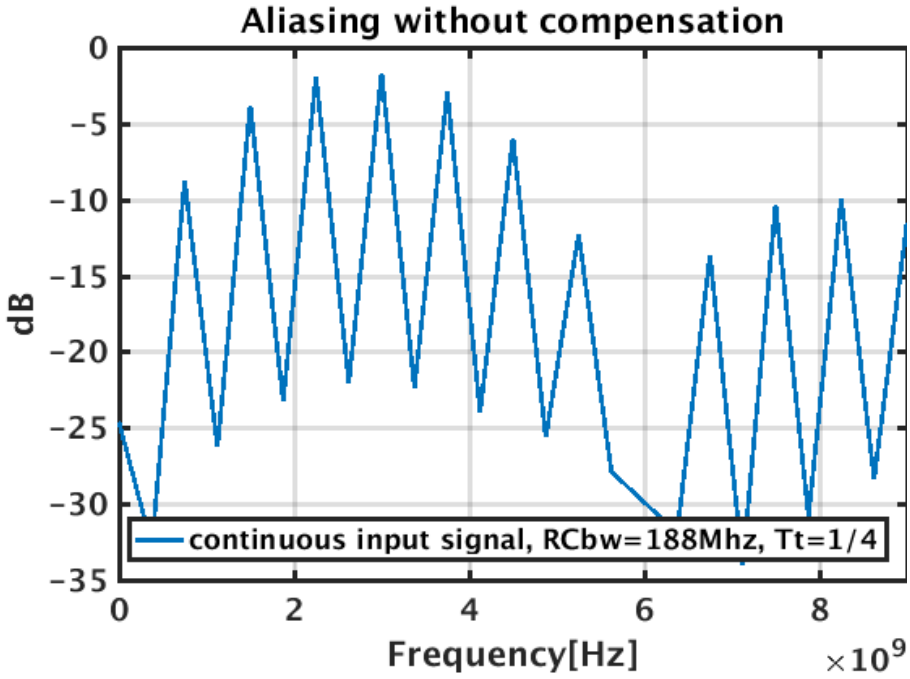


Figure 37: The aliasing problem. Conversion gain from the shown frequencies with selected down-conversion frequency of 3 GHz.

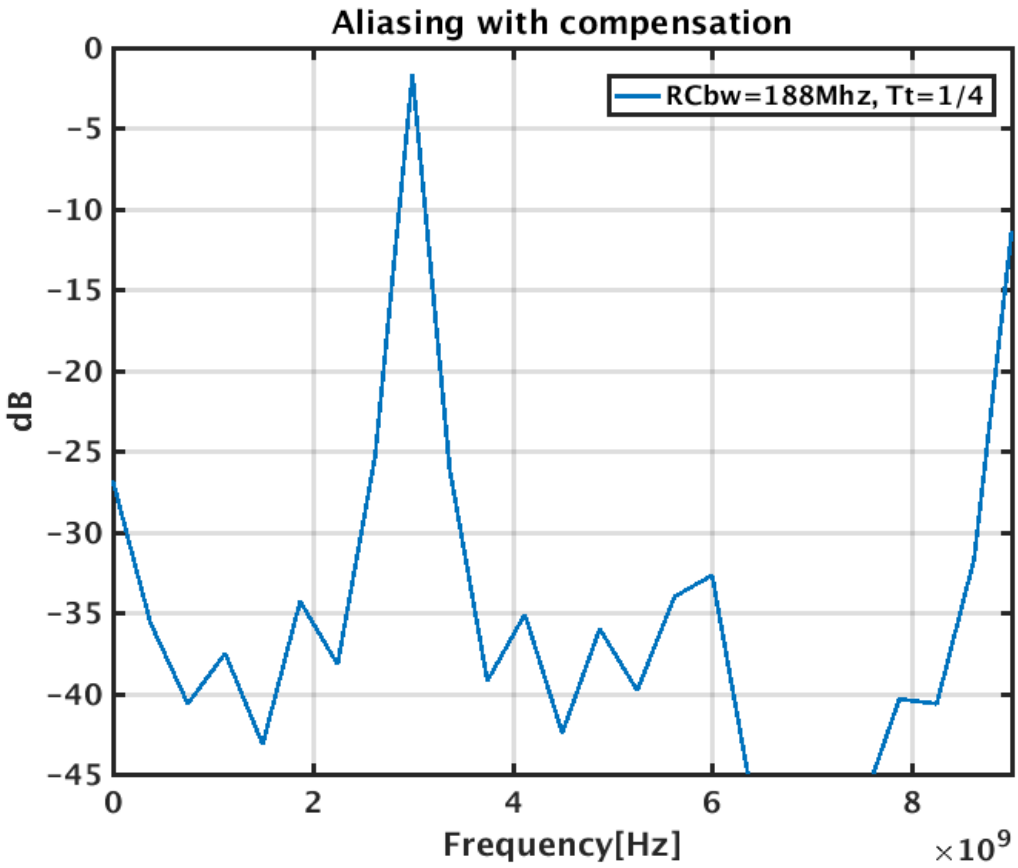


Figure 38: Aliasing with the compensation circuitry.

5 Conclusion

In this work, a receiver front-end structure for beam-steering multi-antenna arrays was studied. Introduction to beam-steering and the benefits of implementing it with time delays instead of phase shifts were presented.

A Matlab model for visualising time delay beam-steering was developed. The model computes and displays the array factor of an antenna array that receives or transmits with given delays between the antennas. It can be used to determine the effects of delay resolution and delay errors between the transmit/receive paths.

Sampling mixer concept is introduced to generate a true time delay receiver. The concept is made possible by current CMOS technologies that allow the creation of digital control signals for the mixer switches at RF frequencies. It is based on sampling the RF input with a down conversion pulse. The time delays and beam-steering are enabled by sampling different antenna inputs at different times and summing the samples coherently.

The sampling mixer operation is controlled with the signals controlling the mixing switches. These signals can be thought of as a continuous LO, with some of the pulses possibly skipped. The effects of pulse skipping was studied with Eldo simulations. Importantly, the conversion gain of the mixer was found to not be negatively affected by skipping LO pulses, which permits delays longer than one carrier cycle. Controlling the relative lengths of the down-conversion pulses (T_t/T_c) was studied and simulated. The effect of this on gain and instantaneous bandwidth of the mixer was found out. The baseband bandwidth also defines the band-pass response of the mixer at the RF input. All of the simulations were performed with ideal components.

Aliasing of noise and possible blockers was identified as a problem of the concept. To address this, an aliasing compensation circuitry was added. It consists of parallel mixer branches which sample the input with delays compared to the original branch. Combined power consumed in LO buffering in the branches is equal to a case of one mixer driven with a continuous LO. Adding the branches does not interfere with the beam-steering capability.

The concept was tested to work with up to 3.5 carrier cycles of delay between the antenna inputs. In theory, the concept doesn't limit the maximum delays as long as $\tau < 1/(2BW)$, but the circuits get more complex with longer delays. Increasing the delay by one cycle necessitates addition of 1 mixer per antenna and one re-sampler to the whole receiver.

In conclusion, the sampling mixer concept with aliasing compensation through polyphase decimation achieves the goal of allowing beam-steering with true time delays longer than one carrier cycle. The findings of this thesis support the feasibility of implementation of the sampling mixer concept.

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