

Failure Mechanisms of Lead-Free Chip Scale Package Interconnections under Fast Mechanical Loading

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The reliability of chip scale package (CSP) components against mechanical shocks has been studied by employing statistical, fractographic, and microstructural research methods. The components having high tin (Sn0.2Ag0.4Cu) solder bumps were reflow soldered with the Sn3.8Ag0.7Cu (wt.%) solder paste on Ni(P)|Au- and organic solderability preservative (OSP)-coated multilayer printed wiring boards (PWBs), and the assemblies were subjected to the standard drop test procedure. The statistically significant difference in the reliability performance was observed: the components soldered on Cu|OSP were more reliable than those soldered on Ni(P)|Au. Solder interconnections on the Cu|OSP boards failed at the component side, where cracks propagated through the (Cu,Ni)₆Sn₅ reaction layer, whereas interconnections on the Ni(P)|Au boards failed at the PWB side exhibiting the brittle fracture known also as “black pad.” In the first failure mode, which is not normally observed in thermally cycled assemblies, cracks propagate along the intermetallic layers due to the strong strain-rate hardening of the solder interconnections in drop tests. Owing to strain-rate hardening, the stresses in the solder interconnections increase very rapidly in the corner regions of the interconnections above the fracture strength of the ternary (Cu,Ni)₆Sn₅ phase leading to intermetallic fracture. In addition, because of strain-rate hardening, the recrystallization of the as-soldered microstructure is hindered, and therefore the network of grain boundaries is not available in the bulk solder for cracks to propagate, as occurs during thermal cycling. In the black pad failure mode, cracks nucleate and propagate in the porous NiSnP layer between the columnar two-phase (Ni₃P + Sn) layer and the (Cu,Ni)₆Sn₅ intermetallic layer. The fact that the Ni(P)|Au interconnections fail at the PWB side, even though higher stresses are generated on the component side, underlines the brittle nature of the reaction layer.

Key words: Lead-free, reliability, printed wiring board (PWB) metal finish, Weibull analysis, failure mechanisms, twinning, strain-rate hardening, recrystallization

INTRODUCTION

As portable electronic devices become functionally and structurally increasingly complex, good reliability performance is a major requirement. The products must sustain, in addition to thermomechanical stresses generated by heat dissipating elements, different kinds of dynamic mechanical stresses in their service environments. At the same time, as

component technologies used in the portable products, such as chip scale packages (CSP), employ increasing interconnection densities and thus decreasing interconnection volumes, shock impacts to these products are becoming a notable reliability concern.¹ Because portable products are more likely to be dropped than affected by changes in thermal conditions, the emphasis of reliability research is gradually shifting from studying the effects of thermomechanical cycling to mechanical shock loading or power cycling.

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Along with this development, new requirements for environmentally friendly electronics production have also been raised worldwide. This concerns especially the removal of lead from consumer electronics within the European Union by the July 1, 2006.^{2,3} The most favorable material combination for lead-free soldering would be plain copper conductors and pure tin solder. However, owing to too high melting point—from the reflow soldering point of view—and inadequate mechanical properties of pure Sn, this relatively simple solution is presently not used in volume production. Most lead-free solder candidates are based on Sn with two or more major alloying elements. Similarly, plain copper is hardly ever used as board or component metallization due to the oxidation of copper at room temperature under atmospheric conditions. Thus, lead-free surface finishes on copper soldering pads, such as gold on nickel-phosphorous Ni(P) metallization or organic solderability preservative (OSP), are required. The employment of these surface finish materials together with various lead-free bump and solder materials will lead to new multimaterial interconnection systems and generate also new materials compatibility issues that need to be solved for the sake of reliability. Accordingly, the continuing miniaturization, increased component power, and environmentally friendly lead-free production will create additional requirements for investigating the reliability of portable electronics especially under mechanical shock-loading conditions.

Only few papers have been published on the board level reliability of high-density assemblies under drop conditions.^{4–7} Results from these studies show that the intermetallic layers between the solder and contact metallizations are prone to fail in the drop tests, and therefore the properties of the intermetallic layers are in a particularly important position for the reliability of portable electronics. Intermetallic reactions between lead-free solders and various metallizations have been studied widely. Especially, the reactions between Ni(P)|Au-coated soldering pads and solders have been studied extensively.^{8–17} Likewise, the cracking of interconnections soldered on the Ni(P) metallization has also been reported in these papers and the occurrence of the failure is typically explained by the oxidation or contamination of the plating bath that affects the quality of the metallization.

Hence, because high local stresses and more complex stress distributions caused by mechanical shocks are encountered in modern portable electronic equipments, failure modes and mechanisms controlling the reliability of the CSP interconnections under shock loading conditions are of great interest and importance, and therefore they will be investigated in this article. The reliability is being studied by employing a large number of test structures and by investigating statistically the differences between times to failure. Detailed fractographic and microstructural studies will be carried out in order to

obtain a better understanding of the failure modes and mechanisms.

MATERIALS AND METHODS

The component was a CSP-sized Sn0.2Ag0.4Cu-bumped 12 mm × 12 mm ball grid array packaged (BGA) component having 500- μ m bump diameter and 800- μ m pitch. The height of the bumps was 480 μ m. The number of bumps per component was 144 and the weight of the component was about 0.3 g.

The high-density circuit boards (1 + 6 + 1 build-up FR4) were manufactured by Aspocomp Group (Salo, Finland) with two different protective coating options on the Cu soldering pads: Ni(P)|Au [Ni: 2 μ m, Au: ~0.02 μ m, 9wt.%P in Ni] and OSP (0.2–0.5 μ m). The test board was designed according to the JEDEC board level drop test standard (JESD22-B111).¹⁸

The circuit boards were assembled using Sn3.8Ag0.7Cu (Multicore, Munich, Germany) solder paste. The solder paste was printed (DEK 265 Horizon, Weymouth, UK) with a 100- μ m-thick electroformed Ni stencil and metal squeegees. The mounting machine (Philips ACM Micro, Eindhoven, Netherlands) was set to achieve the highest possible accuracy ($\mu + 5\sigma < 30$ μ m, $C_{pk} = 1.67$) and the reflow was carried out in a conventional forced convection oven (EPM/Heraeus EWOS 5.1 N₂, Hanau, Germany) under air atmosphere. The temperature profile was set according to the recommendations of the solder paste manufacturer. The peak temperature underneath the CSP component was measured with the profilometer (ECD Super M.O.L.E. Gold, Milwaukie, OR) as 241°C ± 0.5°C, and the time above 217°C was 50 sec ± 1 sec depending on the component location.

After the post-reflow inspection, the assemblies were drop tested according to the JESD22-B111 standard. Two deviations from the standard were made. (a) Multiple drops due to the bounce back after the initial impact were not eliminated because no means were available to do this. The first bounce back was about 30% of the initial drop height. (b) 1.5 k Ω resistance through the daisy chain network was used as the failure criterion instead of 1 k Ω , in order to exclude the noise inherent in the measurements. The drop test equipment is composed of a fixture where the circuit boards are attached, a sledge that holds the fixture, and a rigid strike surface. The sledge travels up and down on guide rods. The drop height was set to 82 cm in order to achieve the peak deceleration of 1,500 g for the duration of 0.5 ms (half-sine pulse) required by the standard. The test boards were mounted on support pins with screws at the four corners of the board (Fig. 1). The components faced downward during the test. Strains on the test board were measured (National Instruments PXI-6052E/SCI-1520/SCI-1314, Austin, TX) with strain gauges (1 mm × 1 mm) attached on the PWB on several locations, two of which are shown in Fig. 1 (SG). The strain gauges were attached on the opposite side of the board relative to the components. Deceleration was measured (PXI-4472) simultaneously. The event

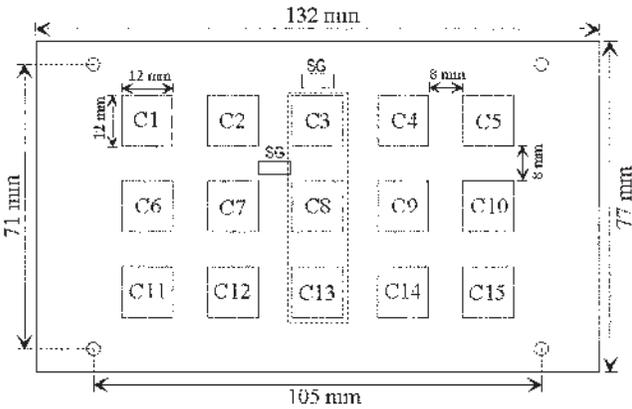


Fig. 1. Layout and dimensions of the drop test board.

detector was connected to the test boards by soldering. A failure was recorded when the resistance through the daisy chain network exceeded the threshold resistance for 200 ns three times in a sequence of five drops. All electrical connections were checked before interpreting the increase as a failure. The assemblies were dropped until all components had failed in order to obtain enough statistical data for the Weibull analysis. The primary failure mechanism was determined from additional assemblies that were dropped until the first failure.

The failure mechanisms were studied from cross sections prepared by standard metallographic methods. Cross sections were investigated with optical (Olympus BX60, Tokyo, Japan) and scanning electron (JEOL 63 35F, Tokyo, Japan) microscopes. Polarized light was used in the optical microscope because the reflection is dependent on grain orientation, and thus differently oriented grains appear in the micrographs in different colors. The distributions of elements at the interconnection reaction zones were analyzed by the energy-dispersive x-ray spectroscopy (Oxford, INCA). The as-soldered interfaces were further characterized by transmission electron microscopy (TEM, JEOL 2000FX, Tokyo, Japan). The TEM studies were undertaken to investigate the structure of the PWB side interfacial region of the solder interconnections on the Ni(P)|Au boards.

The reliability of the solder interconnections was studied by making use of the statistical Weibull reliability analysis. The three-parameter cumulative Weibull distribution function is given by

$$F(t) = 1 - \exp \left[- \left(\frac{t - \gamma}{\eta} \right)^\beta \right] \quad (1)$$

where $F(t)$ is the cumulative density function, η is the characteristic lifetime, β is the shape parameter, and γ is the failure free lifetime. Because the β parameter is dependent on the failure rate, the failure mechanisms can be identified by its value. If the failure data plots with a concave trend and the fit of the regression is therefore poor, this may indicate the presence of a failure free lifetime and the third parameter γ should be introduced. Otherwise, the γ equals zero. The

difference in reliability performance is evaluated on the basis of average drops-to-failure. Parametric methods require the assumption that the data are normally distributed. The test for normality can be carried out by the Shapiro–Wilk test, for instance, which calculates a W statistic, which is given by

$$W = \frac{\left(\sum_{i=1}^n a_i x_i \right)^2}{\sum_{i=1}^n (x_i - \bar{x})^2}$$

where x_i is the ordered sample value and a_i is a constant generated from the mean, variance, and covariance of the order statistics from a normal distribution.¹⁹ The W statistic approaches one for normally distributed samples. When the drops-to-failure does not follow the normal distribution, nonparametric methods must be used to test the equality of two populations. The Wilcoxon Rank-Sum Test procedure is the most widely used test for such purposes.²⁰

RESULTS AND DISCUSSION

The drop tests were carried out with two different coating options on the test boards with ten replications of each. In order to make use of as many data points as possible in Weibull analysis, the locations where the components experience nearly equal mechanical loadings were determined on the basis of the drops-to-failure, strain measurements, and finite-element modeling (FEM). Three middle components (components on C3, C8, and C13 in Fig. 1) were pooled to form a single sample per coating option. To validate the pooling of component locations, the tensile stresses in the interconnections at different component locations during the test were calculated by FEM.⁴ To confirm the results of the FE calculation, the strains of the board were measured. Figure 2 shows the measured and calculated longitudinal strain histories during the first bending. The strain histories in Fig. 2 show that, although the measured strains are higher than the calculated ones, the maximum value is of the

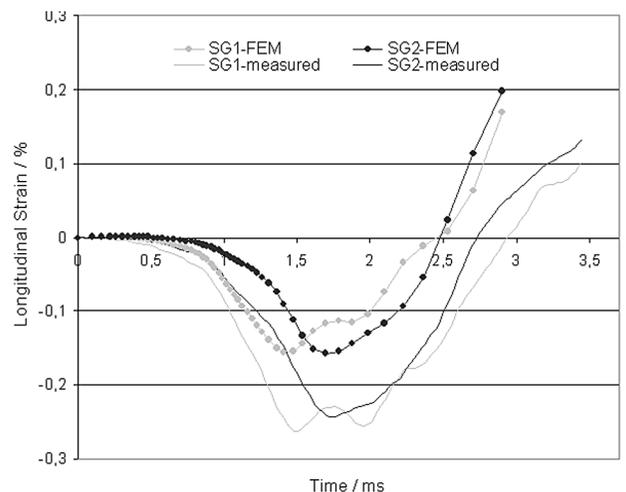


Fig. 2. Comparison of the measured and calculated longitudinal strains on the board at two different locations (Fig. 1).

same magnitude for both locations. The difference in the median drops-to-failure was also studied separately for both coating options using the Wilcoxon Rank-Sum Test, and no significant differences could be found. Figure 3 presents the Weibull plots of the Ni(P)|Au- and Cu|OSP- assemblies. The decision to use the two- or three-parameter form of the Weibull distribution was based on the goodness-of-fit test.

The characteristic lifetimes (η) were 7 and 13 drops, and the shape parameters (β) with 95% confidence intervals were 1.8 ± 0.2 and 1.4 ± 0.1 for the Ni(P)|Au and Cu|OSP assemblies, respectively. The failure free lifetime in the case of Cu|OSP assemblies was two drops. Because the significance of the differences between the η values cannot be tested statistically, it must be evaluated by other means. Based on the Shapiro–Wilk Test for normality, neither the Ni(P)|Au- nor the Cu|OSP- assemblies had normally distributed drops-to-failure distribution. Therefore, nonparametric methods must be used to infer difference in their reliability performance. In engineering sciences, the statistical confidence levels of more than 95% can typically be considered sufficient to reject the null hypothesis, and therefore, all the tests in this paper are carried out at less than 5% risk level. The result of the Wilcoxon Rank-Sum Test points out that the Cu|OSP pad metallization gives significantly better reliability at the 0.01% risk level. The significance between the beta parameters should be tested as well. Therefore, the 95% confidence interval of the difference in the beta parameters was calculated. The confidence interval for the difference is 0.37 ± 0.31 , and thus, the difference is statistically significant; *i.e.*, the analysis suggests that the failure mechanisms are different in the two combinations.

The failure analyses revealed that the electrical breakdown of the components' daisy-chain structures was caused by brittle fracture at one or the other of the opposite interfacial regions of the solder interconnections: the region between the bulk solder and soldering pad or the region between the bulk solder and the component side metallization. The interconnections soldered on the Ni(P)|Au failed from the PWB side along a complex reaction product layer between the Ni(P) metallization and the $(\text{Cu,Ni})_6\text{Sn}_5$ intermetallic compound layer, whereas those soldered on Cu|OSP pads failed from the component side $(\text{Cu,Ni})_6\text{Sn}_5$ layer.

Since the as-soldered microstructure contains only a few large colonies, the high-angle boundaries of which are rarely located at the corner regions of the interconnections, the structure does not provide potential sites for cracks to nucleate and propagate in the bulk solder without recrystallization.²¹ However, the detailed microscopic studies executed after the reliability testing revealed no traces of the recrystallization even after several months of storage at room temperature.

The differences between the failure mechanisms being operative during fast mechanical loadings and in thermal cycling tests can be explained as follows: The drop tests were carried out at room temperature (~ 295 K), which is relatively high ($0.6T_{\text{MR}}$) as compared to the melting range (MR) of the solder alloy (~ 490 – 500 K). Therefore, the flow stress of solder interconnections is strongly dependent on the strain rate, as shown in Fig. 4.^{22,23} The solder alloys become remarkably stronger as the strain rate increases from that occurring in thermal cycling tests ($\sim 10^{-3}$ %/sec) to that used in drop tests ($\sim 10^3$ %/sec).

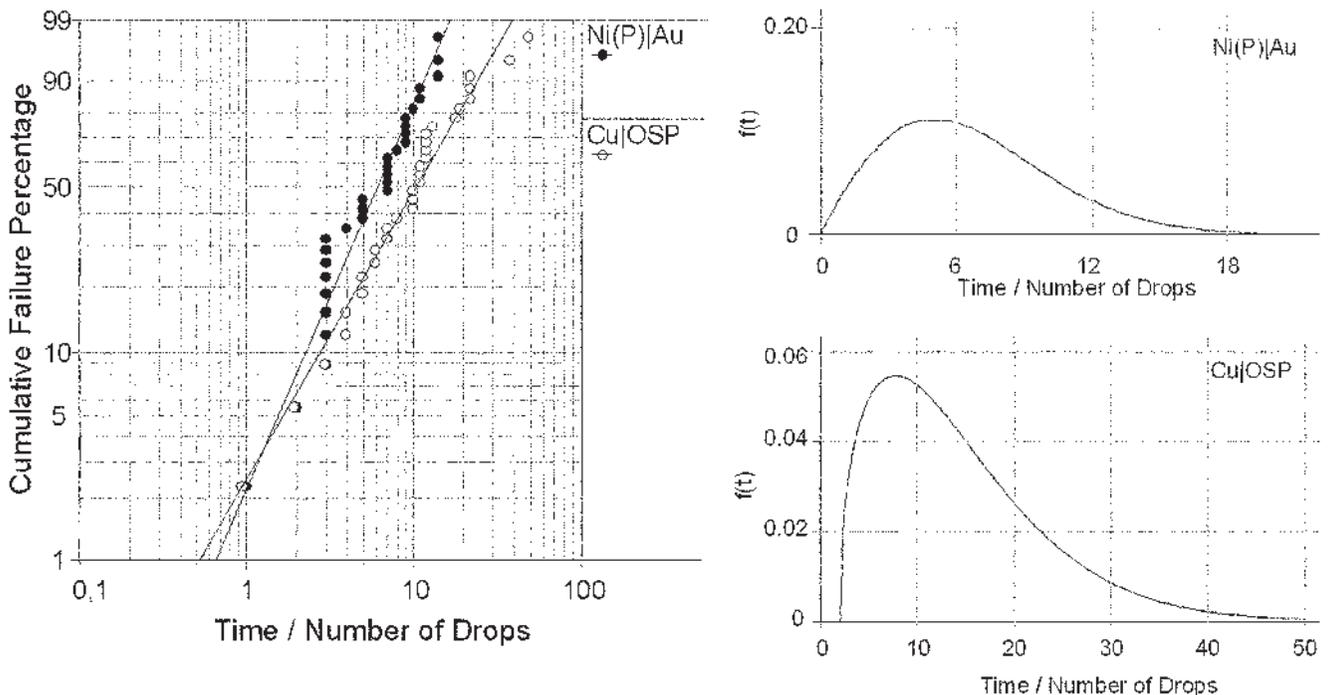


Fig. 3. Weibull reliability plots and the probability density functions for the CSPs on different protective coatings

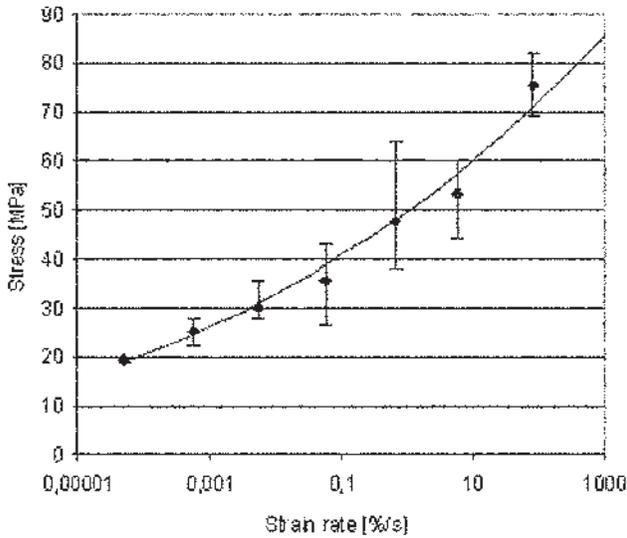


Fig. 4. Flow stress versus strain rate of a Sn2Ag0.5Cu solder joint at room temperature.

According to Fig. 4, the flow stresses of solder materials are expected to be about 2 to 3 times higher in drop tests than in the thermal cycling test. Due to strain-rate hardening, the solder interconnections do not have time for marked plastic deformation, and the critical reduction (*i.e.*, degree of deformation) needed for the recrystallization is not exceeded. The fact that plastic deformation occurring by dislocation slip is limited under shock loading conditions is evidenced also by the presence of numerous deformation twins. It has been reported that as the strain rate is increased, the twinning becomes the dominant deformation mechanism at the expense of slip.²⁴ The deformation twins are typically observed at the corner regions of the interconnections (Fig. 5) where stresses are also the highest. It has been measured that the flow stresses in the range of 7–25 MPa are required to nucleate twins in Sn at room temperature, and considerably smaller stresses are needed for further thickening of the twins.²⁵ Thus, due to the strain-rate hardening of the solder interconnections, the stresses become much higher and more concentrated in the corner regions of interconnections,⁴ where they exceed the fracture strength of the weakest reaction layer. Therefore, cracks propagate in the reaction layers, instead of the bulk solder, as typically observed after thermal cycling.

Cu|OSP Assemblies

The components' under bump metallization consisted of ~0.6–0.8- μm -thick electrochemical Ni on the top of which there had been a very thin layer of gold. The gold layer dissolves completely into the solder bumps during the reflow bumping stage. So, during the assembly reflow, the molten SnAgCu solder becomes in contact with the component side Ni layer, and the first phase to form at the Ni|solder interface is $(\text{Cu},\text{Ni})_6\text{Sn}_5$. The reasons for the formation of Cu_6Sn_5 , instead of expected Ni_3Sn_4 , have been discussed elsewhere.⁸ The morphology of

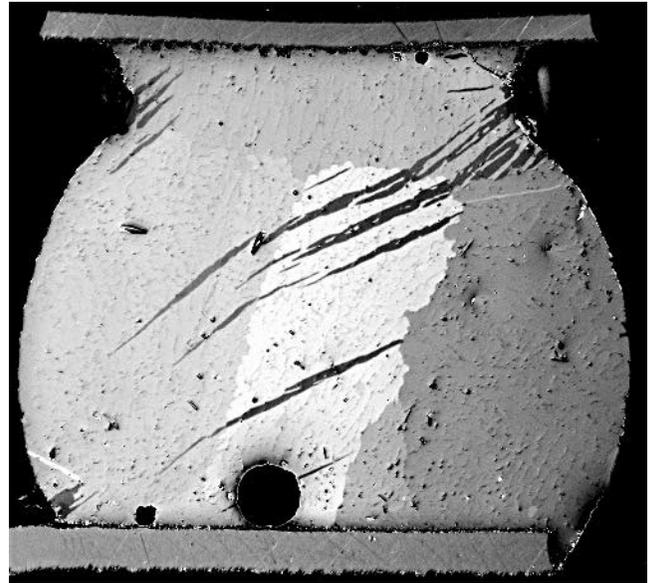


Fig. 5. Structure of the bulk solder after drop test: mechanical twins in the cellular solidification structure.

the reaction layer is typically of scallop type. The relatively thick, also scallop shaped, and irregular intermetallic compound layer visible on the PWB side is the binary Cu_6Sn_5 . A very thin layer of Cu_3Sn can be also observed with light optically as well as with scanning electron microscopy (SEM) between Cu pads and Cu_6Sn_5 .

The micrograph taken using SEM (Fig. 6) shows the typical component side failure, where the crack has propagated through the ternary $(\text{Cu},\text{Ni})_6\text{Sn}_5$ layer. In all the failures observed, the cracks have nucleated—for geometric reasons—in the bulk solder a short distance away from the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ layer and then moved to this intermetallic layer, which obviously provides a favorable path for brittle fracture. Some minor cracking was also observed in the PWB side reaction zone of the interconnections. However, in all the cases studied, the cracks, which caused the electrical failures, located at the component side reaction zone.

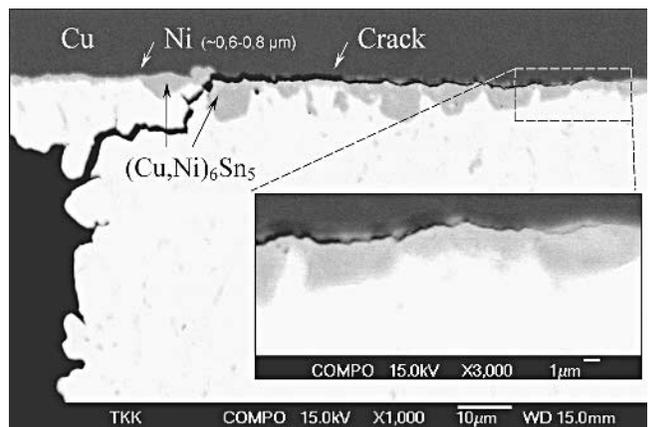


Fig. 6. The primary failure mode in the Cu|OSP interconnections: the cracking of the component side $(\text{Cu},\text{Ni})_6\text{Sn}_5$ layer.

The effect of additional elements in the reaction between Cu and Sn has been reported in the literature.^{26–28} The addition of Ni has been observed to have a minor impact on the formation and thickness of the intermetallic compound layer, but it produces severe cracking of the intermetallic phase. Kulojärvi²⁸ noted in her thesis that Ni weakens the mechanical properties of Cu_6Sn_5 . The cracking of the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ was occasionally visible even in the after reflow reference samples. The brittle nature of the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ compound is further emphasized by small secondary cracks seen sometimes branching out from the primary path.

The effect of Ni on the mechanical properties of Cu_6Sn_5 is being studied, and the results will be published later. It is interesting to note, however, that according to our most recent TEM studies, Ni will also precipitate as Ni_3Sn_4 phase inside $(\text{Cu},\text{Ni})_6\text{Sn}_5$. The identification of the solubility of the precipitated phase at room temperature must be done and the question of whether the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ -matrix is then stable (the ordered long-period superlattice) or metastable (the simple η -form of the NiAs structure) remains to be solved.

The cracks on the PWB side of the interconnections propagate mostly in the Cu_6Sn_5 layer, as shown in Fig. 7. It is typical that the cracks propagated progressively with the number of drop impacts. Furthermore, cracks on the PWB side are not very common. As discussed previously, the complete fracture is always found on the component side, where the cracking is typically much more severe. It is therefore concluded that the fracturing of the PWB side intermetallic layers (Cu_6Sn_5 or Cu_3Sn) is not the primary mechanism for electrical failure of the Cu|OSP assemblies.

Ni(P)|Au Assemblies

During electroless coating of the PWB solder pads, Ni is deposited together with phosphorus, because the hydrophosphite is used as a reducing agent in the plating bath. On the top of the Ni(P) coating, there is a thin Au layer to protect the Ni from oxidation and

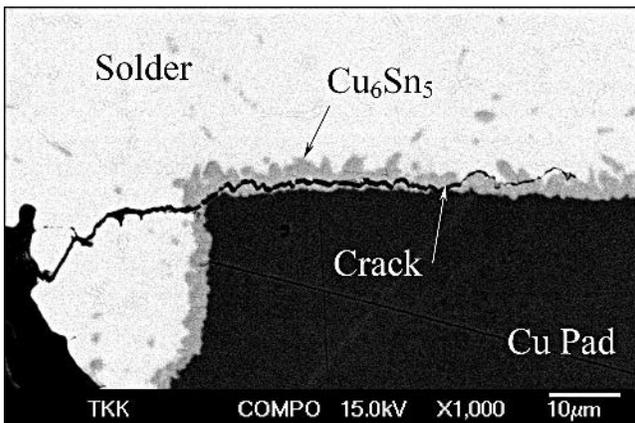


Fig. 7. Fracture in the PWB side Cu_6Sn_5 of the Cu|OSP interconnection.

thereby to promote solderability. During soldering, a thin layer of Au dissolves instantly into molten solder and $(\text{Cu},\text{Ni})_6\text{Sn}_5$ is formed on the Ni(P) layer.

The Ni(P)|Au assemblies, unlike the Cu|OSP assemblies, exhibit severe cracking in the PWB side. The results of the FEM of the CSP interconnections show that in drop tests, the stresses at the component side interfacial region are more than two times as large as those on the PWB side due to the geometry of the interconnections and the materials used.⁴ Therefore, the fact that the interconnections fail at the PWB side emphasizes the brittle nature of the reaction layer. The cracks propagate in a very narrow reaction zone between the two-phase layer (dark gray) and the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ intermetallic layer, as shown in Fig. 8. Further support for this observation can be obtained from the distributions of the elements over the cracked region, even though the concentration profiles can be taken only qualitatively because of the crack interfaces. Figure 9 presents the energy-dispersive spectroscopy (EDS) line analysis of the P and Sn concentrations across a crack. The crack can be located in the graph, where the P and Sn concentrations decrease considerably (between about 4.5 μm and 5 μm in the abscissa). The two-phase layer and electroless Ni(P) are to the left from the indicated location of the crack, and to the right there is a solder interconnection.

With the help of TEM, it was discovered that the interfacial region between Ni(P) and $(\text{Cu},\text{Ni})_6\text{Sn}_5$ is composed on two layers, as shown in Fig. 10. The dark phase in Fig. 8b is the two-phase layer of Ni_3P and Sn. In this two-phase layer, Sn (white stripes) is located between columnar Ni_3P crystals. Between the two-phase layer and $(\text{Cu},\text{Ni})_6\text{Sn}_5$, there is a porous microcrystalline (or amorphous) phase layer, which

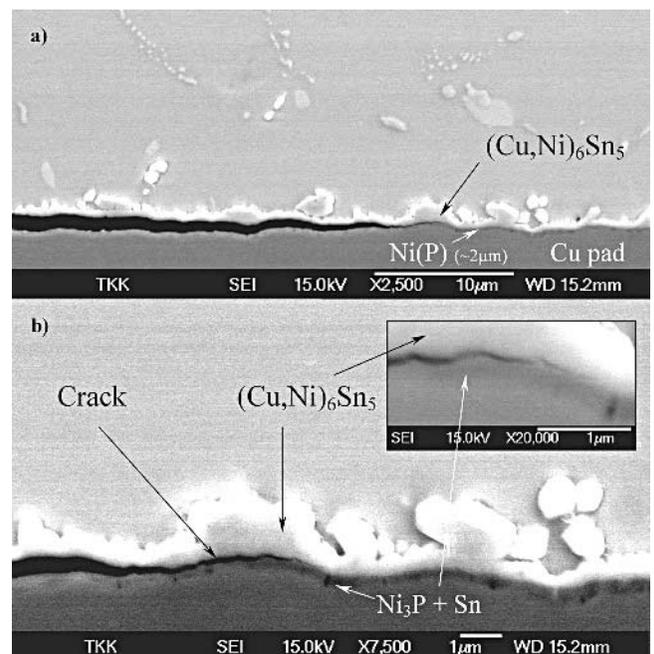


Fig. 8. Tip of the crack between the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ and the two-phase layer on the Ni(P) coating.

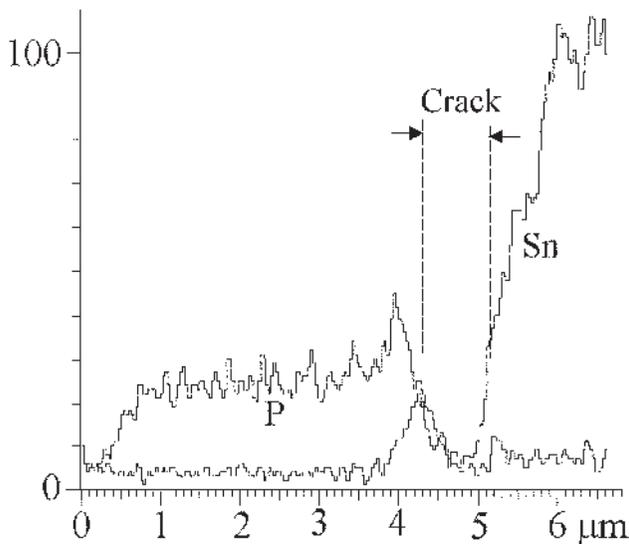


Fig. 9. EDS line scans of tin and phosphorous across a crack.

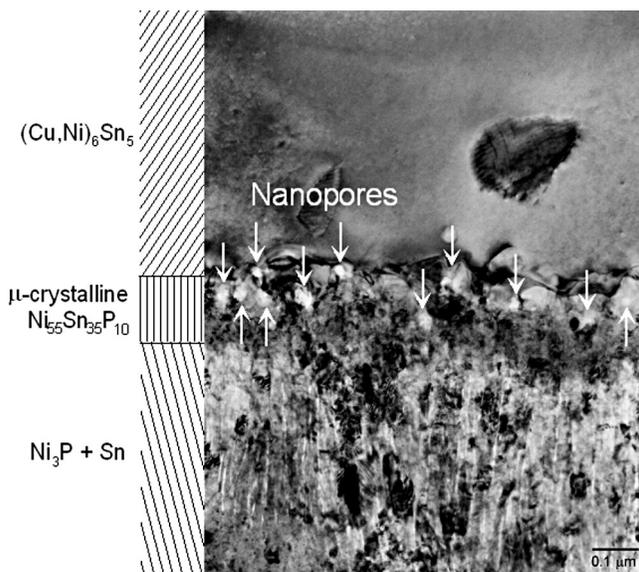


Fig. 10. Bright-field image of the reaction zone between electroless Ni(P) metallization and the near-eutectic SnAgCu solder (magnification: 100,000 \times). Between the Ni₃P and Sn two-phase layer, there is a thin porous ternary solution phase containing nickel, tin, and phosphorus.

contains nickel, tin, and phosphorus. It is this thin layer in which the cracks are located (Fig. 8) in the case of the Ni(P)|Au coating. The formation of these P-induced reaction products has been discussed in more detail elsewhere.⁹

Thus, based on the SEM/EDS and TEM studies, it can be concluded that the brittle rupture of the porous ternary phase in between the (Cu,Ni)₆Sn₅ and the columnar two-phase (Ni₃P + Sn) layer is the primary failure mechanism in the case of the Ni(P)|Au assemblies.

CONCLUSIONS

The reliability of the lead-free CSP component has been studied by using a very high loading rate in the drop test as well as by employing statistical, fracto-

graphic, and microstructural research methods. Two different failure modes were observed: the interconnections on the Ni(P)|Au-coated soldering pads failed from the PWB side—along the porous reaction layer—whereas the interconnections on the OSP-coated pads failed from the component side (Cu,Ni)₆Sn₅ intermetallic layer. These failure modes differ from those being characteristic for thermally cycled solder interconnections. The local recrystallization of solder interconnections, typical for thermally cycled interconnections, enhances cracks to nucleate in and propagate through the bulk solder interconnections. However, no recrystallization was observed in the drop-tested assemblies. Most obviously the critical reduction needed for the onset of recrystallization is not exceeded in drop tests, because the solder interconnections hardly deform plastically due to strong strain-rate hardening under very fast deformation. Owing to the strain-rate hardening, the stresses at the corner regions of the interconnections increase locally above the fracture strengths of the interfacial reaction layers, and therefore, the interconnections fail either by intermetallic fracture or by the cracking of the porous ternary phase. It seems evident that dissolved Ni lowers the fracture strength of (Cu,Ni)₆Sn₅. Likewise, high phosphorous content in the electroless Ni layer may have a detrimental effect on the reliability of lead-free interconnections, when tested under mechanical shock loading conditions.

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