Reprinted with permission from the publisher.
In: Microsystem Technologies 2004.
Vol. 10, No. 5, pp. 346–350.

"Plug-up"–a new concept for fabricating SOI MEMS devices

J. Kiihamäki, J. Dekker, P. Pekko, H. Kattelus, T. Sillanpää, T. Mattila

Abstract This paper reports a novel process sequence for fabricating micromechanical devices on silicon-on-insulator (SOI) wafers. Among the merits of the described process are its improved immunity to stiction and elimination of conductor metal endurance problems during sacrificial etching in hydrofluoric acid. With this novel process one can controllably embed vacuum cavities within SOI substrates. Further processing of such cavity wafers enables realization of a wide variety of micromechanical devices based on single crystalline silicon or even integrated read-out circuitry.

1
Introduction

In recent times, conventional surface and bulk micromachining have been rivalled by the so-called Silicon-on-Insulator (SOI) micromechanics. This technology is based on direct wafer bonding combined with advanced silicon dry-etching techniques. The buried silicon oxide is used as a sacrificial layer in an analogous way to the well-known surface micromachining technology. The use of bonded SOI wafers as starting material for micromechanical devices was introduced by E. H. Klaassen [1], as wafer bonding and new deep silicon etching [2] methods were quickly developing. SOI micromachining makes use of single crystalline silicon, which shares or surpasses the excellent mechanical properties of polysilicon and additionally carries very low intrinsic stress, which would be very difficult to reach using chemical vapour deposited thin films. In the standard approach, a SOI-based device is fabricated by pattern-etching access windows into the structural layer of the SOI, followed by local sacrificial oxide removal in concentrated hydrofluoric acid (HF), as shown in Fig. 1. Contact metallisation is added for wiring purposes. The basic dual-mask process is very simple but suffers from certain limitations:

1) Metallisation. If the conductor and pad metallisation is formed in an early phase, as shown in Fig. 1 (Standard), it will be exposed to the aggressive HF-based silicon dioxide etchant during the subsequent release etching cycle. The selection of IC-compatible metals that are inert and well adhering in HF is very limited. Additionally, the metal should also form good ohmic contact to with silicon and be easily bondable. On the other hand, if the sacrificial etching were performed prior to depositing and pattern-etching the metallisation, lithography would be difficult over the high topography steps existing on the wafer.

2) Stiction. Another issue that has retarded the emergence of SOI micromachined devices on the consumer market is the phenomenon called stiction. It is associated with the atomic-scale smoothness of silicon-oxide interfaces in SOI. The perfectly polished wafer surface is a prerequisite for successful bonding and SOI wafer fabrication, but unfortunately it is also the most important source of failure. If the delaminated membrane or beam is intentionally or accidentally brought into direct physical contact with the carrier wafer, the micromechanical structure sticks permanently to the substrate.

The literature offers many descriptions of possible solutions to the above problems. One can use modified etching solutions that do not readily attack aluminium, or noble metals to replace Al. Stiction in SOI is more difficult to avoid. Our procedure called Plug-up and introduced in Fig. 1 tackles both of these problems. Metallisation can be prepared over smooth topography after cavity formation and polysilicon bumps limit the area in case of possible physical interface contact. The Plug-up sequence makes use of liquid-permeable polysilicon [3–5]; the details of the fabrication sequence are given in the Experimental section.

Vacuum shells have earlier been studied for making a wafer-level vacuum environment for improving the resonator Q value [5, 6] or for protecting micromechanical devices from the environment. The sacrificial layer is usually removed via lithographically patterned etch holes [6, 7] or via semipermeable polysilicon [3–5].

An optional way to make comparable cavity wafers would be pre-processing of the wafers prior to bonding and thinning [8]. The Plug-up procedure's advantages over that system include (1) membranes of constant thickness, (2) front-side alignment marks remain on the

Received: 18 July 2003 / Accepted: 12 November 2003

J. Kiihamäki (✉), J. Dekker, P. Pekko, H. Kattelus,
T. Sillanpää, T. Mattila
VTT, Tietotie 3, Espoo, Finland
e-mail: Jyrki.Kiihamaki@vtt.fi

K. Järvi and T. Häkkinen are gratefully acknowledged for the device fabrication. The Finnish National Technology Agency, Okmetic, VTI Technologies, and Micro Analog Systems participated in funding this work. The ultrasonic devices were fabricated in collaboration with Autotank, Oras, Suunto, Vaisala, and Enermet.

DOI10.1007/s00542-004-0414-3

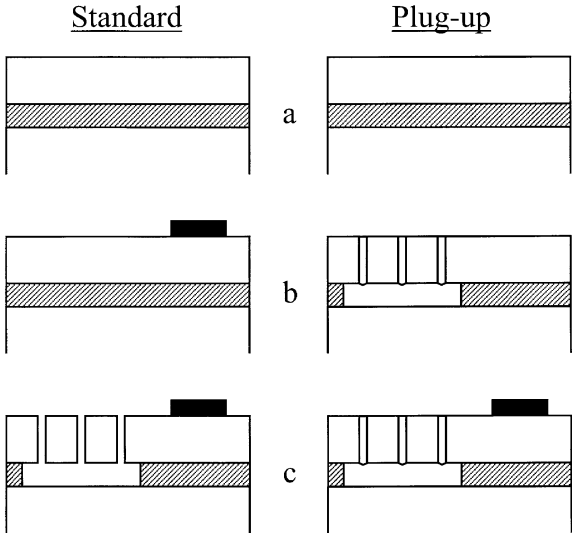

Fig. 1a–c. Schematic process flow of the standard SOI process sequence (left) and Plug-up sequence (right)

wafer, (3) aligned bonding is not needed, (4) MEMS manufacturer does not need bonding, grinding or polishing equipment, (5) bumps preventing stiction are simple to prepare, and (6) pressure inside the cavity is mainly determined by the closing method and not by the atmosphere of bonding.

2
Experimental

2.1
Sample preparation

The Plug-up sequence is schematically presented in Fig. 2. The starting material is micromechanical bonded SOI with 5–20 μm device layer thickness and 1–2 μm thick buried oxide over the low-resistivity carrier wafer. After determining the area to be delaminated from the substrate, its interior is patterned into an array of 1–2 μm wide circular or square-shaped dots. These are replicated into the device layer of SOI through ICP etching using the Bosch process in STS ASE. The subsequent HF dip attacks the buried oxide slightly, as shown in Fig. 2a. A thin layer of polysilicon is then deposited using the low-pressure chemical vapour deposition (LPCVD) technique by controlling the deposition parameters in such a way that the film contains a controlled density of nanometer-scale pinholes [5]. The areal density of the pinholes must exceed $1/\mu m^2$ in our geometry (Fig. 2b). Immersing the wafer in HF results in local removal of the buried oxide (Fig. 2c). After careful rinsing and drying, pinhole-free polysilicon is deposited over the wafer to completely plug up the holes (Fig. 2d). The pressure inside the cavity remains in the 100 Pa vacuum range where the deposition process takes place. After etch-back, the cavity wafer is rigid, identical to standard SOI wafers from the fabrication point-of-view, and a variety of processing steps can be performed on it without difficulty, including any standard metallisation (Fig. 2e). Some device types like pressure sensors or ultrasonic transducers do not require further processing after this, while others may still call for relief of laterally moving resonators, comb electrodes or other features. Such a release step can now be made with high-yield dry processing (Fig. 2f).

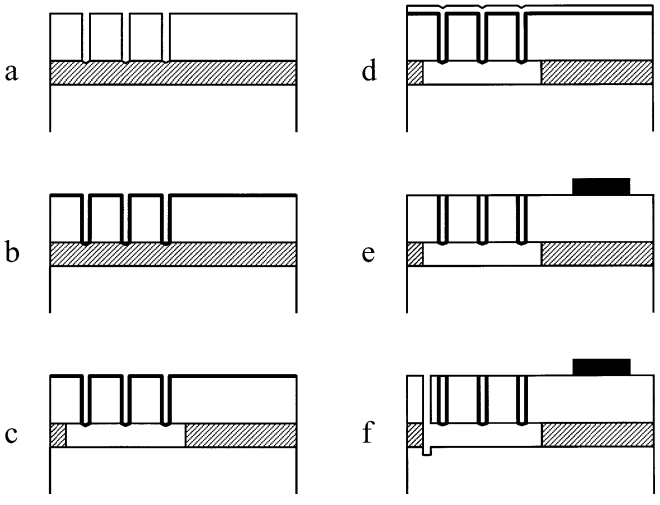

Fig. 2a–f. Schematic process flow of the Plug-up sequence. **a** Perforation of structure layer, **b** deposition of HF permeable polysilicon, **c** sacrificial etching, **d** closing of cavities, **e** metallisation (back-end) **f** optional release of horizontally moving structures

2.2
Characterisation

After sacrificial layer etching, the delaminated area was inspected using a microscope equipped with an infrared-sensitive video camera [10]. The near-infrared wavelengths available were able to transmit the typical device layer thickness in micromechanical SOI. Membrane deflection by atmospheric pressure (LPCVD vacuum inside cavity) was measured using a stylus force of 0.5 mg in the Dektak V200 profilometer. Resonance frequencies of completed micromechanical devices were characterised at wafer level using an impedance analyser (HP4294A) and probe station. The vacuum measurements were performed on diced and encapsulated devices using a network analyser (HP4396B) and temperature-controlled vacuum chamber.

2.3
Device examples

Absolute pressure sensors were fabricated with monolithically integrated read-out electronics. These results will be reported in detail elsewhere [12]. Capacitive micromachined ultrasonic transducers were also fabricated using the Plug-up technology on SOI. Transmission and detection of ultrasound were demonstrated.

3
Results and discussion

Infrared microscopy reveals that sacrificial layer etching through the polysilicon pinholes is a reliable process (Fig. 3a). With the pinhole density produced by our polysilicon deposition, all wells are transparent to the HF etchant and the etching product flow when the well diameter exceeds about 1.2 μm. For refill and etch-back

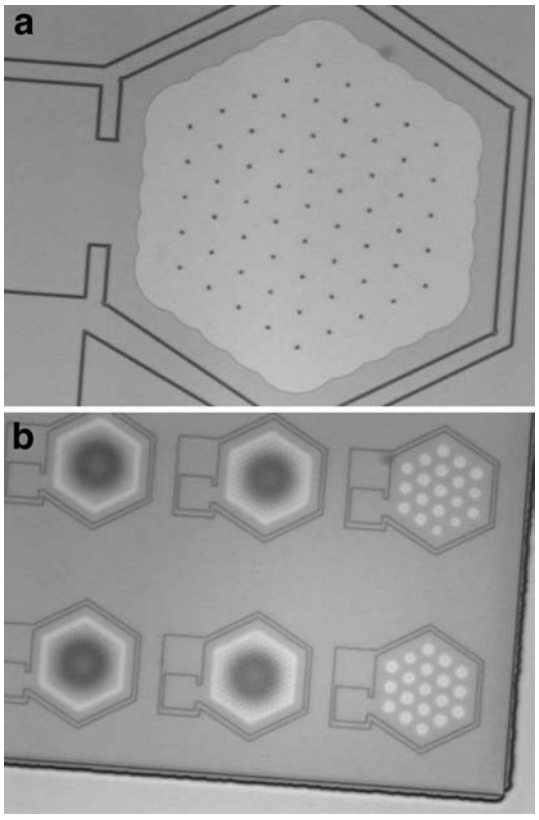

Fig. 3. **a** Near IR image of hexagonal cavity after sacrificial etching, **b** IR images of hexagonal cavities after closing and etch-back with different perforation hole patterns

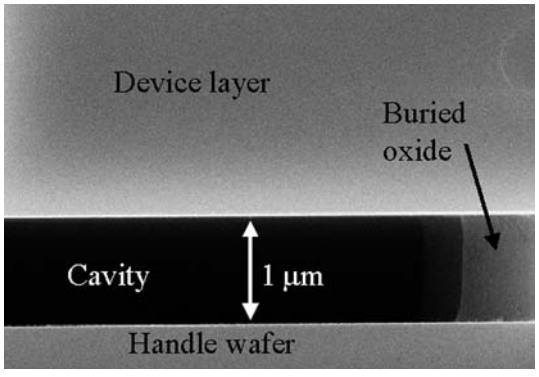

Fig. 4. Detail of the inside of the cavity. The walls of the cavity are clean and no films are deposited inside the cavity

processes use of the smallest possible trenches would be advantageous, but when using sub-micron well diameters the fluid flow may be restricted at some locations and not all membranes are fully delaminated from the substrate. The reason is either inadequate deep etching or lack of pores in the thin polysilicon layer at the bottom of the small trench. In Fig. 3b, successful encapsulation of the cavities in a vacuum by a pinhole-free polysilicon overcoat is observed through membrane deflection. Grey shades resulting from interference appear in the near-infrared photograph. The deflection of the membrane was quantified with a low contact force stylus profilometer to be about 300 nm for a 250 μm wide hexagon for a device layer thickness of 8 μm. The low accuracy of the profilometer measurement is caused mainly by difficulty in setting the scan line precisely over the centre of the cavity. During enclosure, practically no deposition occurs through the pinholes onto the cavity walls, as can be seen in the SEM micrograph of Fig. 4.

An SEM micrograph of an anti-stiction bump formed on the bottom of the membrane by a short HF dip is shown in Fig. 5. Driving a membrane with dimensions comparable to those shown in Fig. 3 electrostatically against the substrate does not result in stiction. The polysilicon plugs constitute a negligible portion of the structural layer, and single crystalline silicon dominates the mechanical properties of the devices.

No notching was seen at the bottom of the structure layer when laterally moving structures and air holes for breaking the vacuum cavity were dry-etched onto the structure layer. Typically notching is seen when high aspect ratio trenches are etched and an insulating etch stop layer is used [13]. However, when etching is done above the vacuum cavity, there is no insulator layer that can be charged and notching is avoided. A SEM micrograph of a released beam without notching is shown in Fig. 6.

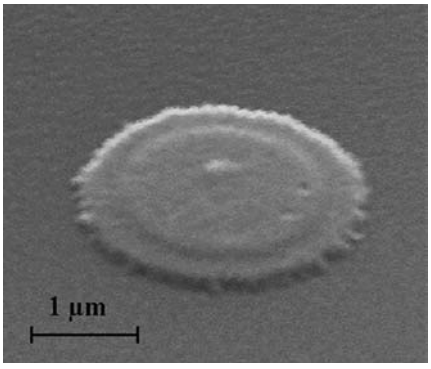

Fig. 5. SEM micrograph of an anti-stiction dimple formed by wet etching on the bottom of the structure layer

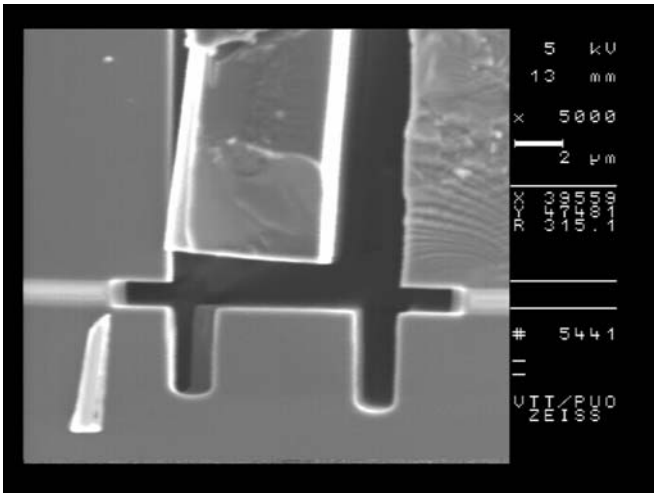

Fig. 6. Cross-section of a beam above a Plug-up cavity. Etching is continued to the substrate and no notching occurs

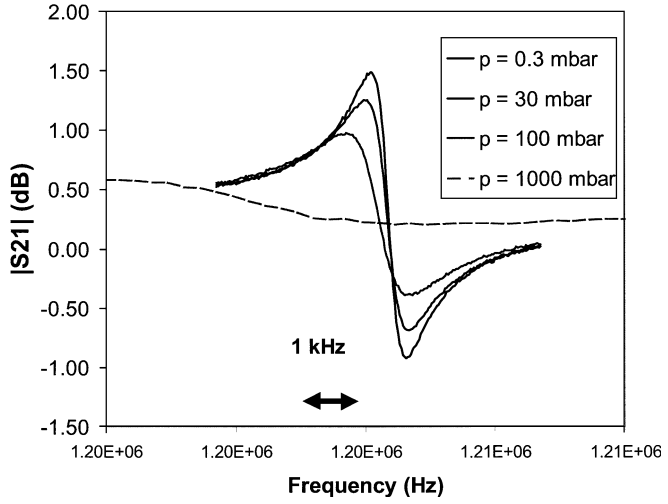

Fig. 7. Measured resonance peak of a hexagonal cavity resonator, external pressure as a parameter

Resonance frequencies of enclosed test membranes were measured inside a vacuum chamber by varying the chamber pressure. A set of resonance curves for a hexagonal 300 μm diameter resonator of 8 μm thickness is shown Fig. 7 with the pressure of the measurement chamber as a parameter. The Q value under in an external vacuum is around 1000 and in atmospheric pressure about 200. The resonance frequency shifted with temperature according to the temperature coefficient of Young's modulus for single crystal silicon.

Absolute pressure sensors were fabricated using the Plug-up technology for pressure ranges up to 500 kPa. CMOS-based readout circuitry was monolithically integrated. For a flat circular plate of constant thickness and uniformly distributed load (pressure) over an entire surface, the deflection can be determined as follows [9]:

$$\delta = \frac{3\,p\,r^4\,(1-\nu^2)}{16\,E\,t^3} \quad ,$$

where p is the applied pressure, r is the radius of the cavity, ν is the Poisson ratio and E is Young's modulus for the plate material, and t is the plate thickness. Because the sensitivity is proportional to the fourth power of the membrane radius, a well-controlled lateral etching rate of the sacrificial oxide is a prerequisite. Pressure sensors were successfully demonstrated [12].

Another practical device demonstrator realized using the Plug-up cycle on SOI was a capacitive micromachined ultrasonic transducer (cMUT). A matched pair of closed cavities was used as an ultrasonic transmitter and receiver at the resonance frequency of 1.78 MHz; a schematic description of such a system is given in Fig. 8. It takes about 60 μs for a sound wave to travel the separation distance of 20 mm. The dashed line is the AC voltage applied to the transmitter and the solid line is the output voltage of the detecting circuit. The receiving sensors are excited in their mechanical resonances and it takes several periods before the amplitude reaches its maximum. The bias voltage across the sensors was 60 V.

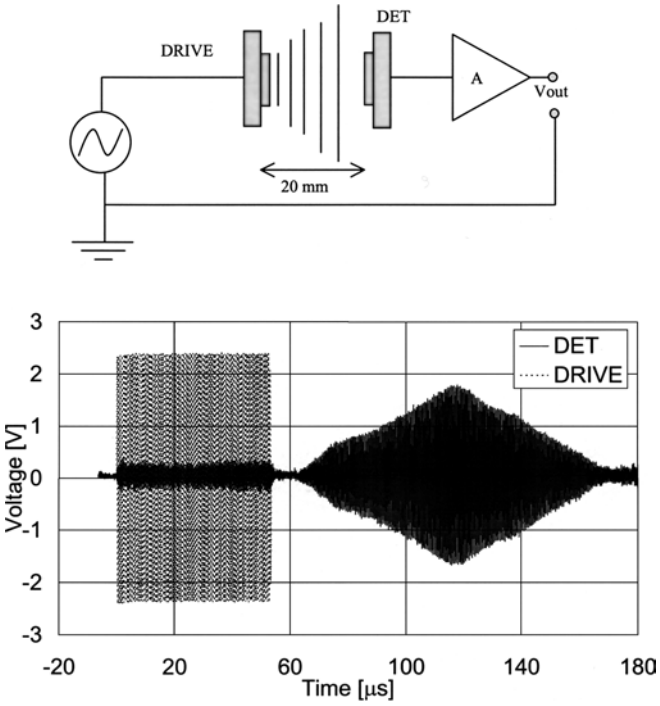

Fig. 8. (Top) Ultrasonic transmitter/receiver configuration. (Bottom) Input and output waveforms of the ultrasonic flow measurement setup

4 Conclusions

This paper describes a novel process for making micromechanical SOI devices with an abundance of advantages over the conventional methods. The key issue in this process is the controlled formation of hermetically sealed cavities in the SOI structure and the resulting clean single crystal surface after the etch-back steps, which enables versatile back-end processing. The quality of the resulting single crystal devices is good and they do not show any signs of degradation due to processing. Monolithical integration with active electronics is possible in a synergetic manner, so that several fabrication steps are common for electronic and mechanical devices [11]. An absolute pressure sensor and an ultrasonic transmitter-receiver pair are presented as device examples. Dicing and packaging of such hermetically sealed devices is quite straight-forward. Fabrication of open structures is also possible using Plug-up technology with the advantage of dry processing for structure relief.

References

1. **Klaassen EH et al.** (1996) Silicon fusion bonding and deep reactive etching: a new technology for microstructures. Proc Transducers'95, Stockholm, Sweden, June 1995, 556, Sensors and Actuators A 52: 132–139
2. **Bhardwaj JK; Ashraf H** (1995) SPIE Proceedings 2639, 224
3. **Lebouitz KS et al.** (1995) Transducer's 95 and Eurosensors IX, June 25–29, Vol. 1, pp. 224–227
4. **Kageyama Y et al.** (2000) J Vac Sci Tech A, 18(4): 1853–1858
5. **Saarilahti J; Blomberg M; Häärä A; Kattelus H** (2002) A novel method for processing capacitive micromechanical ultrasonic

transducers (cMUT) Proc. IEEE Ultrasonics Symposium. 2: 1071–1074
6. **Guckel H et al.** (1992) Solid-State Sensor and Actuator Workshop, 5th Technical Digest., IEEE, 153–156
7. **Ladabaum I et al.** (1996) IEEE Ultrasonics Symposium Proceedings, 1: 335–338
8. **Prochaska A; Baine P; Mitchell SJN; Gamble HS** (2000) Proc. SPIE, 4174: 244–255
9. **Young WC** (1989) Roark's Formulas for Stress & Strain, 6th edition, McGraw-Hill, New York
10. **Kiihamäki J** (2002) Measurement of oxide etch rate of SOI structure using near IR microscopy. Physica Scripta. Vol. T101 185–187
11. **Kiihamäki J; Ronkainen H; Pekko P; Kattelus H; Theqvist K** (2003) Modular Integration of CMOS and SOI-MEMS Using Plug-up Concept. Technical digests of 12th International Conference on Solid-State Sensors, Actuators and Microsystems, TRANSDUCERS03, Vol. 2, pp. 1647–1650
12. **Ylimaula M; Åberg M; Kiihamäki J; Ronkainen H** (2003) Monolithic SOI-MEMS Capacitive Pressure Sensor with Standard Bulk CMOS Readout Circuit. Proceedings of 29th European Solid-State Circuits Conference, ESSCIRC2003, pp. 611–614
13. **Hwang GS; Giapis KP** On the origin of the notching effect during etching in uniform high density plasmas. J Vac Sci Technol B15(1), 70