

A Dual-Band RF Front-End for WCDMA and GSM Applications

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Abstract—An RF front-end for dual-band dual-mode operation is presented. The front-end consumes 22.5 mW from a 1.8-V supply and is designed to be used in a direct-conversion WCDMA and GSM receiver. The front-end has been fabricated in a 0.35- μm BiCMOS process and, in both modes, can use the same devices in the signal path except the LNA input transistors. The front-end has a 27-dB gain control range, which is divided between the LNA and quadrature mixers. The measured double-sideband noise figure and voltage gain are 2.3 dB, 39.5 dB, for the GSM and 4.3 dB, 33 dB for the WCDMA, respectively. The linearity parameters IIP3 and IIP2 are -19 dBm, $+35$ dBm for the GSM and -14.5 dBm and $+34$ dBm for the WCDMA, respectively.

Index Terms—BiCMOS analog integrated circuits, direct conversion, low noise amplifiers, mixers, multimode, radio receivers.

I. INTRODUCTION

CURRENT wireless terminals provide dual- or multiband operation mainly for cellular capacity reasons. In the near future, as third-generation wireless systems are launched, there will be an increasing demand for multimode terminals, which will allow access to different systems providing various services. The coexistence of second- and third-generation cellular systems requires multimode, multiband mobile terminals. The optimal multimode terminal should be as simple and small as possible. Hence, it would be advantageous if the receiver could share as many of its building blocks as possible in all operation modes. The recently published RF receivers for multiband terminals have been implemented by using several parallel front-ends [1], [2]. Although a high integration level can be achieved, the parallel architecture wastes significant chip area. The front-end presented in this paper can use the same signal path in both modes, with the exception of the first stage in the LNA [3].

The receiver should additionally be able to accommodate the different radio standards with different bandwidths and modulations. Therefore, different channel and image filters are required in the receiver. If such filters are realized with expensive and bulky external passive structures, the size and cost of a multimode receiver increases. The selected architecture should minimize the number of external filters required, thus performing most of the filtering on the chip with active structures. In ad-

dition, dual-band channel selection filters for such applications are feasible [4]. Suitable architectures for multimode, multiband receivers include direct conversion, low-IF, and image rejection receivers [2].

The RF front-end is targeted at GSM and third-generation WCDMA applications and designed using specifications related to these standards [5], [6]. The main characteristics of the two systems are shown in Table I. The challenges set by standards for the RF designer are related to the different reception bands. The GSM operates at 900 MHz, while the WCDMA bands are around 2 GHz. In addition, the two systems have totally different channel spacing and symbol rates. This clearly affects the channel filtering, but the $1/f$ -noise can cause significant degradation in noise performance, particularly in the case of direct conversion receivers with a narrow channel bandwidth [7].

The paper is organized as follows. Section II covers issues related to the direct conversion RF front-end. The building blocks and issues related to the layout are described in Section III. Experimental results are presented in Section IV and the paper is summarized in Section V.

II. RF FRONT-END FOR DIRECT CONVERSION RECEIVERS

The RF front-end uses the direct conversion architecture, which is suitable for a high integration level, although it has some well-known disadvantages compared to the superheterodyne architecture [8], [9]. A block diagram of the designed RF front-end is shown in Fig. 1. It has two separate single-ended inputs, one input for each standard. The separate inputs are required because to our knowledge there are no multiband preselection filters available. Furthermore, if the two reception bands were connected simultaneously to the same input, the spurious responses may corrupt the reception. With the exception of the input transistors and matching inductors of the LNA, all on-chip devices are utilized in both modes. The single-ended-to-differential conversion is performed before the signal downconversion, thus enabling a double-balanced mixer topology. The single-ended-to-differential converter additionally improves the LO-to-RF isolation and separates the two differently sized resonators of the LNA from the mixer. The RF front-end requires a single LO port because one mode is selected to be operational at a time. If the receiver had two LO signals, spurious tones could corrupt the reception, particularly if the A/D converters are implemented on the same chip [10]. The LO is external and a 90° phase shift is performed off-chip. In multiband receivers, it is impractical to perform the quadrature generation by poly-phase filters. Each standard at a different frequency band would require its

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TABLE I
WCDMA AND GSM SYSTEM CHARACTERISTICS

	WCDMA	GSM
Main application	Data	Voice
Access method	DS-CDMA	TDMA
Duplexing	FDD	TDD/FDD
Modulation	QPSK	GMSK
Receive bands		
Base station [MHz]	1920-1980	880-915
Mobile station [MHz]	2110-2170	925-960
Channel spacing	5 MHz	200 kHz

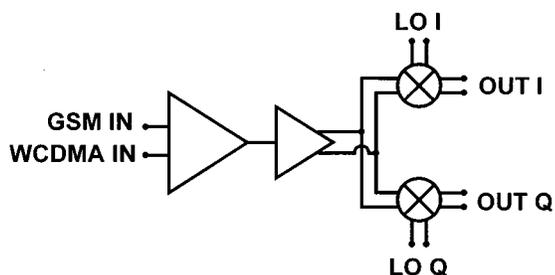


Fig. 1. Block diagram of the RF front-end.

own filter structure, thus leading to parallel filters and very complicated interface design. A possible solution generating quadrature LO would be to use divide-by-two circuits. The signal paths between the different blocks are ac-coupled with 10-pF on-chip capacitors. Hence, the low-frequency distortion components generated by the second-order nonlinearities in the LNA and single-ended-to-differential converter are filtered out before downconversion. Otherwise, they could partly leak through the mixer to the output. A fully differential signal path could also be used throughout the front-end to reduce the effect of common-mode distortion and noise [11]. However, it would double the power consumption of the LNA, increase the chip area, and require a balun in front of the LNA, thus increasing the loss between the antenna and the receiver. The front-end has a tunable gain to relax the baseband linearity and gain control requirements. The gain control is divided between the mixer and the LNA. The combined current consumption of the LNA and single-ended-to-differential converter is 6.6 mA in GSM and 6.1 mA in WCDMA mode, respectively. A single mixer uses 3 mA.

III. CIRCUIT DESIGN

A. LNA

The schematic of the LNA operating in WCDMA mode with maximum gain is shown in Fig. 2. The LNA uses the conventional common-emitter topology with cascode transistors in all gain and mode settings to achieve a good reverse isolation with high gain and low NF. Transistors Q1 and Q2 are used as the

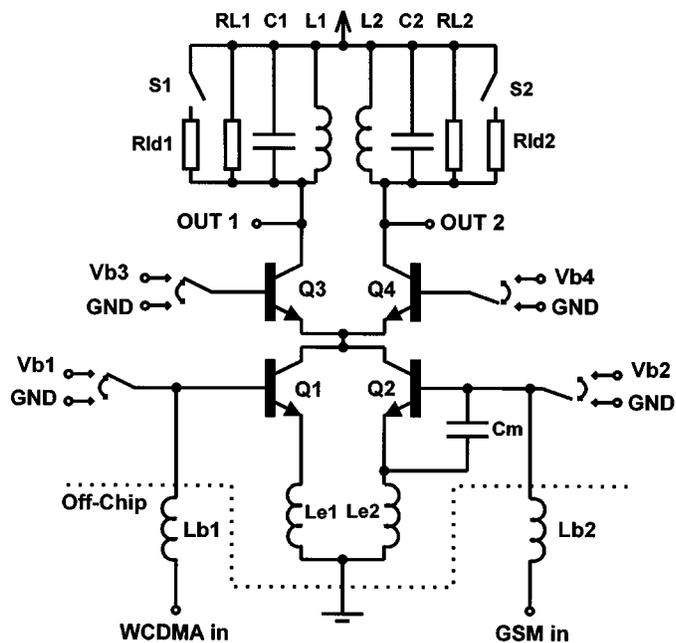


Fig. 2. Schematics of the LNA.

input transistors for different modes. The base and emitter inductors of the transistors Q1 and Q2 are used for matching. In the GSM mode, the capacitor C_m is also added between the base and emitter of Q2 to reduce the value of base inductor L_{b2} to a realizable value. Depending whether the LNA is used in WCDMA or in GSM mode, either of the input transistors is biased on while the other is off. The transistor, which is turned off has a negligible effect on the NF and the signals coming to the base of this transistor are shunted to chip ground. Therefore, the signals laying at the reception band of another standard and thus passing the preselection filter cannot desensitize the LNA. The LNA has two damped resonators, which are used as load in different modes. The resonance frequencies are 950 MHz and 2.1 GHz, respectively. The damping resistors $RL1$ (250 Ω) and $RL2$ (150 Ω) give a sufficient bandwidth for both mobile terminal and base station usage and tolerance against the different process variations without deteriorating the noise performance of the LNA. The -1 -dB bandwidths are 350 and 150 MHz for WCDMA and GSM resonators, respectively. The active output port and the load resonator of the LNA are selected with the biasing of the cascode transistors.

The LNA has two gain steps in both modes, which are implemented in the following manner. In the maximum gain, the LNA uses the damped resonator of the appropriate mode as a load. For example, in WCDMA mode, the Q1 acts as an input transistor, Q3 as a cascode, and $RL1$, $C1$, $L1$ as load. Depending on the chosen standard, the first gain step is realized by connecting another resistor in parallel with the resonator by closing the PMOS switch $S1$ or $S2$ to reduce the Q-value of the resonator. The sizing of the switch constitutes a tradeoff between on-resistance and parasitic capacitance, which both affect damping and resonant frequencies. The gain step is 3.2 dB in GSM mode and 2.8 dB in WCDMA mode at the resonant frequency, respectively. A larger gain step in the LNA is performed connecting the resonator tuned for the other mode as a load. In that case, the

TABLE II
MEASURED PERFORMANCE IN WCDMA AND GSM MODES

	WCDMA	GSM
NF(DSB) @max gain [dB]	4.3	2.3
NF(DSB) @min gain [dB]	15.9	12.3
Voltage gain max [dB]	33	39.5
Voltage gain min [dB]	6.5	12
IIP3 @max gain [dBm]	-14.5	-19
IIP3 @min gain [dBm]	-7	-7.5
IIP2 @max gain [dBm]	+34	+35
IIP2 @min gain [dBm]	+32	+34
ICP -1dB @max gain [dBm]	-25	-29
ICP -1dB @min gain [dBm]	-20	-23
LO-to-RF isolation [dB]	>58	>68
S11 [dB]	<-18	<-12
P(LO) [dBm]	-10	-10
Power dissipation [mW]	22.5	21.5
Supply voltage [V]	1.8	1.8
Chip area [mm ²]	3.5	3.5

trade off each other. The linearity of the input transconductors can be maintained since the drain currents through the devices do not need to be lowered. The additional dc currents, I_1 – I_2 , are fed through resistively degenerated long-channel PMOS transistors.

The bipolar switching transistors (Q1–Q4) are used as the functional mixer core instead of the respective NMOS transistors due to their lower flicker noise. In addition, the bipolars provide a higher f_T , which is required in order to achieve as symmetrical on-off switching as possible. Thus, the second-order distortion caused by the nonideal LO signal duty cycle is minimized. In addition, MOS switches typically require a larger swing to exhibit complete switching compared to bipolars. This relaxes the LO cross coupling and isolation performance. The mixers provide adjustable voltage conversion gain with three 4-dB gain control steps. The maximum voltage conversion gain is 14 dB. The gain control is implemented by switching additional resistor pairs between the mixer output terminals. The mixer has an RC lowpass pole at the output to relax the out-of-band linearity requirements of the following baseband stages and it is designed to drive a circuit as in [15].

The mixer has not been implemented and measured as a stand-alone circuit due to the uncertainties in the linearity measurements of a single direct-conversion mixer without an LNA and on-chip LO buffers [2]. Nevertheless, the comparison between the stand-alone simulations of the mixer and the measurements of the whole front-end match very well. The simulated IIP3 of the mixer is +10 and +8 dBm for WCDMA and GSM, respectively. The simulated double-sideband noise figure is 9.5 dB at both bands.

D. Layout

The microphotograph of the circuit is shown in Fig. 5. The designed front-end has been implemented using a 25-GHz f_T BiCMOS process with a 0.35- μ m minimum MOS gate length. The chip area is 3.5 mm² including the bonding pads. The two

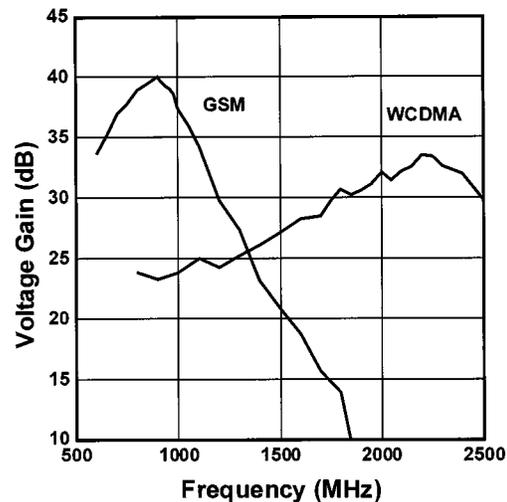


Fig. 6. Maximum gain responses on both modes.

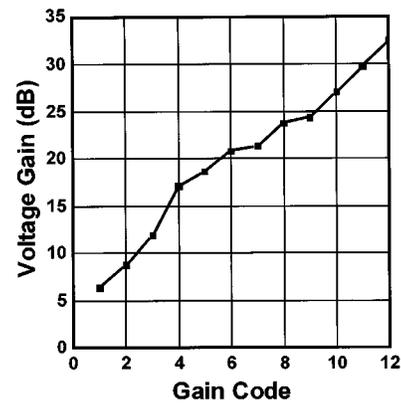


Fig. 7. Gain of WCDMA mode at different tuning codes.

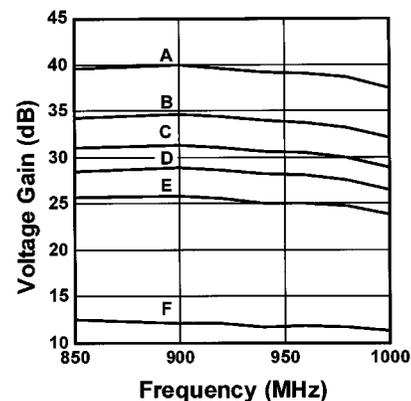


Fig. 8. RF response with six different gain settings in the GSM mode.

RF input pads are brought as close as possible to the LNA input transistors in order to minimize the wiring parasitics, which would affect NF and input matching. The LO and RF wiring are brought orthogonally to each other and grounded properly on both sides in order to achieve a good LO-to-RF isolation. Also, the LO and RF wiring do not overlap even in the commutating switches. The balanced mixers have been drawn as symmetric as possible to minimize the second-order distortion.

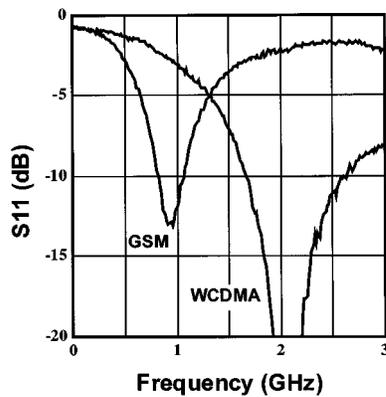


Fig. 9. Input matching on both bands.

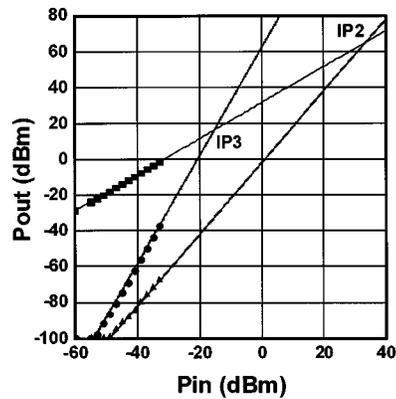


Fig. 11. Linearity of RF front-end in WCDMA maximum gain mode.

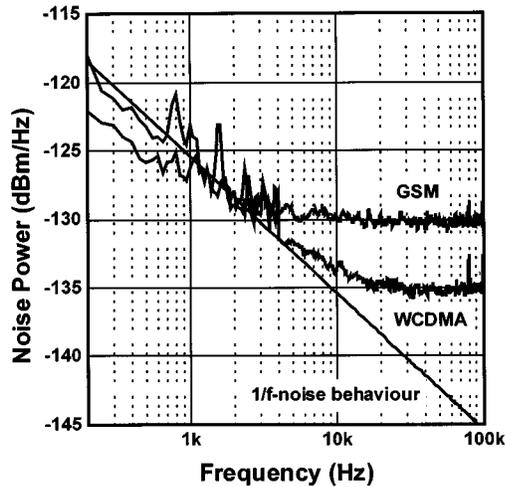


Fig. 10. Output noise power in WCDMA and GSM maximum gain settings.

IV. EXPERIMENTAL RESULTS

In direct-conversion receivers, the mixer output does not need to drive $50\text{-}\Omega$ impedance [8]. However, an external instrumentation buffer with a high input impedance was used to drive the $50\text{-}\Omega$ measurement equipment. The front-end chip was bonded directly on a high-frequency ceramic printed circuit board (RO4350), which is a compatible material with the standard FR4. All measurement results presented in this paper include the PCB. The main benefit of using RO4350 material compared to FR4 is its lower dissipation factor (0.0040), thus reducing the input losses.

The measured performance of the RF front-end is summarized in Table II. The RF responses of the both modes with the maximum gain settings are shown in Fig. 6. The simulated maximum gain was 39 dB in both modes. In GSM mode, this gain was achieved while in the WCDMA maximum gain was only 33 dB. Thus, the noise figure in WCDMA mode was also higher than expected according to the simulations. The difference between simulated and measured gain in WCDMA mode was due to inaccurate transistor models at higher frequencies. Instead, all other measured values matched very well to simulations. Fig. 7 illustrates all 12 possible gain values that can be achieved in WCDMA mode, while Fig. 8 shows the RF responses of six different gain settings in GSM mode. In Fig. 8,

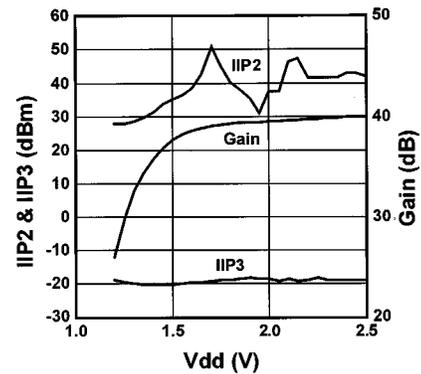


Fig. 12. Gain, IIP2, and IIP3 as a function of supply voltage in the GSM mode.

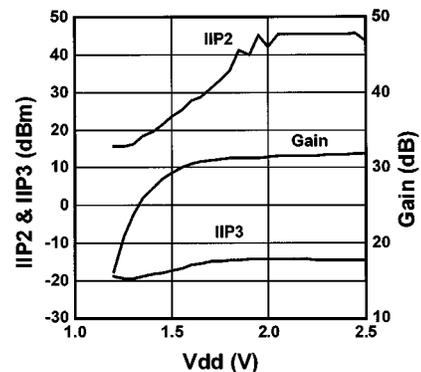


Fig. 13. Gain, IIP2, and IIP3 as a function of supply voltage in the WCDMA mode

curve A illustrates the maximum gain setting. Curves B–D show the mixer gain steps as the LNA gain is at maximum. Curves E and F present the LNA gain steps while the mixer has minimum gain. Total gain control range is 27 dB for both modes. The variation in the gain, due to the RF response, between the mobile station reception and base station reception bands is less than 1 dB in all settings. The input matching in Fig. 9 is independent of the front-end gain because the biasing of the input transistor remains the same with the different gain settings. The reported S11 values for GSM and WCDMA cover both mobile station and base station reception bands.

Fig. 10 illustrates the frequency response of the output noise power with maximum gain in both modes. The noise figures are 2.3 and 4.3 dB for GSM and WCDMA, respectively. The low-

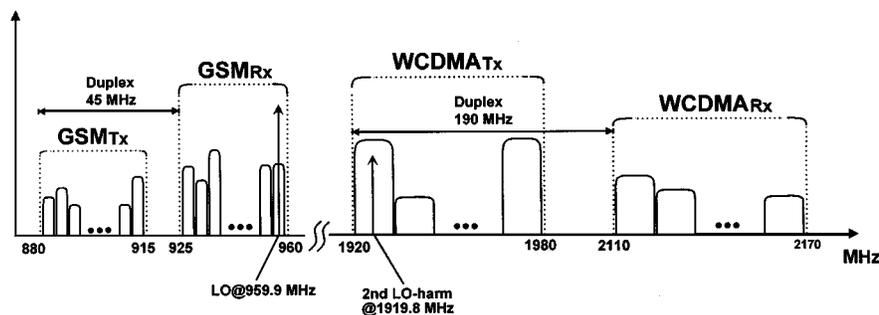


Fig. 14. Frequency bands of GSM and WCDMA showing a possible mixing between two bands.

flicker noise corner was achieved with bipolar LO switching transistors and with a sufficient gain in the front-end. The contribution of the flicker noise in the total noise figure is almost negligible even in the GSM. The measured noise figure in the GSM mode when integrated from 200 Hz to 100 kHz increases only by 0.2 dB compared to white noise. In WCDMA, the flicker noise is insignificant.

Several samples have been measured in order to achieve reliability in the measurement results. As the noise, gain, and third-order linearity performances remain almost constant from sample to sample, some variations in the second-order characteristics can be found. This obviously indicates a dependence on the circuit balance, i.e., device mismatch and symmetry. However, the worst IIP2 values, regardless of the mode, were found to be +32, while the highest were above +45 dBm. Fig. 11 illustrates the linearity of the front-end in WCDMA mode in the maximum gain. The effects of the supply voltage to gain, IIP2 and IIP3, are illustrated in Figs. 12 and 13 for GSM and WCDMA, respectively. To get some perspective of the front-end blocking performance, several tests with a large blocker were applied in both modes. The gain of the small wanted signal is compressed by 1 dB with a blocker of -32 dBm at 600/1600/3000 kHz offset and -27 dBm at 10/15 MHz offset from the wanted signal in GSM and WCDMA, respectively. A comparison of the results with the specifications reveals that the 3-MHz in-band GSM test blocker would probably fail. When comparing the results to specifications, it should be noted that the measurements do not include the preselection filter, which loss must be added to results and the test should be done with modulated signals.

A large input signal from the unselected standard can also desensitize the reception. This can happen when the signal from the other system is mixed with the spurious and harmonic tones of the operating standard. This can cause problems, particularly if the front-end has a single input for both standards, i.e., there would be a dual-band preselection filter. A situation in which the two standards selected can desensitize the front-end is illustrated in Fig. 14. It is assumed that the handset operates in the GSM mode. It is connected to the highest GSM band and receives at 959.9-MHz frequency. Simultaneously, there is a nearby mobile station connected to the lowest WCDMA band transmitting at the 1922.5-MHz center frequency. This channel can be strong and mix with the second harmonic of the LO signal, causing an unwanted harmonic in the reception band, thus desensitizing the signal reception. The out-of-band blocker

can be as high as 0 dBm, according to the GSM specifications [6]. No effect on the wanted GSM signal was measured with a -15 dBm input blocking signal. Thus, if the out-of-band attenuation of the WCDMA preselection filter at the reception band of the mobile station is 30 dB, the front-end would tolerate more than +15 dBm blocker. Hence, the problem is insignificant in this case.

V. CONCLUSION

A dual-band dual-mode RF front-end is presented in this paper. The front-end is applicable to WCDMA and GSM direct-conversion receivers. With the exception of the LNA input transistors and matching inductors, all on-chip devices are utilized in both modes. An on-chip active balun permits the use of single-ended RF input and double-balanced mixers. The balun provides a single-ended-to-differential conversion at a large frequency range required in multiband receiver with high linearity and acceptable noise. The converter uses a common-emitter and common-collector structure with a dummy transistor and separate supply pads to guarantee symmetrical output loads. The current boosting in quadrature mixers enables low voltage operation with sufficient gain, linearity, and noise. The power consumption from a single 1.8-V supply is only 22.5 mW. The 27-dB gain control range divided between LNA and mixers.

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REFERENCES

- [1] K. L. Fong, "Dual-band high-linearity variable-gain low-noise amplifiers for wireless applications," in *ISSCC Dig. Tech. Papers*, Feb. 1999, pp. 224–225.
- [2] S. Wu and B. Razavi, "A 900-MHz/1.8 GHz CMOS receiver for dual-band applications," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2178–2185, Dec. 1998.
- [3] J. Ryyänänen, K. Kivekäs, J. Jussila, and A. Pärssinen, "A dual-band RF front-end for WCDMA and GSM applications," in *Proc. Custom Integrated Circuits Conf.*, May 2000, pp. 175–178.
- [4] T. Hollman, S. Lindfors, M. Länsirinne, J. Jussila, and K. Halonen, "A 2.7 V CMOS dual-mode baseband filter for PDC and WCDMA," in *Proc. Eur. Solid-State Circuits Conf.*, Sept. 2000, pp. 176–179.
- [5] "3rd Generation Partnership Project (3GPP) Technical Specification Group (TSG) RAN WG4 UE Radio Transmission and Reception (FDD)," TS 25.101, vol. V3.1.0, 1999.

- [6] "Digital Cellular Telecommunications System (Phase 2+); Radio Transmission and Reception," GSM 05.05 V8.2.0, 1999.
- [7] B. Razavi, "A 2.4-GHz CMOS receiver for IEEE 802.11 wireless LAN's," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1382–1385, Oct. 1999.
- [8] A. A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1399–1410, Dec. 1995.
- [9] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 428–435, June 1997.
- [10] A. Pärssinen, J. Jussila, J. Rynnänen, L. Sumanen, K. Kivekäs, and K. Halonen, "A wide-band direct conversion receiver with on-chip A/D converters," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 2000, pp. 32–33.
- [11] A. Rofougaran, J. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF front-end IC for a direct-conversion wireless receiver," *IEEE J. Solid-State Circuits*, vol. 31, pp. 880–889, July 1996.
- [12] J. Crols and M. Steyaert, "A single-chip 900 MHz CMOS receiver front end with a high performance low-IF topology," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1483–1492, Dec. 1995.
- [13] A. Pärssinen, J. Jussila, J. Rynnänen, L. Sumanen, and K. Halonen, "A wide-band direct conversion receiver for WCDMA applications," in *ISSCC Dig. Tech. Papers*, Feb. 1999, pp. 220–221.
- [14] W. Sansen and R. Meyer, "An integrated wide-band variable-gain amplifier with maximum dynamic range," *IEEE J. Solid-State Circuits*, vol. SSC-9, pp. 159–166, Aug. 1974.
- [15] J. Jussila, A. Pärssinen, and K. Halonen, "A channel selection filter for a WCDMA direct conversion receiver," in *Proc. Eur. Solid-State Circuits Conf.*, Sept. 2000, pp. 236–239.



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