Jan Rautiainen

Quasistatic CV characterization: Overview and implementation of a complete measurement system with comparison to other CV methods

School of Electrical Engineering

Thesis submitted for examination for the degree of Master of Science in Technology.

Espoo 29.11.2015

Thesis supervisor:

Prof. Hele Savin

Thesis instructor:

M.Sc. (Tech.) Navneet Kumar

Aalto University
School of Electrical Engineering

AALTO UNIVERSITY
SCHOOL OF ELECTRICAL ENGINEERING

ABSTRACT OF THE
MASTER'S THESIS

Author: Jan Rautiainen

Title: Quasistatic CV characterization: Overview and implementation of a complete measurement system with comparison to other CV methods

Date: 29.11.2015 Language: English Number of pages:12+66

Department of Micro- and Nanosciences

Professorship: Semiconductor technology Code: S-69

Supervisor: Prof. Hele Savin

Instructor: M.Sc. (Tech.) Navneet Kumar

Capacitance-voltage measurements are a versatile tool for characterizing semiconductor-dielectric interfaces and can be used to determine dielectric film thickness, charge, and surface state density as well as other physical parameters. The measurements can be performed using charge-based quasistatic or impedance-based high-frequency methods. The parameters of the measured structure are then extracted by comparing the capacitance-voltage response of these different methods with each other or with the response of a theoretical model of an ideal structure. Alternatively a contactless corona charge-based characterization method can be used. In this thesis the different methods, each with their advantages and disadvantages, are compared. Additionally a comprehensive guide for performing these measurements and extracting physical parameters from the measured data as well as the necessary background physics are provided emphasizing quasistatic measurements. None of the covered methods could replace the others under all possible circumstances so comprehension of the strengths and weaknesses of the different methods is required. Quasistatic method has the advantage of measuring surface state density over a wider region in the semiconductor bandgap than the other methods. As a consequence a significant part of the measurements were dedicated to surface state density extraction and comparison of results with newer corona charge-based technology.

Keywords: Capacitance-voltage, CV, MOS, COCOS, semiconductor, thin film, charge, surface states

AALTO-YLIOPISTO
SÄHKÖTEKNIIKAN KORKEAKOULU

DIPLOMITYÖN
TIIVISTELMÄ

Tekijä: Jan Rautiainen

Työn nimi: Kvasistaattinen CV -karakterisointi: Yleiskatsaus ja kokonaisen mittausjärjestelmän toteutus sekä vertailu muihin CV -menetelmiin

Päivämäärä: 29.11.2015 Kieli: Englanti Sivumäärä:12+66

Mikro- ja nanotekniikan laitos

Professuuri: Puolijohdeteknologia Koodi: S-69

Valvoja: Prof. Hele Savin

Ohjaaja: DI Navneet Kumar

CV -mittaukset ovat monipuolinen työkalu puolijohteiden ja eristeiden välisten rajapintojen karakterisointiin, mahdollistaen kalvon paksuuden, varauksen, pintatilojen tiheyden ja muiden fyysisten parametrien määrittämisen. Mittaukset voidaan suorittaa kvasistaattisina tai korkeataajuuksisina. Mitatun rakenteen parametrit voidaan tämän jälkeen selvittää vertaamalla rakenteen kvasistaattisia tai korkeataajuisia CV -vasteita toisiinsa tai teoreettisen mallin ideaalisen rakenteen vasteeseen. Vaihtoehtoisesti voidaan käyttää kontaktitonta koronavarukseen perustuvaa karakterisointimenetelmää. Tämän diplomityön tarkoitus on vertailla eri menetelmien vahvuuksia ja heikkouksia. Lisäksi tarkoituksena on tarjota kattava hakuteos mittausten suorittamiseen, fyysisten parametrien määrittämiseen mitatusta datasta sekä vaadittava taustateoria painottaen erityisesti kvasistaattisia mittauksia. Yksikään käsitellyistä menetelmistä ei kyennyt korvaamaan muita kaikissa mahdollisissa olosuhteissa joten eri menetelmien vahvuuksien ja heikkouksien tunnistaminen on välttämätöntä. Kvasistaattisen menetelmän etuna on pintatilatiheyden määrittäminen laajemmalta osalta puolijohteen kiellettyä energia-aluetta muihin menetelmiin nähden. Tämän vuoksi tulosten käsittelystä huomattava osa on omistettu pintatilatiheyden määrittämiseen mittaustuloksista ja tulosten vertailuun uudemman koronavarausteknologian kanssa.

Avainsanat: Kapasitanssi-jännite, CV, MOS, COCOS, puolijohde, ohutkalvo, varaus, pintatilat

Acknowledgements

I would like to thank Hele Savin for giving me the opportunity to complete this thesis in the Electron Physics Group (EPG) and the time and effort spent in supervising this thesis. I would also like to thank Navneet Kumar for his time and efforts as my thesis instructor.

Special thanks to Antti Haarahiltunen for helping me make significant progress during the difficult initial stages of the measurements.

Even the best data does little good unless presented clearly and efficiently (So imagine how useful mine would have been!), therefore I wish to thank Tapani Pihlajamäki for introducing me to Tikz and PGFplots, helping get started with them as well as his general help with LaTeX.

I also wish to thank Guillaume von Gastrow, Heli Seppänen, Yameng Bao, and Päivikki Repo from EPG in no particular order for the useful data and source material they provided me with.

Big thanks to Annastiina Raunio and Juha Heinonen for proofreading my thesis and helping me transform my caveman text into something legible.

Finally, I wish to thank Annastiina Raunio, my family, and everyone who showed their interest and support towards my work.

Otaniemi, 29.11.2015

Jan Rautiainen

Contents

Abstract . . . ii
Tiivistelmä (in Finnish) . . . iii
Acknowledgements . . . iv
Contents . . . v
Abbreviations . . . vii
Symbols . . . viii
List of Figures . . . x
List of Tables . . . xii

1 Introduction **1**

2 Theory **3**
2.1 MOS CV curve . . . 3
2.1.1 MOS junction and initial band bending . . . 3
2.1.2 MOS regions of operation . . . 4
2.2 CV characterization . . . 8
2.2.1 Fundamental physical parameters of the MOS structure . . . 8
2.2.2 Circuit equivalent of a MOS structure . . . 11
2.2.3 Theoretical CV curve of the ideal MOS . . . 13
2.2.4 Extraction of physical parameters . . . 17
2.3 Instrumentation for CV measurements . . . 22
2.3.1 Charge- and current-based CV measurement . . . 23
2.3.2 Impedance-based CV measurement . . . 29
2.3.3 Cabling and error compensation . . . 30

3 Measurements **32**

3.1 Operating the ICS 3.5.1 32

3.2 Sample preparation and practical phenomena 38

3.2.1 Contact preparation 38

3.2.2 Noise comparison between gate- and substrate-connected bias 38

3.2.3 Effects of delay time in low-frequency CV 39

3.2.4 Noise filtering from the measured data 41

3.2.5 Hysteresis 42

3.2.6 Leakage current 43

3.3 Results 44

3.3.1 Parameter extraction from measured data 44

3.3.2 Extracted parameters for measured samples 50

3.3.3 Comparison with COCOS results 51

4 Conclusion **54**

Bibliography **58**

A Theoretical CV curve (MATLAB) **59**

B Berglund integral (MATLAB) **62**

C Curve smoothing (MATLAB) **64**

D V_G Second derivative (MATLAB) **65**

Abbreviations

AC	Alternating current
ALD	Atomic layer deposition
Al_2O_3	Aluminum oxide
AlN	Aluminum nitride
CO_3^-	Carbon trioxide
COCOS	Corona oxide characterization of semiconductors
CPD	Contact potential difference
CV	Capacitance-voltage
DC	Direct current
FFT	Fast Fourier transform
H_3O^+	Hydronium
HF	High-frequency
HfO_2	Hafnium oxide
ICS	Interactive Characterization Software
IV	Current-voltage
LF	Low-frequency
MIS	Metal-insulator-semiconductor
MOS	Metal-oxide-semiconductor
MOSCAP	Metal-oxide-semiconductor capacitor
n-Si	N-type doped silicon
polySi	Polycrystalline silicon
p-Si	P-type doped silicon
QV	Charge-voltage
RF	Radio frequency
Si	Silicon
SiO_2	Silicon oxide
SMU	Source-measure unit
TiO_2	Titanium oxide

Symbols

A	Gate area
B	Susceptance
C	Capacitance
C_{acc}	Accumulation layer capacitance
C_{dep}	Depletion region capacitance
C_{inv}	Inversion layer capacitance
C_F	Fixed capacitance (QV and feedback charge methods)
C_{FB}	Flat band capacitance
$C_{hf,min}$	Minimum value of high-frequency capacitance
$C_{hf,m}$	Measured high-frequency capacitance
C_{it}	Interface state capacitance
C_{lf}	Low-frequency capacitance
C_{MOS}	MOS capacitance (when part of a circuit with other capacitances)
C_{ox}	Oxide capacitance
C_S	Semiconductor surface capacitance
$C_{S,hf}$	Semiconductor high-frequency surface capacitance
C_L	Semiconductor high-frequency surface capacitance (Lindner approximation)
$C_{S,lf}$	Semiconductor low-frequency surface capacitance
D	Dissipation constant (high-frequency measurements)
D_{it}	Interface state density
E_0	Neutral level (interface states)
E_C	Conduction band energy
E_F	Fermi energy
E_g	Bandgap energy
E_V	Valence band energy
F	Unitless electric field
G	Conductance
J	Current (COCOS method)
k	Boltzmann constant
N	Dopant density (acceptor or donor)
N_A	Acceptor dopant density
N_D	Donor dopant density
n_i	Intrinsic carrier density
q	Elementary charge
Q	Charge

Q_C	Corona charge (COCOS method)
Q_S	Semiconductor surface charge
Q_{fix}	Fixed (oxide) charge
Q_m	Mobile (oxide) charge
Q_{it}	Surface state charge
Q_{ot}	Oxide trapped charge
Q_{ox}	Oxide charge (any type)
R	Resistance
R_{MOS}	MOS resistance (when part of a circuit with other resistances)
t_{delay}	Delay time (feedback charge method)
t_{ox}	Oxide thickness
T	Temperature
u_B	Normalized semiconductor bulk potential
u_S	Normalized semiconductor surface potential
v	Normalized band bending
V	Voltage
V_0	Output voltage
v_m	Match point for band bending (Lindner approximation)
V_{CPD}	Contact potential difference (COCOS method, equivalent of Φ_{GS})
$V_{CPD,d}$	Contact potential difference in dark (COCOS method)
$V_{CPD,i}$	Contact potential difference under illumination (COCOS method)
V_{FB}	Flat band voltage
V_G	Gate voltage
$V_{G,0}$	Gate voltage initial point (Berglund integral)
V_{ox}	Voltage over the oxide
V_S	Band bending (COCOS method, equivalent of ψ)
X	Reactance
Z	Impedance
Z_O	Short circuit impedance (high-frequency measurements)
Z_S	Short circuit impedance (high-frequency measurements)
ε_0	Vacuum permittivity
ε_r	Dielectric constant
ε_S	Semiconductor electric permittivity
θ	Phase angle (high-frequency measurements)
λ_i	Intrinsic Debye length
λ_N	Extrinsic Debye length
ϕ_B	Semiconductor bulk potential
ϕ_S	Semiconductor surface potential
Φ	Contact potential
Φ_G	Gate work function
Φ_{GS}	Gate-substrate contact potential
Φ_S	Substrate work function
χ	Electron affinity
ψ	Band bending
ψ_0	Band bending initial point (Berglund integral)
ω	Voltage frequency (radians)

List of Figures

1.1 MIS structure 1

2.1 Initial band bending without bias voltage 5
2.2 CV curve of an ideal p-type MOS 6
2.3 MOS energy bands in different regions of operation 6
2.4 Surface states 9
2.5 Circuit equivalent of a MOSCAP 11
2.6 Effects of gate area, oxide thickness, and doping density to the fringing field 12
2.7 Effects of doping density and oxide thickness on the CV curve 16
2.8 Obtaining the relation of band bending and gate bias $\psi(V_G)$ using the Terman method 18
2.9 Obtaining flat band voltage by curve fitting 20
2.10 Ramp method 23
2.11 QV method 24
2.12 Feedback charge method 25
2.13 Feedback charge method. Delay time and measured waveform 25
2.14 Common Q/t curves 26
2.15 Circuit equivalents of common Q/t curves 26
2.16 Corona deposition on the sample surface 27
2.17 Contact potential difference as a function of corona charge 28
2.18 AC impedance meter 29
2.19 AC impedance 30
2.20 Connection of the coaxial cable shields 31

3.1 Choosing the measurement instruments 32
3.2 List of measurement instruments 32

3.3 Entering the measurement setup menu 33
3.4 Measurement setup 33
3.5 Selecting the measured sample device 33
3.6 Choosing the measurement instrument 34
3.7 Setting up the SMUs for KI595 34
3.8 Setting up the SMUs for HP4192 34
3.9 Additional options setup 35
3.10 Measurement parameters for KI595 35
3.11 Measurement parameters for HP4192 36
3.12 Measurement icon 36
3.13 Initiating the measurement 36
3.14 Autoscaling the curve 37
3.15 Bias voltage connected to gate 38
3.16 Bias voltage connected to substrate 39
3.17 Delay time effects on inversion capacitance and vertical shifting 40
3.18 Delay time effects on inversion capacitance, vertical shifting and noise . . . 41
3.19 Second derivatives of smoothed CV curves 42
3.20 Hysteresis in HfO_2-Si 43
3.21 TiO_2-Si conduction band 43
3.22 Leaking TiO_2-Si MOS 44
3.23 Measured Al_2O_3-Si CV and Q/t 45
3.24 Measured Al_2O_3-Si CV with theoretical curve 47
3.25 Second derivatives from smoothed CV curves 48
3.26 Measured Al_2O_3-Si D_{it} 49
3.27 Measured Al_2O_3-Si CV before and after annealing 51
3.28 COCOS measured Al_2O_3-Si CV before and after annealing 51
3.29 D_{it} curves of the before-anneal sample displaying the effects of curve smoothing 52
3.30 Contact CV and COCOS measured D_{it} before and after annealing 52

List of Tables

2.1 Flat band voltages calculated with equation 2.44 21

2.2 Flatband voltages calculated with equation 2.45 21

2.3 Gate-substrate potential differences Φ_{GS} in Al-SiO_2-Si structure 22

3.1 Parameters for minimum and maximum oxide thickness 46

3.2 Summary of parameters for sample 6A 49

3.3 Parameters for all measured samples 50

Chapter 1

Introduction

The metal-insulator-semiconductor (MIS) capacitor is a layered structure consisting of a doped semiconductor substrate, an insulating layer, and a conductor layer called gate. The cross section of a MIS structure is presented in figure 1.1.

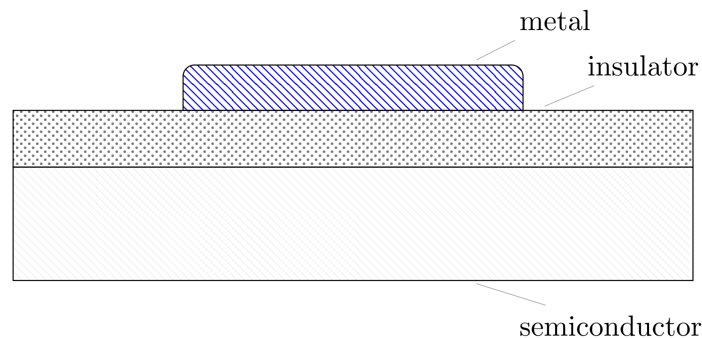


Figure 1.1: MIS structure.

The insulating layer is usually an oxide. The oxide can be grown by oxidizing the top layer of the semiconductor substrate eg. thermally grown silicon dioxide SiO2 or by external deposition eg. atomic layer deposition (ALD) of aluminum oxide Al2O3. The oxide not only acts as an electric insulator between the top and bottom layers, but also passivates the semiconductor surface. In the advent of MIS technology a metal, typically aluminum, was used as the gate material on top of the oxide layer, hence the more commonly encountered name metal-oxide-semiconductor (MOS). In the mid 1970s metals gave way to polycrystalline silicon (polySi) as the material of choice because the higher melting point of polySi allowed higher temperatures to be used in other process steps facilitating device fabrication. The forfeit of metal from the structure also eliminated the possibility of unwanted diffusion. However, for historical reasons the term MOS persisted even after metal gates were no longer used. Lately metal gates have regained popularity since Intel reintroduced them in 2007 together with 45 nm process and hafnium oxide replacing silicon oxide. The MOS capacitor (MOSCAP) is one of the simplest electronic devices and while it is not widely used in itself, as a voltage controlled capacitor, it is the building block of larger entities such as the MOS transistor, which is ubiquitous in today's world.

The basic principle of capacitance-voltage (CV) measurement is to apply a bias voltage

sweep over MOS to obtain a capacitance curve as a function of voltage. Contact CV measurements can be performed using charge-based quasistatic or impedance-based high frequency measurements. By comparing the CV data from these two different methods with each other or with a theoretical model of an ideal structure various parameters of the MOS structure can extracted.

The increased computational power available has enabled increasingly complex and detailed modeling of the MOS structure and its CV characteristics. These new models are often required to include quantum mechanical phenomena as the dimensions of individual devices are approaching the scale of tens of atoms. The most significant of these quantum effects is leakage current, caused by quantum tunneling through the oxide barrier in the sub 10 nm scale.

Physical parameters that can be obtained from CV characterization include but are not limited to oxide thickness, different kinds of charge trapped in the MOS structure, band bending in the semiconductor, and density of surface states in the semiconductor-dielectric interface. Contact CV measurement can detect capacitances from 10^{-14} F to 10^{-6} F, dielectric thicknesses from 10 nm to 1000 nm, surface state densities of $10^{10}/\mathrm{eV/cm}^2$ to $10^{13}/\mathrm{eV/cm}^2$, oxide charges from $5{\cdot}10^9/\mathrm{cm}^2$ to $10^3/\mathrm{cm}^2$, and doping profiles from $10^{14}/\mathrm{cm}^3$ to $10^{18}/\mathrm{cm}^3$ down to depths of 10 nm to 10 μm. [1]

CV measurements are a simple and efficient tool for determining various physical properties of semiconductor-dielectric thin film interfaces, which form the basis for modern electronics and photovoltaics devices. CV characterization has been widely used since the 1960s and despite its old age it continues to be an essential tool for research and industry alike. While the principles of contact CV measurement have remained unchanged, the limits of the technique have been constantly pushed further by developments in accuracy and resolution of measurement devices. Conventional contact CV has been challenged by the corona oxide characterization of semiconductors (COCOS), in which the metal gate is replaced by a corona charge deposition. Since preparation of a gate is not required the COCOS method offers significant advantages in speed and convenience. As an added benefit the method is less vulnerable to leakage current through the dielectric. However, as in any craft, one tool is rarely the best for all needs. The purpose of this thesis is to provide a comparison between different CV characterization methods, as well as a comprehensive guide for performing these conventional contact CV measurements with an emphasis on the quasistatic method.

Chapter 2 provides the theoretical background necessary for understanding MOS CV response, the means to calculate the response of an ideal MOS structure, as well as an overview of different measurement methods and their effects on the resulting data. Chapter 3 contains hands-on guidance for performing CV measurements and parameter extraction from the measured data. Chapter 4 concludes with a brief summary of the possibilities and limitations offered by the different methods, as well as suggestions for future improvements.

Chapter 2

Theory

2.1 MOS CV curve

Before studying MOSCAP behavior under different bias voltage conditions, a basic comprehension of the MOS junction band diagram at zero bias in thermodynamic equilibrium is beneficial. For the sake of simplicity, and to avoid using the two similar looking words "conductor" and "semiconductor", a metal gate is assumed. Nevertheless the theory in this chapter will also hold for polySi and other conductor gates.

2.1.1 MOS junction and initial band bending

When the bulk metal and semiconductor are brought together into contact the band bending in semiconductor surface resembles that of a Schottky diode. If the density of interface states D_{it} in the semiconductor is low, the Schottky-Mott model can be used to determine the type of band bending. Interface states and their effects will be discussed in more detail later in this chapter. Using the Schottky-Mott model the band bending will be determined by the electron affinity χ and bandgap E_g of the semiconductor, potential loss over the oxide insulator, and Fermi levels E_F of the gate and semiconductor. For both materials the position of Fermi level is directly expressed by the work function $q\Phi$. In a doped semiconductor Fermi level is a function of dopant density and type, donor or acceptor, as well as temperature. Room temperature is assumed in the derivations of this thesis so the semiconductor Fermi level will be decided by the type and amount of doping. The semiconductor electron affinity is an inherent material property, affected by crystal termination in the interface, but unaffected by doping.

The purpose of this section is to study MOSCAP before any external bias is applied, at zero bias equilibrium conditions, so the Fermi levels of gate and semiconductor have to be aligned. A MOSCAP behaves as a Schottky barrier with an interposed dielectric [2]. As with the Shottky barrier, the band bending is caused by the electric field, which arises in the interface as Fermi levels align. Since the electric field cannot penetrate the metal gate, all of the band bending occurs also in the semiconductor side. In a Shottky barrier the potential from the work function difference of gate and substrate $\Phi_G - \Phi_S$ directly

translates to semiconductor band bending ψ so that

$$\Phi_G - \Phi_S = -\psi\,. \tag{2.1}$$

However, in a MOSCAP a part of the potential is lost over the dielectric reducing the amount of band bending. The amount of potential lost over the dielectric V_{ox} depends on the dielectric layer thickness and permittivity. The external bias required to counteract the potential loss over the dielectric and the band bending is the flat band voltage

$$V_{FB} = \Phi_G - \Phi_S = -V_{ox} - \psi\,. \tag{2.2}$$

Another key difference is that the dielectric also acts as a near perfect insulator, so current across the junction is zero. Since current is zero Fermi levels must be flat because current is proportional to the gradient of the Fermi level.

Band bending at zero bias for p-type and n-type semiconductors joined with high- and low work function metals is illustrated in figures 2.1a, 2.1b, 2.1c, and 2.1d [3] [2]. In these figures the low $q\Phi$ gate has a work function of 4.1 eV which corresponds to aluminum and the high $q\Phi$ has a work function of 5.3 eV which is close to that of gold. Work functions for p-type and n-type silicon are 5 eV and 4.4 eV respectively corresponding to a dopant density of $1.4 * 10^{15}/\mathrm{cm}^3$ at 290 K°. The dielectric is SiO_2 with an E_g of 9 eV [4]. The choice of zero level in these energy band diagrams is arbitrary since only energy differences matter. An electrical ground or earth referenced Fermi level is a good, common choice for zero level, because its practically infinite reservoir of charge is unaffected by charge transfer and it can be considered to be in good thermodynamic equilibrium.

The only purpose of the Schottky-Mott model approach is to provide an overview of which way the bands will bend initially, before any external bias voltage is applied. In practice, its suitability for qualitative study is questionable, not only because the effects of interface states, but also because work functions are dependent on crystal orientation, surface relaxation effects, and chemical bonds formed between the two materials at the interface. [3]

2.1.2 MOS regions of operation

After examining the initial conditions at zero bias we can now start applying bias voltage to identify the different regions of operations for the MOS. In the following description of the regions of operation, negative bias voltage refers to gate being at lower, and positive at higher potential than substrate. Before identifying different regions of the MOS CV curve the capacitance of the CV curve has to be defined. For a linear capacitor such as a tuning capacitor in electronics the definiton is

$$C_{stat} = \frac{Q}{V_G} \tag{2.3}$$

where Q is the total charge and V_G is the bias voltage. However, for a nonlinear capacitor such as MOS this is not the case. In this thesis the capacitance in all the following equations will refer to differential capacitance

$$C = \frac{dQ}{dV_G}\,. \tag{2.4}$$

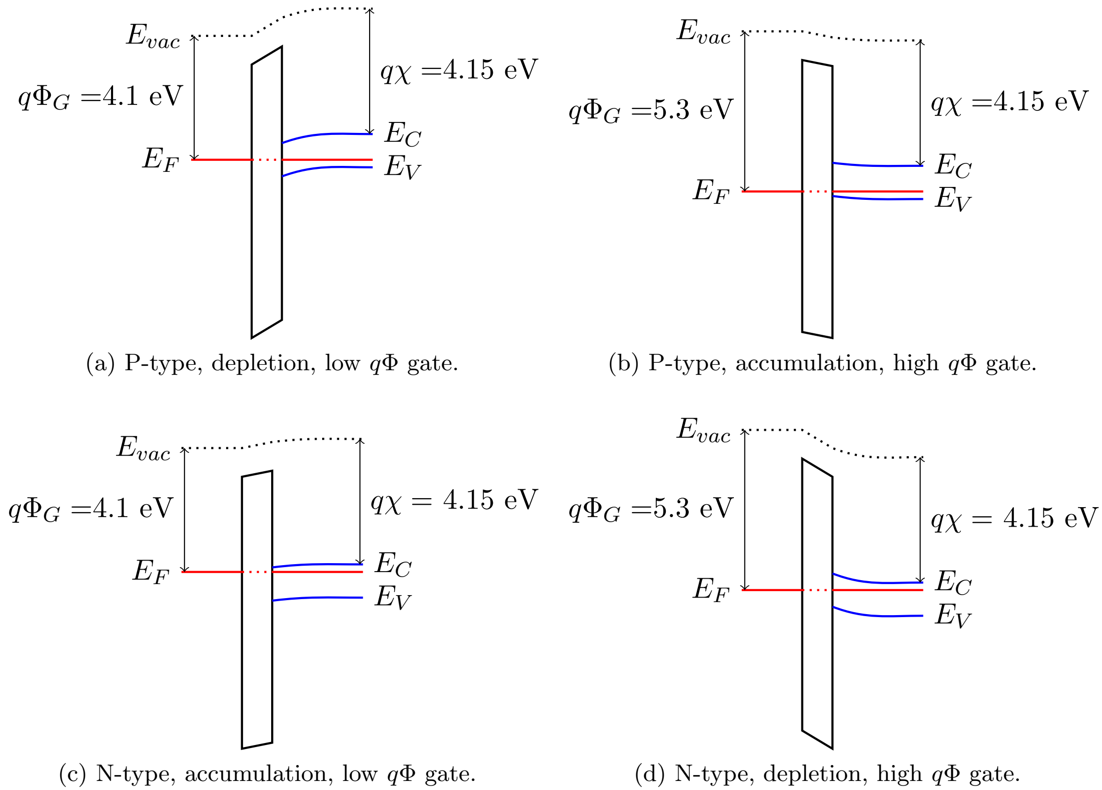


Figure 2.1: Initial band bending without bias voltage. Gate on the left, semiconductor on the right. Energy levels are drawn to scale. [5] [4]

Theoretical high- and low-frequency response CV curves of an ideal p-type MOSCAP are presented in figure 2.2 illustrating the different regions of operation. Band structures of respective regions of operation for a p-type MOSCAP are presented in figure 2.3 [4]. It should be noted that an ideal MOSCAP has no contact potential difference between the gate and substrate. Because the Fermi levels in both sides of the dielectric are already aligned there is no Fermi level shifting in the semiconductor and the energy bands stay flat. Since the bands stay flat an ideal MOSCAP is in flat band condition under zero external bias. The energy bands in figure 2.3 are therefore not those of an ideal MOSCAP, but instead indicate a low work function gate, such as in figure 2.1a eg. Al-SiO_2-p-Si MOSCAP. Physical parameters that can be extracted from the CV curve are discussed in more detail in chapter 2.2, different high- and low-frequency measurement techniques in chapter 2.3.

Accumulation

In accumulation region the majority charge carriers of the semiconductor form a layer of high carrier density at the semiconductor surface. In the case of p-type semiconductor this layer of charge will be positive and comprised of holes. To achieve accumulation, a negative bias must be applied to the gate to bend energy bands in the semiconductor upwards. In the case of p-type substrate and high work function gate as in figure 2.1b, the valence band bends above the Fermi level at the interface and the MOS is already in accumulation, even without external bias. For an n-type substrate the accumulation

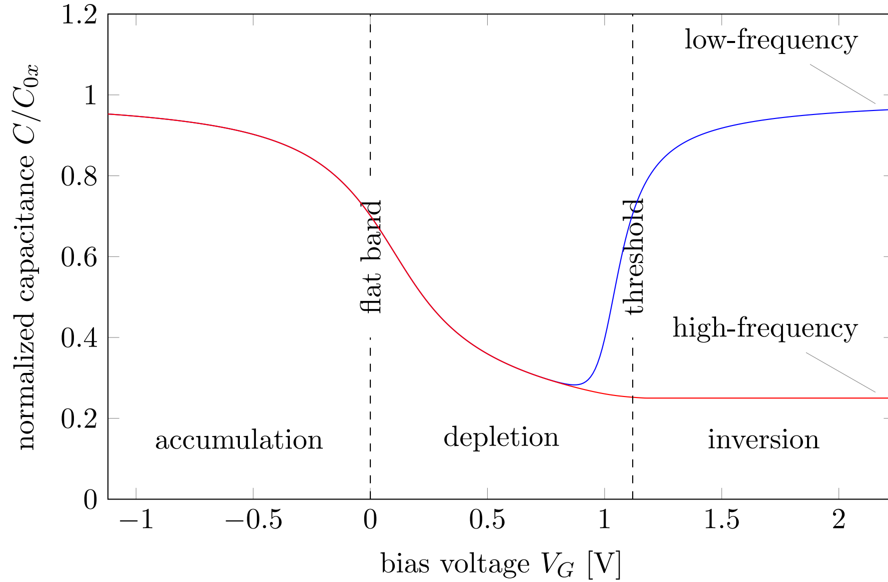


Figure 2.2: CV curve of an ideal p-type MOS.

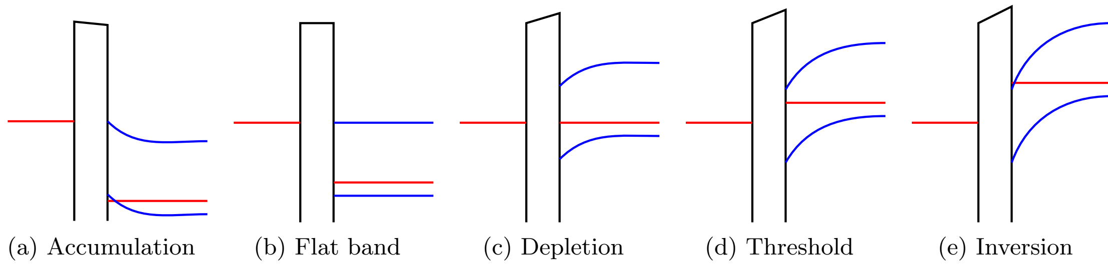


Figure 2.3: Gate on the left, semiconductor on the right. Work functions of the gate and semiconductor are not equal under flat band condition so the structure is not an ideal MOS.

charge layer will be negative and comprised of holes. Electrons are attracted to the surface by applying a positive gate voltage, which bends the energy bands downwards. In case of n-type substrate and low work function as in figure 2.1c the conduction band bends below the Fermi level resulting an accumulation without external bias as with the p-type example above. As the surface in accumulation gains increased conductivity due to the large number of available carriers a depletion region is formed in the bulk from where the carriers are drained.

Flat band

Between the accumulation and depletion regions, at a specific bias voltage is the flat band condition. As the name implies, the conduction and valence bands in semiconductor are flat and exhibit no bending at the interface. Because the bands are flat the potential at the semiconductor surface equals the potential in the bulk, thus there is no electric field in the semiconductor. The MOS structures is figures 2.1a and 2.1c would require a negative gate

voltage to achieve flat band condition. Likewise an opposite, positive voltage is required for the structures of 2.1b and 2.1b for the same result.

Depletion

In depletion region the semiconductor surface is depleted of free charge carriers. Using a p-type example, the positive gate bias repels holes from the semiconductor surface, leaving only the immobile, negative acceptor dopant ions into the depletion layer. However, because the ionized acceptors are immobile they cannot act as charge carriers and conductivity of the surface drops. Since charge neutrality has to be maintained, increasing the bias voltage further causes the depletion layer to extend deeper into the bulk as more negative charge, in the form of immobile acceptors, is required to counteract the increasing positive gate charge. On the other hand, increase of doping density makes the depletion layer shallower as more acceptor charge is available per unit volume to balance out the gate charge. In the band diagram depletion region appears as the Fermi level being closer to middle of the bandgap than conduction or valence band at the interface. MOS structures in figures 2.1a and 2.1d are in depletion region without external bias voltage.

Threshold and inversion

As the gate voltage in our p-type example is increased further, a layer of free electrons starts to form into the semiconductor surface. In an n-type sample respectively an increasingly negative gate voltage would yield a layer of holes. When the number of minority carriers reaches the number of dopant ions the semiconductor is in the threshold of inversion. In the threshold band diagram in figure 2.3d this condition manifests as distance from E_C to E_F in the surface being equal to distance from E_F to E_V in the bulk. In inversion the minority carrier concentration has exceeded the dopant concentration. Using our p-type example the negative charge from increasing electron concentration becomes so high that the surface is inverted to n-type. In strong inversion the depletion layer reaches its maximum depth as the inversion charge in the surface prevents the electric field from reaching deep into the bulk and prevents the depletion layer from growing further. In accumulation and depletion the majority carrier flow in and out of the semiconductor depletion layer determines the MOSCAP capacitance response to AC gate voltage. As long as the period of the AC gate voltage is much longer than the dielectric relaxation time of the semiconductor substrate majority carriers will follow the changes of AC electric field [6]. In inversion however, the response is determined by minority carriers. The minority carriers are slowly formed through thermal and photoelectric recombination and generation processes, which cause the low- and high-frequency CV curves to diverge in inversion. The relaxation times naturally vary between materials but generally frequencies below 10 Hz can be considered low and frequencies above 10 kHz can be considered high.

Deep depletion

Deep depletion region occurs when gate voltage is swept too quickly for inversion layer to form. With no minority carriers available, the charge neutrality must be satisfied by ionized dopants alone. In order to supply the growing demand for ionic charge the depletion layer

extends beyond its thermal equilibrium maximum width and capacitance falls below the high-frequency minimum. Since the structure is not in thermal equilibrium deep depletion is only a temporary state unlike the other regions of operation. Deep depletion ends either when minority carrier generation in the depletion layer reaches the rate required for steady state, or an avalanche breakdown ensues. If voltage sweep is stopped before the avalanche breakdown happens, minority carrier generation eventually restores thermal equilibrium and capacitance returns to its inversion value. [6]

2.2 CV characterization

In order to extract physical parameters any two of these three curves are needed: a theoretical CV curve, a low-frequency CV curve, or a high-frequency CV curve. The choice of these two curves determines the methods used. This section will first focus on identifying and quantifying various physical parameters from the way in which they deform or shift the theoretical curve, and afterwards presenting the assumptions upon which the ideal MOS model is based and deriving its theoretical curve. Different CV measurement methods, their physical principles, strengths and weaknesses are discussed in more detail in section 2.3 of this chapter.

2.2.1 Fundamental physical parameters of the MOS structure

Physical parameters that can be extracted from the CV curve can be divided to oxide, interface and semiconductor properties. Important oxide properties such as oxide permittivity, thickness and charge can be easily obtained. Interface state density and distribution are the only interface properties covered in this thesis, but also the most important interface quality metrics. Semiconductor surface capacitance is used for the theoretical curves, but it is not considered an interesting property from a measurement point of view, since it is affected mainly by semiconductor permittivity, which is usually known beforehand and can be acquired from literature. The utility of CV measurements can be further expanded by other auxiliary measurements to obtain properties such as surface state conductance or carrier lifetime, but these auxiliaries are not discussed within the scope of this thesis.

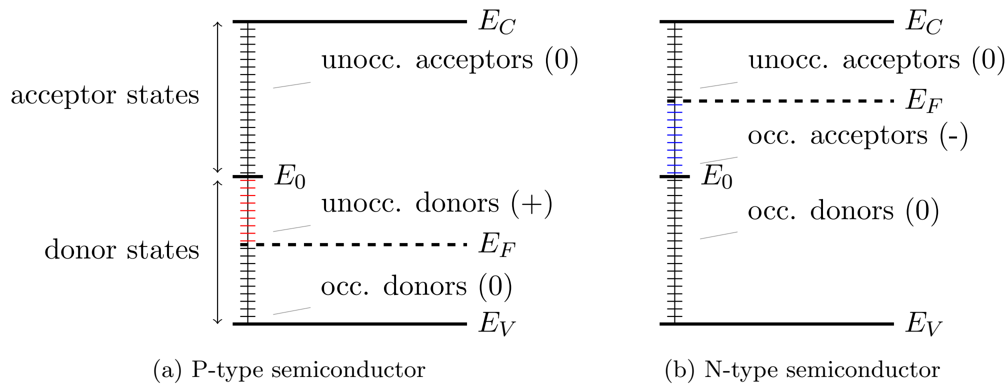
Doping type and profile

The type of semiconductor doping can simply be deduced from the high-frequency curve. A p-type substrate will go from accumulation to inversion, or as seen in a CV curve in figure 2.2 from high capacitance to low respectively, as the bias is swept from negative to positive. For n-type substrates the behavior will be opposite. In order to accurately probe the doping concentration profile, the effects of free charge carriers have to be mitigated, because CV characterization is measuring differential change in charge produced by differential change in voltage, and free carrier concentrations depend exponentially on bias voltage. Ionized dopant concentrations on the other hand, contribute only as a prefactor to the exponential term. Therefore dopant concentration cannot be obtained accurately in accumulation or inversion. Depletion region is required for probing, and maximum probing depth is the maximum depletion layer depth. For this reason deep depletion region is ideal for

probing the dopant concentration profile as it can extend the depletion layer depth beyond its equilibrium state maximum value. Probing depth is then limited to the maximum attainable depletion layer depth before avalanche breakdown.

Surface state density

Surface states are energy states in the bandgap. As name implies they exist only in the material interface, decaying quickly after only a few atomic layers into the bulk. In bulk the energy bands and the forbidden regions, bandgaps, separating them arise from the periodicity of the crystal lattice. In surface the periodic structure is terminated and the loss of periodicity leaves the surface atoms to complete the resulting dangling bonds without all the neighboring atoms that would be available in a bulk site. These dangling bonds behave like donor and acceptor levels behave in the bulk, some of them donating, some of them capturing electrons and becoming positively or negatively charged in the process. Both types of surface states may exist simultaneously in the same interface and are separated by the neutral level E_0 in the energy level diagram. An energy band diagram of a semiconductor surface is presented in figure 2.4.



(a) P-type semiconductor (b) N-type semiconductor

Figure 2.4: Surface states. For simplicity surface state density is assumed to be constant over the entire energy range of the bandgap, which usually is not a valid approximation.

Acceptor states are located above the neutral level E_0 and donor states below [7]. Donor levels are neutral when occupied and positively charged when unoccupied. Acceptor levels are negatively charged when occupied and neutral when unoccupied. Therefore if Fermi level resides precisely at E_0 the surface is charge neutral. For Fermi levels below E_0 the surface will be positively charged, correspondingly Fermi levels above E_0 will lead to a negatively charged surface. Since the added surface charge has to come from somewhere, if Fermi level is not aligned with E_0, even a bare semiconductor surface in vacuum will have a depleted region.

Because Fermi level moves with gate bias, surface state occupancy is bias dependent. Without surface states the gate charge would be balanced by accumulation or inversion charge alone, however when surface states counteract a part of the gate charge less accumulation or inversion charge from the semiconductor side is needed to reach charge neutrality. To compensate for this, and to reach the same level of accumulation or inversion charge as without surface states, gate voltage has to be increased further. At very high

levels of surface state density D_{it} most of the gate bias is compensated by charge in surface states and even substantial 4-5 V change in gate bias will produce a negligible 0.1 V change in band bending. The Fermi level is then effectively "pinned" to the neutral level E_0.

Surface states affect the CV curve by stretching it horizontally along the voltage axis, and by introducing an additional capacitive component C_{it}, which is mostly visible as an increase of total capacitance in depletion and high-frequency inversion regions. The uniformity of stretching along the bias range depends on the energy dependence of D_{it}. If D_{it} has low energy dependence so that it is effectively constant over most of the bandgap, the stretching will be uniform. If D_{it} changes abruptly as a function of energy the stretching of the CV curve will be uneven along the bias axis, adding plateus where D_{it} is highest and steepening the slope of the CV curve closer to the value of ideal $D_{it} = 0$ MOS where D_{it} is lowest. The sharpness of D_{it} induced features depend on temperature in which the measurement is performed. At very low temperatures The Fermi-Dirac distribution approaches a step function with the step located at Fermi level so that a very narrow, discrete level of energy in the bandgap is probed at each value of gate bias. At 300 °K however, the Fermi-Dirac distribution is no longer a step function, but a slope that extends approximately 0.05 eV to both sides of the Fermi level. This results in the features of $D_{it}(E)$ profile being smoothed over the width of a 0.1 eV sliding window. Also as a direct consequence, probing closer than 0.05 eV to a band edge will result in state density of the band edge interfering with measured D_{it} values. However, if a low temperature is desired for a sharper $D_{it}(E)$ profile the effects of carrier freeze-out should also be considered. [8] [6]

In order to remove the C_{it} effects of surface states from the measurement, a high-frequency CV curve has to be measured using a high enough (≈100 MHz) frequency so that surface states are unable to respond within a period of the AC gate voltage. However, surface states will still be able to follow the bias voltage so the horizontal stretching effect will remain. The elimination of stretching from the CV graph requires a different approach: the measurement has to be then performed using short, sub-microsecond [6] bias voltage pulses instead of a ramp or staircase bias. However, measurements at such high frequencies are problematic as the series resistance and probe wire inductance start to dominate the measured admittance. Most of the interface states can be neutralized by using hydrogen or hydrogen/nitrogen mixed gas surface anneals at around 450 °C [7].

Oxide charge

Fixed oxide charge Q_{fix} is a byproduct of the oxidation process. It is a positive charge inside the oxide near the semiconductor interface and is not in an electric contact with the semiconductor so it is unaffected by gate bias. The amount of fixed oxide charge created in the oxidation process is inversely proportional to the final oxidation temperature, higher temperatures leading to smaller Q_{fix}. Other affecting factors are oxidation ambient, cooling conditions, and crystal orientation. If the thermal budget of device fabrication process does not allow for high oxidation temperatures the amount of fixed oxide charge can be reduced by argon or nitrogen anneal at 600 °C. The anneal reduces Q_{fix} to a level attained in 1200 °C oxidation regardless of what temperature the oxidation was performed in. Oxide trapped charge Q_{ot} is comprised of electrons or holes trapped in the oxide. These trapped charge carriers may result from Fowler-Nordheim tunneling, avalanche injection, ionizing

radiation or other mechanisms. Like Q_{fix}, Q_{ot} can also be reduced by low temperature thermal anneal. Since both Q_{fix} and Q_{ot} are static charges unaffected by gate bias, unlike D_{it} they shift the CV curve instead of spreading it. Positive charge will shift the CV to the left, since increasingly negative gate voltages are required to counteract the positive charge. However, the shape of the curve will be unaltered. [7]

The third type of oxide charge is mobile ionic charge Q_m. Mobile ionic charge is commonly located near the metal gate interface where it originally entered the oxide layer or at the opposite end of the layer, in the semiconductor interface where it has drifted under the effect of an applied electric field. The Q_m charge is caused by ionized alkali metal atoms which are mobile in SiO2 even in low temperatures. The effects of slowly moving mobile oxide charge in the CV curve can be indistinguishable from fixed oxide charge and oxide trapped charge in the time frame of a regular CV measurement. However, if bias-temperature aging treatment is used that CV curve can be shifted in the voltage axis. In bias-temperature aging the sample held at a moderately elevated temperature to facilitate ionic movement and a gate bias is maintained for an extended period of time. Negative bias-temperature aging will shift the CV curve to the right leaving the shape of the curve unaltered, likewise a positive aging will shift the curve to the left. [6]

2.2.2 Circuit equivalent of a MOS structure

The circuit equivalent of a MOSCAP structure is presented in figure 2.5. [7]

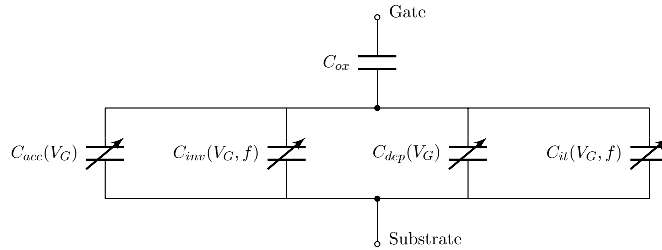


Figure 2.5: Circuit equivalent of a MOSCAP.

The oxide capacitance C_{ox} is connected in series with accumulation and inversion layer capacitances C_{acc} and C_{inv}, interface state capacitance C_{it}, and depletion layer capacitance C_{dep}, which are connected in parallel. C_{ox} can be considered constant, independent of gate bias voltage V_G and frequency f of the AC component. Semiconductor capacitance C_S which is referred to later in section 2.2.3 consists of the parallel connection of $C_{acc} + C_{inv} + C_{dep}$. Oxide capacitance can be defined as a parallel-plate capacitor

$$C_{ox} = \varepsilon_0 \varepsilon_r \frac{A}{t_{ox}} \tag{2.5}$$

with gate area A, oxide thickness t_{ox}, oxide electric permittivity ε_r, and vacuum permittivity ε_0. Equation 2.5 can also be applied to C_{dep}, however since depletion layer depth is bias voltage dependent C_{dep} is not constant. Likewise, C_{acc}, C_{inv}, and C_{it} are also bias dependent, as the rate of charge stored in accumulation or inversion layer as well as in interface states respectively, varies with gate voltage. In addition to bias dependence, C_{inv} and C_{it} are also frequency dependent.

In deep accumulation C_{acc} dominates over C_{inv}, C_{it}, and C_{dep} in the parallel connection. The total capacitance of the MOSCAP

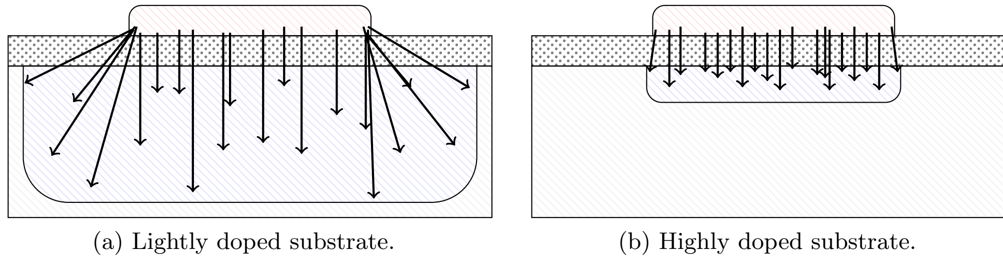
$$C = \frac{C_{ox}(C_{acc} + C_{inv} + C_{it} + C_{dep})}{C_{ox} + C_{acc} + C_{inv} + C_{it} + C_{dep}} \tag{2.6}$$

can then be approximated as

$$C = \frac{C_{ox}C_{acc}}{C_{ox} + C_{acc}} \,. \tag{2.7}$$

As C_{acc} tends towards infinity in equations 2.6 and 2.7 it approaches short circuit in figure 2.5 so that total capacitance of the structure $C = C_{ox}$ in deep accumulation as shown in figure 2.2. Using the measured total capacitance in accumulation and substituting $C = C_{ox}$ into equation 2.5 oxide thickness can be solved. The requirement is that $C_{ox}/C_S << 1$ in deep accumulation. For very thin oxides of under 10 nm the C_{ox}/C_S ratio can become so high that the requirement for solving C_{ox} from the curve is no longer fulfilled [9]. However, for the ideal Si-SiO_2 MOS in theoretical derivations of section 2.2.3 all practically applicable oxide thicknesses and doping densities will yield a C_{ox}/C_S ratio below 0.03 which is acceptable for solving C_{ox} from the accumulation capacitance of the curve.

Oxide thickness together with potential barrier height are the deciding factors of the magnitude of tunneling current through the oxide. Tunneling currents in silicon oxide become significant for oxide thicknesses below 5 nm and will prevent the inversion layer from forming because minority carriers tunnel through the oxide to the gate. Thicker oxide also serves to reduce the effects of fringing field especially with lightly doped substrates as illustrated in figure 2.6.



(a) Lightly doped substrate. (b) Highly doped substrate.

Figure 2.6: Effects of gate area, oxide thickness, and doping density to the fringing field. Electric field lines point from the positive charges in the gate towards the negatively charged ionized donors in the depleted space charge region of the p-type substrate. In lightly doped substrate field line density is increased at the edges of gate and field lines are no longer perpendicular to the surface.

Depletion region depth cannot be driven to its maximum value when avalanche breakdown occurs at the edges of the gate at lower gate biases than in the center. For very high doping densities of over 10^{18} cm^{-3} tunneling, rather than avalanche breakdown, will determine the maximum value of depletion region depth. To obtain accurate results for measured capacitance the dimensions of the metal contact have to be large compared to the combined thickness of the oxide and depletion region. However, increasing gate dimensions increases total capacitance of the structure as shown in equation 2.5. One has to then bear in mind the capacitance range limitations of the instruments used for measurements when increasing gate size. Appropriate gate dimensions are therefore confined by the limitations set by oxide thickness, substrate doping density, and measurement instruments. [6]

In depletion region the charge in semiconductor surface consists of charged surface states and ionized donors or acceptors, depending on material type. The respective capacitances C_{it} and C_{dep} dominate over C_{acc} and C_{inv} because the surface is depleted of free carriers. Equation 2.6 then becomes

$$C = \frac{C_{ox}(C_{it} + C_{dep})}{C_{ox} + C_{it} + C_{dep}} . \quad (2.8)$$

In figure 2.5 C_{acc} and C_{inv} are replaced with open circuit.

In inversion region two different outcomes are possible depending on the frequency of bias AC component. At low frequencies (≈1-100 Hz) minority carrier generation and recombination processes are able to follow the changes in bias field. This leads to minority carriers greatly outnumbering the charge from ions of the depletion region and surface occupied surface states. The total capacitance of the structure then behaves as in the case of accumulation approximation of equation 2.7, with C_{acc} being replaced by C_{inv} which dominates over the other capacitances connected in parallel. As a result, for low frequencies, $C = C_{ox}$ in inversion as shown in figure 2.2. At high frequencies ($\gg$1000 Hz) minority carrier generation and recombination processes are no longer able to follow the changes in bias field, as a result total capacitance behaves as in depletion. If frequency is increased even further ($\gg$1 MHz) surface states also are no longer able to charge and discharge during an AC cycle. The depletion capacitance equation 2.8 is then reduced to

$$C = \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}} \quad (2.9)$$

and C_{it} in addition to C_{acc} and C_{inv} are replaced with open circuit in figure 2.5. [7]

2.2.3 Theoretical CV curve of the ideal MOS

The following properties are usually assumed for the ideal MOS structure: (1) The gate is equipotential. (2) The oxide is a perfect insulator and contains no charge. (3) There are no interface states, or trap states in the bulk. (4) Doping distribution in the semiconductor is perfectly uniform. (5) The semiconductor is sufficiently thick so that a field free bulk region can exist far from the surface. (6) Back contact to the semiconductor is ohmic. (7) The structure is-one dimensional, so all the field lines are perpendicular to the surface. (8) The contact potential between metal and semiconductor is zero. [10]

Low-frequency curve

To compute the theoretical curve of figure 2.2 two out of three following parameters are required: oxide capacitance, oxide thickness, and gate area. The missing third parameter can then be calculated using equation 2.5. An acceptable estimate for oxide capacitance can be obtained by measuring MOS capacitance in accumulation as derived in equation 2.7. Gate area can be determined visually using a microscope and oxide thickness for instance by using ellipsometry. In addition, in the measurements of chapter 3 it was discovered that the permittivity of very thin dielectrics is possibly lowered from bulk values reported in literature. As a consequence, especially when measuring MOS structures with dielectric thicknesses below 100 nm it is recommended to know all three of the aforementioned parameters since the permittivity cannot be treated anymore as a constant. Determining

oxide capacitance accurately is of paramount importance as it is used as a reference point for calculations. Poor accuracy of C_{ox} will therefore result in recurring inaccuracy of derived results. In addition to the parameters above, dopant type (n-type or p-type) and dopant density are also required. Dopant type is easily determined from a measured high-frequency CV curve since the capacitances in accumulation and inversion are highly asymmetric. If dopant density is not known it can be calculated as shown in chapter 2.2.4, however, uniform doping density is assumed in the ideal MOS model.

Low frequency MOS capacitance is calculated by first solving normalized band bending v for each value of gate voltage using [6]

$$v(V_G) = \frac{q}{kT}\left(V_G + \frac{Q_s}{C_{ox}}\right) \tag{2.10}$$

where v is defined as the difference between normalized surface potential u_S and normalized bulk potential u_B [6]

$$v = u_S - u_B \tag{2.11}$$

where [6]

$$u_S = \phi_S \frac{q}{kT} \tag{2.12}$$

and [6]

$$u_B = \phi_B \frac{q}{kT}\,. \tag{2.13}$$

Bulk potential ϕ_B can be solved for p-type substrates using [6]

$$\phi_B = \ln\left(\frac{n_i}{N_A}\right) \tag{2.14}$$

and for n-type substrates using [6]

$$\phi_B = \ln\left(\frac{N_D}{n_i}\right) \tag{2.15}$$

where n_i is the intrinsic charge carrier density, N_A and N_D are acceptor and donor densities respectively. Surface charge Q_S in equation 2.10 is calculated using [6]

$$Q_S(v) = \mathrm{Sgn}(-v)\frac{\varepsilon_s}{\lambda_i}\frac{kt}{q}F \tag{2.16}$$

where F is the unitless electric field [6]

$$F(v) = \sqrt{2}\sqrt{(-v)\sinh(u_B) - \cosh(u_B) + \cosh(v + u_B)} \tag{2.17}$$

and λ_i is the intrinsic Debye length [6]

$$\lambda_i = \sqrt{\frac{\varepsilon_s kT}{2q^2 n_i}}\,. \tag{2.18}$$

After solving $v(V_G)$ by substituting the necessary equations above into equation 2.10 the semiconductor capacitance per unit area can then by calculated and multiplied by gate area A for low frequency semiconductor capacitance $C_{S,lf}$ using [6]

$$C_{S,lf}(v) = A\left(\mathrm{Sgn}(v)\frac{\varepsilon_s}{\lambda_i}\frac{\sinh(v + u_B) - \sinh(u_B)}{F}\right)\,. \tag{2.19}$$

However, equation 2.19 cannot be solved for $v = 0$ which occurs at zero bias so for $V_G = 0$ [6]

$$C_{S,lf}(0) = A\,C_{FB} \tag{2.20}$$

is used instead. C_{FB} is the flat band capacitance per unit area given by [6]

$$C_{FB} = \frac{\varepsilon_s}{\lambda_N} \tag{2.21}$$

where λ_N is the extrinsic Debye length [6]

$$\lambda_N = \sqrt{\frac{\varepsilon_s kT}{q^2 N}}\,. \tag{2.22}$$

The solved semiconductor low-frequency capacitance $C_{S,lf}(V_G)$ and oxide capacitance C_{ox} are then combined for the total MOS low-frequency capacitance C_{lf} by using

$$C_{lf}(v) = \left(\frac{1}{C_{S,lf}} + \frac{1}{C_{ox}}\right)\,. \tag{2.23}$$

High-frequency curve

High-frequency MOS capacitance is calculated using derivations by Lindner [11] improved by Brews [12]. First the band bending for each value of gate voltage is solved similarly to low-frequency case above using equation 2.10. However, instead of equation 2.19 semiconductor capacitance per unit area for a p-type semiconductor is now

$$C_L = \frac{C_{FB}\,\mathrm{Sgn}(v)(1 - e^{-v})}{\sqrt{2}\sqrt{(v-1) + e^{-v}}} \tag{2.24}$$

and for a n-type semiconductor

$$C_L = \frac{C_{FB}\,\mathrm{Sgn}(v)(-1 + e^{v})}{\sqrt{2}\sqrt{(-v+1) + e^{v}}}\,. \tag{2.25}$$

The p-type semiconductor high-frequency capacitance for is then

$$C_{S,hf}(v) = A\,C_L(v); \qquad v \le v_m \tag{2.26}$$
$$C_{S,hf}(v) = A\,C_L(v_m); \qquad v > v_m \tag{2.27}$$

and for a n-type semiconductor

$$C_{S,hf}(v) = A\,C_L(v); \qquad v \ge v_m \tag{2.28}$$
$$C_{S,hf}(v) = A\,C_L(v_m); \qquad v < v_m \tag{2.29}$$

where v_m is the match point in band bending at which ionized impurities and minority carriers contribute equally to the square of the total surface density. Beyond the match point in equation 2.27 minority carriers will pin the band bending to a constant value even though gate bias is further increased. The optimal match point approximation for any doping density in p-type semiconductor is found to be

$$v_m = 2.10|u_B| + 1.33 \tag{2.30}$$

and in n-type semiconductor

$$v_m = -(2.10|u_B| + 1.33)\,. \tag{2.31}$$

The deep depletion curve in figure 2.2 was obtained by omitting the pinning to v_m in equation 2.27, allowing the band bending to continue further by using equation 2.26 for the entire bias range. The total MOS capacitance C_{hf} for high-frequency is then obtained by substituting $C_{S,hf}$ instead of $C_{S,lf}$ into equation 2.23.

Example curves

All low- and high-frequency CV curves in this thesis and their respective band bending curves were calculated using the formulas presented in this section (2.2.3). The resulting curves were found to be in accordance with the reference curves by Goetzberger. [13]

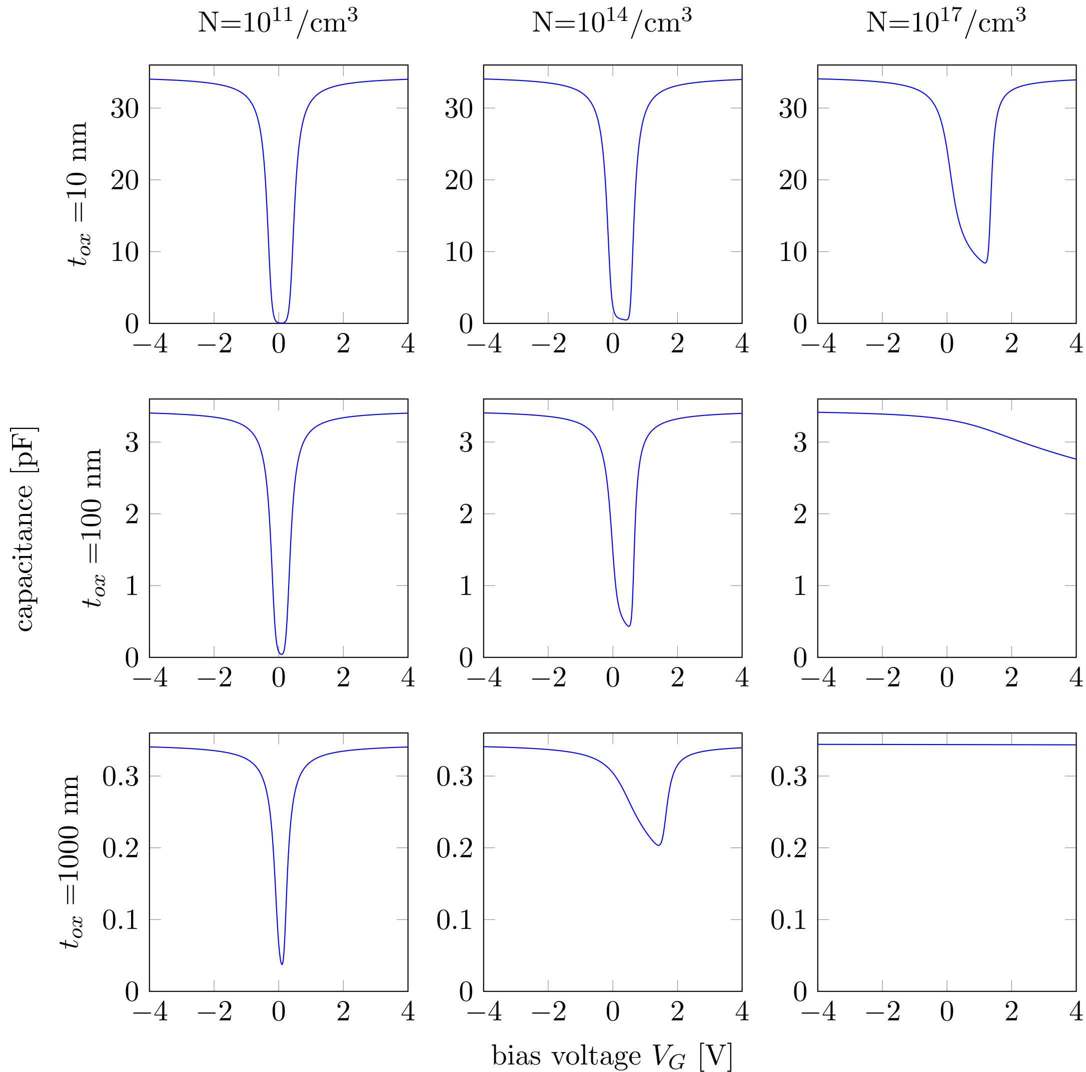


Figure 2.7: Effects of doping density and oxide thickness on the CV curve. Gate area is 10^{-8} m^2. Capacitance axis is linear with scaling adjusted for each t_{ox}.

The low-frequency curves in figure 2.7 illustrate the effects of doping density and equivalent SiO_2 thickness to the CV curve shape in a p-type MOS. High doping densities shift the Fermi level towards the majority carrier band edge from the midgap. This causes the flat band voltage, which is always at zero bias for theoretical curves, to shift towards accumulation from depletion. Also the minimum capacitance in depletion increases with doping density and higher biases are required to drive the MOS into depletion. This need for higher biases is further increased by thicker oxides since a bigger part of the bias potential is lost over the oxide. Thicker oxides also decrease the maximum capacitance of the CV curve. When the maximum capacitance decrease due to oxide thickness is combined with the minimum capacitance increase from higher doping densities the minimum and maximum of the curve drift towards each other, and the CV curve approaches a flat horizontal line. The CV curve loses all of its characteristic features from which physical parameters are extracted. At high doping level with thick oxide this resulting straight line resembles the CV response of a macroscopic metal plate capacitor.

2.2.4 Extraction of physical parameters

Dopant density profile

Dopant density profile can be calculated as a function of distance w from surface using

$$N(w) = -2\left(\frac{1 - C_{lf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right)\left(q\varepsilon_s \frac{d}{dV_G}\left(\frac{1}{C_{hf}^2}\right)\right)^{-1} \tag{2.32}$$

by Brews [14] and generalized to all frequencies by Zohta [15]. Here ε_s is the semiconductor permittivity, C_{lf} and C_{hf} are measured low- and "true" high-frequency capacitances respectively, "true" high frequency being a frequency high enough so that both, the minority carriers and the interface states, are unable to follow the gate voltage V_G cycle ($\geq$1 MHz). If surface state density is negligible or the measurement is performed using short bias pulses to remove the effects of interface state stretching along the bias voltage axis equation 2.32 can be shortened to

$$N(w) = -2\left(q\varepsilon_s \frac{d}{dV_G}\left(\frac{1}{C_{hf}^2}\right)\right)^{-1} \tag{2.33}$$

by Van Gelder and Nicollian [16]. In both cases $N(w)$ is calculated for each value of gate bias and corresponding values of w are then solved from

$$w = \varepsilon_s\left(\frac{1}{C_{hf}} - \frac{1}{C_{ox}}\right). \tag{2.34}$$

For uniform doping densities, or to obtain an average, the maximum-minimum method [6]

$$\frac{N_A}{\ln(N_A/n_i) + \frac{1}{2}\ln(2\ln(N_A/n_i) - 1)} = \frac{4kT\varepsilon_{ox}^2}{q^2\varepsilon_s t_{ox}^2}\left(\frac{C_{ox}}{C_{hf,min}} - 1\right)^{-2} \tag{2.35}$$

can be used to extract N_A from the maximum C_{ox} and minimum $C_{hf,min}$ values of the measured curve. The equation is transcendental and has to be solved through numerical iteration. Because interface state density strongly affects the minimum capacitance of the curve the equation holds only for true high-frequency curves or low frequency curves from structures with negligible interface state density.

Interface state density

Extraction of surface state density D_{it} using a measured high-frequency CV curve and a theoretical curve was developed and first used by Terman [17]. High frequency in the context of surface states refers to frequencies at which even the fastest surface states are unable to follow the AC small-signal component of bias voltage. The fastest surface states will respond to frequencies up to 100 MHz [6] which is several orders of magnitude above the "high frequency" ($\approx$ 1 kHz - 1MHz) used in context of minority carrier response. Thus the shortcoming of Terman method is the difficulty of obtaining a "true" high-frequency curve in which all of the surface state response is eliminated

To obtain D_{it} using the Terman method a theoretical curve of total MOS capacitance as a function of band bending $C(\psi)$

$$\psi = \phi_S - \phi_B \tag{2.36}$$

is compared to a measured $C(V_G)$ curve. The parts of curve from accumulation to depletion are most suitable for this task. For each value of capacitance the amount of band bending is determined from the theoretical curve and the corresponding amount of gate bias required to achieve this band bending from the measured curve as presented in figure 2.8 [6].

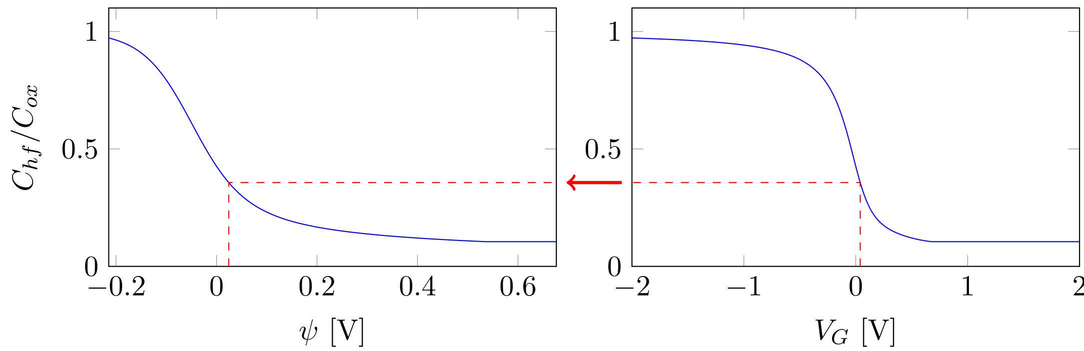


Figure 2.8: Obtaining the relation of band bending and gate bias $\psi(V_G)$ using the Terman method.

Because surface states are unable to follow the small signal oscillation they do not add to the total capacitance as in figure 2.5, so capacitance values remain unaltered compared to the theoretical curve but the horizontal stretching due to DC bias remains as explained in section 2.2.1. This horizontal stretching affects only the amount of V_G needed to achieve a desired value ψ. Surface state capacitance C_{it} is then extracted from the relation between V_G and the band bending ψ using [7]

$$C_{it}(\psi) = C_{ox}\left(\frac{dV_G}{d\psi} - 1\right) - C_S(\psi) \tag{2.37}$$

and [6]

$$D_{it}(\psi) = \frac{C_{it}(\psi)}{qA} \tag{2.38}$$

It should be noted that equation 2.38 uses $m^{-2}eV^{-1}$ as units, for joules instead of electron volts the correct form is [7]

$$D_{it}(\psi) = \frac{C_{it}(\psi)}{q^2 A}\,. \tag{2.39}$$

Berglund [18] developed and was the first to use the method for low-frequency CV and theoretical curve. Whereas the high-frequency method was based upon the horizontal stretching caused by interface states, the low-frequency approach extracts C_{it} through the increase of capacitance at each gate bias value, especially in depletion where the effect is most pronounced. Starting from equation 2.6 where C_{acc}, C_{inv} and C_{dep} are combined into C_S so that

$$C(V_G) = \frac{C_{ox}\left(C_{it}(\psi) + C_S(\psi)\right)}{C_{ox} + C_{it}(\psi) + C_S(\psi)} \tag{2.40}$$

is rearranged to

$$C_{it}(V_G) = \left(\frac{1}{C(\psi)} - \frac{1}{C_{ox}}\right)^{-1} - C_S(\psi) \tag{2.41}$$

where $C(\psi)$ is the measured total low-frequency MOS capacitance as a function of band bending. The resulting C_{it} is then substituted to equation 2.39 for D_{it}. It should be emphasized that the capacitances in equations 2.40 and 2.41 should be expressed as a function of band bending, not gate voltage. Since the purpose of equation 2.41 is to determine D_{it} through the added capacitance C_{it} at each point of the curve, the measured $C_S + C_{it}$ in the brackets and the theoretical C_S do not refer to corresponding points of the curve if expressed as a function of gate voltage. As previously stated, the horizontal stretching caused by interface states only affects the amount of gate voltage needed to achieve a certain amount of band bending. The relation between band bending and capacitance for $C_S(\psi)$ and $C(\psi)$ is not affected by interface states. For this reason the $C_S(\psi)$ derived for the ideal $D_{it} = 0$ curve in section 2.2.3 can be used regardless of the D_{it} of the measured curve, but $C_S(V_G)$ can not. The Berglund integral can be used to obtain a correspondence between band bending and gate voltage $\psi(V_G)$ for equation 2.41. Omitting the derivations of the Berglund integral, the change in band bending $\Delta\psi$ between given gate biases V_G and $V_{G,0}$ is

$$\Delta\psi = \psi_0 + \int_{V_{G,0}}^{V_G} \left(1 - \frac{C_{lf}(V_G)}{C_{ox}}\right) dV_G \tag{2.42}$$

where $V_{G,0}$ is an arbitrarily chosen gate voltage and ψ_0 the corresponding band bending. Because ψ_0 is not known, $V_{G,0}$ can be for instance chosen so that band bending does not strongly vary with bias as in strong accumulation or inversion, as suggested by Nicollian and Brews [6]. Integration from strong accumulation to strong inversion should yield E_G/q where E_G is the bandgap energy [7]. Values larger than E_G/q indicate gross non-uniformities in the oxide or at the oxide-semiconductor interface, making the analysis invalid [7]. Schroder [7] however suggests using the flat band voltage C_{FB} as the starting point of integration so than ψ_0 becomes zero. With the experimental relation between ψ and V_G established, a derivative could be taken and equation 2.37 could be used. However, equation 2.41 does not require differentiation of measurement data which is always prone to error.

Another approach is to use $C_S(V_G)$ with the stretching caused by D_{it}, but without the added capacitance by the combination of low- and high-frequency measurements, which eliminates the need for theoretical curve. This method was first introduced by Castagné and Vapaille [19]. The theoretical C_S in equation 2.41 is replaced by C_S obtained from a high-frequency measurement and C_{it} then becomes

$$C_{it}(V_G) = \left(\frac{1}{C_{lf}(V_G)} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{hf}(V_G)} - \frac{1}{C_{ox}}\right)^{-1}. \tag{2.43}$$

Flat band voltage

The easiest method to obtain flat band voltage from the measured CV curve for a given oxide thickness and dopant density is to first calculate the flat band capacitance using [7]

$$C_{FB,m} = C_{ox}\left(1 + \frac{1360\sqrt{T/300}}{t_{ox}\sqrt{N}}\right)^{-1} . \tag{2.44}$$

It is worth noting that the units for t_{ox} and N are [m] and [m^{-3}]. If one wishes to use [cm] and [cm^{-3}] instead, the 1360 in numerator is divided by 10. The equivalent gate voltage $V_{FB,m}$ can then be located from the measured curve. Equation 2.44 holds only for Si substrates with a with a uniform dopant distribution, large semiconductor bulk and a SiO_2 insulator. Thin silicon bulks for example in silicon-on-insulator (SOI) wafers may lack the necessary thickness to fully accomodate the space charge region.

Another easy solution is available for true high-frequency CV curves with no C_{it}. In this case C_{FB} can be determined from the theoretical curve using the capacitance at zero bias or by using equation 2.21. The equal capacitance value and its respective $V_{FB,m}$ can then be located in the measured curve.

A solution can also be graphically obtained by finding the maximum of [7] [9]

$$\frac{d^2}{dV_G^2}\left(\frac{C_{ox}}{C_{hf,m}}\right)^2 . \tag{2.45}$$

Any noise in the measured curve will be greatly amplified by the second derivative so smoothing the data or using a theoretical curve that has been fitted into the data might be necessary. This method is for true high-frequency or low D_{it} low-frequency curves.

Since oxide charge does not change the curve shape but instead only shifts it along the bias axis, the flat band voltage for low D_{it} curves can also be obtained by curve fitting as in figure 2.9.

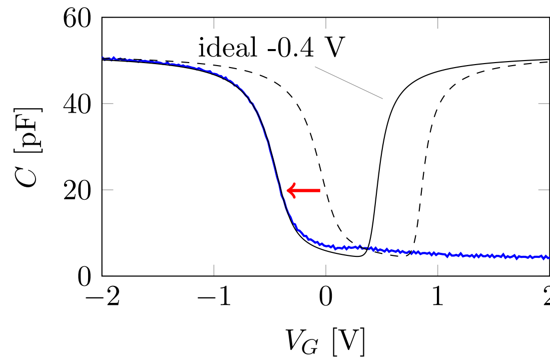


Figure 2.9: Obtaining flat band voltage by curve fitting. Dashed black line represents unaltered ideal curve calculated using the permittivities, dielectric thickness, gate area, and dopant density of the sample. Solid black curve has been shifted by -0.4 volts to the left fitting it accurately to the blue measured curve. Flat band voltage for the measured curve is therefore -0.4 V.

A simple test was conducted, comparing the accuracies of equations 2.44 and 2.45 using the theoretical curve of an ideal p-type MOS. This was done, because in order for a V_{FB} determination method to be applicable it should at least provide accurate results for an ideal MOS structure. The flat band voltage of an ideal MOS should be at $V_G = 0$ for all combinations of doping density N and oxide thickness t_{ox}. Blue values in tables 2.1 and 2.2 are within reasonable margin of error to be of practical use. Red values deviate too much from the true value of $V_G = 0$. For an ideal n-type MOS the respective values would be negative.

Table 2.1: Flat band voltages calculated with equation 2.44.

	t_{ox} [nm]			
N [cm^{-3}]	10	50	250	1250
10^{12}	0.00	0.00	0.00	0.00
10^{14}	0.00	0.00	0.00	0.01
10^{16}	0.00	0.00	0.02	0.07
10^{18}	0.01	0.03	0.14	0.72

Table 2.2: Flatband voltages calculated with equation 2.45.

	t_{ox} [nm]			
N [cm^{-3}]	10	50	250	1250
10^{12}	0.02	0.03	0.03	0.05
10^{14}	0.03	0.03	0.10	0.37
10^{16}	0.05	0.16	0.70	3.44
10^{18}	0.50	1.40	6.86	>10

Both equations produce good results with low t_{ox} and N, but equation 2.45 starts to deviate increasingly from the true value of V_{FB} as t_{ox} and especially N, which has a pronounced effect, are increased.

Equation 2.44 is constant with respect to gate-substrate contact potential difference Φ_{GS} and oxide charge Q_{ox}. It is also based on $C_{FB,m}/C_{ox}$ having a certain ratio at flatband position. For these reasons horizontal stretching due to large D_{it} or shifting due to Φ_{GS} or Q_{ox} do not affect the outcome as long as the material and large bulk assumptions of the model are fulfilled.

Equation 2.45 on the other hand is based on the CV curve reaching its maximum curvature at flat band voltage. The maximum value of curvature can be affected by D_{it} induced horizontal stretching, but if D_{it} is constant over the bandgap, which is a reasonable approximation for Si(100)-SiO_2 interfaces [20], the curve will be uniformly stretched over the entire bias range and the location of the maximum will still be at flat band bias. If D_{it} varies greatly over the bandgap the curvature can be significantly altered resulting in maximum value at wrong gate bias. Horizontal shifting due to Q_{ox} on the other hand will not change the shape of the curve and $V_{FB,m}$ will simply shift accordingly. However, the approximation of constant D_{it} is very rarely applicable, even with high quality interfaces, since not only the material choices, but also crystal orientations significantly change the $D_{it}(E)$ function [20] [21]. Therefore, in practice the most reliable way to obtain accurate V_{FB} is theoretical curve fitting.

Oxide charge

After V_{FB} has been obtained oxide charge can be solved using [7]

$$Q_{ox} = (\Phi_{GS} - V_{FB})\, C_{ox}\,. \tag{2.46}$$

For p-type substrates Φ_{GS} can be obtained from [7]

$$\Phi_{GS} = K - \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{2.47}$$

and for n-type substrates respectively by using [7]

$$\Phi_{GS} = K + \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{2.48}$$

where [7]

$$K = \Phi_G - (\chi + (E_C - E_i)/q)\ . \tag{2.49}$$

In silicon the intrinsic Fermi level E_i is in middle of the bandgap so equation 2.49 can be written as

$$K = \Phi_G - (\chi + (E_g/2)/q)\ . \tag{2.50}$$

Electron affinity χ of silicon is 4.15 eV [5], bandgap E_g 1.12 eV [6] and intrinsic carrier concentration n_i 10^{10} cm^{-3} at 290 °K [6]. Gate work function $q\phi_G$ for an aluminum gate is 4.1 eV [5]. For an Al-SiO_2-Si structure K is then -0.61 V. Using these values, Φ_{GS} for various doping densities is presented in table 2.3. The calculated values should be treated only as approximations since work functions can vary significantly depending on crystal orientation, surface relaxation effects and other specifics [3] which were discussed earlier in section 2.1.1.

Table 2.3: Gate-substrate potential differences Φ_{GS} [V] in Al-SiO_2-Si structure for various doping levels at 290 °K. Calculated using by equations 2.47 and 2.48.

	N [cm^{-3}]					
	10^{13}	10^{14}	10^{15}	10^{16}	10^{17}	10^{18}
p-type	-0.78	-0.84	-0.89	-0.95	-1.01	-1.06
n-type	-0.44	-0.38	-0.32	-0.26	-0.21	-0.16

2.3 Instrumentation for CV measurements

Three different fundamental capacitance measurement methods are currently available for semiconductor CV characterization [1]. Charge- or current-based measurement, AC impedance-based CV measurement, and radio frequency (RF) technology which is not covered in this thesis [1]. A number of characterization methods often used in conjunction with conventional CV, such as conductance method [6], are also not within the scope of this thesis and will be left out. In addition, charge-based measurements can be performed by using a corona charge deposition instead of an evaporated metal gate with the corona oxide characterization of semiconductors (COCOS) -method. COCOS was used as a

reference method for verifying some of the results measured in chapter 3. Therefore basic understanding of the method is beneficial and COCOS is briefly discussed in section 2.3.1, which provides an overview of the fundamental basics of charge- and-current based methods that are usually utilized for quasistatic measurements. Basics of impedance-based measurements for high frequencies are likewise discussed in section 2.3.2 and section 2.3.3 will provide a brief overview on calibration, connections, various error sources and practical matters of measurement.

2.3.1 Charge- and current-based CV measurement

Quasistatic capacitance measurement is the simplest and least expensive method, requiring only two source-measure units (SMUs) [1]. The low-frequency capacitance of MOS is usually obtained by measuring charge instead of impedance, since impedance measurements are very noisy at low frequencies [7].

Ramp method

The ramp method of measuring low frequency capacitance was originally proposed by Kuhn [22], Castagné [23] and Kerr [24]. In the ramp method illustrated in figure 2.10 a low-frequency AC signal of 1-10 Hz on top of a slowly increasing ramp bias is connected preferably to the substrate of the sample MOS capacitor. The current i at the output of circuit is then simply

$$V_O = -RC_{MOS}\frac{dV_G(t)}{dt} \tag{2.51}$$

which can be rearranged to

$$C_{MOS} = -\frac{V_O}{R}\left(\frac{dV_G(t)}{dt}\right)^{-1} \tag{2.52}$$

for the MOS capacitance C_{MOS}. If the derivative of $V_G(t)$ is sufficiently low a low-frequency CV curve is obtained. Because the circuit is effectively an active differentiator any noise in the signal is amplified by $2\pi fRC_{MOS}$. Additionally, since amplification increases with respect to frequency the signal to noise ratio declines towards the lower frequencies, which are required for a true equilibrium low-frequency equilibrium CV curve. Ramp method is also very susceptible to leakage current caused by thin or poor quality oxides because the output current is no longer correctly proportional to the capacitance C_{MOS} [7]. [25]

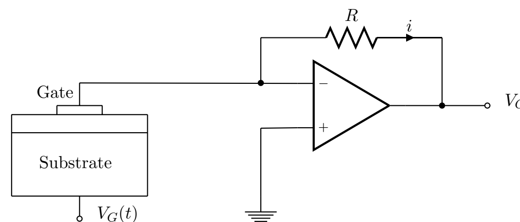


Figure 2.10: Ramp method.

Static and QV methods

Another, more accurate [6] [25] method for measuring low-frequency capacitance, the static method, was described by Ziegler and Klausmann [26]. The method was later extended by Brews and Nicollian [27] and renamed the QV method, presented in figure 2.11. In addition to being more accurate than the ramp method, the QV method also provided a better approximation for equilibrium under ideal DC bias conditions, since the bias is applied in voltage steps instead of a continuous ramp. However, there are drawbacks: Extremely high instrument and fixture impedances are required, only part of the gate bias is applied over C_{MOS} and the voltage gain is low. Despite the low gain, for devices requiring very low frequencies the signal to noise ratio is improved over the ramp method. As with the ramp method, the substrate of the MOS is connected to the voltage source, but now the voltage is applied in incremental steps ΔV_G. The gate is connected to a known, fixed, voltage independent capacitance C_F, which together with C_{MOS} forms a capacitive divider. The midpoint of this divider is monitored by a high impedance buffer and the voltage output of the buffer is then an indication of the charge in C_F. MOS capacitance is then obtained using [25]

$$C_{MOS} = C_F \left(\frac{\Delta V_O}{\Delta V_G - \Delta V_O} \right) . \tag{2.53}$$

Since only part of the gate bias increment V_G is applied over the C_{MOS} due to the capacitive divider there is a tradeoff in choosing C_F. If $C_F > C_{MOS}$ then most of ΔV_G appears over C_{MOS} so more charge is transferred. The voltage over C_F is then smaller lessening buffer requirements, but the changes in ΔV_O also become smaller and therefore harder to measure. Conversely, if $C_F < C_{MOS}$ then most of ΔV_G appears over C_F and less charge is transferred. Measuring of ΔV_O will be easier but errors caused by the impedance are increased. Usually C_F is chosen to be roughly equal to C_{MOS} to balance these effects. [25]

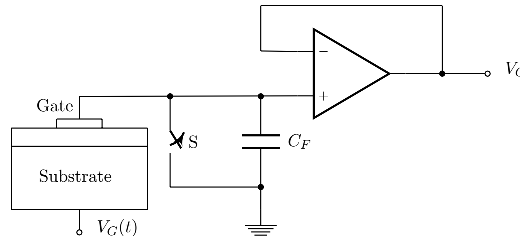


Figure 2.11: QV method.

Feedback charge method

The feedback charge method in figure 2.12 first reported by Markgraf et al. [28] combines the advantages of ramp and QV methods [25].

Incremental voltage steps ΔV_G are utilized as with the QV method but the charge is measured with a feedback charge amplifier instead. The input is thus a virtual ground and requirements for high impedance insulation are reduced and gain is increased. Compared to the ramp method, the feedback charge method uses an integrator circuit instead of a differentiator circuit, providing the benefits of improved noise immunity, compensation for

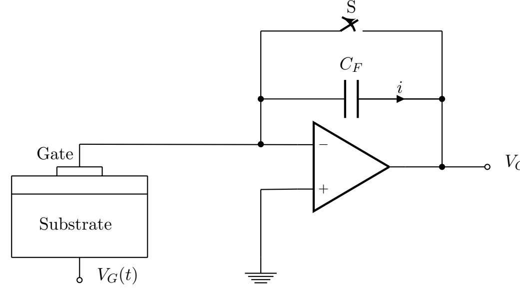


Figure 2.12: Feedback charge method.

leakage current and eliminating the problem of diminishing gain and noise to signal ratio at low frequencies [7]. [25]

In addition to measuring C_{MOS} the feedback charge method also measures the current Q/t flowing through the MOS at the end of each voltage step measurement cycle. The integrator is initiated by opening the switch S and driving the bias voltage step ΔV_G, or square wave as in the figure 2.13 through the MOS and the circuit. Charge is measured before the step (Q_1) and twice in rapid succession after a user defined delay time (Q_2, Q_3). MOS capacitance is then obtained using [25]

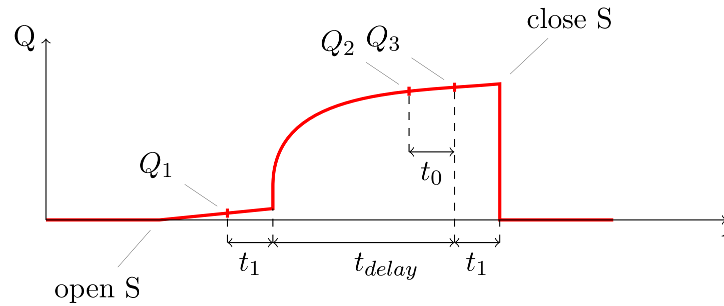


Figure 2.13: Feedback charge method. Delay time and measured charge waveform.

$$C_{MOS} = -C_F \left(\frac{\Delta V_O}{\Delta V_G} \right) \tag{2.54}$$

where [25]

$$\Delta V_O = -\frac{\Delta Q}{C_F} \, . \tag{2.55}$$

Substituting equation 2.55 into equation 2.54 yields then [25]

$$C_{MOS} = \left(\frac{Q_3 - Q_1}{\Delta V_G} \right) \, . \tag{2.56}$$

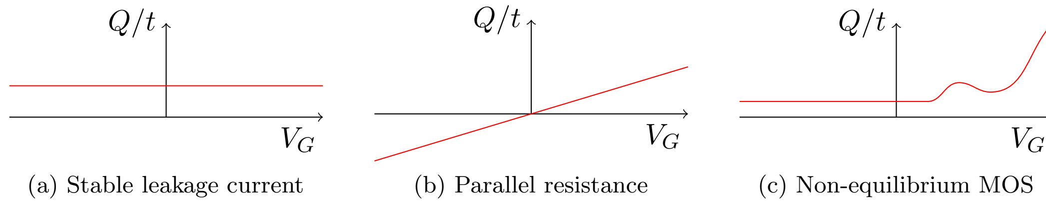
Leakage current through the MOS is a useful indicator for quality of measurement results. A Q/t value of close to zero indicates equilibrium. A nonzero, but stable Q/t can be used as a corrective value to compensate for the leakage induced errors. Q/t is obtained from the waveform of figure 2.13 using [25]

$$Q/t = \frac{Q_3 - Q_2}{t_0} \, . \tag{2.57}$$

If Q/t is stable the leakage corrected capacitance is then [25]

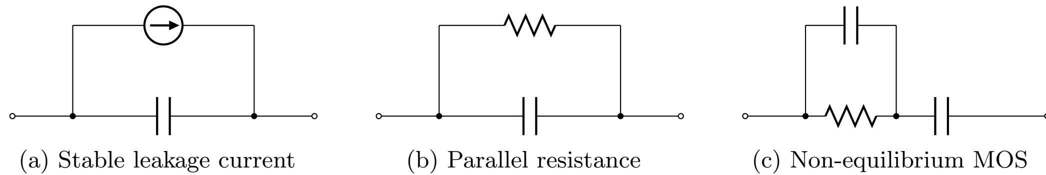
$$C_{MOS,corr} = \frac{(Q/t)(t_{delay} + t_1)}{\Delta V_G}\,. \qquad (2.58)$$

Some of the common Q/t curves and their interpretations are presented in figures 2.14 and 2.15 [25].



(a) Stable leakage current (b) Parallel resistance (c) Non-equilibrium MOS

Figure 2.14: Common Q/t curves.



(a) Stable leakage current (b) Parallel resistance (c) Non-equilibrium MOS

Figure 2.15: Circuit equivalents of common Q/t curves.

COCOS method

Charge-based CV measurement can also be performed by using corona charging in air to deposit ionized H_3O^+ or CO^{-3} charge on the oxide as illustrated in figure 2.16. Charge is deposited by applying ≈10 kV potential to a point electrode or a line electrode for covering larger areas. The whole wafer can be charged prior to localized charging to prevent surface charge gradients. Negatively biased source attracts positive ions while ambient molecules rapidly capture free electrons to form negative ions. Conversely, a positively biased source will attract free electrons and positively charged ions will follow the field lines to the sample. [29]

The deposited charge will act as a gate for the duration of the measurement which is performed without physical contact by oscillating an electrode a fraction of a millimeter above the surface [30]. The sample is then measured in the dark and under strong illumination [30]. Frequency-modulated light can also be used for sample illumination to eliminate the need to vibrate the electrode [29]. The vibrating electrode measures contact potential difference to the substrate and remains capacitively coupled to the sample throughout the measurement requiring no physical contact [30]. Wilson et al. [31] report that the deposited charged ions are stable on the dielectric surface up to 250 °C and can be easily removed by de-ionized water rinsing. The ions also have very short mean free paths of $\approx 10^{-}7$ m in atmospheric pressure and lose most of their kinetic energy before hitting the surface thus causing no damage in the impact. These two properties combined would make the COCOS method non-destructive for the sample. However, in

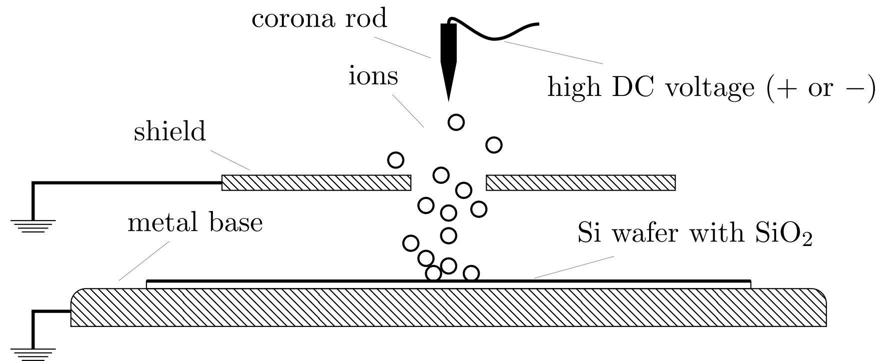


Figure 2.16: Corona deposition on the sample surface.

measurements of chapter 3 it was discovered that the corona deposition would persist through the de-ionized water rinsing as well as removal attempts with isopropanol and cleanroom paper. Significant charge remained even after vacuum evaporation of aluminum contacts. In addition, Dautrich et al. [32] report that the corona charging in itself is also damaging to the sample if corona deposition is done using high fields of 6.5MV/cm and above, inducing paramagnetic centers and causing defects. Lower field values of 4MV/cm and below caused negligible damage.

Another benefit of COCOS method over conventional MOS CV, reported by Edelman et al. [33] is smaller leakage current in thin oxides of ≈5 nm and less in equivalent SiO_2 thickness. Comparison with literature data indicates that the corona ion neutralization current is many orders of magnitude lower than the corresponding tunneling currents in MOS capacitors.

On the other hand, a shortcoming of the COCOS method is that the light in the illuminated measurements has to reach the semiconductor surface. Therefore the insulating dielectric layer needs to be thin enough or transparent in the desired wavelength range to reach the surface. Conventional MOS CV has no such requirements and the dielectric can even be impenetrable to light or highly reflective with no effects on the measurement.

The core concept of COCOS method is to measure contact potential difference V_{CPD} between the grounded semiconductor and the oscillating electrode. The contact potential is determined either by calibrating the current versus the bias voltage or by adjusting the bias until the current is zero [29]. The former method is faster and employed in wafer mapping [29]. The AC current J is [31]

$$J = V_{CPD}\frac{dC}{dt}\,. \tag{2.59}$$

A change in deposited corona charge Q_C causes a change in contact potential difference. The change in contact potential difference between the grounded semiconductor and the electrode is then divided between change in potential loss over the oxide ΔV_{ox} and potential loss over the semiconductor space charge region ΔV_S so that [31]

$$\Delta V_{CPD} = \Delta V_{ox} + \Delta V_S\,. \tag{2.60}$$

A critical aspect separating COCOS method from conventional MOS CV methods is the sample illumination. Sample is measured in dark as with conventional methods, but

additionally under strong illumination, which collapses the space charge region. With the space charge region collapsed, potential loss can only take place in the oxide causing any change in $\Delta V_{CPD,i}$ to equal the change ΔV_{ox} yielding [31]

$$\Delta V_{CPD,i} = \Delta V_{ox} \, . \tag{2.61}$$

Since illumination has no effect on potential loss over the oxide, the change in potential over space charge region for each value of ΔV_{CPD} and Q_C can then be obtained from the difference between the curves measured in dark and under strong illumination illustrated in figure 2.17 by using [31]

$$\Delta V_S = \Delta V_{CPD,d} - \Delta V_{CPD,i} \, . \tag{2.62}$$

Since V_S is now known for each value of V_{CPD} and Q_C, it is possible to calculate ΔQ_{it} by solving ΔQ_S using equation 2.16 and all of its prerequisite equations substituting V_{CPD} for V_G and V_S for $\phi_S - \phi_B$. Since the oxide charge is fixed $\Delta Q_{ox} = 0$ and the obtained Q_S together with Q_C then yield [31]

$$\Delta Q_{it} = -\Delta Q_S - \Delta Q_C \tag{2.63}$$

which can then be used to obtain surface state capacitance C_{it}

$$C_{it} = \frac{\Delta Q_{it}}{\Delta V_S} \tag{2.64}$$

which is then substituted into equation 2.38 or 2.39 for D_{it}. Since the curves in figure 2.17 are voltage as a function of charge $V(Q)$ the slope of the curve represents inverse capacitance $1/C$. The low slope of the illuminated curve then represents the inverse maximum capacitance C_{ox}^{-1} of MOS which occurs when the space charge region has effectively zero depth. The dark curve reaches this maximum capacitance in strong accumulation where the two curves overlap. Respectively, the bottom value of capacitance in depletion is reached when the $V(Q)$ slope of the dark curve is steepest. Density of states can therefore be determined only in the depletion region, since outside of the steep part of the dark curve the illuminated and dark curves are practically parallel making ΔV_S in equation 2.62 zero and causing C_{it} in equation 2.64 to approach infinity.

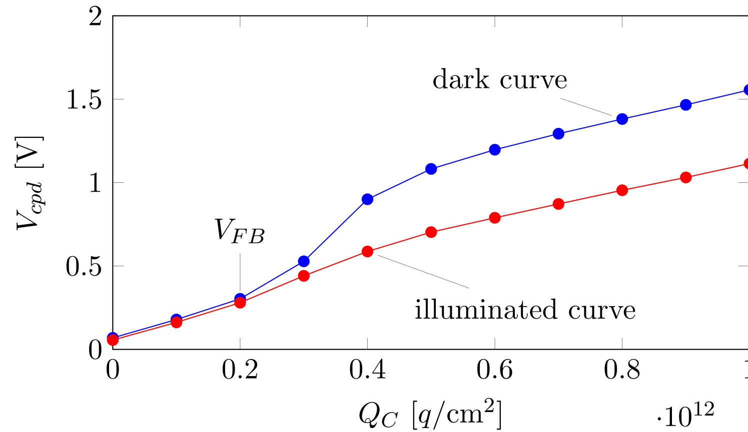


Figure 2.17: Contact potential difference as a function of corona charge.

In COCOS method flat band voltage is considered to be the V_{CPD} at which the dark and illuminated curves part [31]. It is noteworthy that this interpretation places flat band voltage to the point where capacitance starts to decrease from its deep accumulation value as opposed to equation 2.45 for conventional contact measurements where flat band voltage is at the maximum of the second derivative of capacitance. This is not in agreement with the results provided by equations 2.44 and 2.45 which were verified for the ideal curve in tables 2.1 and 2.2. The differences between conventional MOS and COCOS flat band are primarily due to work function differences between the gate and CPD electrode [31].

2.3.2 Impedance-based CV measurement

AC impedance meters measure complex impedance typically using four-point measurement with sensing on the grounded side of the MOS as presented in figure 2.18. The DC bias and AC small signal voltage are supplied from the high current HCUR terminal. Voltage over the MOS is measured between the high- and low-potential terminals HPOT and LPOT. Current over the MOS is measured in the low current terminal LCUR. Meters of this type usually have a frequency range of 1 kHz to 10 MHz and are therefore used for obtaining high-frequency CV curves. [1]

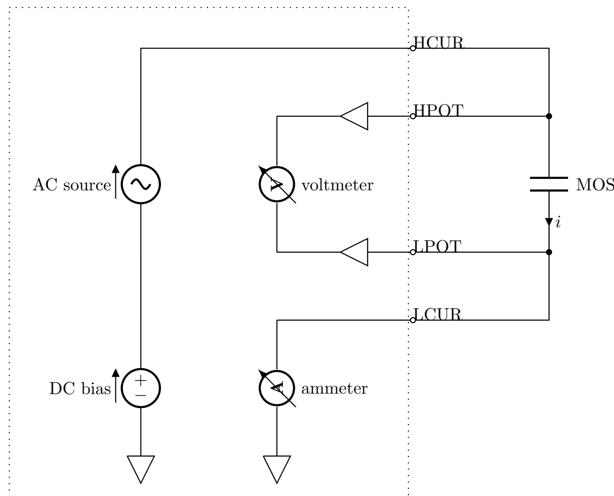


Figure 2.18: AC impedance meter.

The presence of a capacitive or an inductive impedance component causes a phase shift between the current and voltage. Capacitance of the MOS can be calculated from this phase shift while resistance is determined from the attenuation. This phase shift in the points connecting CUR and POT wires in both sides of the sample should be preserved to their respective input terminals in order to accurately determine the impedance of the MOS structure. Due to this, cable lengths are an issue, unlike in charge-based low-frequency measurements. From the points where CUR and POT wires connect to their respective terminals the wires should be of equal electrical length.

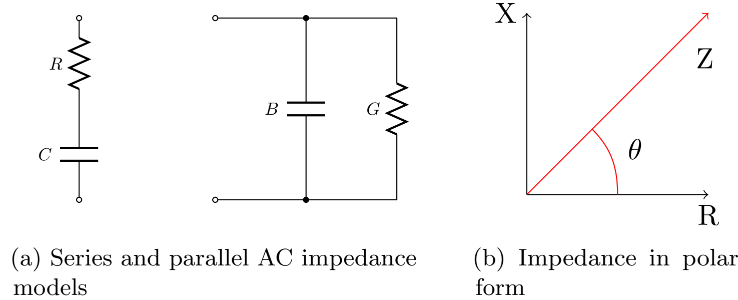
The MOS is represented either by a series or parallel model as illustrated in figure 2.19a. In series mode the phase shift angle θ and in parallel mode the dissipation factor D where

$$\theta = \arctan\left(\frac{X}{R}\right) = \arctan\left(\frac{1}{\omega C_{MOS} R_{MOS}}\right) \tag{2.65}$$

and

$$D = \frac{G}{B} = \frac{1}{\omega C_{MOS} R_{MOS}} \tag{2.66}$$

respectively, are good metrics for determining the quality of the CV measurement [1]. An ideal MOS is purely capacitive with infinite resistance R or zero conductance G, so a close to zero D or θ, depending on the model used for measurement, is usually one indicator for good results. Likewise, measurements with D or θ values of one of above rarely produce good quality CV curves.



(a) Series and parallel AC impedance models

(b) Impedance in polar form

Figure 2.19: AC impedance.

2.3.3 Cabling and error compensation

Section 2.3.2 described different circuits and their operating principles for a CV measurement system. However, the choice and implementation of cable connections from the CV instrument to the probe station forms the other, equally critical half of the complete system. Problems arise especially if the same probe station is intended for CV, IV and pulsed or ultra-fast IV. CV measurements demand the use of coaxial cables with remote sense leads, and in case of high-frequency impedance-based measurements also precisely controlled cable lengths. DC IV measurements are best accomplished with low noise triaxial cables with remote sense leads. Ultra-fast IV requires 50Ω coaxial cable, but the remote sense leads create an impedance mismatch problem. RF CV requires its own special type of cables. Unfortunately none of these cabling methods are compatible with each other. [1]

For CV measurements the shields of the coaxial cables should be connected together with a very short jumper cable as illustrated in figure 2.20. The probe head bodies should be connected together, because in a CV measurement system the shield of the coaxial cable is a part of the measurement path. A large loop area resulting in a large inductance directly into the measurement path will be created if the shields are not connected, resulting in errors. Good quality CV measurements require a well implemented shield connection and the quality of this connection is further emphasized as the measurement frequency is increased. However, for DC IV measurements the probe body should be floated at guard potential so the jumper has to be removed when switching from CV to DC IV measurements. [1]

Gain and offset errors can be compensated for by using load correction as well as open- and closed-circuit correction. Load correction is obtained by using a known reference load

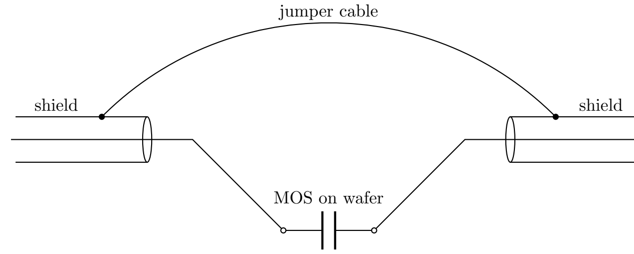


Figure 2.20: Connection of the coaxial cable shields.

and comparing the measured value to the reference value for an adjustment rate α so that

$$\alpha = Z_{measured}/Z_{known}\,. \tag{2.67}$$

For example, to correct a gain error a 100 pF capacitance measured at 1 MHz could be compared to a 1590 Ω reference since they should produce an equal Z. A limitation of load correction is that it works best when the reference value is close to the value of the device being measured. For this reason load correction is not very useful for research applications where the measured devices are usually not mass produced and identical copies of each other. Short circuit correction is obtained by connecting the probes together or to the same contact pad. The effects of short circuit correction are emphasized when measuring very big capacitances, which translate to very small impedances. Conversely, for open circuit correction the probes are set into their actual measurement positions, but without anything connecting them, leaving the circuit open. Open circuit correction has the most pronounced effect when measuring small capacitance, big impedance devices. All three corrections are applied to a measured value by using [1]

$$Z_{corrected} = \left(\frac{1}{Z_{measured}/\alpha - Z_s} - \frac{1}{Z_o}\right)^{-1} \tag{2.68}$$

where Z_s and Z_o are the short and open circuit impedances respectively. In an ideal situation α would have a value of 1, Z_s would be zero and Z_o infinite making $Z_{measured}$ equal to $Z_{corrected}$. It should be noted that poorly performed corrections will produce more erroneous results than no corrections at all. To facilitate the correction process many modern CV meters have built in load, short and open circuit corrections. [1]

Chapter 3

Measurements

3.1 Operating the ICS 3.5.1

All measurements were performed using Interactive Characterization Software (ICS) version 3.5.1 by Metrics Technology Inc. Low-frequency CV was measured with the Keithley 595 quasistatic CV-meter, which uses the feedback charge method. High-frequency CV was measured with the Hewlett-Packard 4192A LF impedance analyzer.

This section (3.1) will describe how to create a measurement project with the ICS 3.5.1. After ICS has finished loading, the first step is to create a new project. If a project with desired settings already exists it can be loaded by choosing "File" and "Open" from the top toolbar. A project can contain different measurements with a variety of instruments each having one or several different configurations.

The next step is to choose the measurement instruments from the icon highlighted with red circle in figure 3.1. This will open a list of instruments presented in figure 3.2. From the list, the "KI595" is chosen for low-frequency feedback charge CV and "HP4192" for high-frequency impedance CV.

Figure 3.1: Choosing the measurement instruments.

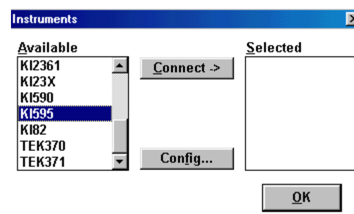


Figure 3.2: List of measurement instruments.

After choosing the instruments for the project, it is time to set up the actual measurements from the "Edit test setup"-icon highlighted by the red circle in figure 3.3. This will open

the measurement setup editor in figure 3.4.

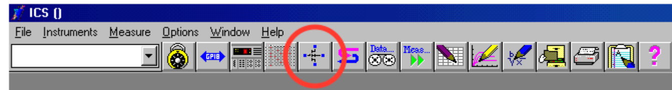


Figure 3.3: Entering the measurement setup menu.

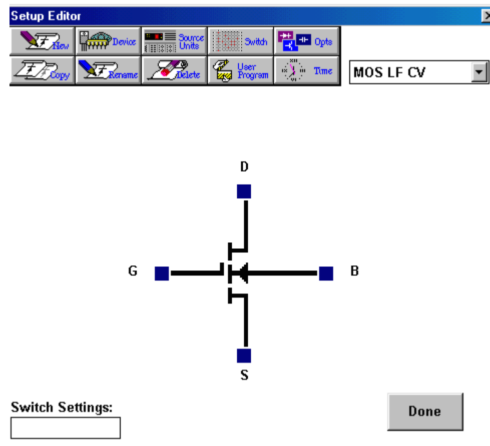


Figure 3.4: Measurement setup.

Each measurement can have its own name, device under test and sweep parameters. First, a new measurement is created from the "New"-icon and provided with a name. In the example "MOS LF CV" is chosen as the name of this measurement. Next, a device under test is selected from the "Device"-icon, which opens the list in figure 3.5. From the list "CAP" is chosen for MOS CV measurements.

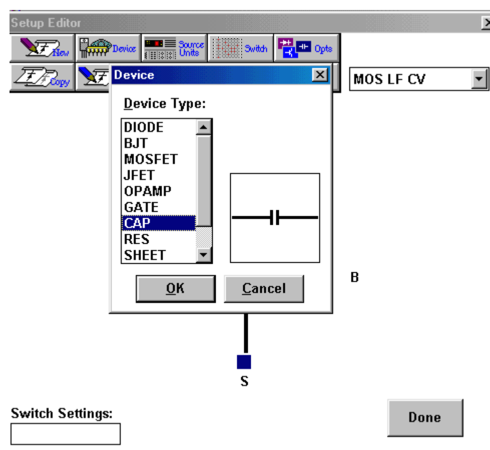


Figure 3.5: Selecting the measured sample device.

Next the source measurement units (SMUs) are added from the "Source units"-icon in figure 3.4. Since low-frequency CV is being set up first, source units in figure 3.6 are chosen for "KI595" and assigned as in in figure 3.7. An SMU is selected from the list and assigned to a desired terminal by clicking the terminal. The choice is cancelled by clicking the terminal again while its assigned SMU is selected. In this example "KI595.IN" is assigned

to terminal A and "KI595.OUT" to terminal K. Setup for HP4192 in high-frequency CV is done in a similar fashion in figure 3.8.

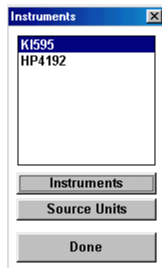


Figure 3.6: Choosing the measurement instrument.

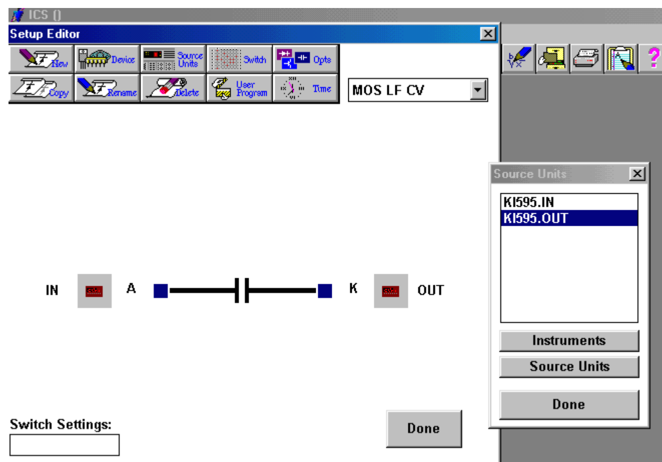


Figure 3.7: Setting up the SMUs for KI595.

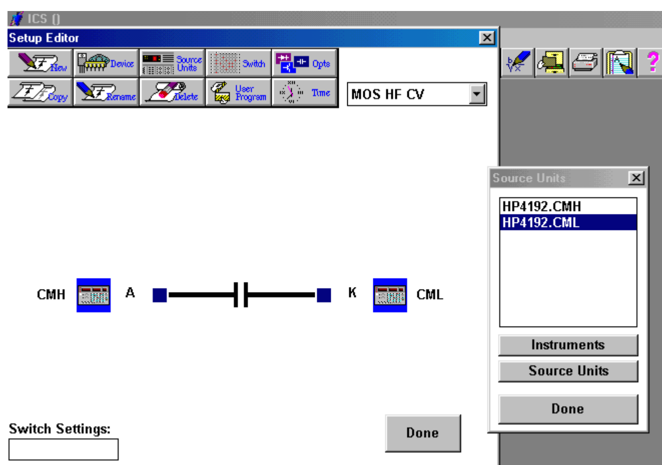


Figure 3.8: Setting up the SMUs for HP4192.

The "Additional options"-icon in figure 3.4 allows the user to choose whether capacitance or current, bias voltage or Q/t is displayed in the Keithley 595 front panel during the measurement (figure 3.9). Leaving the setting to capacitance is recommended for the first measurements from a new contact, since it is the only indicator of contact quality during

an ongoing measurement. After the contact has been verified to be of good quality the setting can be switched to display bias voltage, since this allows the operator to monitor the progress of the measurement.

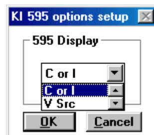


Figure 3.9: Additional options setup.

The menu for measurement parameters for the KI595 in figure 3.10 is accessed by clicking the "OUT" SMU assigned to terminal K in the setup editor main view in figure 3.7.

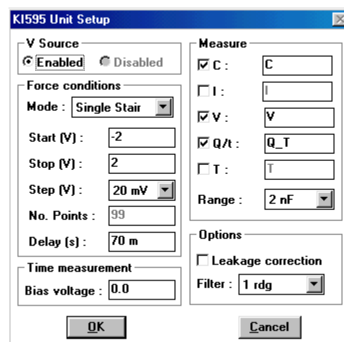


Figure 3.10: Measurement parameters for KI595.

The Keithley 595 allows start and stop biases between -20 and 20 volts. The measurement can also be performed from negative bias to positive or the other way around. Sweeping from accumulation to inversion is faster, since it is recommended to hold the sample under starting bias for a while before beginning the sweep if starting from inversion. Step voltage determines the density of data points in voltage axis, 50 mV is recommended for initial test measurements while 10 mV will provide denser datapoints which is useful especially when seeking flat band voltage using equation 2.45. Delay time can be chosen between 0.07 and 199 seconds, and it is up to the user to determine the optimal delay. At too low delay values the MOS will be unable to reach equilibrium and a low-frequency curve will not be obtained. Too high delays will needlessly increase measurement time at best and measure incorrectly high accumulation and inversion capacitances at worst. Depending on the sample, values between 5 and 30 seconds were found sufficient for a low-frequency equilibrium curve in dark measurements. Under illumination, 0.1 seconds was enough for all tested samples. In addition, the user can choose which parameters are measured and logged, capacitance, bias voltage and Q/t being the default selections. The leakage correction performed under expectations in most cases. Samples that provided good curves even without the correction gained nothing from the added correction while poor quality curves often degraded even further. Finally a sliding average window can be used for smoothing the measured curve. Filter value of "1 rdg" equals no averaging.

The high-frequency measurement is set up similarly by choosing "New" in measurement setup editor in figure 3.4. The name in this example is set as "MOS HF-CV". After naming the new measurement the SMUs are set up as in figure 3.8, terminal A was chosen for "CMH" and terminal K for "CML". The measurement parameters menu for HP4192 in

figure 3.11 is accessed by clicking the "CMH" SMU assigned to terminal A in the setup editor main view.

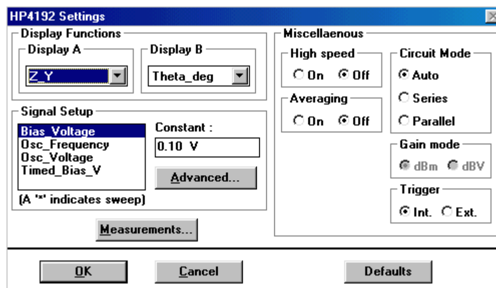


Figure 3.11: Measurement parameters for HP4192.

Display A and B options are for meter front panel display during measurements. Oscillation frequency was chosen between 100 kHz and 1 MHz for most of the samples. An upper limit of 13 MHz for signal frequency is reported in HP4192 specifications, but in practice the quality of measurement results showed a quick decline as frequency was increased past 1 MHz, which was deemed the optimal level. Deficiencies in cabling, incorrect cable length compensation or probe station structure are the likely causes for poor performance near the frequency maximum. Signal oscillation voltage of 20 mV was used for most measurements to ensure small signal AC conditions.

After the measurement setup is complete the setup editor can be closed and measurement started by clicking the "Measure"-icon in figure 3.12 which opens the menu in figure 3.13, and by choosing "Single". The desired measurement profile can be chosen between "MOS LF-CV" and "MOS HF-CV" profiles.

Figure 3.12: Measurement icon.

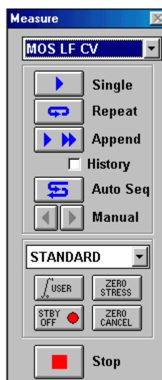


Figure 3.13: Initiating the measurement.

After the measurement has finished, which is indicated in KI595 front panel by a "trig" text and in HP4192 front panel by bias returning to zero, the measured CV data should be automatically plotted in the ICS main view. If no curve is visible, incorrect focusing or

too high zoom levels are the usual causes. Selecting "Axis" and "Auto scale" in figure 3.14 will fit the whole curve to the visible axis for a quick evaluation before exporting the data.

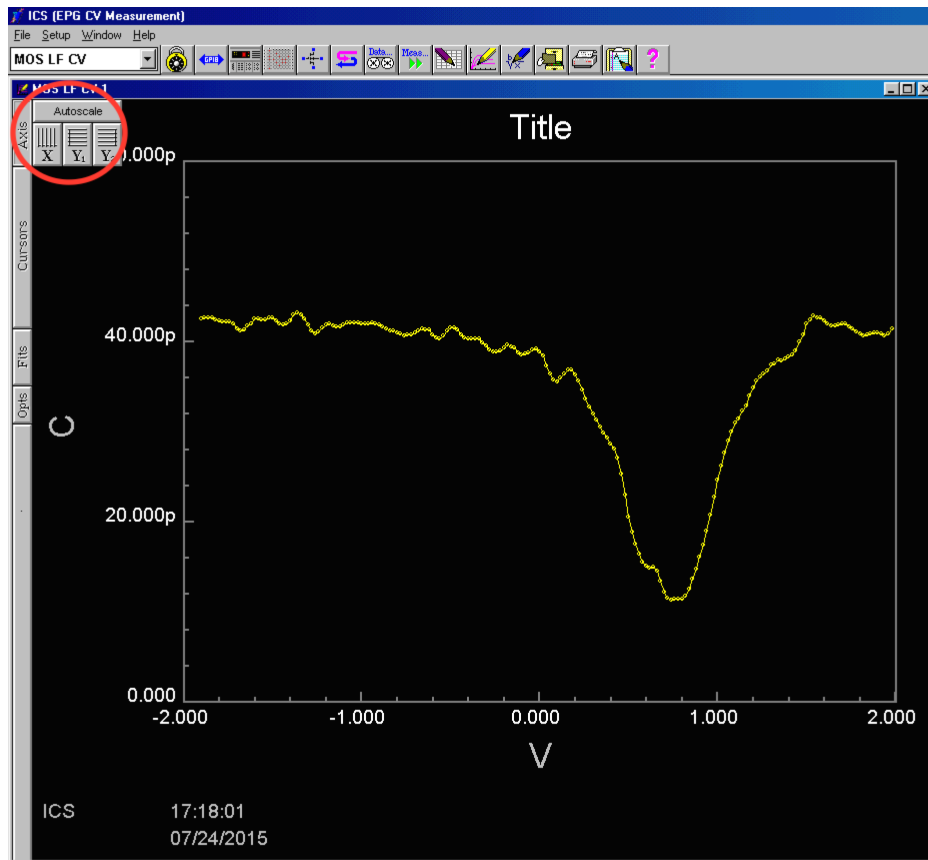


Figure 3.14: Autoscaling the curve.

If the project does not yet have a name, which is visible in the top blue bar in figure 3.14, a name can be assigned or changed by selecting "File" and "Set project name". Finally the data can be exported from the top left menu by selecting "File" and "Export". It should be noted that the exported data contains only measurement vectors selected by the user and minimal information of selected sweep parameters. Some important parameters, such as delay time, have to be manually edited into the exported file by using a text editor. Naturally the program has no awareness of the connections in the measurement setup, so it is also recommended to document which way the meter terminals are connected to the sample. This way it is possible to later define for instance whether negative bias in the curve refers to the gate or the substrate being at lower potential. If a bias voltage is manually set over the sample, the time under bias before starting the measurement has to be manually documented as well. Maintaining bias over the sample before initiating the measurement is useful if the bias sweep starts from inversion or if hysteresis due to mobile charge in the dielectric is being investigated.

3.2 Sample preparation and practical phenomena

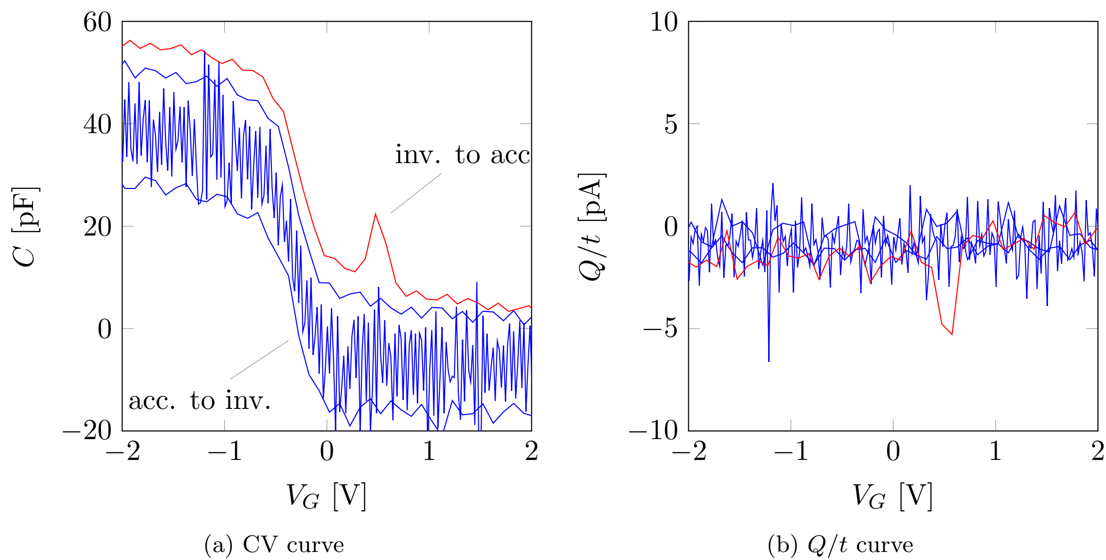
3.2.1 Contact preparation

One of the nine samples contained various microfabricated devices, such as MOSCAPs and transistors on a p-Si wafer with SiO_2 dielectric, with both the gate and substrate connections on the same side of the wafer. Other samples consisted of uniform silicon and ALD deposited dielectric layers with no individual devices or surface geometry. All of the samples except for the SiO_2 on p-Si underwent similar preparations.

Gate contacts were prepared by thermally evaporating 200-400 nm of aluminum on the dielectric. The aim was to create sufficiently thick gates to withstand the wear and tear caused by the repeated probe needle insertions. Back contacts to the silicon substrate were prepared by scratching the oxide surface with a diamond pen and applying indium-gallium eutetic to ensure a good ohmic contact. The back contact was then pressed against a copper plate as recommended [6], since the eutetic which remains adhesive in room temperature will contaminate the probe station otherwise. Contact to the sample was established by connecting the needles into the aluminum gate and the copper plate.

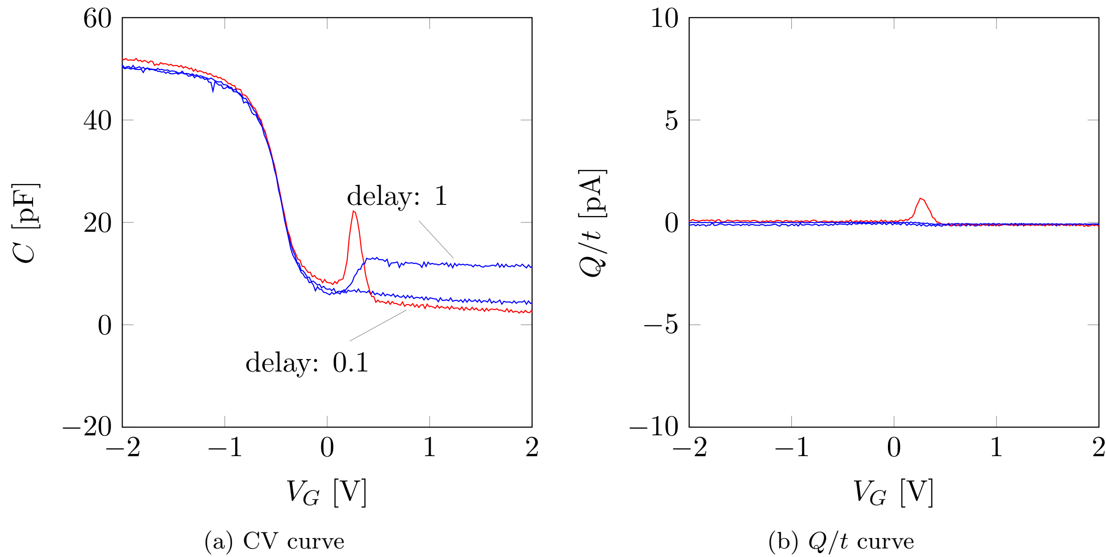
3.2.2 Noise comparison between gate- and substrate-connected bias

Connecting the bias voltage terminal to the substrate will significantly reduce the noise in measured curves. Therefore the bias source or high terminal needle should be connected to the copper plate while the low terminal is connected to the gate. The significance of connecting the bias voltage to the MOS substrate instead of gate is illustrated in figures 3.15 and 3.16.



(a) CV curve (b) Q/t curve

Figure 3.15: Bias voltage connected to gate. Measured CV and Q/t using delay times of 0.1 and 1 display not only significant noise, but also vertical drifting between measurements. Blue curves are swept from accumulation to inversion, red from inversion to accumulation.



(a) CV curve

(b) Q/t curve

Figure 3.16: Bias voltage connected to substrate. Noise levels are significantly reduced and consistency between curves improved compared to figure 3.15. Blue curves are swept from accumulation to inversion, red from inversion to accumulation.

Since all the measurements were performed with bias connected to the substrate, all of the voltage axes in the following results had to be inverted to be consistent with chapter 2 and most of the literature where the bias appears to be connected to the gate. Negative bias voltage in the figures of chapter 3.2 figures therefore refers to the gate being at a lower potential than the substrate.

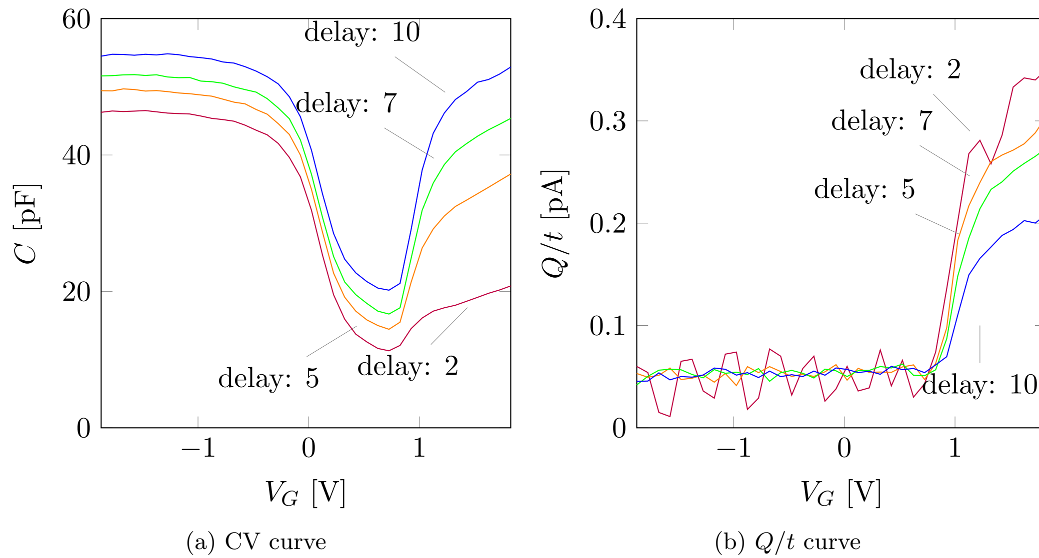
3.2.3 Effects of delay time in low-frequency CV

Inversion capacitance

The choice of delay time t_{delay} is a compromise between equilibrium, noise, and offset properties of the CV curve. At too low values of t_{delay} the MOS is unable to reach the appropriate low-frequency inversion capacitance and the resulting curve will resemble a high-frequency curve. Figure 3.17 illustrates the transition from low-frequency curve towards a high-frequency curve as t_{delay} is reduced. In figure 3.17a the lowest t_{delay} CV curve approaches high-frequency flatness in inversion and the Q/t curve in figure 3.17b transitions further away from its ideal flat state displayed in accumulation and depletion. The Q/t curve matches the non-equilibrium behavior discussed in section 2.3.1 and the example curve shown in figure 2.14c. The minimum t_{delay} for reaching full inversion region capacitance, which is characteristic for a low-frequency curve, varied from 1 to 30 seconds depending on the sample.

Vertical shifting

In addition to the inversion region curve shape, increasing t_{delay} usually caused an uniform increase in capacitance over all bias voltages as displayed in figure 3.17a. Whether the effect is caused by a problem in feedback charge method, the construction of the Keithley595 meter or problems in the measurement, is unknown. A choice must be then made how to align the curves since accumulation and depletion capacitances cannot depend on t_{delay}.



(a) CV curve

(b) Q/t curve

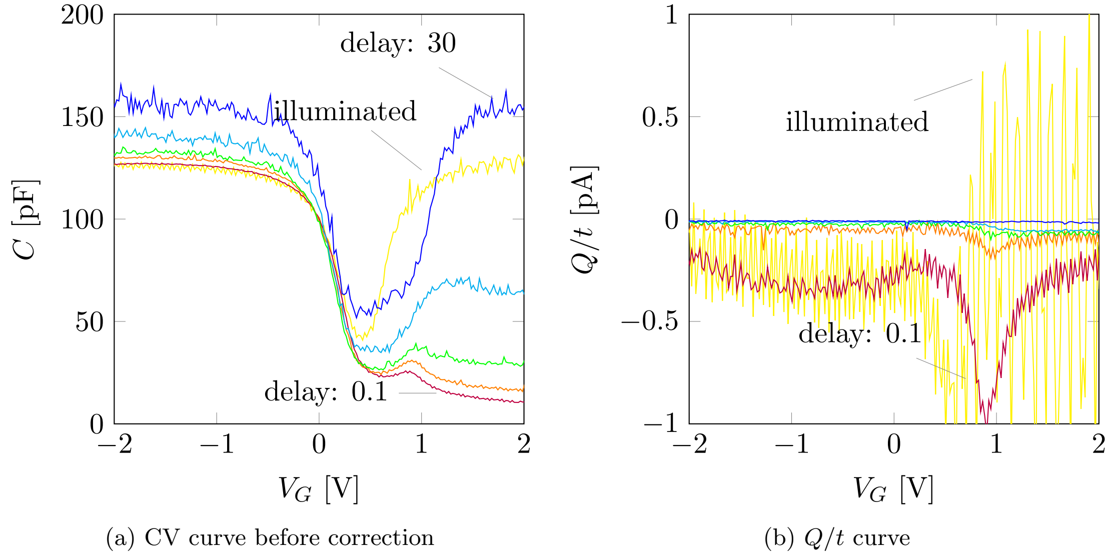
Figure 3.17: Delay time effects on inversion capacitance and vertical shifting. Curves are measured from a SiO_2-Si sample.

The fact that dielectric permittivities for ideal curves had to be reduced from their bulk values in order to fit the ideal curve into the data suggests that the higher t_{delay} curves would be correct. Because the high t_{delay} curves have higher capacitances, the ideal curves that were always too high, would need to be adjusted downwards less, requiring a smaller adjustment to ε_r bulk values than when aligning to low t_{delay} curves. However, some adjustment is still required. In addition, it is possible that permittivity starts to lower from its bulk value as layer thicknesses reach down to tens of nanometers. It is also possible that the provided dielectric thicknesses, which were measured by ellipsometry, are incorrect.

On the other hand, lowest delay capacitances can be assumed to be more accurate excluding the inversion region since the CV curve shape usually became increasingly deformed as t_{delay} increased towards its maximum value of 199. Another point in favor of lower t_{delay} curves being more accurate is that the calculated D_{it} are closer to COCOS reference results. Also, in some cases the probe station was intentionally left open to illuminate the sample with ambient light. This was done to obtain a low-frequency curve much faster than normal to check the quality of the contact before starting the actual measurements from which parameters were extracted. The accumulation capacitance of illuminated curves matches the capacitance of low t_{delay} curves. However, while depletion capacitance is significantly increased due to all the increased free carrier generation, the depletion capacitance for high t_{delay} curves was still higher in most cases, which suggests false results.

Noise

In addition to the two aforementioned effects, t_{delay} also affects noise levels in most of the measured curves as shown in figure 3.18. While Q/t curves in figure 3.18b are improved the smoothness of the CV curves in 3.18a declines as t_{delay} is increased. Curves were measured using t_{delay} of 0.1, 1, 3, 10, and 30 seconds.



(a) CV curve before correction

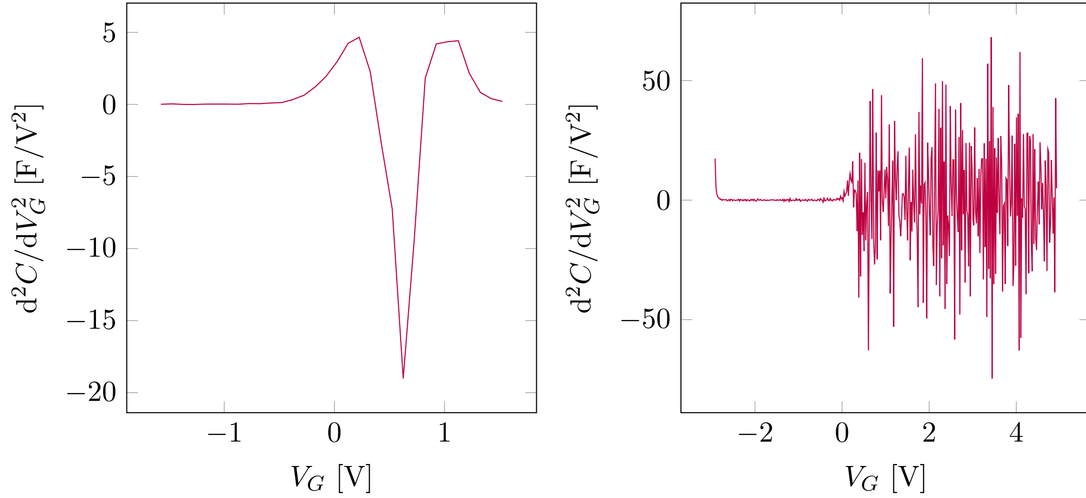
(b) Q/t curve

Figure 3.18: Delay time effects on inversion capacitance, vertical shifting and noise. The elevated depletion capacitance of the illuminated curve is nearly equal to the high delay curve, suggesting that the high delay curve has shifted upwards.

3.2.4 Noise filtering from the measured data

Calculation of flat band voltages from the curves was attempted mostly by ideal curve fitting. Cross-checking was performed whenever possible by using equation 2.45, since equation 2.44 was applicable only for the SiO_2 on p-Si sample. If equation 2.45 is used for V_{FB} extraction, differentiating a measured curve twice is required, making noise a significant problem. Out of the nine measured samples only the SiO_2 and the Al_2O_3 sample 6A provided curves with low enough noise, so that the flat band voltage peak of the second derivative could be distinguished from the noise induced peaks and results from several curves were consistent with each other. In addition to the problems with V_{FB} extraction, high noise made it difficult to calculate accurately D_{it} levels of $10^{11}/\text{ev}/\text{cm}^2$ and below.

Reducing the effects of noise in the measured curves was attempted by two different methods. First method was to smoothen the curve by using a moving average window of five sample points with the operated data point in middle of the window. This was done to prevent the horizontal shifting along the voltage axis, caused by moving averages in which the operated point is in the leading edge of the window. The magnitude of the second derivative maximum was not relevant, only its position in the voltage axis. The second method was MATLAB's fast fourier transform (FFT)-based "fftfilt"-function. The level of usefulness and results provided by the two methods proved fairly similar, FFT filtering



(a) Second derivative of a low-noise CV curve (b) Second derivative of a high-noise CV curve

Figure 3.19: Second derivatives of smoothed CV curves. Low-frequency curves from p-type samples were used. The left peak corresponds to flat band voltage, right peak is ignored and it disappears if a high-frequency curve is used. Conversely for n-type samples the right peak corresponds to flat band voltage and left peak is ignored.

being slightly more consistent. The difference in second derivatives of low- and high-noise curves after curve smoothing is presented in figure 3.19. In the low-noise curve the first peak corresponds to flat band voltage. Despite the smoothing, the flat band peak in the high-noise curve is impossible to distinguish from the noise induced peaks.

3.2.5 Hysteresis

One of the advantages of contact CV over the COCOS method is the ability to perform repeated measurements. Repeated measurements are useful for exposing and studying hysteresis effects caused by slow moving mobile charges in the dielectric. The sample is maintained under accumulation bias over extended period of time, then bias is swept from accumulation to inversion in the measurement process. Afterwards the measurement is repeated using opposite direction by first holding the sample under inversion bias and then sweeping from inversion to accumulation. The consecutive runs should produce identical curves which have shifted horizontally with respect to each other from which mobile charge can be determined using [7]

$$Q_m = -C_{ox} \Delta V_{FB} \,. \tag{3.1}$$

Since in COCOS method the corona charge remnants from previous measurements disturb the following measurements from the same point, only a single bias sweep from accumulation to inversion is preferred, which leaves the hysteresis effect undetected.

Figure 3.20 shows hysteresis in HfO_2-Si. Bias voltage in red curves is swept from inversion to accumulation meaning from left to right in the figure. Blue curves are swept from accumulation to inversion. The hystersis effect is clearly connected to the sweep direction. The effect was also confirmed by manually applying a bias voltage over the sample for

the duration of one minute, followed by seeking the capacitance minimum by measuring discrete voltage points using the front panel of the meter. Hysteresis in HfO_2 has also been reported by Wong et al. [35] and Pereira et al. [36]. All the curves display full low-frequency inversion capacitance, despite the low t_{delay} times of 0.1 and 1 seconds used, whereas the other samples required delay times in the order of 10 seconds for a true low-frequency curve.

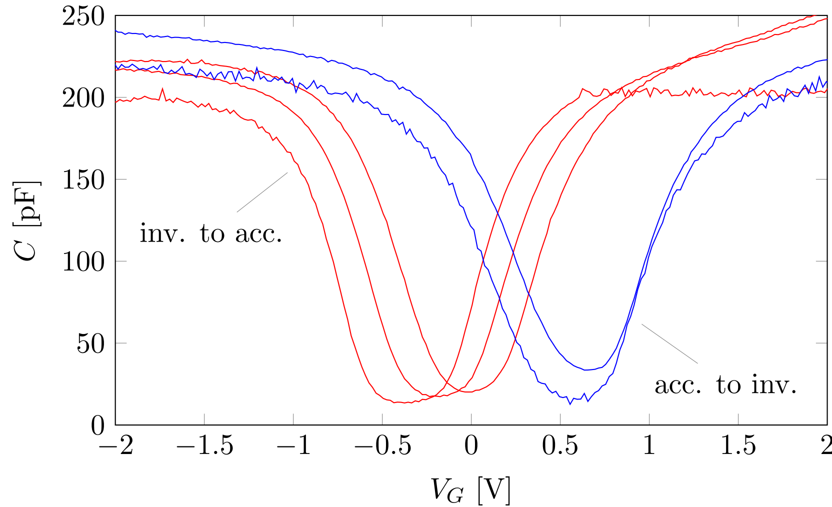


Figure 3.20: Hysteresis in HfO_2-Si.

3.2.6 Leakage current

A shortcoming of low-frequency CV compared to high-frequency CV and COCOS is its vulnerability to leaky dielectrics. For demonstration a TiO_2 on n-Si sample was used. TiO_2 on n-Si is expected to perform poorly in CV measurements, because the majority carrier band edge has an offset of zero volts [34] in the TiO_2-Si interface, as illustrated in figure 3.21.

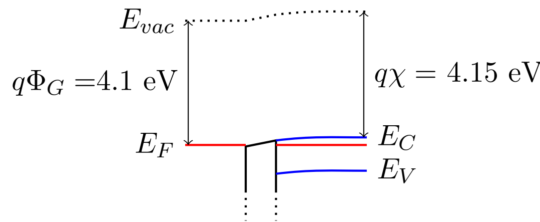


Figure 3.21: TiO_2-Si conduction band

Because of the zero offset, the conduction bands of the Al gate, TiO_2 insulator, and n-Si substrate form an almost flat conduction band over the entire structure with no potential barrier whatsoever. As a result leakage currents were too high for low-frequency measurements to be performed. Varying capacitances could be measured at zero bias, but applying any bias over the structure caused the Keithley595 to display the current overload warning and stop measuring. As expected, high-frequency measurement attempts

succeeded better for a leaky structure. The data in figure 3.22 has the characteristic features of a CV curve, but the curve quality is still too low for parameter extraction. Dissipation factor D discussed in section 2.3.2 indicates the amount of leakage current as measured conductance divided by susceptance. For ideal MOS conductance should be zero but throughout the measurement the dissipation factor was in the range of 3-10. Because charge can easily pass through the oxide, charge cannot accumulate on the semiconductor surface and as a result accumulation capacitance remains significantly below the level predicted by the ideal curve.

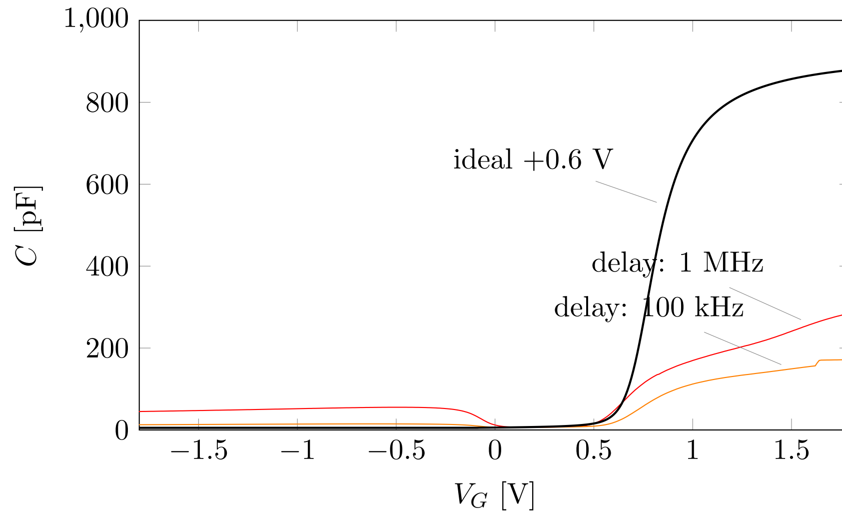


Figure 3.22: Leaking TiO_2-Si MOS. Since charge cannot accumulate on the semiconductor surface, due to the leaking through the oxide, the accumulation capacitance can not rise to its expeted level. Higher frequency is less affected, as expected.

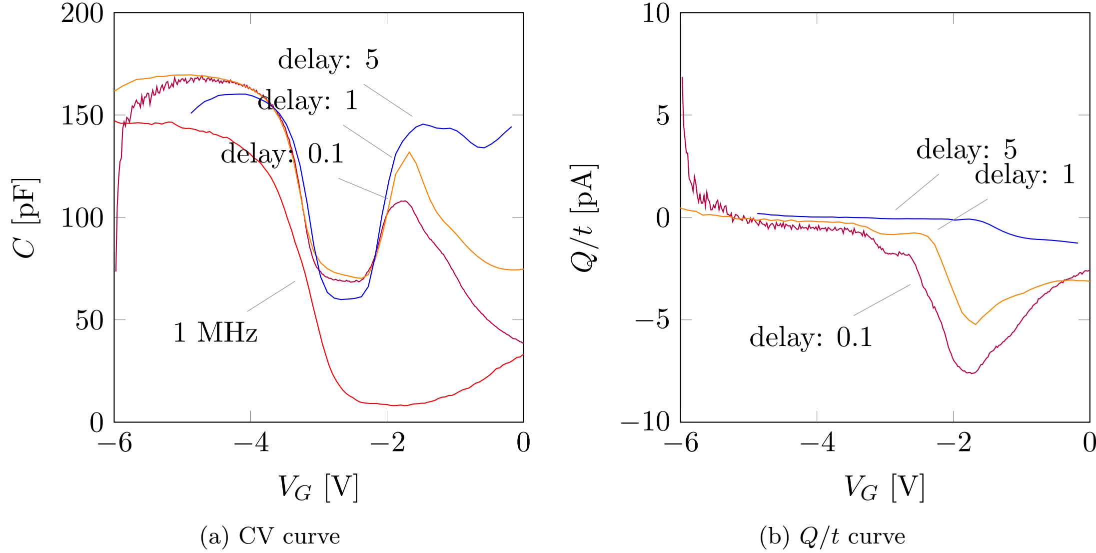
3.3 Results

In section 3.3.1 the parameter extraction process is exemplified using sample 6A, which has Al_2O_3 on p-type silicon. Extracted parameters for all the measured samples are listed in section 3.3.2.

3.3.1 Parameter extraction from measured data

Measured CV and QT curves for sample 6A are presented in figures 3.23a and 3.23b. Low-frequency CV was measured with delay times of 0.1, 1, and 5 seconds. Additionally, a high-frequency curve at 1 MHz was included. Unlike most samples sample 6A did not exhibit the vertical shifting of low-frequency curves that was described in section 3.2.3. All three low-frequency curves are aligned in slope between accumulation and depletion at -3.5 V so manually aligning the curves to the same level is not required. The Q/t value in the delay: 5 curve is flat from -5 V to -2 V displaying equilibrium condition and signifying a true low-frequency curve in the aforementioned voltage range. For voltages above -2 V the Q/t is no longer flat, which can be seen as a droop in the respective bias area of the CV curve, making the deep inversion part of the curve useless for D_it extraction. The

high-frequency curve should align with the low-frequency curve in deep accumulation. Whether the measured low-frequency capacitances are incorrectly high or high-frequency capacitance incorrectly low is unknown so the differences will be ignored for now.



(a) CV curve

(b) Q/t curve

Figure 3.23: Measured Al_2O_3-Si CV and Q/t.

Oxide thickness, oxide capacitance, gate area, and oxide permittivity

First step of the parameter extraction process is determining the maximum capacitance from the measured curves, which corresponds to C_{ox}. Since the delay: 5 curve shows anomalous behavior near the starting point of the sweep, the maximum capacitance will be determined from the faster delay: 0.1 and delay: 1 curves, yielding a highest possible $C_{ox,min}$ of 170 pF. The smallest possible $C_{ox,min}$ is 150 pF from the high-frequency curve.

The second step of the extraction process is to measure the gate area A. The rectangular aluminum gates have an area of $6 \cdot 10^{-4}$ cm^2 with an error margin of ±5%.

With C_{ox} and A, the oxide thickness can now be calculated by using a relative permittivity ε_r of 9 for the Al_2O_3 [34] and equation 2.5

$$C_{ox} = \varepsilon_0 \varepsilon_r \frac{A}{t_{ox}} .$$

The smallest possible oxide thickness $t_{ox,min}$ of 27 nm is obtained with a gate area that is 5% smaller than the measured $6 \cdot 10^{-4}$ cm^2 and C_{ox} of 170 pF. The largest possible $t_{ox,min}$ is 35 nm with a gate area 5% larger than measured value and C_{ox} of 150 pF. Obtaining the t_{ox} of 25nm measured using ellipsometry would require lowering the Al_2O_3 permittivity from 9 to 6.7 - 8.4 for the 35 nm and 27 nm results respectively. Relation between parameters is presented in table 3.1.

Table 3.1: Parameters for minimum and maximum oxide thickness.

	t_{ox} [nm]	C_{ox} [pF]	A [cm^2]	ε_r
min t_{ox}	27	170	$0.95 \cdot 6 \cdot 10^{-4}$	9
avg t_{ox}	30	160	$1.00 \cdot 6 \cdot 10^{-4}$	9
max t_{ox}	33	150	$1.05 \cdot 6 \cdot 10^{-4}$	9
min ε_r for $t_{ox} = 25$ nm	25	150	$1.05 \cdot 6 \cdot 10^{-4}$	6.7
max ε_r for $t_{ox} = 25$ nm	25	170	$0.95 \cdot 6 \cdot 10^{-4}$	8.4

Dopant density

Next the average dopant density is calculated using the maximum-minimum method in equation 2.35

$$\frac{N_A}{\ln(N_A/n_i) + \frac{1}{2}\ln(2\ln(N_A/n_i) - 1)} = \frac{4kT\varepsilon_{ox}^2}{q^2\varepsilon_s t_{ox}^2}\left(\frac{C_{ox}}{C_{hf,min}} - 1\right)^{-2}$$

which requires a true high-frequency curve, because D_{it} will increase the C_{min} value in a low-frequency curve. The average t_{ox} of 30 nm and ε_r of 9 from table 3.1 were used together with C_{ox} and $C_{hf,min}$ of 150 pF and 9 pF from the high-frequency curve in figure 3.23a. Calculated dopant density N_A is $2.5{\cdot}10^{15}/\text{cm}^3$, which is three times higher than the reported value of $8{\cdot}10^{14}/\text{cm}^3$ from resistivity measurements, making the result fairly accurate. Shifting the high-frequency curve 20 pF higher so that it aligns with the low-frequency curves in accumulation would increase the calculated doping density by an order of magnitude, suggesting that the unaltered curve is closer to the correct curve shape. The minimum value of the curve has significantly higher impact than maximum value when calculating dopant density. If the minimum value is kept at 9 pF but the maximum of the high-frequency curve is stretched up to 170 pF to align with the low-frequency curves in accumulation, the resulting N_A is $1.9{\cdot}10^{15}/\text{cm}^3$, which is in closer agreement with the dopant density from resistivity measurements. It is then possible that the high-frequency curve has failed to achieve its proper accumulation height for some reason, but the minimum value is correct. Later it is shown that the ideal curve aligns with the minimum value of the high-frequency curve in depletion as it should, further supporting the claim that the minimum value of the high-frequency curve is correct.

Theoretical curve

With the necessary parameters extracted, the theoretical ideal CV curve in figure 3.24 can now be calculated using the equations in section 2.2.3. Parameters from the top row of table 3.1 were chosen since they provided the best fit into the measured curves. Dopant density of $8{\cdot}10^{14}/\text{cm}^3$ from resistivity measurements was used for this example, but the differences in curve shape with the calculated dopant density of $2.5{\cdot}10^{15}/\text{cm}^3$ is negligible.

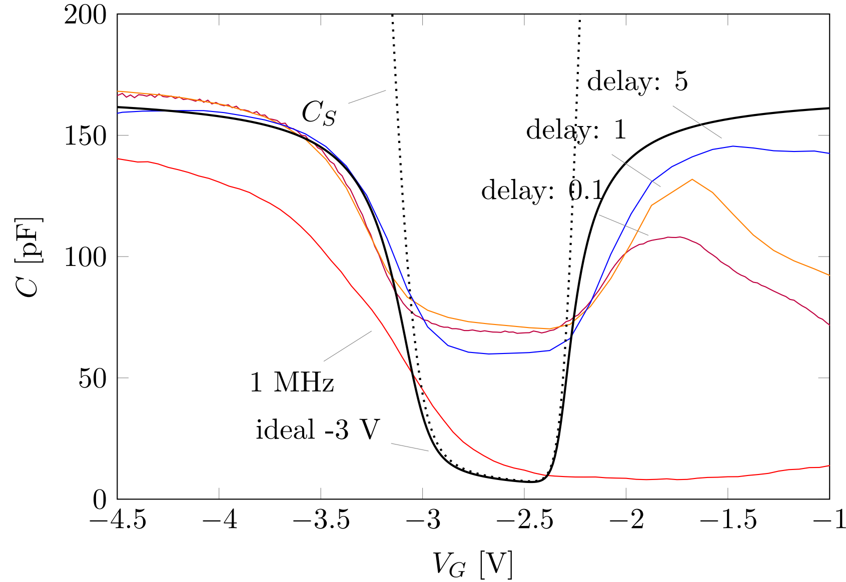


Figure 3.24: Measured Al_2O_3-Si CV with theoretical curve. The theoretical curve has been shifted -3 V to the left to fit into the measured curves indicating a flat band voltage of -3 V. At high frequencies D_{it} does not contribute additional capacitance which is why the high-frequency curve aligns with the ideal $D_{it} = 0$ curve in depletion. Low-frequency depletion capacitance is increased due to D_{it} contribution.

Flat band voltage

Flat band voltage can be determined from the -3 V shift to the ideal curve in figure 3.24 or calculated by using equation 2.45

$$\frac{d^2}{dV_G^2}\left(\frac{C_{ox}}{C_{hf,m}}\right)^2$$

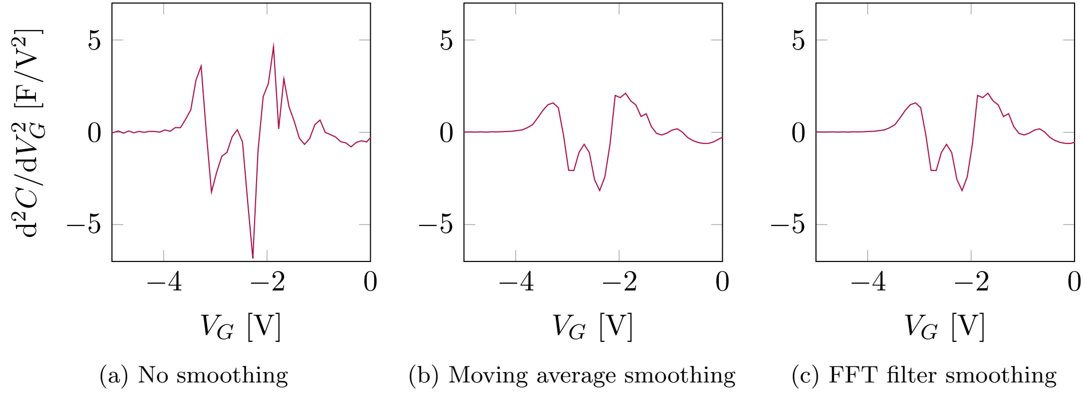
which yields V_{FB} of -3.2 V. Second derivatives of raw and filtered curves are presented in figure 3.25. The results between the two methods are in reasonably good agreement.

Oxide charge

Oxide charge Q_{ox} is calculated using equation 2.46

$$Q_{ox} = (\Phi_{GS} - V_{FB})\, C_{ox}$$

with the gate-substrate contact potential Φ_{GS} of -0.89 V from table 2.3. Using C_{ox} of 170 pF from the top row of table 3.1, which were the values used for the ideal curve, yields Q_{ox} of $3.88 \cdot 10^{12}/\text{cm}^2$ and $4.24 \cdot 10^{12}/\text{cm}^2$ for a V_{FB} of -3 V and -3.2 V respectively. The high positive charge is most likely due to corona charge remnants from COCOS measurements that were performed on the sample earlier.



(a) No smoothing (b) Moving average smoothing (c) FFT filter smoothing

Figure 3.25: Second derivatives of delay:1 curve. The left peak corresponds to flat band voltage.

Surface state density

Density of states can be obtained using equation 2.41

$$C_{it}(\psi) = \left(\frac{1}{C(\psi)} - \frac{1}{C_{ox}}\right)^{-1} - C_S(\psi), \ .$$

If only midgap D_{it} is required the C and C_S can be replaced with the depletion region minima of the measured curve and ideal curve. This is due to C_S being approximately equal to the capacitance of the ideal curve at the depletion region minimum as shown in figure 3.24. For D_{it} over a wider range in the bandgap the delay: 5 curve was used in order to extract the D_{it} from accumulation to threshold in a range of approximately -4 V to -1.8 V. The other curves are useful only from -4 V to -2.4 V. For accurate results the measured $C(V_G)$ needs to be transformed to $C(\psi)$ using the Berglund integral in equation 2.42

$$\Delta\psi = \psi_0 + \int_{V_{G,0}}^{V_G} \left(1 - \frac{C_{lf}(V_G)}{C_{ox}}\right) dV_G \, .$$

Since the Berglund integral indicates the change of band banding from $V_{G,0}$ to V_G, which is then added to a known value of band bending ψ_0, it is necessary to know the band bending in a single point of the CV curve. The flat band point where band bending is zero is then the natural choice for $V_{G,0}$, making ψ_0 zero and removing it from the equation. For the D_{it} calculation V_{FB} of -3.1 V was used. To avoid integrating twice, first from flat band to accumulation, then from flat band to inversion and finally combining the results, the following procedure was used: The integration was performed for the delay: 5 curve from V_G =-4 V to V_G =-1.8 V, obtaining band bending for each respective value of gate bias voltage $\psi(V_G)$

$$.\psi(V_G) = \begin{bmatrix} V_{G,1} & V_{G,2} & \dots & V_{FB} & \dots & V_{G,n-1} & V_{G,n} \\ \psi_1 & \psi_2 & \dots & \psi_{FB} & \dots & \psi_{n-1} & \psi_n \end{bmatrix} \tag{3.2}$$

Then ψ_{FB} was subtracted from each value of ψ in the matrix so that the ψ corresponding to V_{FB} is zero and all the other values of ψ are adjusted accordingly.

$$.\psi(V_G) = \begin{bmatrix} V_{G,1} & V_{G,2} & \dots & V_{FB} & \dots & V_{G,n-1} & V_{G,n} \\ \psi_1 - \psi_{FB} & \psi_2 - \psi_{FB} & \dots & 0 & \dots & \psi_{n-1} - \psi_{FB} & \psi_n - \psi_{FB} \end{bmatrix} \tag{3.3}$$

Now that the $\psi(V_G)$ relation is established, equation 2.41 can be used to calculate C_{it}, which is then substituted into equation 2.38

$$D_{it}(\psi) = \frac{C_{it}(\psi)}{qA}$$

for the results presented in figure 3.26. Locations of E_V and E_C in the ψ-axis are

$$E_V = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) - \frac{E_g}{2} \tag{3.4}$$

and

$$E_C = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) + \frac{E_g}{2}\,. \tag{3.5}$$

For n-type silicon the N_A/n_i in the logarithm is changed to n_i/N_D. The minimum D_{it} of the curve is in good agreement with the COCOS measured minimum of 10^{12}/ev/cm^2.

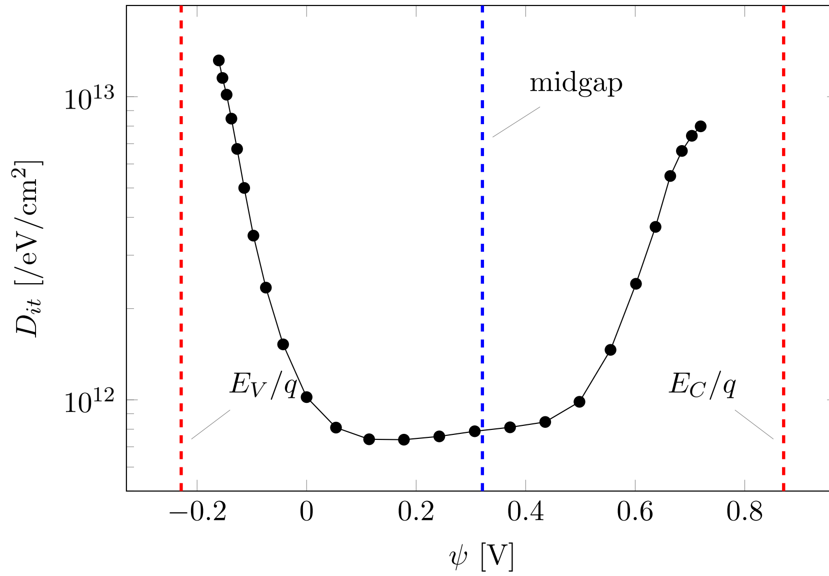


Figure 3.26: Measured Al_2O_3-Si D_{it} using V_{FB} of -3.1 V. The curve could be shifted to the right making it more symmetrical with respect to E_V and E_C by using a V_{FB} of -3.0 V.

Table 3.2: Summary of parameters for sample 6A. Measured oxide charge results are affected by corona charge remnants Q_C of the preceding COCOS characterization. The COCOS measured charge is $4.21 \cdot 10^{10}$ and Q_C at the end of the COCOS sweep was $4.2 \cdot 10^{12}$ so the reference value of $Q_{ox} + Q_C$ consists almost entirely of corona charge remnants. The COCOS measured reference value for D_{it} corresponds to D_{it} curve minimum. Reference value for t_{ox} was obtained using ellipsometry.

	t_{ox} [nm]	C_{ox} [pF]	A [cm^2]	ε_r	V_{FB}	$Q_{ox} + Q_C$ [q/cm^2]	D_{it} [/eV/cm^2]
min	27	150	$5.7 \cdot 10^{-4}$	9	-3.0	$3.9 \cdot 10^{12}$	$7.4 \cdot 10^{11}$
avg	30	160	$6.0 \cdot 10^{-4}$	9	-3.1	$4.1 \cdot 10^{12}$	$4.2 \cdot 10^{12}$
max	33	170	$6.3 \cdot 10^{-4}$	9	-3.2	$4.2 \cdot 10^{12}$	$1.3 \cdot 10^{13}$
ref	25	-	-	-	-	$4.2 \cdot 10^{12}$	$1.0 \cdot 10^{12}$

3.3.2 Extracted parameters for measured samples

In the parameter extraction example of section 3.3.1 adhering to the reported oxide permittivity values [34] was emphasized. This was accomplished by allowing the oxide thickness to differ from the ellipsometry results. However, for most of the measured samples, when ellipsometry thicknesses were used it was discovered that the theoretical curve could be best fitted into the measured data by using oxide permittivities approximately 80% of their reported values. It is possible that the permittivies of these materials are lowered from their bulk values for oxides approaching thicknesses of approximately hundred atomic layers and below. Numerous studies have reported permittivities of certain materials being affected by layer thickness, electric field and other parameters. However, extensive research of this subject was not within the scope of this thesis so it remains unknown whether the lowering of permittivity is an error in the CV process, ellipsometry thickness measurements or an actual physical phenomenon in the thin oxide layers.

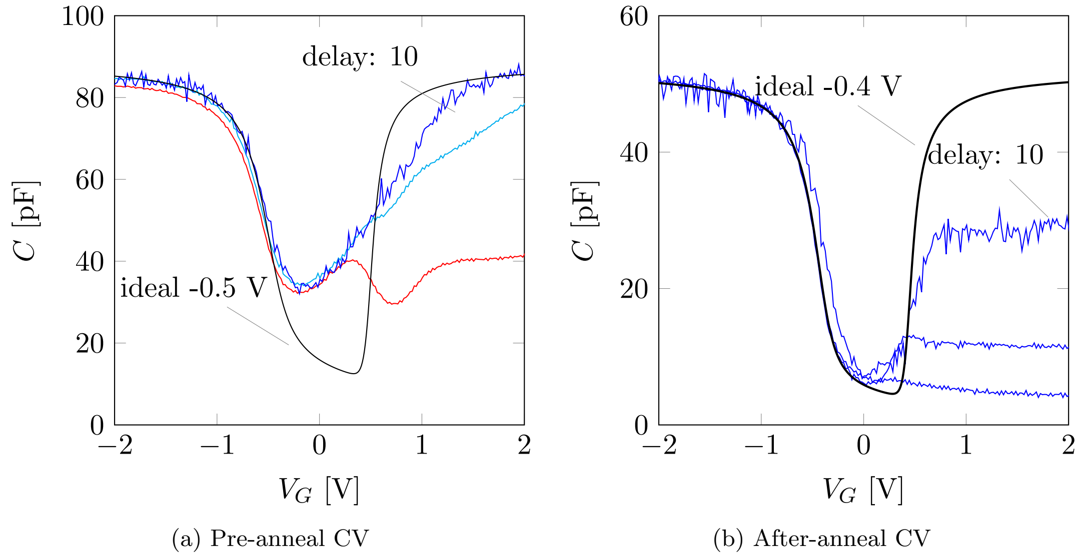
All reported D_{it} are midgap values using the depletion region minima of the measured curve and ideal curve as described in the previous section. Reference values for Q_{ox} and D_{it} were obtained from COCOS measurements and reference values for t_{ox} were measured with an ellipsometer. Sample nC14A could not be properly characterized due to high leakage. Reasons for the high leakage in TiO_2-Si interface were discussed in greater detail in section 3.2.6. Oxide charge for samples nC21D and AlN5A could not be calculated due to hysteresis in the CV curves which prevents V_{FB} acquisition. Mobile charge is not included in table 3.3, but can be calculated using equation 3.1.

Table 3.3: Parameters for all measured samples. Values that could not be calculated due to problems in the measured CV curve are listed as N/A. Values that were not calculated are marked with a dash and the provided reference value is used instead. Reference values marked with a dash were not available.

sample	oxide	substrate [/cm^3]	t_{ox} [nm]	ε_r	V_{FB}	Q_{ox} [q/cm^2]	D_{it} [/eV/cm^2]
6A	-	p-type $2.5 \cdot 10^{15}$	30	9	-3.1	$4.1 \cdot 10^{12}$	$8.6 \cdot 10^{11}$
ref	Al_2O_3	p-type $8.0 \cdot 10^{14}$	25	9	-	$4.2 \cdot 10^{12}$	$1.0 \cdot 10^{12}$
pre an.	-	-	-	7	-0.5	$-7.8 \cdot 10^{11}$	$8.9 \cdot 10^{11}$
ref	Al_2O_3	p-type $1.5 \cdot 10^{16}$	22	9	-	-	$1.9 \cdot 10^{12}$
aft an.	-	-	-	7	-0.4	$-9.0 \cdot 10^{11}$	$6.0 \cdot 10^{10}$
ref	Al_2O_3	p-type $4.9 \cdot 10^{15}$	22	9	-	-	$7.4 \cdot 10^{11}$
1A	-	-	-	7	0.2	$-1.8 \cdot 10^{12}$	$2.2 \cdot 10^{11}$
ref	Al_2O_3	p-type $4.6 \cdot 10^{15}$	22	9	-	-	-
2A	-	-	-	7	1.2	$-3.5 \cdot 10^{12}$	$1.0 \cdot 10^{11}$
ref	Al_2O_3	p-type $4.6 \cdot 10^{15}$	22	9	-	-	-
nC14A	-	-	-	80	N/A	N/A	N/A
ref	TiO_2	n-type $1.5 \cdot 10^{15}$	30	100	-	-	-
nC21D	-	-	-	16	N/A	N/A	$2 \cdot 10^{11}$
ref	HfO_2	n-type $1.3 \cdot 10^{15}$	25	26	-	-	-
AlN5A	-	-	-	8.3	N/A	N/A	$1.9 \cdot 10^{12}$
ref	AlN	p-type $2.5 \cdot 10^{15}$	35	9	-	-	-
SC Lab	-	p-type $2.0 \cdot 10^{15}$	36	3.9	0.1	$-6.2 \cdot 10^{11}$	$1.0 \cdot 10^{11}$
ref	SiO_2	-	-	3.9	-	-	-

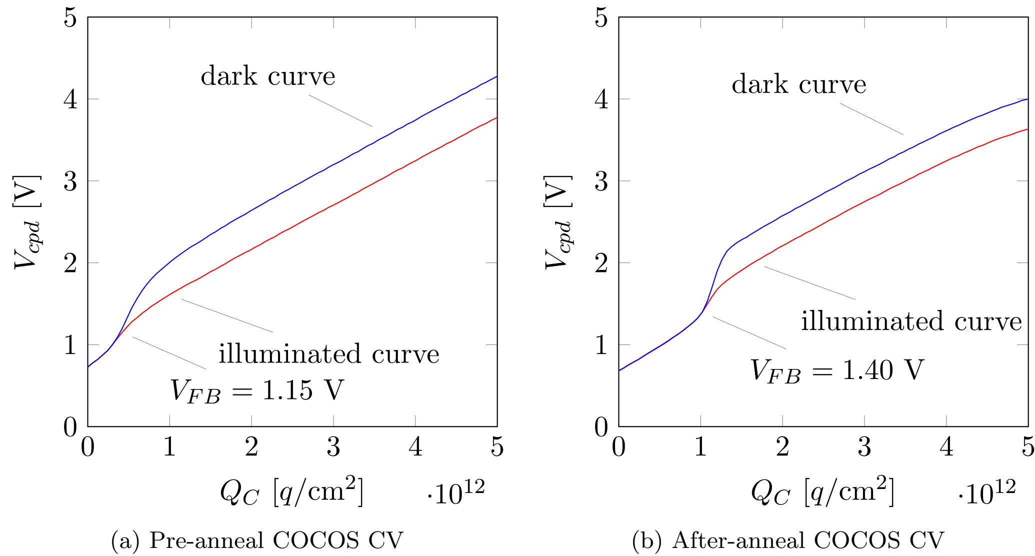
3.3.3 Comparison with COCOS results

The CV and COCOS curves of pre- and after-anneal Al_2O_3 samples are compared in figures 3.27 and 3.28. Contact CV for both samples was measured with delay times of 0.1, 1 and 10 seconds. Even the highest delay time of 10 was insufficient for reaching a true low-frequency curve so all of the curves are useless for extracting D_{it} from depletion to inversion.



(a) Pre-anneal CV (b) After-anneal CV

Figure 3.27: Measured Al_2O_3-Si CV before and after annealing. The 0.1 V increase of V_{FB} after anneal, which is indicated by the shift of the ideal curve, is mostly due to increased oxide charge. Lowered depletion capacitance indicates D_{it} decrease.

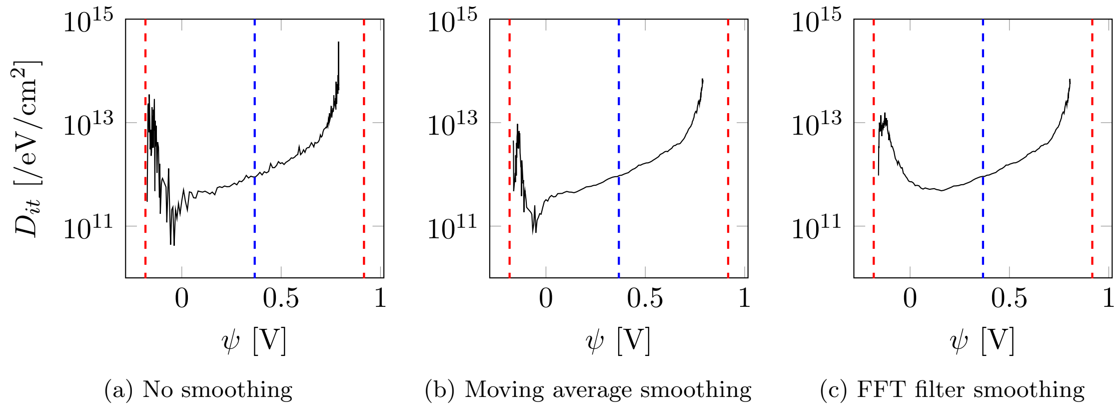


(a) Pre-anneal COCOS CV (b) After-anneal COCOS CV

Figure 3.28: COCOS measured Al_2O_3-Si CV before and after annealing. The increase of V_{FB} due to increased oxide charge is 0.25 V.

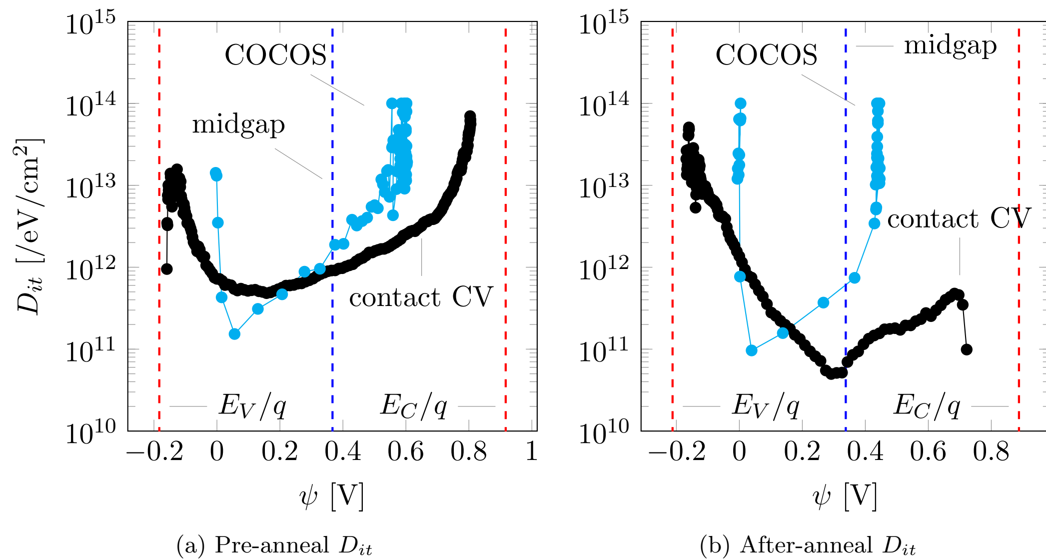
For the purpose of demonstrating the effects of different curve smoothing methods the delay: 10 curves, which have the highest noise levels, were chosen for parameter extraction. Ideal curve fitting was used for V_{FB} extraction with both samples. High noise of the curves prevented the use of second derivative V_{FB} method of equation 2.45 for cross-checking. The contact CV and COCOS curves both show an increase of V_{FB} after the anneal, signifying the increase of negative oxide charge caused by the anneal. Part of the oxide charge increase in table 3.3 is accredited to the lower contact potential of the annealed sample since a lower doping density substrate was used.

Effects of moving average smoothing and fast FFT filter smoothing on the D_{it} curve of the before-anneal sample using the high-noise delay: 10 curve are illustrated in figure 3.29. Comparison between D_{it} from FFT smoothed contact CV curves and COCOS measurements is presented in figure 3.30.



(a) No smoothing (b) Moving average smoothing (c) FFT filter smoothing

Figure 3.29: D_{it} curves of the before-anneal sample displaying the effects of curve smoothing. Dashed red lines are E_V/q and E_C/q, dashed blue line is midgap.



(a) Pre-anneal D_{it} (b) After-anneal D_{it}

Figure 3.30: Contact CV and COCOS measured D_{it} before and after annealing.

The delay: 10 curve in figure 3.27a does not reach full inversion capacitance and is therefore not a true low-frequency equilibrium curve. As a consequence, the D_{it} curves in figures 3.29 and 3.30a are not reliable for band bending values between 0.5 V and E_C/q at 0.917 V. Same applies for the contact CV curve in figure 3.27b, resulting in the D_{it} values contact of the CV curve in figure 3.30b from $\psi = 0.5$ to E_C/q at 0.888 V being false. Both curves display the expected U-shaped D_{it}. Minimum and maximum values of D_{it} for both samples, as well as the midgap values for pre-anneal sample are in good agreement, however the after-anneal sample D_{it} at midgap shows a difference of an order of magnitude.

Contact CV has a larger range in the ψ-axis and higher data point density, especially at the midgap, which is the area of greatest interest. In addition, a characteristic feature of the COCOS D_{it} curve is that there are no data points between flat band $\psi = 0$ and the majority carrier band, which in this case is the valence band at $\psi = -0.183$ V for pre-anneal and at $\psi = -0.212$ V for after-anneal samples. This limitation arises from the fact that the dark and illuminated curves do not diverge from each other before the flat band point and all the parameters are extracted from the differences between the two curves. The E_V, E_C and midgap differences are due to differing doping densities between the two samples.

Both methods are in agreement that the anneal reduced D_{it} in the sample, as is expected. Both methods also indicate an increase of oxide charge after the anneal.

Chapter 4

Conclusion

Nine different samples were measured with dielectric thicknesses ranging from 22nm to 36nm and doping densities from $8{\cdot}10^{14}/\text{cm}^3$ to $1.5{\cdot}10^{16}/\text{cm}^3$. Low-frequency contact CV was emphasized over high-frequency CV, COCOS measurements were used as a reference.

Surface state densities from $6.0{\cdot}10^{10}/\text{eV}/\text{cm}^2$ to $1.9{\cdot}10^{12}/\text{eV}/\text{cm}^2$ were detected, mostly in accordance with results from COCOS measurements. Low-frequency contact CV can theoretically provide surface state density over most of the bandgap, which would provide an advantage over the Semilabs PV2000 used for COCOS measurements. However, for accurate parameter extraction the measured CV curves should be of flawless quality, which tends to increase the amount of measurements needed, causing a steep increase in time consumption of the measurement process. For most samples surface D_{it} was calculated only at midgap, which is in the deepest part of depletion region in the CV curve. The Berglund integral used in the process of calculating D_{it} over a larger energy range is fairly resistant to the effect of noise in the curves, since it is an integration operation. However, the effects of noise and aberrations in the shape of the CV curve are accentuated near accumulaton and inversion regions for D_{it} calculations. The most useful and accurate region for most of the measured samples was therefore the same as with the PV2000.

Another possible benefit of contact CV over COCOS measurements is due to the persistence of the corona charge. If several measurements need to performed repeatedly over time from the same location on the sample, the corona charge, which has proven to be difficult to remove, will affect negatively all measurements following the first measurement. Contact CV has no such limitations. However, contact with probe needles must be established carefully to prevent extensive scratching of the evaporated gate, which can cause the gate area to diminish over time. This effect can be observed as the decrease of maximum capacitance C_{ox} in the curve as the gate area diminishes. Repeated measurements can be useful for exposing and studying hysteresis effects in samples, caused by mobile charge in the dielectric or aging processes in the sample over a long period of time.

The greatest shortcoming of low-frequency CV is its vulnerability to leaks in the dielectric. The COCOS method, which is also based on charge measurement, is not as greatly affected. This is due to corona ion neutralization currents being smaller than tunneling currents over the dielectric in contact CV as reported by Edelman et al. [33]. Leakage correction of the feedback charge method used by the Keithley 595 in low-frequency CV measurements did not prove effective in practice. Good quality curves repeatedly suffered from increased

noise when leakage correction was enabled and poor quality curves were not improved to a useful degree. Use of the leakage correction is therefore not recommended.

In addition to the better performance with leaking dielectrics, the COCOS significantly reduces the time used on sample preparation and measurement. Gate evaporation requires an average of 4 hours, mostly due to the time needed to achieve low enough pressures in the evaporator vacuum chamber. Measuring a low-frequency equilibrium state curve from a slow sample with high data point density and delay time can also take up to an hour of time. High-frequency curves could usually be obtained much faster, usually in less than three minutes.

Impedance-based high-frequency contact CV was given a minor role in this study. While it performed better than low-frequency CV with high leakage samples the curve quality still suffered enough to prevent reliable extraction of sample parameters from the CV data. Another advantage of high-frequency CV over low-frequency CV is the possibility to extract doping density by using the maximum-minimum method, which requires a CV curve that is a "true" high frequency curve at least in the midgap region. Overall, the usefulness of the high-frequency CV could be improved if "true" high frequency curves could be consistently obtained, with all surface state capacitance completely eliminated over the entire curve, not just the midgap. The fastest surface states, which reside closer to conduction and valence bands are still able to respond at 1 MHz frequencies and increasing the measurement frequency beyond 1 MHz caused a significant degradation in curve quality with the HP4192 and probe station setup used in this study. However, since for most of the samples the interface state density was measured only at midgap where the surface state response is slowest [6], the 1 Mhz frequency is sufficient.

A possible source of error stems from the realization that the effective permittivites of dielectrics for most samples were approximately 80% of their reported bulk values. If this indeed is characteristic behavior for dielectric layers that are thinned down to tens of nanometers the dielectric thicknesses measured by ellipsometry could also be affected, since the measurement requires the user to provide a permittivity value for the sample layer. It is also possible that the oxide thickness reference values provided by ellipsometry were incorrect. As a consequence, trying to fit the other parameters into the faulty thickness values caused the deviation from bulk permittivity values in literature.

The two most significant sources of inaccuracy and primary candidates for future improvements in the measurements were the gate area measurements and curve smoothing, assuming the cabling and connections cannot be easily improved. Inaccuracies in gate diameters were 10 μm - 20 μm which is up to 10% of the total gate diameter and translates to a 20% error in gate area and oxide capacitance. The negative effects of this inaccuracy are further magnified by the fact that oxide capacitance acts as a reference point for most of the calculations. Low-noise curves are required for accurately measuring D_{it} values below $10^{11}/\text{eV}/\text{cm}^2$ and for the calculation of flat band voltage using the second derivative method. Effective curve smoothing and noise filtering methods could greatly benefit the measurement system. The moving average and fast Fourier filtering methods, which were used for curve smoothing proved inadequate in many situations. Unless feasible modifications to cabling and connections of the probe station do not provide an improvement, exploring different curve smoothing and noise removal methods on the data could provide higher quality D_{it} and V_{FB} results.

Bibliography

[1] Lee Stauffer. C-V Measurement Tips, Tricks and Traps. Technical report, Keithley Instruments, Inc., 2008.

[2] Gerhard Klimeck. ECE 606 Lecture 21: MOS Electrostatics. *http://nanohub.org/resources/15976*, 2012.

[3] Hans Lüth. *Solid Surfaces, Interfaces and Thin Films.* Springer, 2010.

[4] Chenming Calvin Hu. *Modern Semiconductor Devices for Integrated Circuits.* Pearson, 2010.

[5] Juha Sinkkonen. *Puolijohdeteknologian perusteet.* Helsinki University of Techology, Electron Physics Laboratory, 1996.

[6] E. H. Nicollian and J. R. Brews. *MOS (Metal Oxide Semiconductor) Physics and technology.* Wiley, 1982.

[7] Dieter K. Schroder. *Semiconductor Material and Device Charachterization.* Wiley, 2006.

[8] David A. Deen and James G. Champlain. High frequency capacitance-voltage technique for the extraction of interface trap density of the heterojunction capacitor: Terman's method revised. *AIP Applied Physics Letters*, 2011.

[9] R. J. Hillard, J. M. Heddleson, D. A. Zier, P. Rai-Choudhury, and D. K. Schroder. Direct and rapid method for determining flatband voltage from from non-equilibrium capacitance voltage data. *Journal of the Electrochemical Society*, 1992.

[10] Robert F. Pierret. *Field Effect Devices.* Addison-Wesley, 1990.

[11] R. Lindner. Semiconductor surface varactor. *The Bell System Technical Journal*, 1962.

[12] J. R. Brews. A simplified high-frequency mos capacitance formula. *Solid-State Electronics*, 1977.

[13] A. Goetzberger. Ideal mos curves for silicon. *Bell System Technical Journal*, 1966.

[14] J. R. Brews. Correcting interface-state errors in mos doping profile determinations. *AIP Journal of Applied Physics*, 1973.

[15] Yasuhito Zohta. Frequency dependence of $\Delta V/\Delta(C^{-2})$ of MOS capacitors. *Solid-State Electronics*, 1974.

[16] W. van Gelder and E. H. Nicollian. Silicon impurity distribution as revealed by pulsed mos cv measurements. *Journal of the Electrochemical Society*, 1971.

[17] L. M. Terman. An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes. *Solid-State Electronics*, 1962.

[18] C. N. Berglund. Surface states at steam-grown silicon-silicon dioxide interfaces. *Electron Devices, IEEE transactions on*, 1966.

[19] R. Castagné and A. Vapaille. Description of the SiO_2Si interface properties by means of very low frequency MOS capacitance measurements. *Surface Science*, 1971.

[20] Peter V. Gray and Dale M. Brown. Density of SiO_2-Si interface states. *AIP Applied Physics Letters*, 1966.

[21] D. Schuldis, A. Richter, J. Benick, P. Saint-Cast, M. Hermie, and S. W. Glunz. Properties of the c-Si/Al_2O_3 interface of ultrathin atomic layer deposited Al_2O_3 layers capped by SiN_x for c-si surface passivation. *AIP Applied Physics Letters*, 2014.

[22] M. Kuhn. A quasi-static technique for MOS C-V and surface state measurements. *Solid-State Electronics*, 1970.

[23] R. Castagné. Density of slow states with an insulator-semiconductor-metal capacity determined by charges under linearly growing pressure. *Comptes rendus hebromadaires des séances de l'Académie des sciences*, 1968.

[24] D. R. Kerr. MIS measurement techniques utilizing slow voltage ramps. In *Conference on properties and use of MIS structures, Grenoble, France*, 1966.

[25] Thomas J. Mego. Improved feedback charge method for quasistatic CV measurements in semiconductors. *Review of Scientific Instruments*, 1986.

[26] K. Ziegler and E. Klausmann. Static technique for precise measurements of surface potential and interface state density in MOS structures. *AIP Applied Physics Letters*, 1975.

[27] J. R. Brews and E. H. Nicollian. Improved MOS capacitor measurements using the Q-C method. *Solid-State Electronics*, 1984.

[28] W. Markgraf, M. Baumann, P. Arzt, A. Beyer, and M. Rennau. Einbeziehung der statischen CU-Messung in die Prozessmesstechnik im Zyklus 1. *Wissenschaftliche Zeitschrift der Technischen Hochschule Karl-Marx-Stadt*, 1984.

[29] Dieter K. Schroder. Contactless surface charge semiconductor characterization. *Materials Science and Engineering: B*, 2002.

[30] P. Edelman, A. M. Hoff, L. Jastrzebski, and J. J. Lagowski. New approach to measuring oxide charge and mobile ion concentration. *Microelectronic Manufacturing*, 1994.

[31] M. Wilson, J. Lagowski, L. Jastrzebski, A. Savtchouk, and V. Faifer. COCOS (corona oxide characterization of semiconductor) non-contact metrology for gate dielectrics. *Characterization and metrology for ULSI technology 2000*, 2001.

[32] M. Dautrich, P. M. Lenahan, and A. Y. Kang. Non-invasive nature of corona charging on thermal Si/SiO_2 structures. *Integrated Reliability Workshop Final Report, 2003 IEEE International*, 2003.

[33] P. Edelman, J. Lagowski, A. Savtchouk, M. Wilson, A. Aleynikov, D. Marinskiy, and Joaquin Navarro. Full wafer non-contact mapping of electrical properties of ultra-thin advanced dielectrics on Si. *Materials Science and Engineering: B*, 2002.

[34] J. Robertson. High dielectric constant oxides. *The European Physical Journal of Applied Physics*, 2004.

[35] H. Wong, N. Zhan, K.L. Ng, M.C. Poon, and C.W. Kok. Interface and oxide traps in high-κ hafnium oxide films. *Thin Solid films*, 2004.

[36] L. Pereira, P. Barquinha, E. Fortunato, and R. Martins. Low temperature processed hafnium oxide: Structural and electrical properties. *Materials science in semiconductor processing*, 2006.

Appendix A

Theoretical CV curve (MATLAB)

```
%Theoretical CV curve of ideal MOS
format long;

%                            Voltage sweep
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

V_G = -3:0.01:3; %[V] gate voltage sweep range and datapoint density


%                          Natural constants
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

T = 300; %[K]
k = 1.3806488E-23; %[m^2*kg/s^2/K]
q = 1.6217657E-19; %[C]
e_0 = 8.854187817E-12; %[F/m] vacuum permittivity
e_rSi = 11.7; %silicon relative relative permittivity
e_rSiO = 3.9; %silicon dioxide relative permittivity
e_Si = e_0 * e_rSi;
e_SiO = e_0 * e_rSiO;
n_i = 8.72E15; %[1/m^3] silicon intrinsic carrier density at 300K


%                        Material parameters
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Ntype = 0; %doping type, 0=p-type, 1=n-type
N = 1E21; %[1/m^3] donor/acceptor density

A = 1E-8; %[m^2] gate area
t = 100E-9 ; %[m] oxide thickness

C_ox = e_SiO*A/t; %[F] calculated oxide capacitance for given gate area
%OR
%C_ox = ; %directly measured oxide capacitance

lambda_i = sqrt((e_Si*k*T) / (2*q^2*n_i)); %[m] intrinsic Debye length
lambda_N = sqrt((e_Si*k*T) / (q^2*N)); %[m] extrinsic Debye length
C_FBS = e_Si/lambda_N; %[F/m^2] Flatband capacitance
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

iter = length(V_G);
BB = zeros(1,iter); %empty vector for band bending
C_SLF = zeros(1,iter); %empty vector for semiconductor lf capacitance
C_L = zeros(1,iter); %empty vector for hf Lindner approximation


if (Ntype == 0)
    u_B = log(n_i/N); %normalized bulk potential for p-type substrate
else
    u_B = log(N/n_i); %normalized bulk potential for n-type substrate
end

%sweep for solving band bending "v" as a function of gate voltage "V_G"
options = optimoptions('fsolve','Display','off');
for i=1:iter
    BB(i) = fsolve((@(v) V_G(i) -k*T/q*v +(A/C_ox)*(e_Si*k*T)/...
    (q*lambda_i)*sign(-v) *sqrt( 2*((-v)*sinh(u_B)-cosh(u_B)+...
    cosh(v+u_B) ))),0,'options');
end

%sweep for solving semiconductor low-frequency capacitance A[m]*[F/m^2]
%as a function of "V_G"
for i=1:iter
    if BB(i) == 0
        C_SLF(i) = A*C_FBS;
    else
        C_SLF(i) = A*(sign(BB(i)) *e_Si/lambda_i *...
        (sinh(BB(i)+u_B)-sinh(u_B)) /...
        sqrt(2*((-BB(i))*sinh(u_B)-cosh(u_B)+cosh(BB(i)+u_B)) ) );
    end
end

%total lf capacitance
C_LF = ( 1/C_ox + 1./(C_SLF) ).^-1;
C_norm_LF = C_LF./C_ox;


%HF capacitance
if (Ntype == 0) %p-type
    vm = (2.10*abs(u_B) + 1.33);
    C_Lvm = A/sqrt(2)*sign(vm)*C_FBS*(1-exp(-vm))/sqrt(vm-1+exp(-vm));
    for i=1:iter
        if BB(i) == 0
            C_L(i) = A*C_FBS;
        else
            C_L(i) = A/sqrt(2)*sign(BB(i))*C_FBS*...
            (1-exp(-BB(i)))/sqrt(BB(i)-1+exp(-BB(i)));
        end
    end
    C_SDD = C_L;
    C_SHF = (BB<=vm).*C_L + (BB>vm)*C_Lvm;
else %n-type
    vm = -(2.10*abs(u_B) + 1.33);
    C_Lvm = A/sqrt(2)*sign(vm)*C_FBS*(-1+exp(vm))/sqrt(-vm+1+exp(vm));
    for i=1:iter
        if BB(i) == 0
            C_L(i) = A*C_FBS;
```

```
        else
            C_L(i) = A/sqrt(2)*sign(BB(i))*C_FBS*...
            (-1+exp(BB(i)))/sqrt(-BB(i)-1+exp(BB(i)));
        end
    end
    C_SDD = C_L;
    C_SHF = (BB>=vm).*C_L + (BB<vm)*C_Lvm;
end



%total hf capacitance
C_HF = ( 1/C_ox + 1./(C_SHF) ).^-1;
C_norm_HF = C_HF./C_ox;

%total deep depletion capacitance
C_DD = ( 1/C_ox + 1./(C_SDD) ).^-1;
C_norm_DD = C_DD./C_ox;

%Plotting
figure;
subplot(3,1,1);
hold on;
plot(V_G,C_DD,'m');
plot(V_G,C_LF,'b');
plot(V_G,C_HF,'r');
xlabel('V_G [V]');
ylabel('C [F]');
title('Capacitance');

subplot(3,1,2);
hold on;
plot(V_G,C_norm_DD,'m');
plot(V_G,C_norm_LF,'b');
plot(V_G,C_norm_HF,'r');
axis([min(V_G) max(V_G) -0.1 1.1]);
xlabel('V_G [V]');
ylabel('C [C/C_{ox}]');
title('Normalized capacitance');
subplot(3,1,3);
plot(V_G,(BB*k*T/q));
title('Band bending');
xlabel('V_G [V]');
ylabel('\psi [V]');
```

Appendix B

Berglund integral (MATLAB)

```
%Berglund integral

%Requires parameters from theoretical curve
%Run theoretical curve code first
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
format long;

biasV = V_data; %[V] measured bias voltage V_G vector
cap = C_data; %[F] measured capacitance vector
oxcap = C_data_max; %[F] measured oxide capacitance
startbias = -2; %[V] starting bias
endbias = 2; %[V] ending bias
flatband = V_data_FB; %[V] flat band voltage

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

normcap = cap./oxcap;
width = biasV(2)-biasV(1);
[idx startpoint] = min(abs(biasV-startbias));
[idx endpoint] = min(abs(biasV-endbias));
[idx zeropoint] = min(abs(biasV-flatband));
bandbending = zeros(1,(abs(startpoint-endpoint))); %[V]
idx = 1;

if startpoint <= endpoint
    for i=startpoint:1:endpoint
        bandbending(idx) = (1-normcap(i))*width;
        idx = idx+1;
    end
end

if startpoint > endpoint
    for i=startpoint:-1:endpoint
        bandbending(idx) = (1-normcap(i))*width;
        idx = idx+1;
    end
end

idx = length(bandbending)+1;
totalbendingtemp = zeros(1,idx);
```

```
totalbending = zeros(1,idx-1);
for i=2:idx
    totalbendingtemp(i) = sum(bandbending(1:(i)-1));
end
for i=1:(idx-1)
    totalbending(i) = (totalbendingtemp(i)+totalbendingtemp(i+1))/2;
end
totalbending = totalbending - totalbending(1+zeropoint-startpoint);
totalbendingnorm = totalbending*q/k/T;

iter = length(totalbendingnorm);
for i=1:iter
    if totalbending(i) == 0
        C_Sberglund(i) = A*C_FBS;
    else
        C_Sberglund(i) = A*(sign(totalbendingnorm(i)) *e_Si/lambda_i *...
        (sinh(totalbendingnorm(i)+u_B)-sinh(u_B)) /...
        sqrt(2*((-totalbendingnorm(i))*sinh(u_B)-cosh(u_B)+...
        cosh(totalbendingnorm(i)+u_B)) ) );
    end
end

Cit = ((1./cap(startpoint:endpoint) - 1/oxcap).^(-1) - C_Sberglund')/...
A/q/1E4;

figure;
hold on;
semilogy((totalbending),Cit,'*k');
title('Interface state density');
ylabel('D_i_t [/eV/cm^2]');
xlabel('\psi [V]');
```

Appendix C

Curve smoothing (MATLAB)

```
%CV curve smoothing

%%%%%%%%%%%% Moving average smoothing %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
volt = V_data; %original capacitance vector
cap = C_data; %original capacitance vector
winsize = 5; %averaging window size, use odd numbers, min=3

winreach = (winsize-1)/2;
iter = length(volt); %original datavector length
capsmoothed = zeros((iter-winsize+1),1); %smoothed capacitance vector
voltsmoothed = volt((winreach+1):(iter-winreach)); %smoothed voltage vector
for i=(winreach+1):(iter-winreach)
    capsmoothed(i-winreach) = sum(cap((i-winreach):(i+winreach)))/winsize;
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%



%%%%%%%%%%%% FFT smoothing %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
fftC = fftfilt(ones(winsize,1)/winsize,(AC10_sub_ai+1E-11));
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

Appendix D

V_G Second derivative (MATLAB)

```
% V_G second derivative for calculating V_FB
iter = length(V_data);
CC = (max(C_data)./C_data).^2;
dCC = zeros(1,(iter-1));
d2CC = zeros(1,(iter-2));
diff = -V_data(2)+V_data(1);

for i=1:(iter-1)
    dCC(i) = CC(i+1)-CC(i);
end
for i=1:(iter-2)
    d2CC(i) = (dCC(i+1)-dCC(i))/diff;
end

figure;
plot(-V_data(2:(iter-1)),d2CC);
title('V_F_B 2nd derivative method');
xlabel('V_G [V]');
d2matriisi1 = [(-V_data(2:(iter-1))) (d2CC)'];
```