Aalto University
School of Electrical Engineering
Degree Programme in Micro- and Nanotechnology

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Monolithic Transformers for RF Electronics

Master's Thesis
Espoo, July 5, 2014

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ABSTRACT OF
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In this thesis transformers for RF integrated circuits are investigated. Monolithic transformers are widely used in various RF and high frequency circuits. For instance, transformers are used as power combiners in power amplifiers, in small signal amplifiers they are used for advanced feedback arrangements, they enable integrated filter implementation, they are used as baluns and impedance matching networks, and they can be used as resonators in oscillators.

Unfortunately foundry supported models for on-chip transformers are rarely available and circuit designers need to design and characterize their own transformers using electro magnetic (EM) field simulator. This is a time consuming and laborious task, yet rigorous optimization of transformer characteristics results in significant improvements. Therefore one of the aims of this thesis was to develop an automated EM simulator environment.

The thesis starts with representation of transformer basics and then different types of structures for such devices are introduced and discussed. One structure called "Interleaved Transformer" is chosen to be the basis of the design for its good magnetic coupling, symmetry, high frequency range and need of only two layers. More than 50 samples of these devices are designed and characterized. This is done with the help of an automated layout drawing program that was developed in this thesis. Afterwards, they are compared to illustrate how changing the dimensions can help us achieve desired properties.

From these comparisons we have generated guidelines on how to for instance maximize quality factor, band width, or coupling coefficient. Based on these findings we can conclude what dimensional properties are needed for a specific circuit requirement and finally find out how to choose correct transformer dimensions for given applications.

Keywords:	monolithic transformers, on-chip transformers, on-chip inductors, electro magnetic field simulation
Language:	English

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Saman Bahrampoor

Contents

Abbreviations and Symbols

Symbols

λ	Flux linkage
μ	Permeability, Micron
μ_0	Permeability of free space
ϕ	Magnetic flux
Ω	Ohms
ω	Angular Frequency ($2\pi \times f$)
ω_Z	Zero frequency
ω_P	Pole frequency
$\mathbf{a}_\phi$	Basis vector in spherical and cylindrical coordinate systems
$\mathbf{B}$	Magnetic field (vector)
C	Capacitance, Closed loop
Cu	Copper
dB	Decibel
D_{in}	Inner opening diameter
H	Henry
K	Coupling coefficient
L	Inductance
M	Mutual inductance
N_P	Number of turns in primary
N_S	Number of turns in secondary
Poly-Si	Polycrystalline silicon
Q	Quality factor
R	Resistance, Magnetic reluctance
S	Siemens, Surface area
s	Laplace domain variable,
Si	Silicon
SiO_2	Silicon dioxide
W	Width
Z	Impedance

Abbreviations

AC	Alternating current
ADS	Advanced Design System
AEL	Application Extension Language
BW	Bandwidth
CMOS	Complementary metal-oxide-semiconductor

EM	Electro-magnetic
FDD	Frequency-division duplexing
GSM	Global system for mobile communications
IC	Integrated circuit
imag()	Imaginary part of a number
LNA	Low noise amplifier
LNTA	Low noise transconductance amplifier
MIMO	Multiple-input and multiple-output
mmf	magneto motive force
NT	Number of turns
PA	Power amplifier
RBW	Relative bandwidth
real()	Real part of a number
RF	Radio frequency
SoC	System on a chip
TDD	Time-division duplexing
UMTS	Universal mobile telecommunications system
VCO	Voltage controlled oscillator
WiFi	Local area wireless technology
WLAN	Wireless local area network

Chapter 1

Introduction

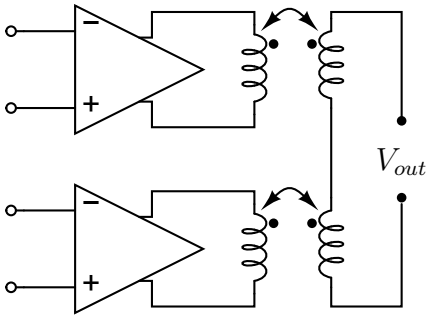
Transformers are commonly utilised in various RF circuits. They can be used in VCOs to cross-couple the active components,, they are used in amplifiers' resonance segments, they can be used as power combiner from separate amplifiers, and they are perfect devices as baluns for matching a balanced to an unbalanced network. For example, Kumar et al. [1] have used transformers and baluns in various sections of their MIMO WLAN SoC.

In [2] a receiver front-end has been made using a transformer-based current gain booster. In [3] a low power radio chipset has been introduced which uses transformer-based power amplifiers. Fabiano et al. [4] have transformer-based structures for the LNTAs in both GSM and UMTS segments in their front-end receivers for TDD and FDD applications (Figure 1.1(b)).

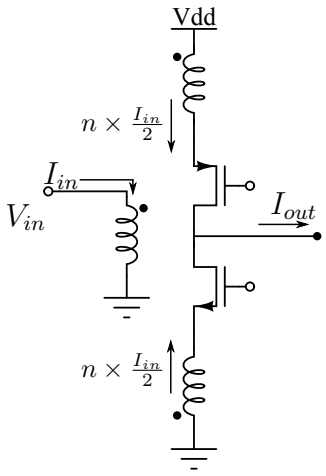
The design of the dual mode PA of [5] combines the signal of two similar PA units at the output, hence requiring transistors with 50% reduction in size. The designs of [6], [7], [8] and [9] also use similar techniques for combining signals from different individual PAs (Figure 1.1(a)).

In [10], authors have used on-chip transformers to make a 100GHz varactor-less VCO which can be used in numerous millimetre wave frequency communication applications. Multiple on-chip transformers are being used in VCO/modulator segment of Wang's differential transceiver [11] which allows for a compact layout. Another transformer-based VCO is that of [12] (Figure 1.1(c)). They have used the reflection of equivalent inductances through on-chip transformers to achieve a great result for the tuning range of the VCO.

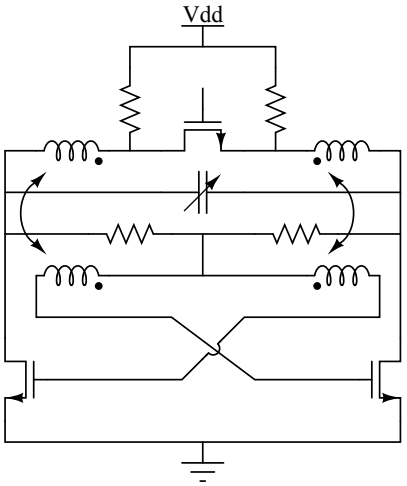
Transceiver of [13] by Brown et al. uses a custom transformer-coupling in the transmitter module to boost the signal swing delivered to the antenna. Authors of [14] have reduced the headroom requirements of their circuit in both the LNA and the VCO segments by magnetic coupling through transformers. Authors of [15] have also used on-chip transformers to tune their



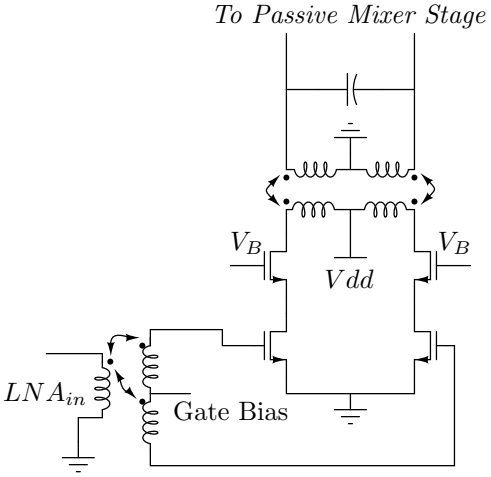
(a) Power combining from two amplifiers using transformers



(b) Single-ended LNTA structure by Fabiano et al.[4]



(c) Schematic diagram of VCO used by Mammei et al.[12]



(d) Simplified schematic diagram of the on-chip transformer and the LNA[19]

Figure 1.1: Common applications of on-chip transformers.

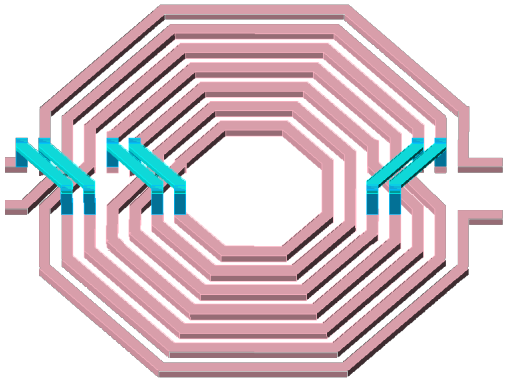


Figure 1.2: An image of a sample transformer of this thesis upside-down to demonstrate both layers, with 4:3 ratio and with exaggerated thickness in both layers for visualization

CMOS quadrature VCO for millimetre wave oscillation frequencies. The VCOs of [16], [17] and [18] also use transformers in various setups. Another common usage of on-chip transformers is impedance matching. Such design technique is adopted by Borna et al. in [19] (Figure 1.1(d)).

In energy harvesting circuit proposed by Im et al. in [20], a transformer is used to boost the self-startup signal and then it is re-used as an inductor. Other possible uses for on-chip transformers are isolated signal transfer[21] and filter integration[22].

As we see so far, there are many cases where a magnetic coupling via on-chip transformers helps the efficiency of certain circuits. But, foundry supported monolithic on-chip transformer models are not available for circuit designers and they need to make their own transformer models and this can be a very time consuming process.

Furthermore, in a CMOS process, there are limitations, such as the thickness of metallizations and available die area, which together with physical limitations (insulator's limited resistance, capacitance between to metal lines, limited magnetic coupling, etc.) and losses in transformers do not allow for a perfect and ideal device. These losses could be because of limited conductivity of the metallizations which increases in higher frequencies as the effective conducting area of the wire reduces due to skin effect.

So, a real transformer will exhibit some signal power loss and limited bandwidth. Circuit designers need to know these limitations and characteristics in any single transformer they use and examine if it complies with the specific demands of their circuits. In order to obtain these specifications, transformers are modelled and then examined in electro-magnetic simulators.

In this thesis, we first investigate the basic physics of magnetic induction.

Then, the operation of transformers by magnetic coupling is discussed and we see why transformers cannot be ideal and posses only limited bandwidth. Next, the EM simulators and simulation methods are introduced. In Chapter 4 the characteristics of transformers generated in this thesis will be compared (one such transformer is illustrated in Figure 1.2) to see the effect of the dimensional properties of transformers on their operation.

In Chapter 5 we re-examine the outcomes of the simulations in Chapter 4 and try to figure out what are the correct dimensions to design and make good transformers for specific needs. For instance, a device designed to be used in a high frequency LNA might not be suitable for a circuit where it is going to be used as a balun. Finally, in Chapter 6 the entire thesis is concluded and we briefly review what has been done.

Chapter 2

Basics of Transformers

2.1 Induction

From the basic physics we know, electricity and magnetism are the same force and one can generate the other. In case we have two closed loops, C_1 and C_2 with respective surface areas of S_1 and S_2, close enough to make considerable magnetic effect on one another (Figure 2.1), if a current I_1 flows through C_1, a magnetic field $\mathbf{B_1}$ will be created which will pass through the surface bounded by C_2.

In such a case, the "mutual flux" ϕ_{12} (with SI unit Weber) could be calculated as:

$$\phi_{12} = \int_{S_2} \mathbf{B_1} dS_2 \tag{2.1}$$

From Faraday's law of electromagnetic induction we know a time dependent current I_1 in C_1 and thus a time-varying ϕ_{12} will induce an electromotive force into C_2, although ϕ_{12} is there even with a DC current for I_1.

Also, Biot-Savart law tells us B_1 is directly related to I_1 and therefore

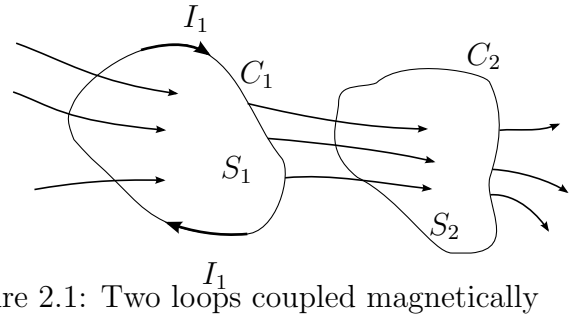


Figure 2.1: Two loops coupled magnetically

ϕ_{12} is also proportional to I_1. So,

$$\phi_{12} = L_{12} I_1 \tag{2.2}$$

Where the mutual inductance of C_1 and C_2, L_{12}, is a constant (with SI unit Henry, abbreviated as H).

If C_2 has N_2 turns, the collective effect of those turns would accumulate to make "flux linkage λ_{12}" which is:

$$\lambda_{12} = N_2 \phi_{12} \tag{2.3}$$

and equation 2.2 will be changed into:

$$\lambda_{12} = L_{12} I_1 \tag{2.4}$$

Or,

$$L_{12} = \frac{\lambda_{12}}{I_1} \tag{2.5}$$

Which means the mutual inductance of two closed loops is in fact the flux linkage of one on the other, per unit current. For a non-linear medium the equation above is changed into:

$$L_{12} = \frac{d\lambda_{12}}{dI_1} \tag{2.6}$$

But a portion of the flux generated by I_1 is only linked with C_1 itself. So,

$$\lambda_{11} = N_1 \phi_{11} \tag{2.7}$$

and

$$L_1 = \frac{\lambda_{11}}{I_1} \tag{2.8}$$

Where $L_1$is the self inductance of loop C_1.

While working with on-chip components, there would be lots of cases in which the mutual inductance of two parallel metalization lines is significant. This is even more so in case of RF transformers. We can calculate the per unit length mutual inductance of such parallel conductors. In Figure 2.2, first we need to find the flux density $\mathbf{B}$ caused by the current in M_1:

$$\mathbf{B} = \mathbf{a}_\phi B_\phi \quad and \quad dl = \mathbf{a}_\phi r d\phi \tag{2.9}$$

$$\oint_C 2B.dl = 2\pi r B_\phi \Rightarrow \mathbf{B} = \mathbf{a}_\phi B_\phi = \mathbf{a}_\phi \frac{\mu_0 I}{2\pi r} \tag{2.10}$$

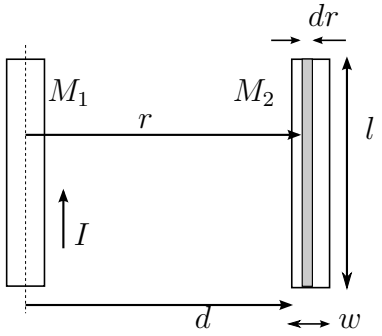


Figure 2.2: Two parallel metalization lines

$$\phi = \int_S B.d\mathbf{s} = \int_d^{d+w} ldr = \frac{\mu_0 Il}{2\phi} \ln \frac{d+w}{w} \tag{2.11}$$

The mutual inductance is then found to be:

$$L_{12} = \frac{\phi}{I} = \frac{\mu_0 l}{2\pi} \ln \frac{d+w}{d} \quad (H) \tag{2.12}$$

And mutual inductance per unit length is:

$$\acute{L} = \frac{L_{12}}{l} = \frac{\mu_0}{2\pi} \ln \frac{d+w}{d} \quad (H/m) \tag{2.13}$$

2.2 How transformers work

2.2.1 Ideal Transformer

A transformer is an AC device used for changing the voltage levels, currents and impedances to match a given network. In low frequency discrete electronics, it is made of at least two coils, named primary and secondary, that share a ferromagnetic core as depicted in the magnetic circuit in Figure 2.3. Considering such a magnetic circuit, Faraday's law of electromagnetic induction gives:

$$N_p \times I_p - N_s \times I_s = R \times \phi \tag{2.14}$$

Where:

- R is magnetic reluctance
- ϕ is magnetic flux
- N_p is the number of turns in primary
- N_s is the number of turns in secondary

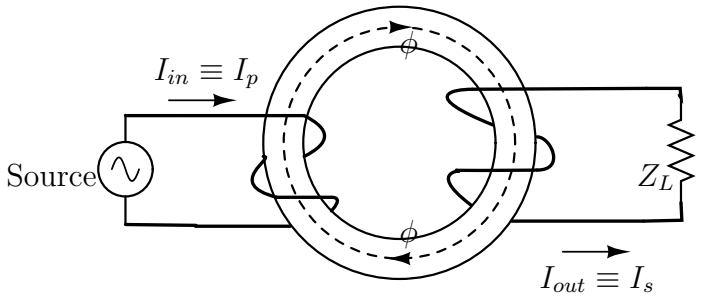


Figure 2.3: A simple Transformer

- I_p is the current in primary
- I_s is the current in secondary
- V_p is the voltage over primary's terminals
- V_s is the voltage over secondary's terminals

According to Lenz law, in Equation 2.14 the induced magneto-motive force (mmf) in secondary would be opposing the ϕ generated by primary's current. If the length of the magnetic circuit is l and its cross section's surface is S, from basic physics of magnetic circuits and reluctance [23] we have:

$$R = \frac{l}{\mu \times S} \tag{2.15}$$

Applying this into Eq. 2.14 gives:

$$N_p I_p - N_s I_s = \frac{l}{\mu \times S} \times \phi \tag{2.16}$$

So:

$$lim_{\mu \to \infty}(N_p I_p - N_s I_s) = 0 \tag{2.17}$$

And thus for magnetic cores with very high magnetic permeability:

$$\frac{N_p}{N_s} = \frac{I_s}{I_p} \tag{2.18}$$

Also from Faraday's Law we have:

$$v_p = N_p \frac{d\phi}{dt} \qquad v_s = \frac{N_s d\phi}{dt} \tag{2.19}$$

$$\frac{V_p}{V_s} = \frac{N_p}{N_s} \tag{2.20}$$

So, the effective load of Z_L at secondary, if seen from primary would look like:

$$Z_{L,eff} = \frac{V_p}{I_p} = \frac{\frac{N_p}{N_s}}{\frac{N_s}{N_p}} \times \frac{V_s}{I_s} = (\frac{N_p}{N_s})^2 \times Z_L \tag{2.21}$$

2.2.2 Lossless Transformer With Inductances

In previous section, the transferring properties of ideal transformers was reviewed. Now, we need to take into account the self and mutual inductances of the two coils. In Equation 2.16 the magnetic flux linkage of two windings is derived:

$$\lambda_1 = N_p\phi = \frac{\mu S}{l}(N_p^2 I_p - N_p N_s I_s) \tag{2.22}$$

$$\lambda_2 = N_s\phi = \frac{\mu S}{l}(N_s N_p I_p - N_s^2 I_s) \tag{2.23}$$

Applying Equation 2.19 into here we get:

$$v_p = L_p\frac{dI_p}{dt} - M\frac{dI_s}{dt} \tag{2.24}$$

$$v_s = M\frac{dI_p}{dt} - L_s\frac{dI_s}{dt} \tag{2.25}$$

Where:

$$L_p = \frac{\mu S}{l}N_p^2 \tag{2.26}$$

$$L_s = \frac{\mu S}{l}N_s^2 \tag{2.27}$$

$$M = \frac{\mu S}{l}N_p N_s \tag{2.28}$$

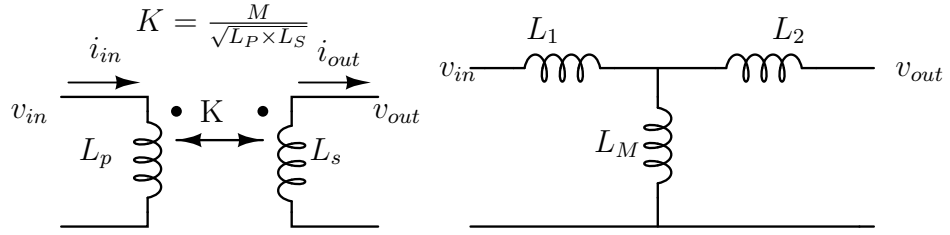
Where M is the mutual inductance between the two windings.

In real transformers, the linkage between the two windings is not perfect and there are leakages. So, a coefficient is defined as the coupling coefficient (k) which describes the correlation between the mutual inductance of two windings and self-inductance of each one of them.

$$M = K\sqrt{L_p L_s} \quad ; \quad 0 < K < 1 \tag{2.29}$$

In case of ideal transformers, there is no leakage flux.

$$K = 1 \Rightarrow M = \sqrt{L_p L_s} \tag{2.30}$$



(a) Circuit model (b) Its T-Network equivalent

Figure 2.4: Non-ideal transformer

It is much easier to calculate impedance transfer of non-ideal transformer in frequency domain rather than in time domain. So, transforming Equations 2.24 and 2.25 into Laplace form:

$$v_p = sL_pI_p - sMI_s \tag{2.31}$$

$$v_s = sMI_p - sL_sI_s \tag{2.32}$$

$$I_sZ_L = sMI_p - sL_sI_s \tag{2.33}$$

$$I_s(Z_L + sL_s) = sMI_p \tag{2.34}$$

$$\frac{I_s}{I_p} = \frac{sM}{sL_s + Z_L} \tag{2.35}$$

$$Z_{in} = \frac{v_p}{I_p} = sL_p - sM\frac{I_s}{I_p} \Rightarrow \tag{2.36}$$

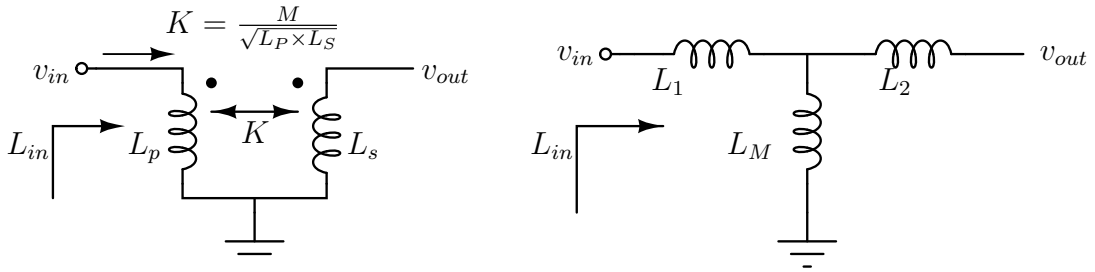
$$Z_{in} = sL_p - \frac{(sM)^2}{sL_s + Z_L} \tag{2.37}$$

2.2.3 Transformer T-network modeling

If a non-ideal transformer at working in low frequencies where parasitic capacitances do not play a significant role, and has negligible Ohmic resistance loss, and thus, is fully inductive, it can be modelled as a two port T-network like Figures 2.4(a) and 2.4(b). In order to define the parameters of the T-model equivalent circuit of such a transformer, we need to find its open-circuit input and output inductances as shown in Figure 2.5 and Figure 2.6 and its input inductance when it has short-circuited output as depicted in Figure 2.7.

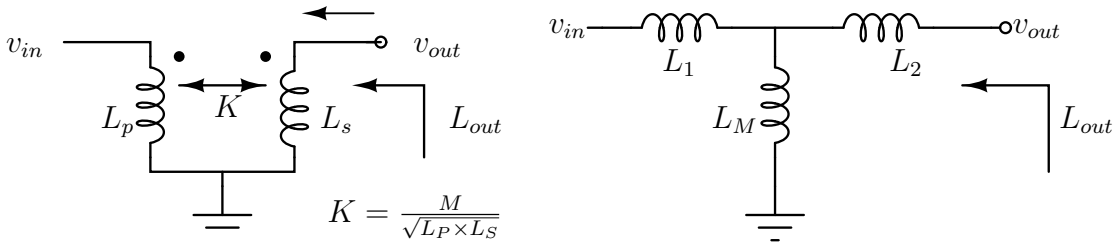
By considering the two circuits equivalent, we get:

$$if : i_{out} = 0 \Rightarrow L_p = L_1 + L_M \Rightarrow L_1 = L_p - L_M \tag{2.38}$$



(a) Transformer (b) T-Network

Figure 2.5: Open-circuit input inductance



(a) Transformer (b) T-Network

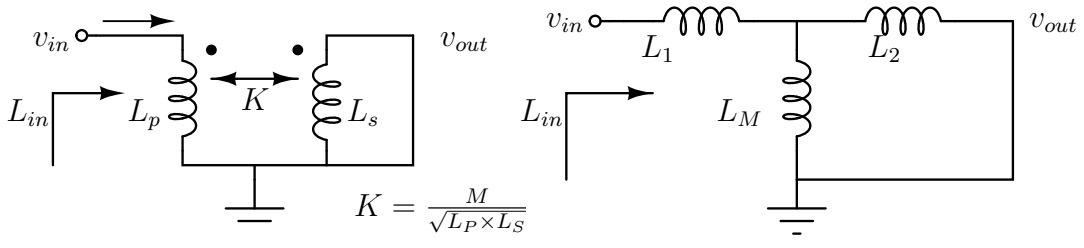
Figure 2.6: Open-circuit output inductance

$$if : i_{in} = 0 \Rightarrow L_s = L_2 + L_M \Rightarrow L_2 = L_s - L_M \tag{2.39}$$

$$if : v_{out} = 0 \Rightarrow M\frac{di_{in}}{dt} - L_s\frac{di_{out}}{dt} = 0 \Rightarrow i_{out} = \frac{M}{L_s}i_{in} \tag{2.40}$$

$$v_{in} = L_1\frac{di_{in}}{dt} - M\frac{di_{out}}{dt} = (\frac{L_p - M^2}{L_s})\frac{di_n}{dt} \Rightarrow \tag{2.41}$$

$$L_{in} = L_p - \frac{M^2}{L_s} \tag{2.42}$$



(a) Transformer (b) T-Network

Figure 2.7: Input inductance, short-circuited output

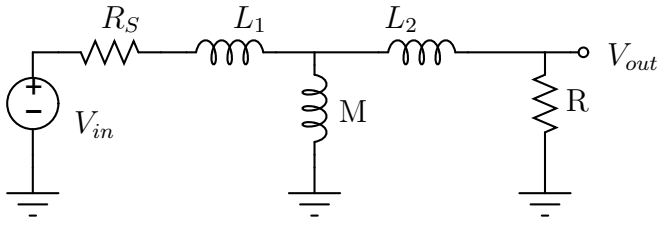


Figure 2.8: Two parallel metalization lines

$$L_{in} = L_1 + (L_M \parallel L_2) = L_1 + \frac{L_M L_2}{L_M + L_2} \tag{2.43}$$

Equations in 2.42 and 2.43 are describing equivalent circuits. So,

$$L_1 + \frac{L_M L_2}{L_M + L_2} = L_p - \frac{M^2}{L_s} \tag{2.44}$$

But we have already calculated the equivalents of L_1 and L_2.

$$L_p - L_M + \frac{L_M(L_s - L_M)}{L_s} = L_p - \frac{M^2}{L_s} \Rightarrow \tag{2.45}$$

$$L_M = M \tag{2.46}$$

2.2.4 Transfer function

Now it is much easier to derive the transfer function and then the bandwidth of the system. We need to include a load and a source resistance to the two-port network as in Figure 2.8.

$$v_{out} = \frac{R}{R + sL_2} \times \frac{\frac{(R + sL_2)sM}{R + s(L_2 + M)}}{sL_1 + R_S + \frac{(R + sL_2)sM}{R + s(L_2 + M)}} \times v_{in} \Rightarrow \tag{2.47}$$

$$H(s) = \frac{v_{out}}{v_{in}} = \frac{sMR}{s^2(L_2M + L_1L_2 + L_1M) + s(MR + MR_SL_1R + L_2RS) + RR_S} \tag{2.48}$$

To make this equation simpler, if we have $R = R_S = 1$ and substitute L_1, L_2, M and K with their equivalents from Equations 2.38 2.39, 2.46 and 2.29, we get:

$$H(s) = \frac{sMR}{s^2(1 - K^2)(L_PL_S) + s(L_S + L_P) + 1} \tag{2.49}$$

Now that we have the transfer function, we can find the filter profile of the transformer and its bandwidth. We can find the only zero of the system easily by having the numerator polynomial of the fraction above to be equal to zero:

$$sMR = 0 \Rightarrow \omega_Z = 0 \tag{2.50}$$

In order to calculate the poles of the system, the denominator must be equal to zero. The denominator polynomial above is in the form of a quadratic equation like:

$$as^2 + bs + c = 0 \tag{2.51}$$

where:

$$a = L_P L_S(1 - K^2) \qquad b = L_p + L_S \qquad c = 1 \tag{2.52}$$

And therefore:

$$\omega_{P1,P2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{2.53}$$

Now, since the zero happens in a lower frequency than both poles, the transformer gives a band-pass filter profile like in Figure 2.9. In this case, the bandwidth will be the difference between the two poles. As we see from Equation 2.54 the smaller the self and mutual inductances become, the wider the bandwidth grows.

$$BW = |P_1 - P_2| = \frac{\sqrt{b^2 - 4ac}}{a} = \frac{\sqrt{L_P^2 + L_S^2 + 2L_P L_S - 4 \times L_P L_S(1 - K^2)}}{L_P L_S(1 - K^2)} \tag{2.54}$$

The other important figure of merit is the relative bandwidth (RBW) which is defined as the bandwidth divided by the central frequency of the pass band.

$$RBW = \frac{|P_1 - P_2|}{|P_1 + P_2|/2} \tag{2.55}$$

$$RBW = 2\frac{\sqrt{b^2 - 4ac}}{b} = \frac{2\sqrt{L_P^2 + L_S^2 + 2L_P L_S - 4 \times L_P L_S(1 - K^2)}}{L_P + L_S} \tag{2.56}$$

We can see for transformers with very good magnetic coupling:

$$\lim_{K \to 1}(RBW) = 2 \tag{2.57}$$

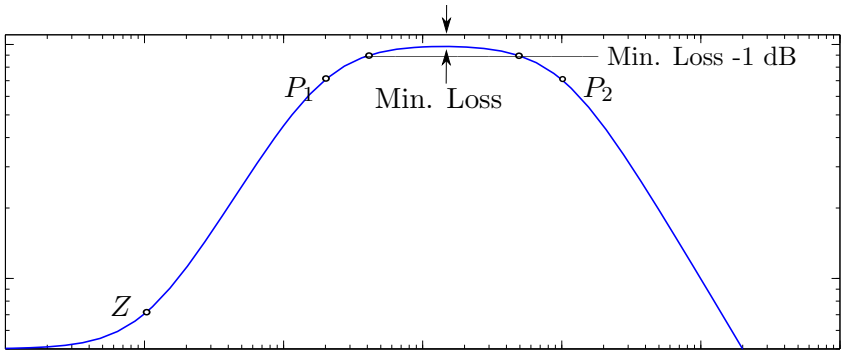


Figure 2.9: Frequency response profile of a transformer

2.3 What we are looking for?

All components need to meet certain criteria for each circuit depending on their application. For transformers, most important figures of merit include:

- Absolute frequency range
- Relative bandwidth
- The two windings' tendency to be lossy in their operational range, or their minimum loss
- Inductances of the coils
- Resistances of two windings
- The coupling factor which relates self-inductances of two windings to their mutual-inductance as we saw in Equation 2.29
- The quality factor which shows how much energy is stored/dissipated in the structure, hence how efficient it is,
- The size of the structure, which can be related to the length and number of turns in the winding and the opening space in the middle of the structure.

For the purpose of examining these parameters, we will use electromagnetic field solvers and compare the results of several transformers to see how the above mentioned parameters change with different dimensional properties of the designed transformers. From the outcomes of these comparisons we will define guidelines for designing suitable transformers for specific applications.

Chapter 3

Transformer Structures

For a long time now, on-chip transformers have been used in various configurations in different RF electronic circuits. There are numerous ways of designing the structure of such devices but they are quite different than discrete component. The main reason is the production technology of ICs in which the components need to be consisting of 2-dimensional objects residing on one single layer of conductor or semiconductor substrate.

3.1 Most Common Structures

In this section we need to investigate what structures are commonly used and see their general differences to choose the right one for our purpose. In general, the structure of choice depends highly on the requirements of the circuit designer and available die surface and layers in the process. Table 3.1 gives a general idea of what to expect from each structure. Each structure is investigated in further detail as follows.

3.1.1 Tapped Transformer

There are many ways of designing planar transformers. For example, this could be achieved by making a single spiral and grounding it in one point in the structure [24], effectively converting it into two separate inductors which are magnetically connected in an asymmetrical structure like the structure shown in Figure 3.1(a). It is probably the simplest way of magnetically coupling two planar spirals. This structure easily allows for any ratio of $N_P : N_S$, but in return, due to the big relative distance between windings of the two spirals it results in a very low coupling factor, K. Obviously, because of having direct connections between two spirals there is a good

chance of propagating high levels of noise between parts of the circuit that use magnetic coupling. On the other hand, due to low surface area between the two spirals, the resulted parasitic capacitance is very low which results in high self resonance frequency. A tapped transformer is made with 3 ports, one of which is connected to the ground node.

3.1.2 Parallel Transformer

Another typical approach could be drawing two spirals in parallel lines as illustrated in Figure 3.1(b). This way the coupling can be higher than the tapped design, but since the two inductors are not exactly the same, it will not be an effective 1:1 transformer. It is also an asymmetrical design like the tapped transformer. Unlike the tapped design, the two spirals cover a large parallel surface area which results in a very large parasitic capacitance, hence, a low self resonance frequency. The other difference between tapped and parallel transformers is that the latter one is a 4-port device.

3.1.3 Frlan Transformer

Similar to the parallel structure, there is the Frlan transformer (Figure 3.1(c)) which is a 4-port and a centre-symmetrical structure. In Frlan design, the two spirals are rotated by 180 degrees to the opposite sides. This not only solves the asymmetry, it also makes it possible to have the two spirals' inductances more closely matched which makes a much better 1:1 transformer. But again like the parallel structure, it has a big parasitic capacitance which means a low self resonance frequency.

3.1.4 Stacked Transformer

The two spirals could be stacked in different layers on top of each other (Figure 3.1(e)), too. This way the magnetic coupling could be very high. Stacked transformers could be built with even more layers resulting in very compact layouts [25][26]. But, there also will be a big area between the two of them which acts as a very big problematic parasitic capacitor and that will limit the bandwidth of the transformer to only very low frequencies and also reduces the quality factor. Note that the thickness and thus the side surface of metal stripes are usually much less than their width and top and bottom surfaces; and also the distance between two metal layers is fixed by the technology where as the distance between two metal wires (here, the loops of the transformers) can be increased as needed. In case of designing on-chip transformers, these two facts mean that the parasitic capacitances between

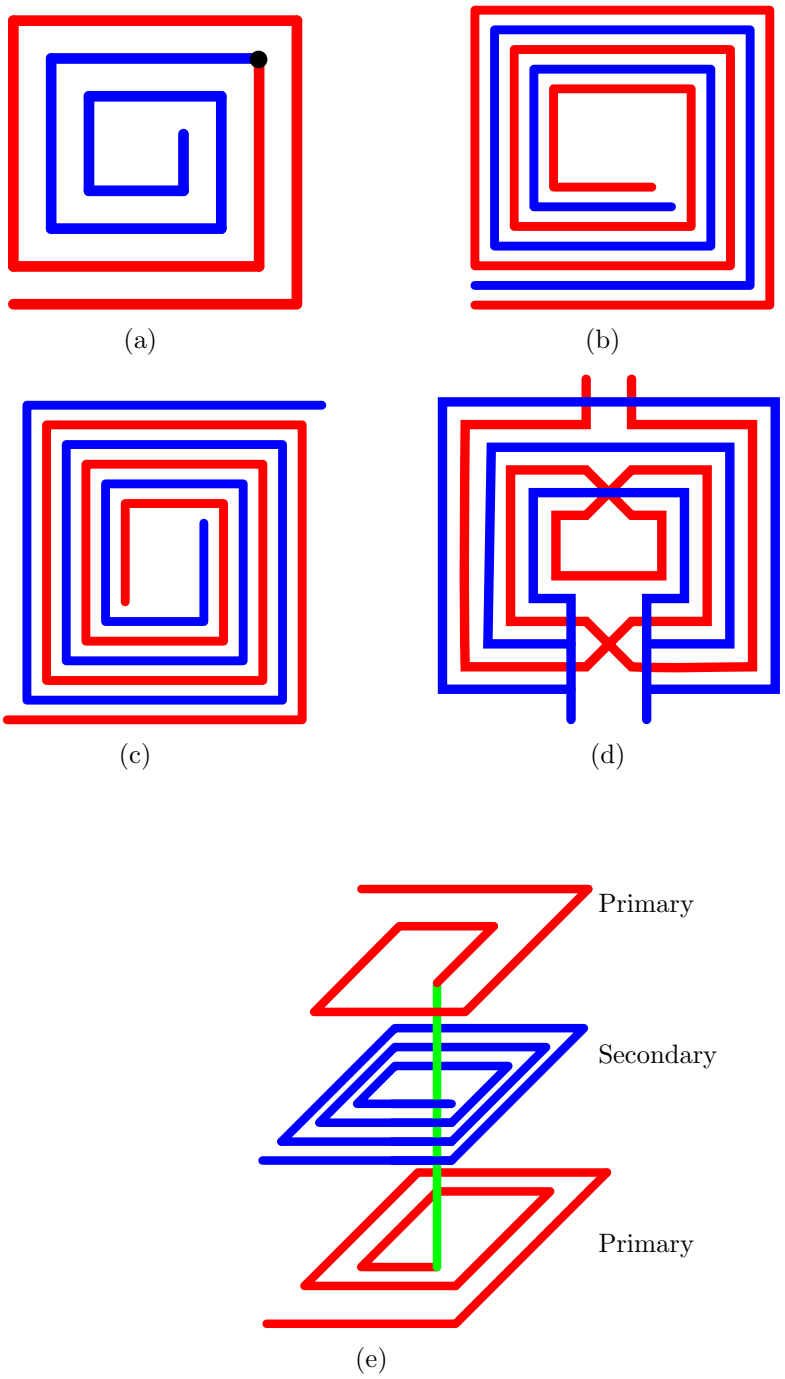


Figure 3.1: Different transformer structures. (a)Tapped; (b) Parallel; (b) Frlan; (d) Step-up; (e) Stacked.

metals in the same layer are relatively much less than the ones between metal

Structure	K	Q	Ratio	Layers	Symmetrical	Ports	Self Resonance Frequency
Tapped	small	high	—	2	no	2+gnd	high
Parallel	medium	medium	1:1	2	no	4	low
Frlan	medium	medium	1:1	2	yes	4	low
Stacked	hign	small	—	≥ 3	no	4	low
Step-up	medium	medium	1:1$\sim$4	3	yes	4	high
Interleaved	high	small	1:1	2	yes	4	high

Table 3.1: Quick comparison of different on-chip transformer structures.

stripes stacked on top of each other.

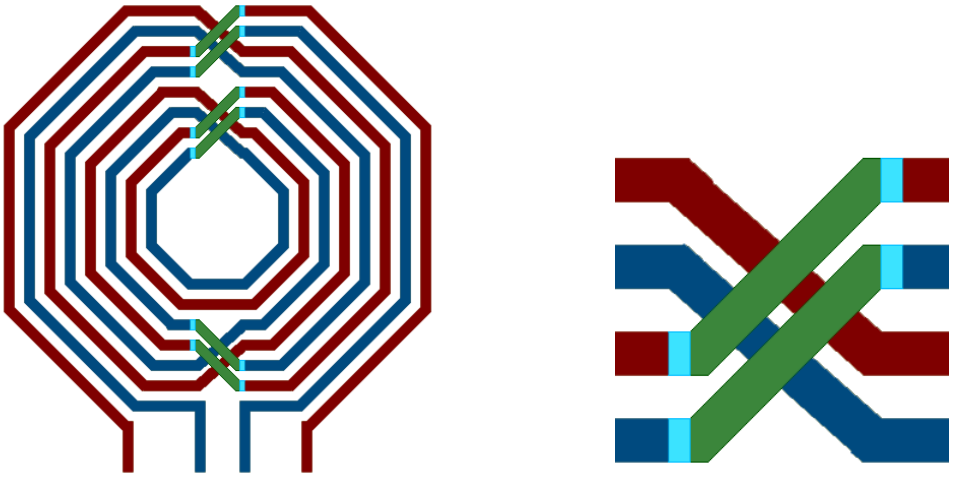
3.1.5 Step-up Transformer

There is also the step-up design depicted in Figure 3.1(d) which has a very good coupling coefficient, small amount of parasitic capacitor and thus a fairly good quality factor[27]. But, again this one needs a extra layer and it can only be made in $1 : N$ ratio and theoretically, it can have any value for N. In this structure, one spiral from one of the former structures is made on one layer and another one is made on the second layer. This latter one is constructed with a mesh of metal wires on a one-loop spiral path. The surface area and hence the capacitance between the two spirals is very small which results in a high self resonance frequency.

3.1.6 Interleaved Transformer

The structure of choice for this thesis is one called "interleaved transformer" as pictured in Figure 3.2(a) and it is a symmetrical structure and a 4-port device in contrast to structures like tapped transformer which are effectively 2-port devices. Each wire loop of any of the windings, with the exception of the most inner and the most outer ones, are surrounded by loops of the other winding. So, there will be a very good coupling coefficient a the small cross-section area between the only two layers used. This results in a small amount of parasitic capacitors and that translates into high operational frequencies. Of course this means that if we want to take advantage of the good coupling factor of this method, the transformer cannot be realized with any turn-ratio and that would be either $N_S = N_P$ or $N_S = N_P + 1$. There is, however, a difficulty with this design. The windings of each side must keep a constant flow direction of current while circling the centre so that the magnetic fields of

adjacent wires of the one inductor would not cancel each other out, resulting in a very poor self inductance. This means each winding must cross itself, as well as the other one, multiple times. This makes for the double-crossing pattern in Figure 3.2(b).



(a) (b)

Figure 3.2: (a): An interleaved transformer with $N_S = N_P = 4$
(b): The Double-cross pattern of the structure

3.2 Substrate

Regardless of the structure design of choice, the transformer must be implanted onto the circuit. This can be either on the same substrate or on another from which it will be later transferred to the main circuit's die with a fabrication process demonstrated in Figure 3.3 [28]. If the substrate is a good insulator such as Quartz, then there will be very little parasitic capacitances between the metals and the substrate.

If the substrate is a standard silicon one, there will be big capacitances between the metals and the grounding substrate, and Eddy currents that will dissipate power, and hence reduce the quality factor. In order to overcome the latter problem, some types of shielding can be used [29] which are made by breaking the poly-Si ground beneath the windings into stripes[30][31], which insulate the structure and passivate the eddy currents like the pattern in Figure 3.4. On the other hand, doing so will in return reduce the effective

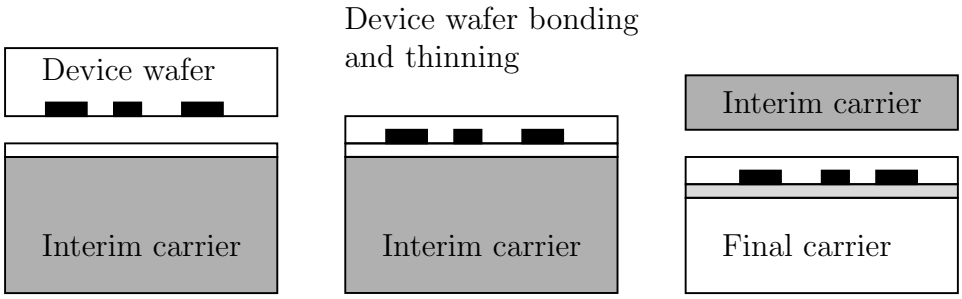


Figure 3.3: An example of the process for transferring to another wafer

thickness of the oxide layer and increase the oxide-capacitance[32]. So, the designer needs to make a trade-off between the two. This effect was tested for an interleaved transformer with 3:4 ratio, inner opening of 120μ, wire width of 10μ and wire spacing of 10μ. It was done with first, a Quartz substrate, then, a plain Silicone substrate without doping, and then with the same Si substrate but with a very simple patterned ground shielding as illustrated in Figure 3.5. The results show the clear advantage of the insulator substrate over semiconductor options in achieved bandwidths. At the same time, although the substrate with patterned shielding in the ground does not perform as well as Quartz, it still manages to reduce the losses by a good margin with the cost of a little less bandwidth. The amount of changes in the inductances were less than a percent and the coupling coefficient stayed almost constant. These results can be seen in Table 3.2. In this thesis, the transformers are designed, simulated and studied for a well-insulating substrate.

Substrate	BW (GHz)	RBW	Peak frequency (GHz)	Min. loss (dB)
SiO_2	23,8	1,301	26,4	-1,34
Plain Si	21,4	1,281	21,4	-1,51
Patterned Si	21,1	1,267	21	-1,39

Table 3.2: Different substrate options and their effects on the performance of transformers.

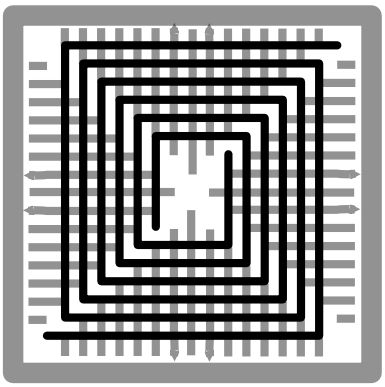


Figure 3.4: An example of patterned ground to passivate eddy currents in a Frlan transformer's substrate.

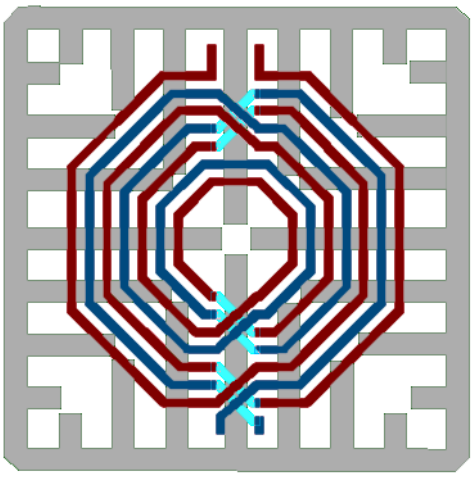


Figure 3.5: Simulated transformer with patterned ground.

Chapter 4

Simulations

After deciding on the structure of choice among the ones discussed in the previous chapter, it had to be characterized so that it could be adapted for different use cases. In order to analyse the effect of various parameters in behaviour of transformers, multiple devices were generated using an automation script in an EM-simulation environment with specific ranges for each design parameter to study and then they were compared to one another.

4.1 Simulation Environment

The EM simulation environment of choice is the ADS software package from Agilent Technologies. This software package includes a few different graphical design environments (schematic, layout, system-level setup, symbol, etc.), Agilent's proprietary comprehensive script language and interpreter for automation called AEL, and a set of very powerful electromagnetic and high frequency circuit simulation tools. AEL has a set of functions, commands and operators which are used to define polygons on a given surface.

The automation script for generating devices first draws polygons on a certain layer which make half-loops for the spirals, but leaves the connection places between them open. After drawing two loops, a double crossing pattern is generated and then the algorithm moves on to draw the next two loops. This process starts with the most inner loops and continues outwards until all the loops of both windings are drawn. Then, the two most outer loops are connected to their respective ports. One of them is a part of the primary while the other belongs to the secondary. Figure 4.1 shows a sample transformer made through these steps with 2:3 turn ratio.

Since the double crosses are connected to four different loops, the algorithm differs based on the total number of loops. Since the ports could be

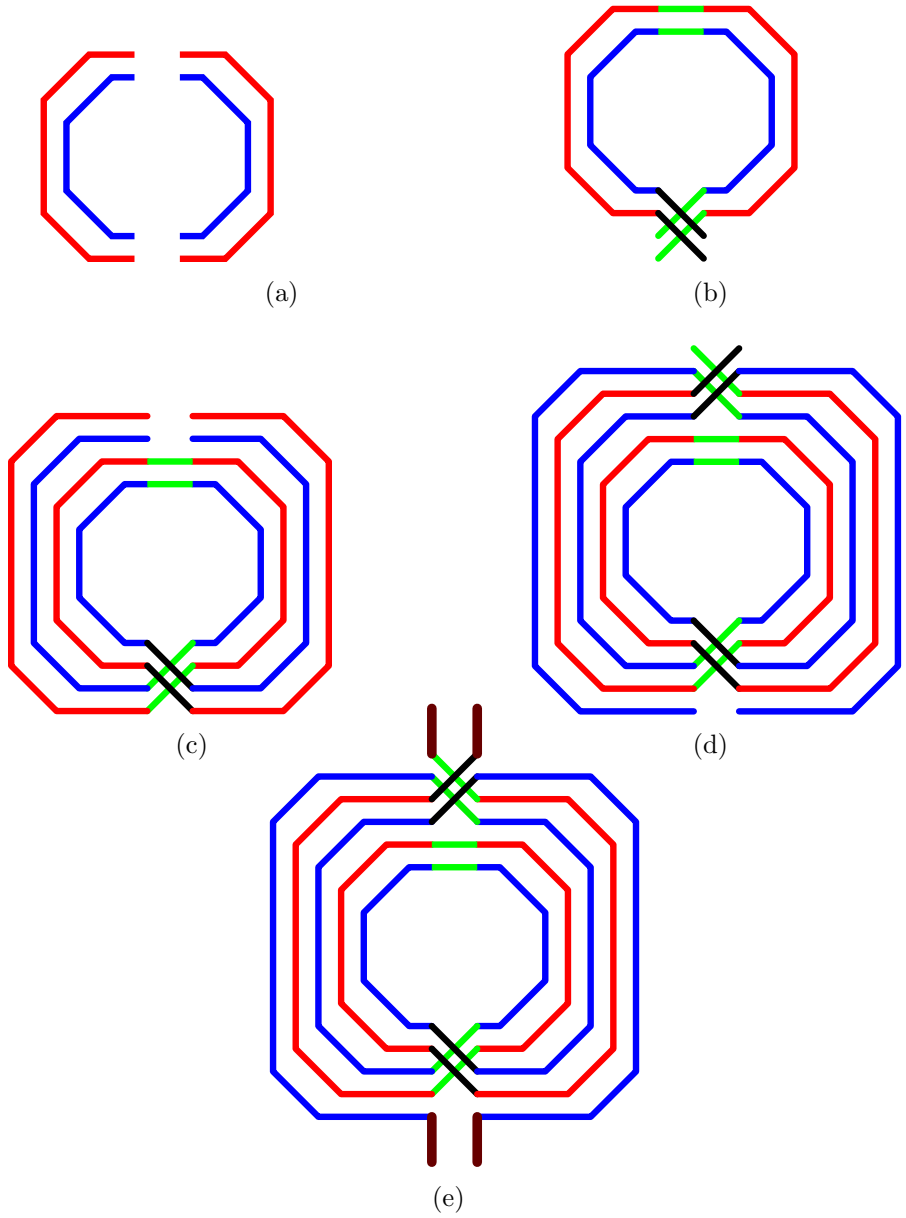
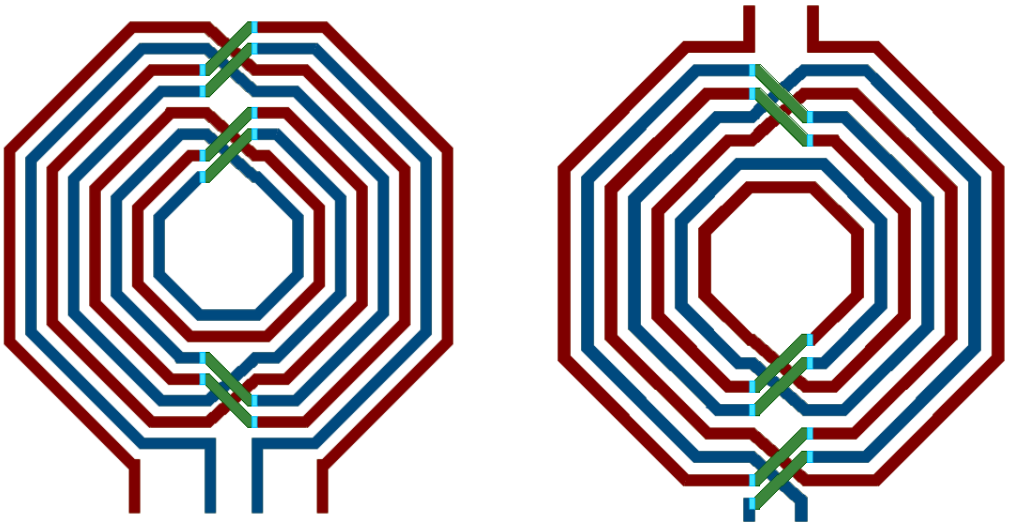


Figure 4.1: Steps for creating a 2:3 interleaved transformer.
(a)Drawing 4 first half-loops. (b) Adding connections for first two loops and adding double crossings. (c) Adding two more sets of half-loops. (d) Adding another set of double crossings and the last two half-loops. (e) Finalizing the design by adding the ports to the two most outer loops.

connected to each of these loops, the remainder of division of total number of loops by 4 defines how to terminate the algorithm and finalize the device. If $N_S = N_P \Rightarrow N_{total} = 2 \times k$, then both couples of ports are on the same side of the device like Figure 4.2(a). If $N_S = N_P + 1 \Rightarrow N_{total} = 2 \times k + 1$, then they will be on opposite sides of the device like Figure 4.2(b). The flow diagram in Figure 4.3 shows the steps in general, and should be modified according to the number of loops and the remainder of its division by four. Since these 4 cases need different parameters in different choices, having them all in one script would make an awful spaghetti code. So, it was decided to run them as separate scripts from separate files. These files are attached in the appendices.



(a) (b)

Figure 4.2: Position of ports
(a): On the same side for an even total number of rounds
(b): On opposite sides for an odd total number of rounds

4.2 Layers and Characteristics

As mentioned in section 3.2, the substrate has a notable effect on the performance of the transformers due to being lossy. In this thesis the substrate of choice is Silicone Dioxide (SiO_2) which is a very good insulator and has a relative permittivity of $\epsilon_r = 3,9$. The device is built in two metallization layers of Copper (Cu) with conductivity of $5,96 \times 10^7 S/m$; but for compensating for defects and impurities in the metallization process, the value of

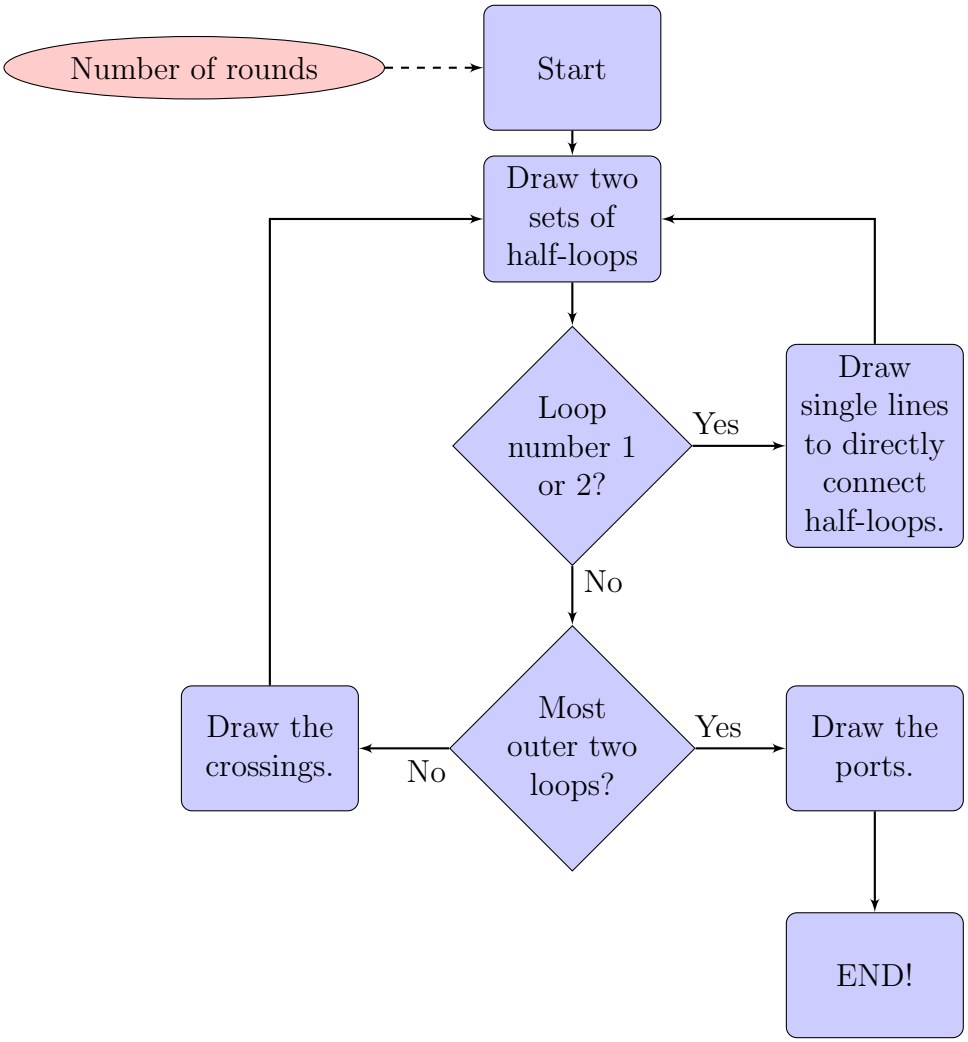


Figure 4.3: The general flow chart of the algorithm that drew the transformers.

the conductivity is decided to be $3,5 \times 10^7 S/m$. The Via (layer number 5) connectors use the same copper. The bottom layer (layer number 4) has a thickness of $1\mu m$ and the thickness of the top layer (layer number 6) is $2\mu m$ and they are embedded in layers of SiO_2 with respective thickness values of $2\mu m$ and $10\mu m$. The substrate's thickness measures to be $500\mu m$. The material definition map is illustrated in Figure 4.4, but of course, they are not to scale. The spirals are made mainly on the top layer which has more thickness and less resistivity, while the bottom layer is left to be used as underpass for crossings of metal lines.

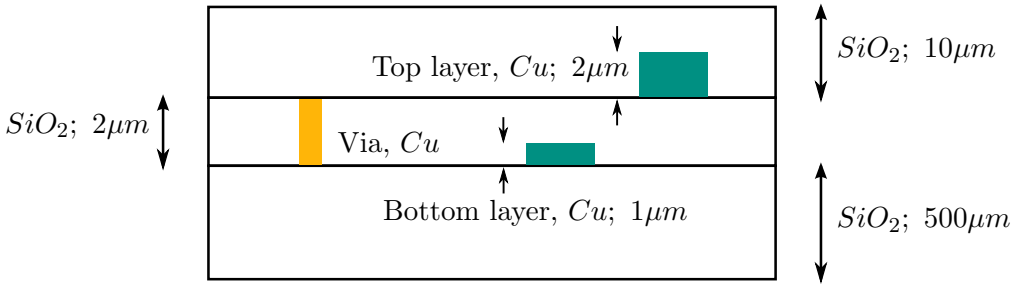


Figure 4.4: Definition of different layers for the devices.

4.3 Interleaved Transformers

As mentioned before, for this thesis an interleaved structure is opted for. This type of structure has a very good coupling coefficient. It is also symmetrical and can be realized with only two layers of metallization. One drawback to this choice is the limitation of turn ratio. If we want to benefit from its good magnetic coupling, the two spirals can have either $N_S = N_P$ or $N_S = N_P + 1$ turn ratios; and in large enough number of turns the second type also will become similar to the first one, creating effectively an almost 1:1 transformer. If the difference is more than one turn, the most outer loops will not have a good magnetic coupling with the more inner ones. Of course, it is common to combine a few 1:1 transformers and create a device with a different effective turn ratio. For example, if two similar 1:1 transformers are connected in parallel on the primary side and in series on the secondary side, the parallel inductances of the primaries would generate a virtual inductance of half that value the inductance of each, and the series inductances of the secondary would make a virtual coil with double the inductance of one of them. This system in result mimics the behaviour of a transformer with half the number of loops of the original device in the primary and double the number of loops

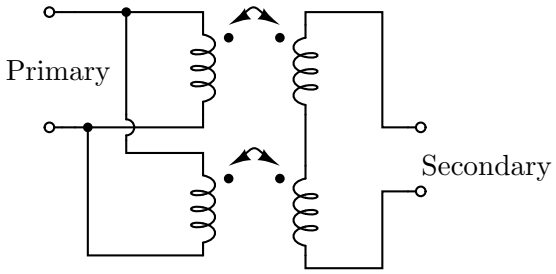


Figure 4.5: Constructing a $1:4$ from two $1:1$ transformers.

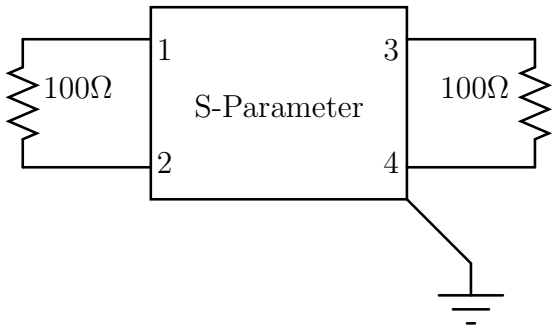
in secondary which is similar to a transformer with $0,5:2 \equiv 1:4$ turn ratio. Figure 4.5 depicts this configuration.

It is also notable that since this structure is only used when the turn ratio of the transformer is close to $1:1$ and for each $N_P + N_S$ there is only one way of achieving that, in the rest of the thesis only this number is used to identify the turn ratio. It is obvious that for any value of "k", if "total number of turns$= 2 \times k$" then the turn ratio is $k:k$, and if "total number of turns$= 2 \times k + 1$" then the turn ratio is $k:k+1$.

4.4 EM Simulation Results

Transformers are magnetic AC devices. This means, in order to model them, we need an electro-magnetic simulation software. The software analyses the transformers as 4-port devices with AC inputs and measures the magnetic and electric fields of each and every piece of conductor. This allows for a very accurate modelling of inductance, capacitance and impedance of passive devices including monolithic transformers. The outcome of the simulation is in the form of a file containing the S-parameters of each simulation for the given frequency range. The S-parameter files are then used as block-level system properties of a 4-port device in a configuration shown in Figure 4.6 to calculate different parameters including port-to-port resistances, capacitances and inductances, frequency response, quality factor and coupling coefficient. Equations used to calculate each of these are mentioned in Table 4.1. Here, the results of the mentioned simulations are investigated.

In total, 54 transformer instances were generated and simulated. For all cases the spacing of wires was kept constant at $10\mu m$ because it only affects the parasitic capacitances between two adjacent metal lines on the same layer and with the thickness being only $2\mu m$, that would be virtually negligible. the other dimensional parameters needed to design the transformers are the number of loops, the width of the wires and the diameter of the most inner



Calculate Z = YES
Frequency Range: 0,1 GHz $\sim$ 30 GHz
Frequency Sweeping Steps: 0,1 GHz

Figure 4.6: Block-level system setup for calculating different parameters from 4-port S-parameter files.

Value (unit)	**Equation**
$L_P(nH)$	$\frac{1\times10^9\times imag(Z(1,1))}{\omega}$
$L_S(nH)$	$\frac{1\times10^9\times imag(Z(2,2))}{\omega}$
L_{ratio}	$\frac{L_S}{L_P}$
$M(nH)$	$\frac{1\times10^9\times imag(Z(2,1))}{\omega}$
Q_P	$\frac{imag(Z(1,1))}{real(Z(1,1))}$
Q_S	$\frac{imag(Z(2,2))}{real(Z(2,2))}$
K	$\frac{imag(Z(2,1))}{\sqrt{imag(Z(1,1)\times imag(Z(2,2))}}$
$R_P(\Omega)$	$real(Z(1,1))$
$R_S(\Omega)$	$real(Z(2,2))$

Table 4.1: Equations used to measure different properties of the system.

loop, also referred to as the inner space opening. Since the crossings are all made in 45° lines, there is a limit (depending on the wire width) for the minimum diameter for this opening that can be used while the most inner loop still keeps its geometry and the crossings do not penetrate into adjacent spaces. This limit tends to be about 6 times the sum of the wire spacing and width. Keeping that in mind, 3 different wire widths were chosen: 10μ, 15μ *and* 20μ. For each of these cases three different inner opening space diameters were investigated: 120μ, 135μ *and* 150μ. And for each of these cases, 6 different devices were generated with different numbers of turns (3:4, 4:5, 5:6, 4:4, 5:5, 6:6). This makes in total 54 different transformers which cover different trends while varying the mentioned physical design parameters of the interleaved monolithic transformers.

Previously it was mentioned that two of the most important parameters for examining a transformer are its actual bandwidth and relative bandwidth. In Section 2.2.4 we discussed that the bandwidth in general in a band-pass transfer function is the difference between the two poles of the system. At those points the gain of the system is 3dB lower than the peak of the system's transfer function, or in case of a lossy systems without gain, 3dB less than the minimum loss value. In this thesis, to achieve a better accuracy for the system loss in the band-pass section of the frequency range and also in order to investigate a worst case scenario, the cut-off frequencies are chosen to be at -1dB loss values. One such frequency response of a transformer with 10 rounds, $W = 10\mu m$ and $D_{in} = 120\mu m$ is demonstrated in Figure 4.7.

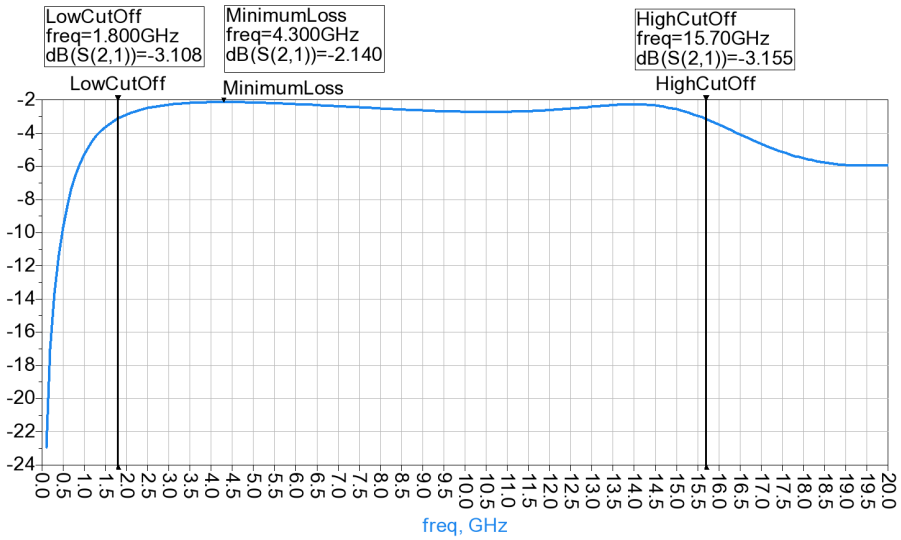


Figure 4.7: The band-pass transfer function of a transformer with -1dB cut-off frequencies.

First of all, we need to know how wide-band the transformers perform in their respective frequency range and that is measured by the relative bandwidth. The data for the measurements of RBW are collected in Table 4.2 and Table 4.3. From these tables we see that generally, the relative bandwidth is about 10% or less higher when $N_P = N_S$ compared to similar cases where one side has more turns than the other side. Otherwise, it seems that the width of the wires while keeping D_{in} constant does not affect the relative bandwidth of the transformers.In case of the changes in relative bandwidth with varying the inner opening diameter the observation suggests that mostly by increasing D_{in} and keeping W constant the RBW decreases.

NT	$W = 10um$	$W = 15um$	$W = 20um$
7	1.3	1.33	1.37
8	1.45	1.37	1.45
9	1.36	1.37	1.43
10	1.59	1.59	1.59
11	1.42	1.42	1.45
12	1.4	1.59	1.6

Table 4.2: How the relative band width changes with total number of rounds ($N_P + N_S$) and with wire width

NT	$D_{in} = 120um$	$D_{in} = 135um$	$D_{in} = 150um$
7	1.3	1.19	1.15
8	1.45	1.56	1.38
9	1.36	1.3	1.27
10	1.59	1.51	1.42
11	1.42	1.39	1.36
12	1.4	1.54	1.48

Table 4.3: How the relative band width changes with total number of turns and with inner opening diameter.

As discussed in Section 2.2.4, another important figure of merit is the actual bandwidth of the transformer.

In general, an LC filter's self resonance frequency is in reverse proportion with the square root of the product of $L \times C$ with the relations in Equation 4.1. In a small transformer with only few loops in each windings, the inductances and capacitances are much smaller than those of bigger transformers with

Number of Turns	Lower Cut-off	Higher Cut-off	Bandwidth
7	6.4	30.2	23.8
8	2.9	18.2	15.3
9	3.6	18.8	15.2
10	1.8	15.7	13.9
11	2.1	12.5	10.4
12	1.3	7.3	6

Table 4.4: Bandwidth and cut-off frequencies in units of GHz and their relations with number of turns ($W = 10\mu m$ & $D_{in} = 120\mu m$ constant).

big inductances. So, we expect the smaller ones to have bigger self resonance frequencies and bandwidths. That is exactly what we see in the simulated transformers. These bandwidths are available in Table 4.4.

$$\omega_0 = \frac{1}{\sqrt{L \times C}} \tag{4.1}$$

Next to examine is how well the windings are magnetically coupled. Figures 4.9 and 4.8 show that by increasing the number of turns, increasing the width or increasing the inner opening diameter, the coupling coefficient of the transformers increases. This increase is almost linear compared to number of turns. Although these changes are clearly seen in these charts, they are not very significant. The K of transformers with similar numbers of turns and different W or D_{in} are only a few percent apart and the difference between the K of transformer with NT=7 and another one with NT=12 is less than 10%.

The width and thickness of metallizations are constant in each transformer structure, except for Via points and crossing underpasses. So, the resistance of each coil is, with a good approximation, proportional to the length of the coil wiring with relations in Equation 4.2. The simulator program measures the resistance and the inductances of each coil. Now, we can compare the inductance of each coil in each transformer to the length of the coil. This has been done in Figure 4.10 which shows an almost linear increase of the inductance with the wire length of the coil. This was done only for the primary as the devices are reversible and both sides are expected to behave similarly.

$$R = \rho \times \frac{L}{W \times t} \Rightarrow L = R \times \sigma \times W \times t \Rightarrow R \propto L \tag{4.2}$$

Another important factor to consider is the proportion of two inductances. There appears to be two different cases: where $N_P = N_S \Rightarrow \qquad NT = 2 \times k$

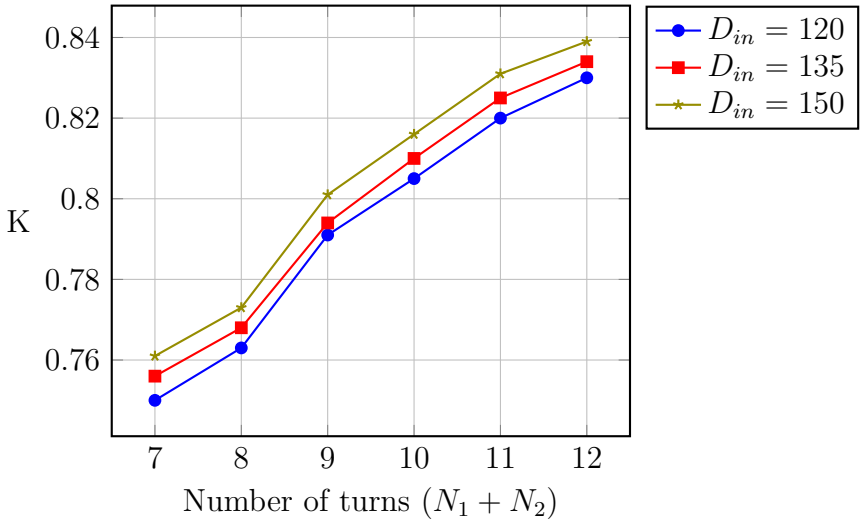


Figure 4.8: The inner space diameter and the number of turns vs. the coupling coefficient with $W = 10\mu m$ constant.

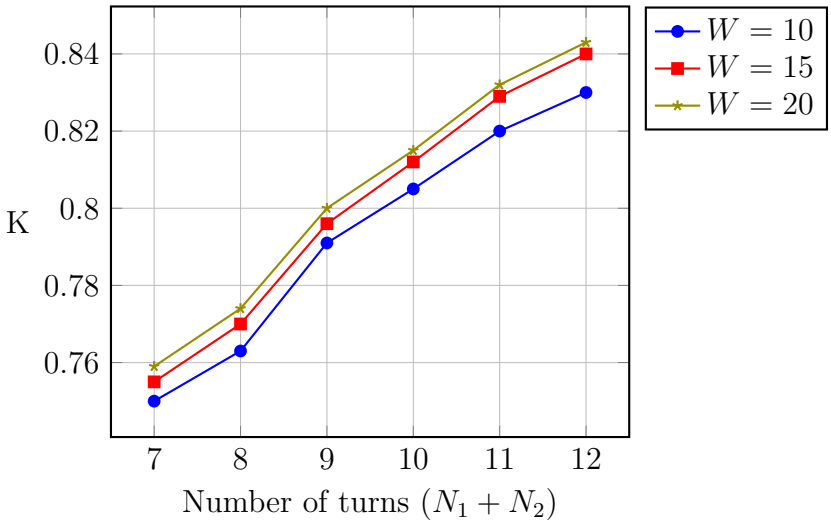


Figure 4.9: The wire width and the number of turns vs. the coupling coefficient with $D_{in} = 120\mu m$ constant.

and where $N_P + 1 = N_S \Rightarrow NT = 2 \times k + 1$. Comparing them in groups and in respect to changes in D_{in} and W results in a clear difference between the two cases which is seen in separation of data points in Figure 4.11 and Figure 4.12.

In case of an even number of turns, inductances are more closely matched and the ratio is closer to 1. This was predictable since as we saw in Chapter 2

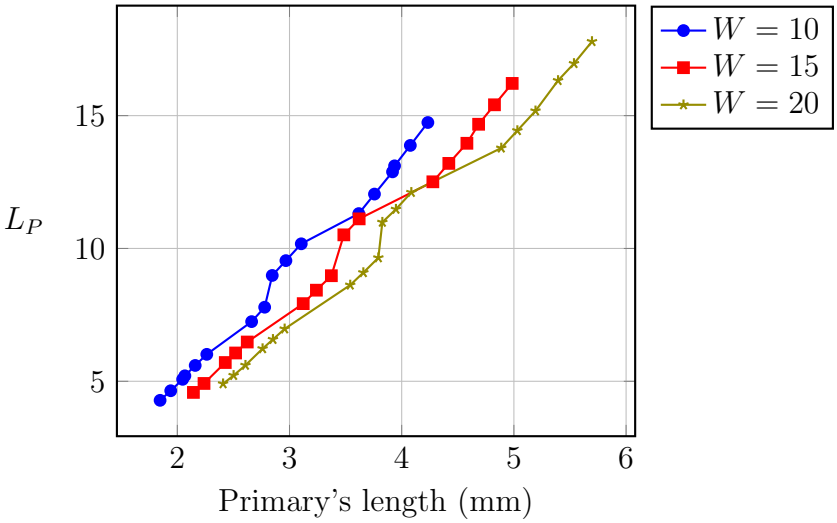


Figure 4.10: Effect of wire length of the primary on its inductance.

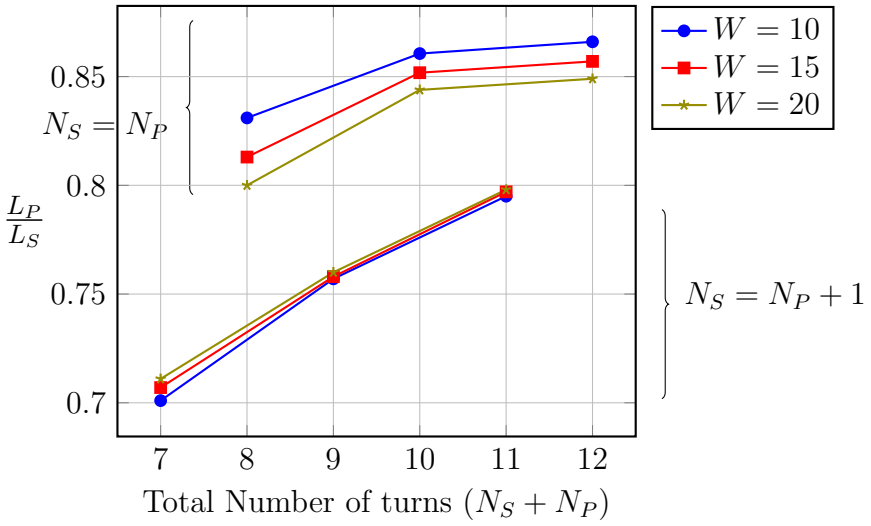


Figure 4.11: Effect of wire width on the proportion of the inductances ($\frac{L_P}{L_S}$).

the inductance of an ideal coil is proportional to its number of turns. But in return, in cases with an odd number of turns the ratio of inductors is almost constant when changing D_{in} and W while they may vary a few percent in the rest of cases.

As we already know, a transformer like any other real device has some energy loss, which we try to keep to a minimum. The minimum loss of the devices in these simulations range from -0,8dB to nearly -2,3dB. In general, the cases with $N_S = N_P$ tend to be more lossy while it doesn't seem to vary

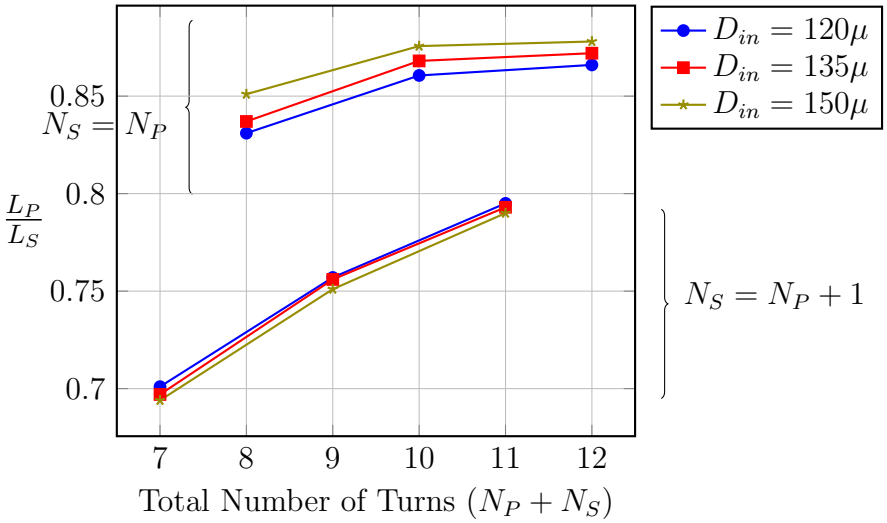


Figure 4.12: Effect of inner opening diameter on the proportion of the inductances ($\frac{L_P}{L_S}$).

significantly with different values of K. But for devices with $N_S = N_P + 1$, their minimum loss value is less than the former ones, but the amount of their energy loss seems to be increasing with higher values of K.

In the end, we expect the quality factor to decline with increasing the coupling coefficient, because a good coupling means transferring most of the energy to the other coil instead of saving it in the magnetic field. This is seen in linear regression trend line in Figure 4.14.

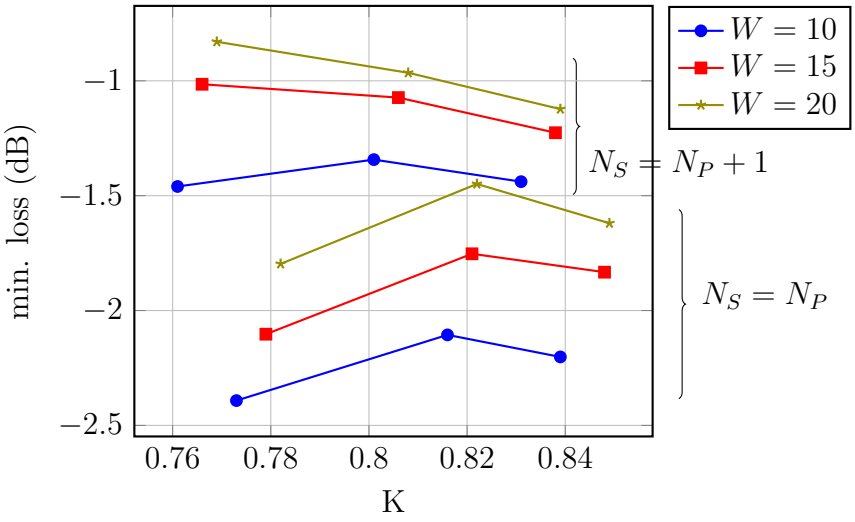


Figure 4.13: How minimum loss Changes with different values of K with 3 different cases of W, and D_{in} being constant.

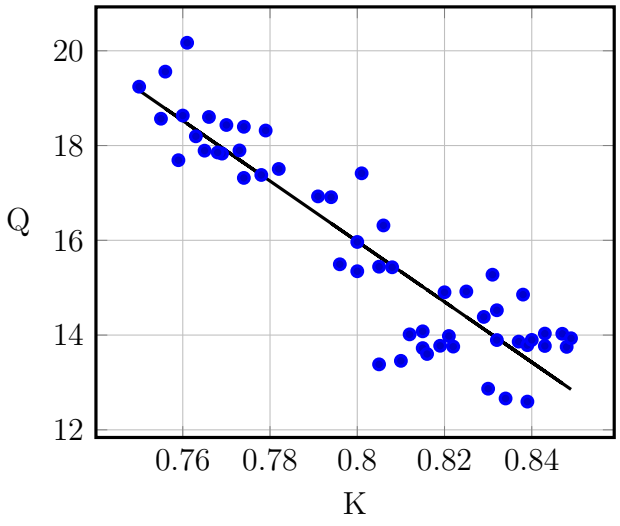


Figure 4.14: Maximum quality factor (Q) vs. different values of K.

Chapter 5

How To Design A Good Transformer?

In order to design a "good" transformer, we need to know what is required for the particular circuit it is going to be used in. There might be applications in which the circuit operates at 1 GHz frequency. Obviously, in such cases a compact $3:4$ transformer with a frequency range of 6,4 $\sim$ 30,2 GHz is not suitable. That needs a large transformer structure with bigger number of turns on each windings; one like a large $6:6$ device with a wide inner opening that works at $1 \sim$ 6,2 GHz (Table 4.4). This transformer is much better suited for applications like Bluetooth and WiFi which operate at 2,4GHz band.

On the other hand, higher-frequency applications need transformers with smaller numbers of loops and narrower inner openings. A 3:4 transformer could operate at frequencies up to 30,2GHz. We can conclude, from what we learned in Section 4.4, that with smaller transformers could work at even higher frequencies.

In cases where matching of the inductances is necessity, a device with even number of rounds is to be used, as we saw in Figure 4.11 and Figure 4.12, they tend to have nearly 50% better matching. Although, the matching of odd-numbered devices ($N_S = N_P + 1$) increases almost linearly with bigger number of rounds.

Another possibility is a need for a transformer as a load balancer. For a good load balancer the most important figure of merit is having higher values of K, where the transformer becomes closer to an ideal transformer (Section 2.2.2). As we saw in the previous chapter, bigger numbers of loops and wider inner openings yield in larger coupling coefficients.

If the transformer device is going to be used also as an inductor, the inductance of the coils is the main factor to consider. Then, from the chart in Figure 4.10 can tell what length the coil should have, and from that we

Desired Property	Requirement
High K	Big — wide D_{in}.
High Q	Low K
High L_{ratio}	$N_S = N_P$.
High Inductance	Big — wide D_{in}.
Low Minimum Loss	$N_S = N_P + 1$ — low K.
High Operational Frequency	Small
High Relative Frequency Range	Small — narrow D_{in} — $N_S = N_P$.

Table 5.1: What different properties need to be realized while designing a transformer.

can derive the resistance and thus the number of rounds in the primary as in Equation 4.2. Also, it is logical to assume in such cases the Q is needed to be as high as possible. Then devices with lower K values should be considered.

There are some specific characteristics which are particularly important for IC designers. These properties are concluded in Table 5.1. I will now try to expand these features and characteristics one by one.

Small die area: If there are constrains on the Silicon die, a completely planar structure could be taking up to much space. We can overcome this problem by making spirals on different layers and stack them on top of each other. As discussed earlier in Section 3.1.4, this stacked transformer structure could be made to have a very dense structure resulting in very compact layouts and very good coupling coefficients. In return, transformers made with this structure exhibit large parasitic capacitances which result in small operational frequencies. If minimizing the die area has a very high priority in the requirements of the device, then stacked transformers are preferred over the interleaved design which was discussed in detail.

High coupling coefficient: A high coupling coefficient means the power is transferred with high efficiency between the two spirals. That is why high K value is a desired property of a transformer. In Section 4.4 and through different simulations we saw that the K value increases to some extent by increasing the number of turns of the spirals, where as the width of the wires and the diameter of the opening in the centre of the device do not considerable effects on the coupling of the spirals.

Low insertion loss: Like all other devices, transformers introduce loss into the signals that pass through them. It is necessary to minimize these signal losses. Amongst the investigated samples, the difference between the best and the worst cases is nearly 1,5dB. The samples with $NT = 2 \times k + 1$ have less minimum loss values. The other contributing factor to this value

is the wire width which defines the ohmic resistance of the spirals. There are cases where changing the wire width from $10\mu m$ to $20\mu m$ decreases the minimum loss of the system from -1,5dB to 0,8dB or from -2,4dB to -0,9dB. This means a wider wire makes a transformer with lower amount of insertion loss.

High relative bandwidth: The relative bandwidths of the transformers shows how wide band they operate in their respective operational frequencies. The RBW increases by only an insignificant amount when increasing the wire width and decreases by a few percent by increasing the D_{in} which could be the result of the slight increase in surface area of parasitic capacitances. Transformers with $NT = 2 \times k$ show about 10% more RBW than comparable ones with $NT = 2 \times k + 1$. Adding more rounds to spirals also adds a few percent to RBW.

Technology view: There are parameters in designing a transformer which are not defined by the circuit designer. For instance, the thickness of metal wires is defined by the fabrication process. Changing it can change the ohmic resistance of the spirals and thus change the insertion loss of the device. Another factor is the number of available layers. In Chapter 3 we saw that some structures need at least 3 layers to be built while some others can be built with as few as only 2 layers. The fabrication process also defines the type of the substrate. The substrate could be made of lossless materials like Quartz, which means it is a good insulator and eliminates eddy currents which affect the properties of the transformer. It also significantly decreases the parasitic capacitances of the substrates. If the substrate is lossy, like standard Silicon wafers, there are methods for improvement of loss properties of the device. For example, the device could be made with a shield and ground patterns like the one in picture 3.4.

As an example, we can investigate a high-K transformer with large inductances to be used in Bluetooth bandwidth. Bluetooth devices operate in 2,4 to 2,485 GHz frequencies. In this example we also assume that the priority of die space consumption is not as high as the other factors. From Table 4.4 we can see that transformers with NT=10 and NT=12 fulfil the frequency range requirement. Of course, the transformer with NT=11 also works in that range, but its lower cut-off frequency at 2,1 GHz is too close to the lower end of the frequency range, so we neglect it. For both other requirements of high K value and large inductance, from Table 5.1 we find that we need a the biggest available transformer with the widest possible D_{in}. In case of transformers made during this thesis, this means we should go with NT=12 and $D_{in} = 150\mu$. We can presume that the insertion loss should be kept to minimum. Unfortunately, this contradicts with having a high coupling coefficient. All we can do is to chose the widest wire width,

which is $W = 20\mu$. It also requires to have $N_S = N_P + 1$, but since non of the transformers with an odd NT can operate safely in the required frequency range, using one of them is not an option. Simulation results for characteristics of the selected transformer are collected in Table 5.2 and its frequency response is shown in Figure 5.1.

Characteristic	Value
L_P	17,79 nH
L_S	15,276 nH
R_P	8,137 Ω
R_S	7,54 Ω
L_{ratio}	0,859
K	0,849
Bandwidth	5,3 GHz
Relative Bandwidth	1,493

Table 5.2: Bandwidth and cut-off frequencies in units of GHz and their relations with number of turns ($W = 10\mu m$ & $D_{in} = 120\mu m$ constant).

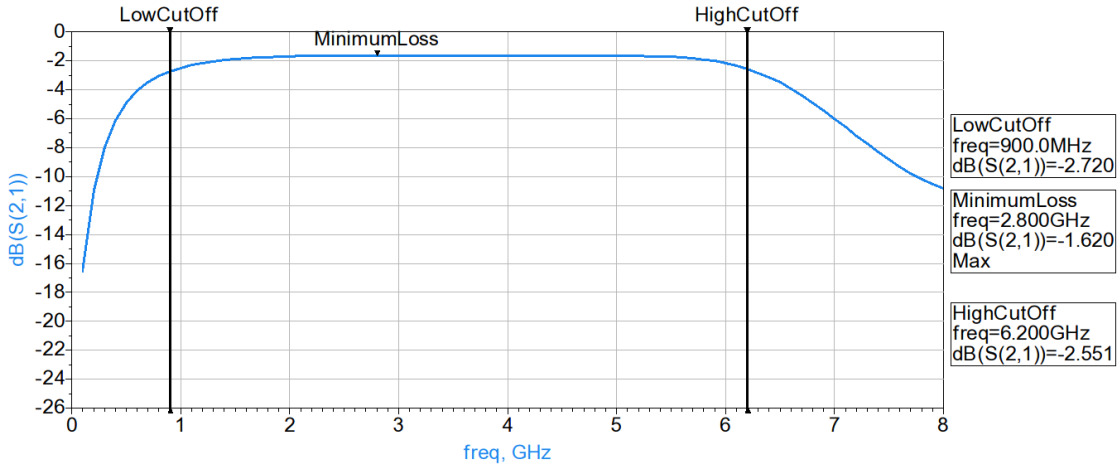


Figure 5.1: Characteristics of the selected transformer in the example above.

Chapter 6

Conclusions

As discussed through out this thesis, transformers are used in various RF circuits. They can be used in VCOs to eliminate the need of a varactor or they can as power combiners in order to collect and add up the power from two PAs and thus reducing the size of the transistors in them. Transformers can be very useful in designing LNAs and they are commonly used as load balancers. These tasks can be achieved through magnetic coupling of two coils in a transformer. Unfortunately, foundry supported monolithic transformer models are not widely available. So, circuit designers need to struggle with different methods to achieve a usable transformer for their RF circuits. There also tends to be limitations like die are, metallization thickness, limited insulation in the processed fabrication and substrate, finite conductivity, etc., and they all add to the complexity of the task. Furthermore, because of these imperfections, transformers are not ideal devices and operate usable only over a finite bandwidth. Each transformer has its own bandwidth, loss and frequency response profile, which a circuit designer needs to be aware when using them.

This thesis aims to generate and characterize a number of on-chip monolithic transformers for the use in RF circuits. First, we examined how inductors work and how a coupling of the inductors can be useful. We saw that even without considering many parasitic capacitances and the resistances of the coils and just because of limited magnetic coupling of the coils, transformers exhibit a band-pass filter profile and they cannot be used in any frequency. Then we investigated different common monolithic transformer structures that are used in different RF circuits. Basic properties, perks and limitations of tapped, Flan, parallel, step-up, stacked and interleaved transformers were discussed and the latter one was chosen for this topic because of its good coupling coefficient, good bandwidth and metal layer requirement.

The next step was simulation of this device. For that purpose 54 trans-

formers with different number of rounds, different sizes and different metal wire widths were created using the AEL automation scripting language in the Agilent Technologies ADS suit which is both a circuit design tool and a very powerful electromagnetic simulation environment. The ADS simulator used defined silicon process layers to construct a 3-Dimensional model of the devices and then used electromagnetic equations and rules such as Lenz law, Maxwell equations and Biot-Savart law to calculate the electromagnetic effects of each conducting element on its surrounding. This lead to S-parameter files for each device and these files were used as references to calculate different parameters that define the properties of transformers.

These properties were collected for all samples and they were compared to one another to give us the information we need when we want to choose the right transformer for our circuits. In the end, the collected data showed what dimensions are needed for the transformers based on the required surface area, frequency range and coupling coefficient.

Bibliography

[1] R. Kumar, T. Krishnaswamy, G. Rajendran, D. Sahu, A. Sivadas, M. Nandigam, S. Ganeshan, S. Datla, A. Kudari, H. Bhasin, M. Agrawal, S. Narayan, Y. Dharwekar, R. Garg, V. Edayath, T. Suseela, V. Jayaram, S. Ram, V. Murugan, A. Kumar, S. Mukherjee, N. Dixit, E. Nussbaum, J. Dror, N. Ginzburg, A. EvenChen, A. Maruani, S. Sankaran, V. Srinivasan, and V. Rentala. A fully integrated 2×2 b/g and 1×2 a-band mimo wlan soc in 45nm cmos for multi-radio ic. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 328–329, Feb 2013.

[2] A.W.L. Ng, S.Y. Zheng, H. Leung, Y. Chao, and H.C. Luong. A 0.9ghz - 5.8ghz sdr receiver front-end with transformer-based current-gain boosting and 81-db 3rd-order-harmonic rejection ratio. In *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, pages 181–184, Sept 2013.

[3] V. Vidojkovic, V. Szortyka, K. Khalaf, G. Mangraviti, S. Brebels, W. Van Thillo, K. Vaesen, B. Parvais, V. Issakov, M. Libois, M. Matsuo, J. Long, C. Soens, and P. Wambacq. A low-power radio chipset in 40nm lp cmos with beamforming for 60ghz high-data-rate wireless communication. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 236–237, Feb 2013.

[4] I. Fabiano, M. Sosio, A. Liscidini, and R. Castello. Saw-less analog front-end receivers for TDD and FDD. *Solid-State Circuits, IEEE Journal of*, 48(12):3067–3079, Dec 2013.

[5] Dixian Zhao, S. Kulkarni, and P. Reynaert. A 60 ghz dual-mode power amplifier with 17.4 dbm output power and 29.3% pae in 40-nm cmos. In *ESSCIRC (ESSCIRC), 2012 Proceedings of the*, pages 337–340, Sept 2012.

[6] Wei Tai, Hongtao Xu, A. Ravi, H. Lakdawala, O. Bochobza-Degani, L.R. Carley, and Y. Palaskas. A transformer-combined 31.5 dbm outphasing

power amplifier in 45 nm lp cmos with dynamic power control for back-off power efficiency enhancement. *Solid-State Circuits, IEEE Journal of*, 47(7):1646–1658, July 2012.

[7] Kyu Hwan An, Younsuk Kim, Ockgoo Lee, Ki Seok Yang, Hyungwook Kim, Wangmyong Woo, Jae Joon Chang, Chang-Ho Lee, Haksun Kim, and J. Laskar. A monolithic voltage-boosting parallel-primary transformer structures for fully integrated cmos power amplifier design. In *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE*, pages 419–422, June 2007.

[8] Paulo Gomes. Monolithic power combiners in cmos technologies for wlan applications. Master's thesis, Instituto Superior Técnico, Universidade Técnica de Lisboa, 2011.

[9] E. Kaymaksut and P. Reynaert. Transformer-based uneven doherty power amplifier in 90 nm cmos for wlan applications. *Solid-State Circuits, IEEE Journal of*, 47(7):1659–1671, July 2012.

[10] Xiang Yi, Chirn Chye Boon, Jia Fu Lin, and Wei Meng Lim. A 100 ghz transformer-based varactor-less vco with 11.2% tuning range in 65nm cmos technology. In *ESSCIRC (ESSCIRC), 2012 Proceedings of the*, pages 293–296, Sept 2012.

[11] Zheng Wang, Pei-Yuan Chiang, P. Nazari, Chun-Cheng Wang, Zhiming Chen, and P. Heydari. A 210ghz fully integrated differential transceiver with fundamental-frequency vco in 32nm soi cmos. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 136–137, Feb 2013.

[12] E. Mammei, E. Monaco, A. Mazzanti, and F. Svelto. A 33.6-to-46.2ghz 32nm cmos vco with 177.5dbc/hz minimum noise fom using inductor splitting for tuning extension. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 350–351, Feb 2013.

[13] J.K. Brown, Kuo-Ken Huang, E. Ansari, R.R. Rogel, Yoonmyung Lee, and D.D. Wentzloff. An ultra-low-power 9.8ghz crystal-less uwb transceiver with digital baseband integrated in 0.18 um bicmos. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 442–443, Feb 2013.

[14] Fan Zhang, Keping Wang, Jabeom Koo, Y. Miyahara, and B. Otis. A 1.6mw 300mv-supply 2.4ghz receiver with -94dbm sensitivity for energy-harvesting applications. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 456–457, Feb 2013.

[15] Liang Wu and H.C. Luong. A 49-to-62ghz cmos quadrature vco with bimodal enhanced magnetic tuning. In *ESSCIRC (ESSCIRC), 2012 Proceedings of the*, pages 297–300, Sept 2012.

[16] J.W.M. Rogers and C. Plett. A 5-ghz radio front-end with automatically q-tuned notch filter and vco. *Solid-State Circuits, IEEE Journal of*, 38(9):1547–1554, Sept 2003.

[17] Xiaoyong Li, S. Shekhar, and D.J. Allstot. Gm-boosted common-gate lna and differential colpitts vco/qvco in 0.18- mu;m cmos. *Solid-State Circuits, IEEE Journal of*, 40(12):2609–2619, Dec 2005.

[18] M. Stmayer, J. Cabanillas, and G.M. Rebeiz. A low-noise transformer-based 1.7ghz cmos vco. In *Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International*, volume 2, pages 224–484, Feb 2002.

[19] A. Borna, C. Hull, Yanjie Wang, Hua Wang, and A. Niknejad. An RF receiver with an integrated adaptive notch filter for multi-standard applications. In *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, pages 185–188, Sept 2013.

[20] Jong-Pil Im, Se-Won Wang, Seung-Tak Ryu, and Gyu-Hyeong Cho. A 40 mv transformer-reuse self-startup boost converter with mppt control for thermoelectric energy harvesting. *Solid-State Circuits, IEEE Journal of*, 47(12):3055–3067, Dec 2012.

[21] Rongxiang Wu, J.K.O. Sin, and S.Y. Hui. Novel silicon-embedded coreless transformer for on-chip isolated signal transfer. *Magnetics Letters, IEEE*, 2:6500103–6500103, 2011.

[22] A.H. Aly, D.W. Beishline, and Badawy El-Sharawy. Filter integration using on-chip transformers. In *Microwave Symposium Digest, 2004 IEEE MTT-S International*, volume 3, pages 1975–1978 Vol.3, June 2004.

[23] David K. Cheng. *Field and Wave Electromagnetics*. Addison-Wesley Publishing Company, 2nd edition, 1989. Chapters 6, 7 and 8.

[24] R.C. Frye, Y.T. Lee, H.T. Kim, and Kai Liu. Compact monolithic low-pass filters using a bridged-tee architecture. In *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*, pages 1–4, June 2011.

[25] Heng-Ming Hsu, Szu-Han Lai, and Chan-Juan Hsu. Compact layout of on-chip transformer. *Electron Devices, IEEE Transactions on*, 57(5):1076–1083, May 2010.

[26] Chee-Chong Lim, Kiat-Seng Yeo, Kok-Wai Chew, Suh-Fei Lim, Chirn Chye Boon, Qiu-ping, A.V. Do, and Lap Chan. An area efficient high turn ratio monolithic transformer for silicon rfic. In *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, pages 167–170, June 2008.

[27] Ockgoo Lee, Kyu Hwan An, Chang-Ho Lee, and J. Laskar. A parallel-segmented monolithic step-up transformer. *Microwave and Wireless Components Letters, IEEE*, 21(9):468–470, Sept 2011.

[28] Sami Franssila. *Introduction to Microfabrication, 2nd Edition*. Wiley, 2010. Chapter 17.

[29] Kiat T. Ng, Behzad Rejaei, and J.N. Burghartz. Substrate effects in monolithic RF transformers on Silicon. *Microwave Theory and Techniques, IEEE Transactions on*, 50(1):377–383, Jan 2002.

[30] Jinglin Shi, Wen-Yan Yin, Kai Kang, Jun-Fa Mao, and Le-Wei Li. Frequency-thermal characterization of on-chip transformers with patterned ground shields. *Microwave Theory and Techniques, IEEE Transactions on*, 55(1):1–12, Jan 2007.

[31] O. El-Gharniti, E. Kerherve, and J-B Begueret. Characterization of si-based monolithic transformers with patterned ground shield. In *Radio Frequency Integrated Circuits (RFIC) Symposium, 2006 IEEE*, pages 4 pp.–, June 2006.

[32] Sunderarajan S. Mohan. *The Design, Modeling And Optimization Of On-chip Inductor And Transformer Circuits*. PhD thesis, Stanford University Department Of Electrical Engineering, 1999.

Appendix A

AEL Script

The devices in this thesis where designed and simulated in the ADS software package provided by Agilent Technologies. ADS includes an automation system that utilizes functions and operators in script file. The script follows a syntax logic called Application Extension Language (AEL).

Structure of AEL scripts

There are double crossing structures used in the design of transformers in this thesis that connect the loops of spirals. Since each double cross is connected to four loops and the ports could be connected to each two consequent loops, total number of turns imposes different placement for ports. This difference is based on the remainder of the division of NT by 4. This has been discussed in Section 4.1 in more detail.

In total, four different scripts were generated to design, draw and generate the layouts of transformers. They are in most aspects similar. They are named as "t[X].ael", where [X] is the the remainder of the division of NT by 4. Here, only one of these files is attached and it is the "t0.ael" file which is intended for the cases where $NT = 4 \times k$. The rest of the files are available for researchers at the Department of Micro- and Nanosciences at Aalto University's School of Electrical Engineering.

```
/*
This file was made by "Saman Bahrampoor" for the ECD Group of
the Department of Micro- and Nanosciences at Aalto University, School of Electrical Engineering

The purpose of this AEL script is to define and draw
octagonal symmetrical interleaved transformers.
This file is intented for transformers in which "N_S=N_P and N_S+N_P=4*k"
where "k" is a natural number.

The program is operated as follows:
```

```
1) in ADS main window choose Tools / command line
2) write command : load("/home/[USER'S PROJECT PATH]/t0.ael")
3) write command : Octasymm(NT,Din,W,S,filename)
   NT is the total number of turns (N_S + N_P)
   Din is the width of the inner opening
   W is the stripe width
   S is the stripe spacing
Example: Octasymm(3,60,10,10,"FirstCoil")
All dimensions are micrometers (um).
*/

//***************************GLOBAL VARIABLES*****************************

decl inDiameter;
decl lWidth
decl wInc=0;
decl S;
decl numOfRounds;
decl saveFileName;
decl x1=0,y1=0,x2=0,y2=0,x3=0,y3=0,x4=0,y4=0;
decl h1=0,j1=0,h2=0,j2=0,h3=0,j3=0,h4=0,j4=0;
decl Lw,Ll,Ls;
decl currentLap=0;
decl loop=0;

decl upperlayer=6;  // the gds index value of the upper metal layer
decl vialayer=5;    // the gds index value of the via layer
decl lowerlayer=4;  // the gds index value of the lower metal layer


//***************************END Of GLOBAL VARIABLES**********************
//************************************************************************
//***************************BEGINNING OF THE PROGRAMM********************

defun drawMyPolygon(m1,n1,m2,n2,m3,n3,m4,n4)
{
       de_add_polygon();
       de_add_point(m1,n1);
       de_add_point(m2,n2);
       de_add_point(m3,n3);
       de_add_point(m4,n4);
       de_end();

       return;
}

/*
This function draws the actual coil shape without crossings
and end terminals.
First, the coordinates of one corner are calculated and
thereafter all the rest coordinates
can be defined from that (for a single round)
*/

defun drawBody()
{

       if(currentLap==0)
       {
              x1=Ll+currentLap*(Lw+Ls);
              y1=round(inDiameter/2)+currentLap*(lWidth+S);
       }
```

```
	x2=x1+Lw;
	y2=y1+lWidth;

	x3=y2;
	y3=x2;

	x4=y1;
	y4=x1;

	if(currentLap==0)		//The shape drawn for the first round
		drawMyPolygon(x1,y1,x2,y2,-x2,y2,-x1,y1);
	if(currentLap==1)		//The shape drawn for the 2nd round
		drawMyPolygon(x1,y1,x2,y2,-x2,y2,-x1,y1);

	drawMyPolygon(x1,y1,x2,y2,x3,y3,x4,y4);		// top-right corner cut
	drawMyPolygon(x4,-y4,x3,-y3,x3,y3,x4,y4);	  // right side
	drawMyPolygon(x1,-y1,x2,-y2,x3,-y3,x4,-y4);	    // bottom-right corner cut

	drawMyPolygon(-x1,y1,-x2,y2,-x3,y3,-x4,y4);	   // top-left corner cut
	drawMyPolygon(-x4,-y4,-x3,-y3,-x3,y3,-x4,y4);	     // left side
	drawMyPolygon(-x1,-y1,-x2,-y2,-x3,-y3,-x4,-y4); // bottom-left corner cut


	return;
}

defun drawCross()
{

	decl min=0,help=0,isneg=0,equalx,equaly,cont=0,bulk=round(lWidth/2);
	decl a1,a2,b1,b2;

	min=S/2+lWidth*tan(rad(22.5))/sqrt(2);
	help=round(min)-min;
	isneg=cos(currentLap*PI+PI);

	if(help<0)
		min=round(min)+1;
	else min=round(min);

	h1=min;
	j1=(y1*isneg);

	h2=h1+Lw;
	j2=j1+(lWidth)*cos(currentLap*PI+PI);

	h3=-h1-wInc;
	j3=j1+(2*lWidth+S+wInc)*cos(currentLap*PI+PI);

	h4=-h2;
	j4=j2+S*cos(currentLap*PI+PI);


	// This while-loop ensures that crossing is at 45 degree angle,
	//              that is:  equalx=equaly

	while(cont<=1)
	{

		equalx=abs(h4-h1);
		equaly=abs(j4-j1);
```

```
            if(equalx<equaly)
                    h1++;
            if(equalx>equaly)
                    h1--;
            cont++;
        }

        h1=x1-(x2-h2);
        h2=abs(equaly)-h1;
        h3=h2-abs(j2-j3);
        h4=h1-abs(j1-j4);

        lWidth=lWidth+wInc;
        Lw=round(lWidth*tan(rad(22.5)));

        a1=x2+Ls; a2=a1+Lw;
        b1=isneg*(y2+S); b2=b1+isneg*lWidth;


if (currentLap<numOfRounds-1){
if ( (currentLap>=0) && (isneg<0) && ((4*round(loop/4))==loop) )
        {
        drawMyPolygon(h1+bulk+(lWidth+S)/2,j1+(lWidth+S)*isneg,
                h2+bulk+(lWidth+S)/2,j2+(lWidth+S)*isneg,
                h3-(lWidth+S)/2,j3+2*(lWidth+S)*isneg,
                h4-(lWidth+S)/2,j4+2*(lWidth+S)*isneg);       //cross
        drawMyPolygon(h1+bulk+(lWidth+S)/2,j1,h2+bulk+(lWidth+S)/2,j2,
                h3-(lWidth+S)/2,j3+(lWidth+S)*isneg,h4-(lWidth+S)/2,
                j4+(lWidth+S)*isneg);       //cross
        drawMyPolygon(h2+(lWidth+S)/2,j1,h2+(lWidth+S)/2,j2,
                x2,isneg*y2,x1,isneg*y1);                     //
        drawMyPolygon(-h2-(lWidth+S)/2,j1,-h2-(lWidth+S)/2+bulk,j2
                ,-x2,isneg*y2,-x1,isneg*y1);

//        a1=x2+Ls; a2=a1+Lw;
//        b1=isneg*(y2+S); b2=b1+isneg*lWidth;

        drawMyPolygon(h2+(lWidth+S)/2,j4,h2+bulk+(lWidth+S)/2,j3,a2,b2,a1,b1);
        drawMyPolygon(h4-(lWidth+S)/2,j4,h3-(lWidth+S)/2,j3,-a2,b2,-a1,b1);                                    //
        drawMyPolygon(h4-(lWidth+S)/2,j4+(lWidth+S)*isneg,h3-(lWidth+S)/2,
                j3+(lWidth+S)*isneg,-a2-min,b2+(lWidth+S)*isneg,
                -a1-2*min,b1+(lWidth+S)*isneg);
        drawMyPolygon(-h4+(lWidth+S)/2,j4+(lWidth+S)*isneg,-h3+(lWidth+S)/2,
                j3+(lWidth+S)*isneg,a2+min,b2+(lWidth+S)*isneg,
                a1+2*min,b1+(lWidth+S)*isneg);

        if (currentLap>2) {
        drawMyPolygon(h2+(lWidth+S)/2,j4-2*(lWidth+S)*isneg,h2+bulk+(lWidth+S)/2,
                j3-2*(lWidth+S)*isneg,a2-2*min,b2-2*(lWidth+S)*isneg,
                a1-min,b1-2*(lWidth+S)*isneg);                              //
        drawMyPolygon(h4-(lWidth+S)/2,j4-2*(lWidth+S)*isneg,h3-(lWidth+S)/2,
                j3-2*(lWidth+S)*isneg,-a2+2*min,b2-2*(lWidth+S)*isneg,
                -a1+min,b1-2*(lWidth+S)*isneg);
        }

        de_set_layer(vialayer);
        drawMyPolygon(h2+(lWidth+S)/2,j4+(lWidth+S)*isneg,h2+(lWidth+S)/2,
                j3+(lWidth+S)*isneg,h2+bulk+(lWidth+S)/2,j3+(lWidth+S)*isneg,
                h2+bulk+(lWidth+S)/2,j4+(lWidth+S)*isneg);
        drawMyPolygon(h4-(lWidth+S)/2,j1,h4-(lWidth+S)/2,j2,
                h4-bulk-(lWidth+S)/2,j2,h4-bulk-(lWidth+S)/2,j1);
```

```
        drawMyPolygon(h2+(lWidth+S)/2,j4+2*(lWidth+S)*isneg,h2+(lWidth+S)/2,
               j3+2*(lWidth+S)*isneg,h2+bulk+(lWidth+S)/2,j3+2*(lWidth+S)*isneg,
               h2+bulk+(lWidth+S)/2,j4+2*(lWidth+S)*isneg);
        drawMyPolygon(h4-(lWidth+S)/2,j1+(lWidth+S)*isneg,h4-(lWidth+S)/2,
               j2+(lWidth+S)*isneg,h4-bulk-(lWidth+S)/2,j2+(lWidth+S)*isneg,
               h4-bulk-(lWidth+S)/2,j1+(lWidth+S)*isneg);


        de_set_layer(lowerlayer);
        drawMyPolygon(h2+(lWidth+S)/2,j4+(lWidth+S)*isneg,-h3+(lWidth+S)/2,
               j3+(lWidth+S)*isneg,h2+bulk+(lWidth+S)/2,j3+(lWidth+S)*isneg,
               h2+bulk+(lWidth+S)/2,j4+(lWidth+S)*isneg);
        drawMyPolygon(h2+(lWidth+S)/2,j4+2*(lWidth+S)*isneg,-h3+(lWidth+S)/2,
               j3+2*(lWidth+S)*isneg,h2+bulk+(lWidth+S)/2,j3+2*(lWidth+S)*isneg,
               h2+bulk+(lWidth+S)/2,j4+2*(lWidth+S)*isneg);

        drawMyPolygon(-h1-(lWidth+S)/2,j1,h4-(lWidth+S)/2,
               j2,h4-bulk-(lWidth+S)/2,j2,h4-bulk-(lWidth+S)/2,j1);
        drawMyPolygon(-h1-(lWidth+S)/2,j1+(lWidth+S)*isneg,h4-(lWidth+S)/2,
               j2+(lWidth+S)*isneg,h4-bulk-(lWidth+S)/2,j2+(lWidth+S)*isneg,
               h4-bulk-(lWidth+S)/2,j1+(lWidth+S)*isneg);

        drawMyPolygon(-h1-(lWidth+S)/2,j1+(lWidth+S)*isneg,h4-(lWidth+S)/2,
               j2+(lWidth+S)*isneg,-h3+(lWidth+S)/2,j3+2*(lWidth+S)*isneg,
               h2+(lWidth+S)/2,j4+2*(lWidth+S)*isneg);
        drawMyPolygon(-h1-(lWidth+S)/2,j1,h4-(lWidth+S)/2,j2,-h3+(lWidth+S)/2,
               j3+(lWidth+S)*isneg,h2+(lWidth+S)/2,j4+(lWidth+S)*isneg);
}


if ( ((currentLap>1) && (isneg>0)) && ((loop-4*int(loop/4))==3 ) )
        {
        drawMyPolygon(h1+bulk+(lWidth+S)/2,j1-(lWidth+S)*isneg,h2+bulk+(lWidth+S)/2,
               j2-(lWidth+S)*isneg,h3-(lWidth+S)/2,
               j3,h4-(lWidth+S)/2,j4);       //cross
        drawMyPolygon(h1+bulk+(lWidth+S)/2,j1,h2+bulk+(lWidth+S)/2,
               j2,h3-(lWidth+S)/2,j3+(lWidth+S)*isneg,
               h4-(lWidth+S)/2,j4+(lWidth+S)*isneg);       //cross
        drawMyPolygon(h2+(lWidth+S)/2,j1,h2+(lWidth+S)/2,
               j2,x2,isneg*y2,x1,isneg*y1);                      //
        drawMyPolygon(-h2-(lWidth+S)/2,j1,-h2-(lWidth+S)/2+bulk,j2
               ,-x2,isneg*y2,-x1,isneg*y1);


        a1=x2+Ls; a2=a1+Lw;
        b1=isneg*(y2+S); b2=b1+isneg*lWidth;

        drawMyPolygon(h2+(lWidth+S)/2,j4,h2+(lWidth+S)/2,j3,a2,b2,a1,b1);
        drawMyPolygon(h4-(lWidth+S)/2,j4,h3-(lWidth+S)/2,j3,-a2,b2,-a1,b1);
        drawMyPolygon(h2+(lWidth+S)/2,j4-2*(lWidth+S),h2+bulk+(lWidth+S)/2,
               j3-2*(lWidth+S),a2-2*min,b2-2*(lWidth+S),a1-min,b1-2*(lWidth+S));                    //
        drawMyPolygon(h4-(lWidth+S)/2,j4-2*(lWidth+S),h3-(lWidth+S)/2,
               j3-2*(lWidth+S),-a2+2*min,b2-2*(lWidth+S),-a1+min,b1-2*(lWidth+S));
        drawMyPolygon(h4-(lWidth+S)/2,j4+(lWidth+S),h3-(lWidth+S)/2,
               j3+(lWidth+S),-a2-min,b2+(lWidth+S),-a1-2*min,b1+(lWidth+S));
        drawMyPolygon(-h4+(lWidth+S)/2,j4+(lWidth+S),-h3+(lWidth+S)/2,
               j3+(lWidth+S),a2+min,b2+(lWidth+S),a1+2*min,b1+(lWidth+S));

        de_set_layer(vialayer);
        drawMyPolygon(h2+(lWidth+S)/2,j4+(lWidth+S)*isneg,h2+(lWidth+S)/2,
               j3+(lWidth+S)*isneg,h2+bulk+(lWidth+S)/2,j3+(lWidth+S)*isneg,
```

```
                h2+bulk+(lWidth+S)/2,j4+(lWidth+S)*isneg);
        drawMyPolygon(h4-(lWidth+S)/2,j1,h4-(lWidth+S)/2,
                j2,h4-bulk-(lWidth+S)/2,j2,h4-bulk-(lWidth+S)/2,j1);

        drawMyPolygon(h2+(lWidth+S)/2,j4,h2+(lWidth+S)/2,j3,
                h2+bulk+(lWidth+S)/2,j3,h2+bulk+(lWidth+S)/2,j4);
        drawMyPolygon(h4-(lWidth+S)/2,j1-(lWidth+S)*isneg,h4-(lWidth+S)/2,
                j2-(lWidth+S)*isneg,h4-bulk-(lWidth+S)/2,j2-(lWidth+S)*isneg,
                h4-bulk-(lWidth+S)/2,j1-(lWidth+S)*isneg);



        de_set_layer(lowerlayer);
        drawMyPolygon(h2+(lWidth+S)/2,j4+(lWidth+S)*isneg,-h3+(lWidth+S)/2,
                j3+(lWidth+S)*isneg,h2+bulk+(lWidth+S)/2,j3+(lWidth+S)*isneg,
                h2+bulk+(lWidth+S)/2,j4+(lWidth+S)*isneg);
        drawMyPolygon(h2+(lWidth+S)/2,j4,-h3+(lWidth+S)/2,j3,
                h2+bulk+(lWidth+S)/2,j3,h2+bulk+(lWidth+S)/2,j4);

        drawMyPolygon(-h1-(lWidth+S)/2,j1,h4-(lWidth+S)/2,j2,
                h4-bulk-(lWidth+S)/2,j2,h4-bulk-(lWidth+S)/2,j1);
        drawMyPolygon(-h1-(lWidth+S)/2,j1-(lWidth+S)*isneg,
                h4-(lWidth+S)/2,j2-(lWidth+S)*isneg,h4-bulk-(lWidth+S)/2,
                j2-(lWidth+S)*isneg,h4-bulk-(lWidth+S)/2,j1-(lWidth+S)*isneg);

        drawMyPolygon(-h1-(lWidth+S)/2,j1-(lWidth+S)*isneg,h4-(lWidth+S)/2,
                j2-(lWidth+S)*isneg,-h3+(lWidth+S)/2,j3,h2+(lWidth+S)/2,j4);
        drawMyPolygon(-h1-(lWidth+S)/2,j1,h4-(lWidth+S)/2,j2,
        -h3+(lWidth+S)/2,j3+(lWidth+S)*isneg,h2+(lWidth+S)/2,j4+(lWidth+S)*isneg);
}
}
if (currentLap==numOfRounds-1){

        drawMyPolygon(a1-(lWidth+S)/2+bulk/2,j1,a1-(lWidth+S)/2+bulk,j2,
                h2+(lWidth+S)/2,j3-(lWidth+S)*isneg,h2+(lWidth+S)/2,
                j4-(lWidth+S)*isneg);
        drawMyPolygon(-a1+(lWidth+S)/2-bulk/2,j1,-a1+(lWidth+S)/2-bulk,j2,
                -h2-(lWidth+S)/2+bulk,j3-(lWidth+S)*isneg,
                -h2-(lWidth+S)/2,j4-(lWidth+S)*isneg);



}
        de_set_layer(upperlayer);
        x1=x2+Ls; y1=y2+S;
        return;
}

defun drawBranch()
{
        decl min=S/2+lWidth*tan(rad(22.5))/sqrt(2);
        decl help=round(min)-min;
        decl isneg=cos(currentLap*PI+PI);

        if(help<0)
                min=round(min)+1;
        else min=round(min);

        decl h1=min;
        decl j1=(y1*isneg);

        decl h2=h1+Lw;
```

```
        decl j2=j1+(lWidth)*cos(currentLap*PI+PI);

        decl h3=-h1-wInc;
        decl j3=j1+(2*lWidth+S+wInc)*cos(currentLap*PI+PI);

        decl h4=-h2;
        decl j4=j2+S*cos(currentLap*PI+PI);


        decl bulk=round(lWidth/2);
        decl myPort1,myPort2;
//        isneg=cos(currentLap*PI+PI);

        decl a1,a2,a3,a4,b1,b2,b3,b4;

        a1=x1;                b1=isneg*y1;
        a2=a1+lWidth;         b2=b1;
        a3=a2;               b3=b1+isneg*3*lWidth;
        a4=a1;               b4=b3;

//        drawMyPolygon(a1,b1,a2,b2,a3,b3,a4,b4);
//        drawMyPolygon(-a1,b1,-a2,b2,-a3,b3,-a4,b4);

        drawMyPolygon(a1+bulk-(lWidth+S)/2,-b1,a2+bulk-(lWidth+S)/2,
               -b2,a3+bulk-(lWidth+S)/2,-b3-(lWidth+S)*isneg,
               a4+bulk-(lWidth+S)/2,-b4-(lWidth+S)*isneg);
        drawMyPolygon(-a1-bulk+(lWidth+S)/2,-b1,-a2-bulk+(lWidth+S)/2,
               -b2,-a3-bulk+(lWidth+S)/2,-b3-(lWidth+S)*isneg,
               -a4-bulk+(lWidth+S)/2,-b4-(lWidth+S)*isneg);

        drawMyPolygon(h2 +(lWidth+S)/2, -j4-1.5*(lWidth+S)*isneg ,
               h2+(lWidth+S),-j4-1.5*(lWidth+S)*isneg,h2+(lWidth+S)
               ,-j4+2*(lWidth+S)*isneg,h2+(lWidth+S)/2, -j4+2*(lWidth+S)*isneg);
        drawMyPolygon(-h2 , -j4-1.5*(lWidth+S)*isneg , -h2-(lWidth+S)/2 ,
               -j4-1.5*(lWidth+S)*isneg , -h2-(lWidth+S)/2 ,
               -j4+2*(lWidth+S)*isneg , -h2,-j4+2*(lWidth+S)*isneg);

        drawMyPolygon(h2 +(lWidth+S)/2, -j4+2*(lWidth+S)*isneg+lWidth ,
               a3-(lWidth+S)/2-bulk , -j4+2*(lWidth+S)*isneg+lWidth ,
               a3-(lWidth+S)/2-bulk,
               -j4+2*(lWidth+S)*isneg , h2+(lWidth+S)/2, -j4+2*(lWidth+S)*isneg);
        drawMyPolygon(-h2 -(lWidth+S)/2, -j4+2*(lWidth+S)*isneg+lWidth ,
               -a3+(lWidth+S)/2+bulk , -j4+2*(lWidth+S)*isneg+lWidth ,
               -a3+(lWidth+S)/2+bulk  , -j4+2*(lWidth+S)*isneg ,
               -h2-(lWidth+S)/2, -j4+2*(lWidth+S)*isneg);


db_create_pin_cc( (a1+a2)/2-bulk,-b3-(lWidth+S)*isneg);
db_create_pin_cc( -(a1+a2)/2+bulk,-b3-(lWidth+S)*isneg);

db_create_pin_cc( h2+3*(lWidth+S)/4, -j4-1.5*(lWidth+S)*isneg);
db_create_pin_cc( -h2-(lWidth+S)/4, -j4-1.5*(lWidth+S)*isneg);
        return;
}



//     ************** MAIN FUNCTION *********************************

defun Octasymm(laps,mDiameter,mWidth,mGap,saveFileName)
{
```

```
       x1=0;y1=0;x2=0;y2=0;x3=0;y3=0;x4=0;y4=0;
       h1=0;j1=0;h2=0;j2=0;h3=0;j3=0;h4=0;j4=0;
       currentLap=0;

/*       if(saveName!=NULL)
              saveFileName=saveName;*/

       api_set_current_window_by_seq_num(2);
       de_select_all();
       de_delete();
       api_set_current_window_by_seq_num(2);

       de_set_preference(GRID_SNAP_X_P,1);
       de_set_preference(GRID_SNAP_Y_P,1);
       de_set_preference(GRID_DISPLAY_X_P,1);
       de_set_preference(GRID_DISPLAY_Y_P,1);
       de_set_preference(MAJOR_GRID_DISPLAY_P,1);
       de_set_preference(MAJOR_GRID_DISPLAY_X_P,1);
       de_set_preference(MAJOR_GRID_DISPLAY_Y_P,1);

       load("destdart");
       if(mDiameter != NULL)
               inDiameter=mDiameter;
       if(mWidth != NULL)
              lWidth=mWidth;
       if(mGap != NULL)
              S=mGap;
       if(inc != NULL)
              wInc=inc;
       if(laps != NULL)
              numOfRounds=laps;

       Ll=round(inDiameter/2*tan(rad(22.5)));
       Lw=round(lWidth*tan(rad(22.5)));
       Ls=tan(rad(22.5))*S;

       decl vs=round(Ls)-Ls;
       if(vs<0)
              Ls=round(Ls)+1;
       else Ls=round(Ls);

       currentLap=0;
       de_set_layer(upperlayer);
//       de_change_units(3,3,1);
//       decl loop=0;
numOfRounds++;
       while(loop<numOfRounds)
       {


              drawBody();    // This draws one loop at a time


              if(loop==(numOfRounds-1))       drawBranch();
              if(loop==(numOfRounds-2));//        drawBranch();
              else drawCross();

              currentLap=currentLap+1;
              loop++;
```

```
       }

       de_view_all();

//       Now the coil layout is ready
//       Next operation saves the design with a given name
//      variable "saveFileName" is given in the command line prompt


 decl WanhaContext  = de_get_current_design_context();

 decl UusContext = de_create_new_layout_view("USER_LIB",
        saveFileName,"layout");
 //Replace USER_LIB with the name of your own design library

        db_copy_context(WanhaContext, UusContext);

        db_save_design_without_prompting(UusContext);

       return;

}
```