Sparsification of Dense Capacitive Coupling of Interconnect Models

Pekka Miettinen, Mikko Honkala, Janne Roos, and Martti Valtonen

***Abstract*—Parasitic elements play a major role in advanced circuit design and pose considerable run-time and memory problems for the post-layout verification, especially in the case of full-chip extraction. This paper presents a realizable RC(LM)-netlist-in–RC(LM)-netlist-out method to sparsify and reduce the capacitive coupling parasitics in circuits with interconnect lines. The method is applicable in conjunction with partitioning-based model-order reduction algorithms to reduce the complete extracted netlists, or as a stand-alone tool to process only the capacitive coupling. It is shown that by using the method, circuits with even dense capacitive coupling can be partitioned and reduced efficiently.**

***Index Terms*—Circuit simulation, interconnect modeling, capacitive coupling, model-order reduction.**

I. Introduction

WITH advancing technology nodes of integrated circuits (ICs), the interconnects between active elements and their non-ideal parasitics play an increasingly important role for the signal behavior. In a typical design flow, extraction tools are used to generate a circuit netlist from the original chip topology for the post-layout verification. To reach desired accuracy, the interconnects and their parasitics need to be modeled with high precision that generates huge RC(LM) netlists, which in turn poses significant run-time and memory problems for the design process. One avenue to speed up the verification step is to apply model-order reduction (MOR) algorithms, (see, e.g., [1] for review) to the extracted netlists, attempting to model the system with a reduced-size representation.

Partitioning is often a desirable feature in MOR methods [2]–[5]. By using partitioning, the original problem can be naturally divided into smaller parts that can be processed separately. This provides a reduction algorithm numerous benefits, such as block-level sparsity, economical memory use, natural parallel processing, and facilitated port handling. In case of very large circuits (e.g., more than 10^8 elements), processing a circuit without prior partitioning may be impossible for many computers due to limiting memory resources.

Unfortunately, partitioning and reduction is problematic if the circuit has considerable coupling or mesh-like structures, such as in Fig. 1(a). If such a circuit is partitioned into subcircuits, the resulting subcircuits typically have a high number of port nodes that connect one subcircuit to other subcircuits. MOR methods can not reduce these nodes easily, since the behavior at each port needs to be communicated somehow to each other port, and with large number of ports the resulting reduced-order model (ROM) becomes large and inefficient. The topic of this paper is to tackle the problem of partitioning and efficient reduction in the case of dense capacitive coupling between interconnects.

For interconnect circuits, parasitic coupling is often the reason for mesh-like structures, and takes form as mutual capacitive and inductive coupling between the interconnect lines. In addition to the often problematic partitioning, tight mesh-like coupling creates denser system matrices, which slows down the MOR process, even if a suitable partitioning can be generated.

The basic idea of the method proposed is to approximate the original circuit with a two-stage reduction. First, the original circuit is considered without the capacitive coupling (i.e., as separate interconnect runs) and partitioned into subcircuits. The subcircuits may be reduced using a pre-existing MOR method of choice (e.g., [2]–[7]). Then, each pair of subcircuits is considered again — this time including the capacitive coupling between the subcircuits — and the coupling effect is reduced separately. Since the latter reduction is realized with positive-valued (R)C macromodels, the method is also easily integratable to existing realizable RC(LM)-in–RC(LM)-out MOR methods.

The benefits of the method are that the netlist partitioning can be easily done, allowing efficient MOR; that even dense capacitive coupling does not generate a dense system matrices for the MOR; and finally that the capacitive coupling is reduced to positive-valued (R)C-macromodels of few elements.

For RLCM-circuits, also the inductive coupling is an important factor to the circuit's signal behavior. Densely coupled mutual inductances can be sparsified in some applications using, e.g., [8], or sparsified and reduced in a manner similar to the method proposed in this paper using [9]. Although the presented method is not directly applicable to reduction of inductive coupling, it facilitates RLCM-circuit reduction in the case of dense capacitive coupling similarly as in the case of RC(L)-circuits. If an RLCM-circuit contains heavy capacitive coupling, it may be impossible to partition and reduce the system efficiently without augmentative methods.

The paper is organized as follows. In Section II, the generation of y-parameter moments from circuit equations, as in [6], is briefly reviewed. Partitioning and further reduction of capacitive coupling by low-order moment-matching is described in Section III. Verification simulation results and conclusions are given in Sections IV and V, respectively.

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II. Circuit equations

Using voltage sources at the ports, the modified nodal analysis (MNA) circuit equations for a linear N-port are [6]:

$$\begin{cases} \mathbf{C}\dfrac{\mathrm{d}\mathbf{x}(t)}{\mathrm{d}t} = -\mathbf{G}\mathbf{x}(t) + \mathbf{B}\mathbf{u}_N(t), \\ \mathbf{i}_N(t) = \mathbf{L}^{\mathrm{T}}\mathbf{x}(t), \end{cases} \tag{1}$$

where $\mathbf{C}$ and $\mathbf{G}$ are the susceptance and conductance matrices, respectively, and $\mathbf{x}$, $\mathbf{u}_N$, and $\mathbf{i}_N$ denote the MNA variables (nodal voltages, and branch currents of inductances and voltage sources), port voltages, and port currents, respectively. Here, $\mathbf{B} = \mathbf{L}$ is a selector matrix consisting of ones, minus ones, and zeros.

The y-parameters can be determined by taking Laplace transformation of (1), and solving for port currents, which results in

$$\mathbf{Y}(s) = \mathbf{L}^{\mathrm{T}}(\mathbf{I} - s\mathbf{A})^{-1}\mathbf{R}, \tag{2}$$

where $\mathbf{A} \equiv -\mathbf{G}^{-1}\mathbf{C}$ and $\mathbf{R} \equiv \mathbf{G}^{-1}\mathbf{B}$. The term $(\mathbf{I} - s\mathbf{A})^{-1}$ can be expanded into a Neumann series to obtain y-parameter moments generated with respect to $s = 0$

$$\mathbf{Y}(s) = \mathbf{M}_0 + \mathbf{M}_1 s + \mathbf{M}_2 s^2 + \cdots, \tag{3}$$

where the block moments, $\mathbf{M}_i = \mathbf{L}^{\mathrm{T}}\mathbf{A}^i\mathbf{R}$, have the dimension $N \times N$. Note that $\mathbf{Y}(0) = \mathbf{M}_0$, i.e., the zeroth moment and describes the DC behavior exactly.

III. Sparsification method

The concept of the sparsification method is presented in Fig. 1. The complete algorithm is described in Fig. 2.

A. Partitioning and main branch reduction

Consider an RC interconnect circuit containing capacitive coupling between the interconnects in Fig. 1(a). First, only the interconnect main branches without the capacitive coupling are processed. The main branches are partitioned into subcircuits (e.g., between nodes (a, b) and (c, d)), such that the capacitive coupling between the interconnects (as shown with dashed lines) is not taken into account when generating the partitions.

In this paper, the partitioning process is done by considering the circuit at DC, where the capacitances and inductances of the interconnects are reduced to open and short circuits, respectively, and the partitioning is thus done only for the separate main branches of the interconnects. The partitioning is performed using hMETIS partitioning algorithm package [10] after generating a hypergraph description of the circuit. This approach is fully applicable only if the interconnects do not have heavy conductive coupling between the lines, in which case additional heuristics are required to distinguish the interconnect branches.

Using a MOR method of choice, e.g., [2]–[6], a ROM is generated using the expansion point $s_0 = 0$ for these subcircuits (i.e., sections of the interconnect main branches). In Fig. 1(c), these models are shown for the reduced y-parameters y^{ab}_{red} and y^{cd}_{red} of the interconnect main branches. The same is repeated for the admittances at the ports $a, \ldots, d$ (e.g., y^{aa}_{red}).

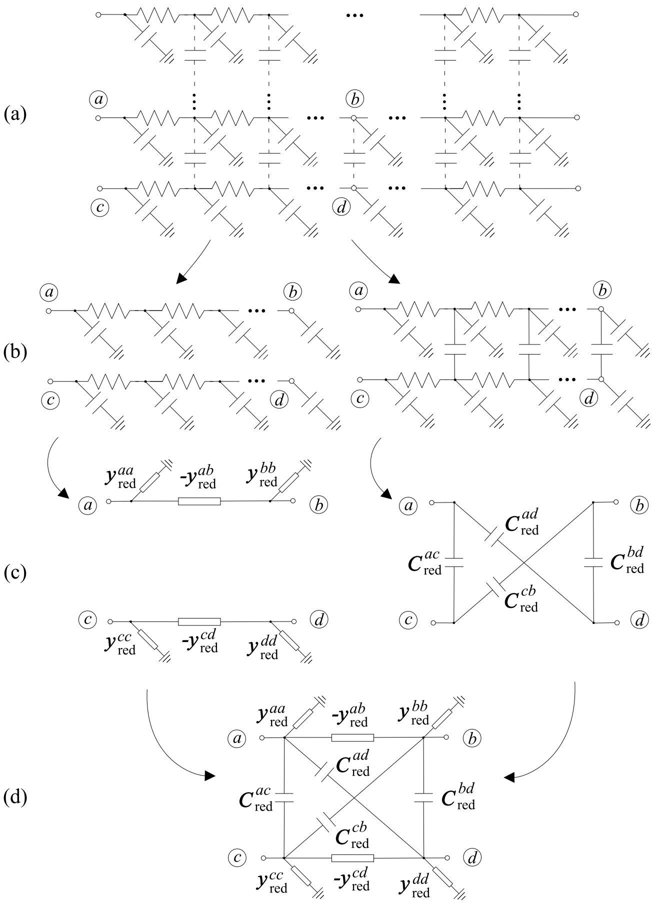

Fig. 1. The reduction method applied in a grid-like RC circuit. (a) The circuit is partitioned into subcircuits of interconnect main branches without capacitive coupling (which is shown with dashed lines), e.g., branches (a,b) and (c,d). (b-c) The main branches are reduced without the coupling, using a MOR method of choice. The capacitive coupling is reduced separately by considering the branches pair-wise, using the low-order approximation presented in Sec. III-B. (c-d) The reduction for the main branches (e.g., y^{ab}_{red}) is combined with the reduction of the coupling (e.g., C^{ac}_{red}). The process is repeated for each main branch and pair of branches that have capacitive coupling.

B. Capacitive coupling reduction

After the reduction of the interconnect main branches, the capacitive coupling is reduced separately. The capacitive coupling between two subcircuits is approximated by considering each pair of subcircuits as a separate 4-port circuit, where the original capacitive coupling between the two subcircuits is re-introduced, e.g., as shown for branches (a, b) and (c, d) in Fig. 1(b). Now, the capacitive coupling between the two lines can be expressed with y-parameters calculated for the 4-port. Using Eqs. (1)–(3), the y-parameter block moments are generated at $s = 0$, and a connection between two ports is approximated using the first two moments (given here for a general y-parameter matrix element (i, j)):

$$\begin{aligned} y^{ij}(s) &= m^{ij}_0 + m^{ij}_1 s + m^{ij}_2 s^2 + \cdots \\ &\approx m^{ij}_0 + m^{ij}_1 s. \end{aligned} \tag{4}$$

This can be realized using a macromodel of a parallel capacitance C^{ij}_{red} and a resistance R^{ij}_{red}. The y-parameters of this macromodel, $\hat{y}^{ij}_{\mathrm{red}}$, are expanded to a Taylor series at $s = 0$,

```
1:  Partition the circuit without capacitive coupling into
    subcircuits of main branches.
2:  for each such subcircuit $i$ do
3:      Generate a ROM for the (main branch) subcircuit
        using a MOR method of choice.
4:  end for
5:  for each unique pair of subcircuits $(j, k)$ do
6:      Consider subcircuits $(j, k)$ including also the ca-
        pacitive coupling between $(j, k)$ to form a new
        $(N_j + N_k)$-port circuit.
7:      Calculate $\mathbf{M}_0$ and $\mathbf{M}_1$ for the $(N_j + N_k)$-port.
8:      for each port node $l$ in subcircuit $j$ do
9:          for each port node $m$ in subcircuit $k$ do
10:             Calculate $C_{\mathrm{red}}^{lm}$ for the $(N_j + N_k)$-port using
                Eq. (6). If positive, place $C_{\mathrm{red}}^{lm}$ between nodes
                $l$ and $m$ in the ROM for the coupling.
11:         end for
12:     end for
13: end for
14: Combine the ROMs generated at steps 3 and 10.
```

Fig. 2. The sparsification algorithm. Note that the subcircuits are considered as general N-ports, as opposed to Fig. 1.

resulting in

$$\hat{y}_{\mathrm{red}}^{ij} = -\frac{1}{R_{\mathrm{red}}^{ij}} - sC_{\mathrm{red}}^{ij}. \tag{5}$$

By matching the two series (4) and (5), the element values for the macromodel are obtained:

$$R_{\mathrm{red}}^{ij} = \frac{-1}{m_0^{ij}}, \qquad C_{\mathrm{red}}^{ij} = -m_1^{ij}. \tag{6}$$

In case of only capacitive coupling between the interconnects — which is assumed in this paper — the interconnect branches have no DC connection, $R_{\mathrm{red}}^{ij} \approx \infty$, and the R_{red}^{ij} element can be omitted from the macromodel.

Regarding the algorithm complexity, one LU-factorization and five matrix multiplications are required to generate the block moments for each pair of partitions that have mutual coupling. Thus, if the circuit has far-reaching coupling and the subcircuits are small, more such pairs are generated and more processing is needed. On the other hand, with small subcircuits the matrices are also small, and since only a pair of subcircuits is analyzed at a time, the memory requirements stay low regardless of circuit size and coupling complexity.

C. Discussion

Regarding the circuit's original y-parameters, the reduction makes two approximations.

1) Truncation: The first approximation is that the y-parameters in each case are calculated considering only a truncated part of the circuit; for the main branches without considering the coupling effect, and for the coupling, considering only a pair of coupled interconnect branches. This enables the generation of distinct partitions from a possibly dense circuit mesh with few subcircuit port nodes, retaining the benefits of partitioning.

This approximation is valid when the partitions used are small and the order of the reduction is low. Since the reduction approximation is made at $s = 0$ (DC) and a typical interconnect main branch is of low-pass filter type, whereas the capacitively coupled parallel interconnect lines form band-pass structures at higher complex frequencies, the low-order moments of the interconnect's y-parameters result dominantly from the main branch. Thus, e.g., for branch (a,b) in Fig. 1(a), the low-order moments calculated from the separate main branch describe the admittance of the branch with sufficient accuracy, if the subcircuit is small enough. Similarly for the coupling effect, due to the interconnect's structure, the second moment calculated from the truncated circuit determines most of the low-order local capacitive coupling behavior.

2) MOR: In the second approximation, the y-parameters are approximated with MOR; for the main branches using a method of choice, and for the capacitive coupling, using the low-order matching presented in this paper. Despite the low-order approximation per partition, high accuracy can be obtained, if the partitions are small. Since the subcircuits are recombined at the end of the MOR process, the final order of the total ROM is (much) higher, depending on the number of subcircuits used [2]. Thus, a trade-off between accuracy and reduction efficiency can be adjusted: with smaller subcircuits the total ROM is more accurate but larger, and vice versa.

D. Passivity and stability

An RLC circuit is passive and thus stable, if all element values in the circuit are non-negative [3] — this is a sufficient (but not necessary) condition for passivity. With typical interconnect circuits, the realization generated with (6) is naturally positive-valued, since the capacitive coupling takes form as floating capacitances between the interconnect branches, and m_1^{ij} is typically negative [3]. In the (rare) case if m_1^{ij} is positive, the y-parameters can be matched with a different positive-valued macromodel, using an RL or RC-model as described in [2] and [3], respectively. This prevents the generation of negative elements, with increased accuracy.

In this paper, however, if a negative capacitance would be generated, it is omitted from the realization for simplicity. This reduces the accuracy of the MOR, but since the original circuit is partitioned into small partitions, the omittance of a rare negative element should generate negligible error. In the test cases in Sec. IV, all of the omitted negative capacitances for the coupling effect were of negligible magnitude.

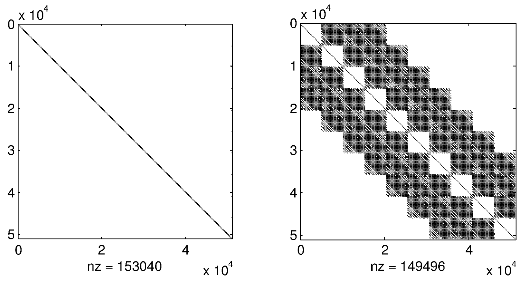

Fig. 3. The $\mathbf{G}$ and $\mathbf{C}$ matrices for `RCu3`, a circuit with 10 parallel buses containing heavy capacitive coupling between the interconnect lines (dense off-diagonal blocks).

TABLE I
TRANSIENT ANALYSIS RESULTS FOR THE ORIGINAL AND REDUCED CIRCUITS (BEST COMPARABLE RESULTS).

circuit		ports	p.size	q_m	nodes	R	C	L	M	mem/Mb	MOR/s	error/%	simul./s	speed-up
RCu1	original	20	-	-	51004	50990	66290	0	0	-	-	-	278	1.0
	C-sp. only	20	500	1	51004	50990	52624	0	0	0.19	59.0	0.05	224	1.2
	PartMOR	20	6000	2	200	390	884	0	0	0.25	18.8	0.08	0.39	712.8
	PartMOR & C-sp.	20	600	2	211	412	1618	0	0	0.18	56.3	0.08	0.57	487.7
	HSPRIM	20	5000	2	700	1850	1518	0	0	1.92	16.7	0.05	0.97	286.6
	HSPRIM & C-sp.	20	500	2	727	1922	2374	0	0	0.20	63.4	0.04	1.16	239.7
RCu2	original	20	-	-	51004	50990	80870	0	0	-	-	-	617	1.0
	C-sp. only	20	800	1	51004	50990	52480	0	0	0.19	64.9	0.08	222	2.8
	PartMOR	20	6000	2	1918	6219	17834	0	0	0.38	41.2	0.10	20.7	29.8
	PartMOR & C-sp.	20	800	2	179	348	1553	0	0	0.19	61.4	0.11	0.54	1142.6
	HSPRIM	20	5000	2	6638	55537	84446	0	0	16.95	78.1	0.09	250	2.5
	HSPRIM & C-sp.	20	1000	4	705	2907	2654	0	0	0.30	64.6	0.12	1.60	385.6
RCu3	original	20	-	-	51004	50990	103310	0	0	-	-	-	3736	1.0
	C-sp. only	20	1000	1	51004	50990	75203	0	0	2.28	635	0.10	266	14.1
	PartMOR	20	10000	2	1496	3119	84017	0	0	0.80	90.5	0.03	2083	1.8
	PartMOR & C-sp.	20	800	2	214	410	36268	0	0	3.38	815	0.07	30.5	122.6
	HSPRIM	20	5000	2	18450	40077	121917	0	0	64.07	438	-[1]	-[1]	-[1]
	HSPRIM & C-sp.	20	1000	2	490	1290	24840	0	0	2.29	638	0.06	19.1	195.2
RCextr	original	3	-	-	998	1398	11961	0	0	-	-	-	43.9	1.0
	C-sp. only	3	1000	1	998	1398	2804	0	0	0.05	4.77	0.08	1.19	36.9
	PartMOR	3	1000	2	216	816	2800	0	0	0.04	4.52	0.02	1.40	31.4
	PartMOR & C-sp.	3	1000	2	16	107	286	0	0	0.04	4.53	0.02	0.11	399.1
	HSPRIM	3	1000	2	695	4126	5235	0	0	0.60	5.68	0.06	7.15	6.1
	HSPRIM & C-sp.	3	1000	2	97	552	535	0	0	0.08	4.84	0.05	0.25	175.6
RLCu1	original	20	-	-	47990	23990	31190	23990	0		-	-	589	1.0
	C-sp. only	20	300	1	47990	23990	25837	23990	0	0.22	55.4	0.56	544	1.1
	PartMOR	20	1000	3	1608	1608	3644	790	0	0.16	26.6	0.52	12.3	47.7
	PartMOR & C-sp.	30	100	3	1602	1602	5892	796	0	0.51	70.0	0.53	17.0	34.7
	HSPRIM	20	1000	4	3960	128780	64780	1605	0	1.37	38.1	0.53	386	1.5
	HSPRIM & C-sp.	20	100	4	3990	15294	13162	1830	0	0.51	71.0	0.56	64.6	9.1
RLCu2	original	20	-	-	47990	23990	34430	23990	0	-	-	-	697	1.0
	C-sp. only	20	300	1	47990	23990	26916	23990	0	0.32	73.4	0.67	542	1.3
	PartMOR	20	500	3	5296	5428	21655	2592	0	0.14	63.2	3.16[2]	196	3.6
	PartMOR & C-sp.	20	100	3	1668	1668	16163	829	0	1.48	113	0.71	43.2	16.2
	HSPRIM	20	40000	6	745	165805	99540	497	0	268.9	74.7	10.44[2]	756	0.9
	HSPRIM & C-sp.	20	200	6	2943	14676	14331	2504	0	0.53	79.9	0.70	59.7	11.7
RLCu3	original	20	-	-	47990	23990	65876	23990	0		-	-	7010	1.0
	C-sp. only	20	300	1	47990	23990	33908	23990	0	0.97	128	0.68	561	12.5
	PartMOR	20	2000	3	24531	16634	73458	11118	0	1.41	181	1.45[2]	4101	1.7
	PartMOR & C-sp.	20	200	3	1162	1162	21936	576	0	2.05	174	0.87	54.2	129.2
	HSPRIM	20	40000	4	1395	614673	307470	669	0	425.3	164	-[1]	-[1]	-[1]
	HSPRIM & C-sp.	20	300	4	2691	13272	18387	1433	0	1.00	138	0.76	65.2	107.5
RLCK3	original	6	-	-	4510	1507	1502	1907	400	-	-	-	11.8	1.0
	PartMOR & C-sp.	6	100	3	99	99	152	50	50	0.04	2.99	0.55	0.20	59.0

[1]: Simulation stopped due to running out of memory. [2]: Better accuracy could not be achieved.

IV. EXPERIMENTAL RESULTS

Eight interconnect circuit are shown in Table I for the purpose of testing partitioning and reduction. The table shows the number of ports, approximate partition size ("p.size", in circuit elements), number of matched block-moments ("q_m"), nodes and circuit elements, memory ("mem/Mb") and time used for the reduction ("MOR/s"), error in transient analysis between original circuit and ROM ("error/%"), transient analysis time ("simul./s"), and how much faster the transient analysis for the ROM is compared to the original circuit ("speed-up").

Time-domain transient analyses was performed on the original circuits and ROMs using APLAC [11] on a Intel(R) Core2 CPU 6700/2.66 GHz 4 GB RAM computer. The difference between the original circuit and ROM transient analysis output voltage curves (i.e., error) was calculated using Eq. (36) in [2].

The reduction methods used to generate the different ROMs in Table I are the following: "C-sp. only": the presented capacitive coupling sparsification method used on the coupling effect, without reducing the interconnect main branches. "PartMOR": a partitioning-based RLC-in–RLC-out MOR method [2]. "PartMOR & C-sp.": PartMOR using the presented capacitance sparsification. "HSPRIM": SPRIM [7], a Krylov-subspace method (with $s_0 = 0$) employing hMETIS partitioning [10] and RLCSYN realization [12] (with $tol = 10^{-7}$), resulting in efficient RLC-in–RLC-out MOR. "HSPRIM & C-sp.": HSPRIM, using also the sparsification method. The methods were implemented using C++ and MATLAB.

The RC circuits RCu1–RCu3 and RLC circuits RLCu1–RLCu3 were obtained using the Predictive Technology Model [13], [14] for top global layer interconnects of the 65 nm technology node, and consist of 10 parallel interconnects. RCu1 contains only light parallel coupling. RCu2 contains more parallel and also sporadic forward coupling, modeling, e.g., gentle bends in the interconnects. RCu3 contains far-reaching dense forward coupling, modeling, e.g., sharp bends or spiral interconnect structures. The circuits RLCu1–RLCu3 contain similar coupling as RCu1–RCu3, with RLC interconnects. Figure 3 shows the **G** and **C** matrices of RCu3,

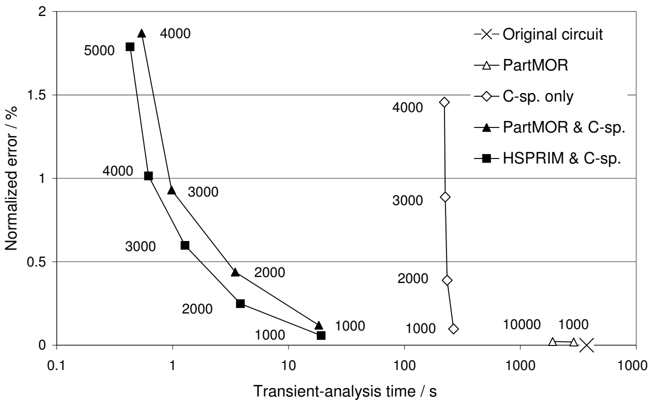

Fig. 4. Transient analysis comparison of circuit RCu3 with various MOR methods using different partition sizes (noted with numbers next to the curves). Note that the analysis time axis is on logarithmic scale. In this comparison, HSPRIM method without the C-sparsification failed to produce any ROMs that could be simulated with the computer setup used (thus, these results are not shown in the figure). In main branch MOR, $q_m = 2$ was used.

demonstrating that the capacitive coupling is modeled as a tight mesh between the interconnects, creating a difficult situation for direct partitioning approaches. The circuit `RCextr` is an interconnect circuit from an industrial radio frequency IC design extracted using NET-AN [15], containing also dense capacitive coupling. Finally, `RLCK3` is a circuit with both inductive and capacitive coupling and is shown as an example that the sparsification can be applied in RLCM-cases as well. For `RLCK3`, [9] was used to generate ROMs for the inductive coupling. The method [9] utilizes a similar reduction approach than the one presented in this paper, where the main branches and the (inductive) coupling are reduced separately, and having good synergy with the presented capacitance sparsification method, requires relatively little additional computation for the mutual inductances. Since [9] can not be applied directly to HSPRIM, results for `RLCK3` are shown only for the PartMOR & C-sp. method.

The table shows the best comparable results for each reduction method (where possible, after a sweep of suitable parameter values): the speed-up in transient analysis for various MOR approaches allowing a similar error in transient analysis. This trade-off between reduction accuracy and efficiency can also be compared in Fig. 4.

The results show that in the case of circuits with only light coupling (`RCu1` and `RLCu1`), the presented sparsification method is not needed, as the partitioning can still be done and reduction succeeds without additional help. With increasing coupling (`RCu2`–`RCu3` and `RLCu2`–`RLCu3`), however, reduction without the capacitance sparsification is inefficient or even impossible (PartMOR and HSPRIM results versus PartMOR & C-sp. and HSPRIM & C-sp.). The sparsification method in itself achieves only modest reduction, but when used together with another MOR method, the sparsification allows partitioning even with dense coupling and improves the reduction efficiency considerably in these cases. Without facilitation, the other MOR methods need to increase the partition size in order to find partitions with a better port-to-internal-node-ratio, which in turn rapidly increases the needed memory (for HSPRIM) and decreses the accuracy. If better accuracy was then sought with a higher q_m, the resulting ROMs increased in size, worsening the reduction efficiency.

Finally, observing the required processing time and memory in Table I, it can be seen that the sparsification method is relatively light and can be applied also in “on-the-fly” MOR applications. However, since the sparsification adds processing time to the MOR, it benefits the reduction most in circuit cases with heavy coupling or if the MOR processing time is not of vital importance, such as with multiple and/or long verification simulations.

V. Conclusions

Partitioning is often a desirable, sometimes even mandatory, processing step in MOR methods. If a circuit contains dense mesh-like structures, such as coupling, partitioning becomes difficult hampering the reduction considerably. Using the method proposed in this paper, dense capacitive coupling between interconnects can be sparsified, enabling partitioning and efficient reduction. Thus, an option to use the presented method substantially improves the reduction’s robustness.

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