Impact of Gallium Nitride Switching Devices on High-Frequency Power Electronics Converters

Bilal Ahmad
Impact of Gallium Nitride Switching Devices on High-Frequency Power Electronics Converters

Bilal Ahmad

A doctoral dissertation completed for the degree of Doctor of Science (Technology) to be defended, with the permission of the Aalto University School of Electrical Engineering and Automation, Remote connection link (e.g. Zoom), on 21 September 2021 at 12:00.

Aalto University
School of Electrical Engineering
Department of Electrical Engineering and Automation
Industrial Electronics and Electric Drives
Supervising professors
Professor Jorma Kyrrä
Aalto University
Espoo, Finland.

Preliminary examiners
Associate Professor Pooya Davari
Aalborg University, Department of Energy Technology
Aalborg, Denmark.

Professor Perti Silventoinen
Lappeenranta University of Technology
Lappeenranta, Finland.

Opponents
Professor Hans-Peter Nee
Royal Institute of Technology, KTH
Stockholm, Sweden.
Author
Bilal Ahmad

Name of the doctoral dissertation
Impact of Gallium Nitride Switching Devices on High-Frequency Power Electronics Converters

Publisher
School of Electrical Engineering

Unit
Department of Electrical Engineering and Automation

Series
Aalto University publication series DOCTORAL DISSERTATIONS 121/2021

Field of research
Power Electronics

Manuscript submitted 6 September 2021
Date of the defence 21 September 2021

Permission for public defence granted (date) 26 August 2021
Language English

☐ Monograph  ☑ Article dissertation  ☐ Essay dissertation

Abstract
Power converters for photo-voltaic (PV) grid are one of the main applications of Gallium Nitride (GaN) switching devices. These converters in grid-connected applications are also required to supply reactive power. During the flow of reactive power, switching devices have to conduct in reverse direction. However, these GaN HEMTs suffer from high voltage drop during the reverse conduction. It is very critical to accurately model these additional losses to achieve the optimized performance. HERIC inverter from transformer-less solar inverter family is chosen for this work due to its high efficiency performance and low leakage current. Conduction losses for the inverter including reverse conduction losses are modelled for various existing uni-polar PWM schemes. Results showed that for loads with low power factor, reverse conduction losses constitute the majority of the total conduction losses. Based on these results, a modified uni-polar PWM scheme is introduced to reduce these losses and enhance the efficiency of the inverter. Fast switching of these GaN HEMTs have made it possible to reduce the size of magnetic components and increase the overall power density of the system. However, fast switching transitions in the converter, generate higher electro-magnetic-interference (EMI) noise. To reduce the noise emissions of the converter it is essential to reduce the parasitic elements in the converter. These parasitic elements facilitate the propagation of high-frequency noise, which will require bulkier EMI filters to comply with power quality standards. Hence, in this work a high voltage gain converter with multi-phase coupled inductor, for electric vehicle (EV) applications, is considered as a case study. A comprehensive model of the inductor structure, including parasitic capacitances is presented in this thesis. The values of those parasitic capacitances are computed with the aid of computer aided simulations and by performing impedance measurements on inductor prototype. EMI measurements of the converter verify that by optimizing the parasitic elements, noise emissions of the converter can be reduced.

GaN devices are also suitable candidates for switching devices in power converters for modernized, more electric aircrafts (MEA). In addition to improving the performance of converters by the application of these switching devices, it is also very critical to review new converter topologies. Two power factor correction (PFC) topologies, Swiss rectifier and Delta rectifier, are considered for this study due to their low number of high-frequency switches. Detailed simulation models of these rectifiers are developed to choose an appropriate topology for their application as front-end rectifier in an isolated AC-DC power supply. After the selection of the rectifier topology, an isolated DC-DC converter is designed and optimized with the aid of an optimization tool. Practical performance of the converter is also enhanced by the application of GaN devices and by minimizing the parasitic elements in the transformer and printed circuit boards (PCBs).

Keywords  WBG, MEA, HERIC, EMC, PFC, EMI, GaN, DC/DC, AC/DC, DC/AC.


ISSN (printed) 1799-4934  ISSN (pdf) 1799-4942

Location of publisher Helsinki  Location of printing Helsinki  Year 2021

Preface

This research work was executed in Industrial Electronics and Electric Drives research group at School of Electrical Engineering and Automation, Aalto University. The whole duration of the research has been partially funded by the School of Electrical Engineering and Automation, Aalto University and by the SAAB-Aalto strategic corporation. I am also grateful to Walter Ahlström foundation for awarding me with three research grants.

Firstly, I would like to express my deepest gratitude to my supervisor, Professor Jorma Kyyrä for his constant guidance around the clock. I really appreciate the fact that I was given the liberty to direct this work. I believe this helped me learn valuable life lessons and I will always be indebted to him for showing this confidence in me.

I am grateful to Erik Agerbjörk and Lars Austrin from SAAB Sweden, for their support and guidance during the practical development of the project. I would also like to show my gratitude to my colleagues Dr. Wilmar Martinez, Dr. Prasad Jayathurathnage, M.Sc. Juha Mäkelä and M.Sc. Aniket Kulkarni for their help and guidance during the whole duration of this research work.

Finally, I am thankful to my family and friends for their emotional support, that was highly needed at times.

Espoo, September 5, 2021,

Bilal Ahmad
## Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preface</td>
<td>5</td>
</tr>
<tr>
<td>Contents</td>
<td>7</td>
</tr>
<tr>
<td>List of Publications</td>
<td>9</td>
</tr>
<tr>
<td>Author's contributions</td>
<td>11</td>
</tr>
<tr>
<td>List of Figures</td>
<td>13</td>
</tr>
<tr>
<td>List of Tables</td>
<td>15</td>
</tr>
<tr>
<td>Abbreviations</td>
<td>17</td>
</tr>
<tr>
<td>Symbols</td>
<td>19</td>
</tr>
<tr>
<td>1. Introduction</td>
<td>21</td>
</tr>
<tr>
<td>1.1 Motivation</td>
<td>22</td>
</tr>
<tr>
<td>1.2 Objectives and Structure of the Thesis</td>
<td>23</td>
</tr>
<tr>
<td>1.3 Contribution of Each Publication</td>
<td>24</td>
</tr>
<tr>
<td>1.4 Major Scientific Contributions of the Thesis</td>
<td>26</td>
</tr>
<tr>
<td>2. Transformer-less DC/AC Solar Inverter</td>
<td>29</td>
</tr>
<tr>
<td>2.1 Transformer-less Solar Inverter</td>
<td>29</td>
</tr>
<tr>
<td>2.1.1 HERIC Inverter</td>
<td>30</td>
</tr>
<tr>
<td>2.2 HERIC Inverter with Reactive Power</td>
<td>32</td>
</tr>
<tr>
<td>2.2.1 Modified PWM</td>
<td>33</td>
</tr>
<tr>
<td>2.3 Efficiency Optimization of HERIC Inverter</td>
<td>34</td>
</tr>
<tr>
<td>2.3.1 Reverse Conduction Losses</td>
<td>34</td>
</tr>
<tr>
<td>2.3.2 Mathematical Model for Different PWM Schemes</td>
<td>35</td>
</tr>
<tr>
<td>2.3.3 Experimental Validation</td>
<td>39</td>
</tr>
<tr>
<td>3. High Voltage Gain DC-DC Converter</td>
<td>43</td>
</tr>
<tr>
<td>3.1 HSU Converter Topology</td>
<td>43</td>
</tr>
</tbody>
</table>
This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.


VI Bilal Ahmad, Prasad Jayathurathnage, Jorma Kyyrä, Wilmar Martinez. FEA based Model for High-Frequency Design Optimization of a Three-Winding Coupled Inductor for HSU Converters. In *21st Euro-
pean Conference on Power Electronics and Applications (EPE ’19 ECCE Europe), Genova, Italy, 10 Pages, Sep 2019.


Author’s contributions

Publication I: “Performance analysis of a transformer-less solar inverter with modified PWM”

The author performed the simulations, analytical analysis and wrote the paper with the help of co-authors.

Publication II: “Modified Modulation Signals for GaN-E-HEMTs Based HERIC Inverter to Improve Reverse Conduction Performance”

The author developed the practical prototype and performed the experiments. Also wrote the paper with the aid of co-authors.

Publication III: “Modified PWM Signals to Reduce Reverse Conduction Losses in GaN Based HERIC Inverter”

Author developed the analytical models and prototype to obtain experimental validation. Paper was written by the author with the help of co-authors.

Publication IV: “Efficiency Optimisation of an Interleaved High Step-up Converter”

Author formulated the paper idea and performed the simulations and experimental validation work. With the help of co-authors, author wrote the paper.
Author's contributions

**Publication V: “Common Mode Noise Analysis for a High Step-Up Converter with GaN Devices”**

The author wrote the paper and also performed the practical implementation work with the aid of co-authors.

**Publication VI: “FEA based Model for High-Frequency Design Optimization of a Three-Winding Coupled Inductor for HSU Converters”**

The author developed the FEM model and performed simulations. Paper was written by the author with the guidance of co-authors.

**Publication VII: “Parameter Extraction Technique for Evaluation of Inductive and Capacitive Elements of Three-Winding Coupled Inductor”**

The author performed the impedance modelling and EMI measurements. Analysis of measurements and writing of the paper was done with help of co-authors.

**Publication VIII: “EMI Standard Compliance of Three-Phase Buck Type PFC Rectifier For Application in Aircraft”**

The author developed the simulation models and wrote the paper with the help of co-authors.

**Publication IX: “Power Supply Design Considerations For 400Hz Aircraft Applications”**

The author developed the scope of the paper and wrote the paper with the help of co-authors.

**Publication X: “Role of Parasitics in a Dual Active Bridge DC-DC Converter with Gallium Nitride devices”**

The author formulated the scope of this paper and helped co-authors during practical implementation and writing of the paper.
List of Figures

1.1 Flow diagram of thesis structure .................................... 26
2.1 Full bridge inverter topology ....................................... 29
2.2 HERIC Inverter and UP PWM Scheme ............................. 30
2.3 HERIC inverter operation modes .................................... 31
2.4 HERIC inverter with inductive load - Conventional UP PWM .................................................. 32
2.5 HERIC Inverter and UP PWM Scheme ................................ 32
2.6 HERIC inverter with inductive load - Modified UP-PWM .......... 33
2.7 THD - Conventional Vs Modified UP-PWM ..................... 34
2.8 Reverse conduction losses normalized with total conduction losses .................................................. 35
2.9 UP PWM with dead time ............................................... 35
2.10 Hybrid UP PWM ..................................................... 36
2.11 Calculated Vs Simulated Average Conduction Losses .......... 38
2.12 Comparison of conduction losses of HERIC inverter switch with modified UP PWM and hybrid UP PWM ................. 39
2.13 HERIC inverter prototype ............................................ 39
2.14 Circuit to generate negative bias for gate driving circuit ........ 40
2.15 Measured output voltage and current of HERIC inverter (CH3 - Purple $V_{AC} : 25 \, V/Div$, CH4 - Green $i_g : 1 \, A/Div$) . 41
2.16 Drain to source voltages of HERIC inverter switches during positive half-cycle - Marked switching transitions to show the switching imbalance (CH1 $V_{DS} : 5 \, V/Div$) .... 41
3.1 Selected HSU converter ................................................. 43
3.2 HSU converter operation modes ..................................... 44
3.3 Practical Evaluation : HSU Converter ............................. 46
3.4 HSU Converter with Parasitic Elements .......................... 46
3.5 Effect of gate resistance on EMI emissions of HSU converter 47
3.6 Stray Capacitances in Three-Winding HSU Inductor ............ 48
3.7 Inductor 3-D Model .................................................. 49
List of Figures

3.8 Reactance Curves for Different Core Sizes ............. 50
3.9 HSU Inductor Equivalent Model ....................... 51
3.10 Test cases for low-frequency model ................... 51
3.11 Test cases for high-frequency model ................... 52
3.12 HSU inductor prototypes ............................. 53
3.13 Experimental setup for conducted emissions measurement 54
3.14 Difference between emissions of converter with inductor ETD49 & ETD59 ...................... 55

4.1 Two stage AC/DC power supply ......................... 57
4.2 Swiss rectifier topology ............................... 59
4.3 Two-stage LC filter ................................... 60
4.4 EMI compliance results of Swiss rectifier ............. 61
4.5 Time domain simulation results of Swiss rectifier: Grid Currents ..................................... 61
4.6 Effect of filter capacitance and switching frequency on Swiss rectifier emissions ..................... 62
4.7 Delta rectifier topology ................................ 62
4.8 Switching pattern of $S_{AB}$ and $S_{BA}$ ................ 63
4.9 Block diagram of closed loop control of Delta rectifier 63
4.10 Time domain simulation results of Delta rectifier: (a) Grid Currents (b) Output DC voltage ............. 65
4.11 EMI compliance results of Delta rectifier ............. 65
4.12 DAB converter ........................................ 66
4.13 Resistance factor vs winding foil thickness .......... 68
4.14 Resistance factor vs interleaving, foil thickness of 0.1 mm 68
4.15 Quality function ($\eta / W$) for selection of magnetic-core material ........................................ 69
4.16 Flow diagram for transformer design ................. 70
4.17 DAB converter practical prototype ..................... 71
4.18 High-frequency noise during DAB operation .......... 72
4.19 Parasitic inductances of the PCB tracks ............ 73
4.20 Improved DAB layout design ........................... 73
4.21 Switching waveforms of DAB with improved layout design 74
4.22 Switching waveforms of DAB converter at multiple switching frequencies (Ch1 (Navy Blue): Voltage across Secondary side Device, Ch2 (Sky Blue): Current through Secondary side Device, Ch3 (Pink): Output Current, Ch4 (Green): Voltage across External Leakage Inductor) .... 75
## List of Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>CM Voltages HERIC Inverter</td>
<td>31</td>
</tr>
<tr>
<td>2.2</td>
<td>Simulation parameters for HERIC inverter</td>
<td>38</td>
</tr>
<tr>
<td>3.1</td>
<td>HSU converter prototype parameters</td>
<td>45</td>
</tr>
<tr>
<td>3.2</td>
<td>Measured Parameters of Inductors</td>
<td>54</td>
</tr>
<tr>
<td>3.3</td>
<td>HSU Converter Parameters</td>
<td>55</td>
</tr>
<tr>
<td>4.1</td>
<td>Simulation parameters for Swiss rectifier</td>
<td>60</td>
</tr>
<tr>
<td>4.2</td>
<td>Simulation parameters for Delta rectifier</td>
<td>64</td>
</tr>
<tr>
<td>4.3</td>
<td>Design parameters of high-frequency isolation transformer</td>
<td>71</td>
</tr>
<tr>
<td>6.1</td>
<td>Lab equipment used for testing</td>
<td>89</td>
</tr>
</tbody>
</table>
Abbreviations

AC  Alternating current
CM  Common mode
CMTI  Common-mode transient immunity
DAB  Dual active bridge
DC  Direct current
DSP  Digital signal processor
DM  Differential mode
EMC  Electro-magnetic compatibility
EMI  Electro-magnetic interference
E-Mode  Enhancement mode
EPC  Equivalent parallel capacitance
EV  Electric vehicle
FB  Full bridge
FFT  Fast fourier transform
GaN  Gallium nitride
HEMT  High-electron-mobility Transistor
HERIC  Highly efficient and reliable inverter concept
HSU  High step-up
IC  Integrated circuit
LISN  Line impedance stabilization network
Abbreviations

**MEA** More electric aircraft

**PCB** Printed circuit board

**PFC** Power factor correction

**PR** Proportional resonant

**PV** Photo-voltaic

**PWM** Pulse-width modulation

**RMS** Root mean square

**Si** Silicon

**SiC** Silicon carbide

**THD** Total harmonic distortion

**UP** Uni-polar

**UPS** Uninterruptible power supplies

**WBG** Wide band gap
Symbols

\( B \) Magnetic flux density

\( C_{12}, C_{23}, C_{31} \) Inter-winding capacitances of the inductor

\( C_{DC} \) DC-bus capacitance

\( C_{DS} \) Drain source capacitance of the switch

\( C_{\text{inter}} \) Inter-winding capacitance of the

\( C_{P1}, C_{P2}, C_{P3} \) Equivalent parallel capacitance of the windings

\( \frac{di}{dt} \) Rate of change of current

\( \frac{dv}{dt} \) Rate of change of voltage

\( f \) Fundamental grid voltage

\( F_R \) Resistance factor

\( f_{sw} \) Switching frequency

\( I \) Peak value of current

\( i_g \) AC grid current

\( J \) Current density

\( k_p \) Proportional gain of the controller

\( L_a, L_b, L_c \) Self-inductance of the windings

\( L_f \) Filter inductance

\( M_{12}, M_{23}, M_{31} \) Mutual-inductances of the inductor

\( N \) Turns ratio

\( P_o \) Output power
Symbols

\( Q \) Quality function of the transformer

\( R_{ds} \) Drain-source resistance of the switch

\( t_d \) Dead time

\( T_r \) Time constant of the controller

\( T_s \) Sampling time

\( V_{AN}, V_{BN}, V_{CN} \) Instantaneous value of phase voltages

\( V_{CM} \) Common-mode voltage

\( V_d \) Voltage drop across the switch during reverse conduction

\( V_{DC} \) DC-bus voltage

\( V_g \) AC grid voltage

\( V_{PH} \) Peak value of phase voltage

\( \phi \) Load angle

\( \eta \) Efficiency
1. Introduction

Power electronics converters facilitate the efficient control of electrical energy [1], and switching devices are the essential components of these power converters. Hence, an improvement in the technology of switching devices will improve the overall performance of the system. Since the inception of the first silicon (Si) transistor from Bell Labs in 1948, it has been the most widely used switching device [2]. However, due to the intrinsic properties of Si material, these devices exhibit limitations in terms of blocking voltage, thermal management and switching speeds [3].

Wide band gap (WBG) semiconductor materials, especially silicon carbide (SiC) and gallium nitride (GaN), show superior material properties over Si. As these materials have higher band gap than Si [4], switching devices made from these materials are better suitable for high-voltage, high-temperature and high-frequency applications. Owing to higher breakdown field strength and electron velocity, GaN or SiC switching devices will have smaller chip size than Si devices for the same blocking voltage. Smaller chip size results in lower switch junction capacitances and hence makes them capable of switching at faster speeds than their Si counterparts [5].

With the practical availability of SiC and GaN switching devices, major breakthroughs have been achieved in improving the performance of power converters. It has been shown in [6] that a 50 – 90% reduction in hard switching losses in variable speed drives can be achieved by replacing conventional Si devices with WBG devices. Similar conclusions had been drawn by various others studies [3, 7–9] regarding application of WBG devices in voltage source inverters (VSI), matrix converters and DC-DC converters. In addition to exceptionally improving the efficiency by reducing switching and conduction losses, the ability of these novel devices to switch at higher frequencies results in reducing the size of magnetic components and hence improving the system’s power density. With the application of SiC switching devices in a DC-AC inverter, an increase of 160% in power density has been reported in [10]. In [11], a 50% reduction in the size of required magnetic components has been reported for a GaN
based converter operating at 1 MHz switching frequency. Hence, it is safe to deduce that WBG switching devices have made it possible for power electronics converters to achieve ambitious performance goals that were not possible with Si switching devices.

1.1 Motivation

As life is not all sunshine and rainbows, these novel WBG devices also give rise to countless new challenges and research questions. One major challenge is parasitic elements in the circuit board. They have detrimental effects on the switching performance of these devices. Especially, GaN HEMTs with low gate-source transient voltage tolerance (−20 V − +7 V), a high gate drive loop inductance can generate high voltage spikes which could potentially destroy the device. This can be avoided by increasing the gate drive resistance but that will ultimately reduce the turn-on speed of the switch and hence increase the switching losses. In addition to gate drive parasitics, power loop parasitic inductance also forms a resonant tank with output capacitance of the switch and could generate high voltage overshoot across the top switch during fast turn-on of bottom switch in a half bridge configuration [5]. Hence, it is very critical to employ modified/novel circuit layout design techniques to minimize the circuit board parasitics for safe and efficient operation of WBG devices.

Unlike silicon (Si) MOSFETs, GaN HEMTs have much higher reverse conduction losses [12]. Forward voltage drop across the body diode of these switches depends on the turn-off gate-source voltage. Since GaN HEMTs have low turn-on threshold voltage ($V_{gs,th} = 1.6V$), it is recommended to use negative turn-off voltage, which further increases the forward voltage drop and reverse conduction losses [5]. Hence, depending on the application, it is very important to model the reverse conduction losses (during reactive power generation or dead-time) and employ methods to reduce them.

Reduction in switching losses due to faster turn-on and turn-off times of these devices comes with the drawback of increase in high-frequency noise. Various studies including [6,13,14] have reached the conclusion that if the WBG switching devices are operated at their full capability of switching speeds, special attention is needed to be paid to high-frequency emissions of the converter. To compensate the increase in high-frequency emissions due to fast switching speeds, an accurate modelling and reduction of parasitic elements in magnetic components is required [15–17].

In addition to switching devices, magnetic components are the major source of losses in the power electronics converter. For an over-all efficient system it is important to optimize the magnetic components for high-frequency operation. Especially with the availability of new magnetic materials, e.g. nano-crytalline magnetic materials, core losses of
the transformer can be reduced by almost 50% [18]. Hence, in addition to off-the-shelf solutions, new optimization tools including new material for high-frequency operation are required [19].

1.2 Objectives and Structure of the Thesis

This research work has been divided into three parts to discuss the challenges which were elaborated in the previous section.

In the first part of this research work, detailed modelling of conduction losses of GaN HEMTs has been discussed. These devices introduce additional losses during reverse conduction and hence hamper the overall efficiency of the converter. Since high efficiency is one of the main motivations of application of WBG devices, it is vital to model these additional losses accurately for overall optimization of the system. Since transformer-less solar inverters provide an efficient solution for integration of photo-voltaic (PV) panels to the grid, HERIC inverter from this family of inverters is chosen to conduct this part of the research. Due to absence of the isolation transformer in transformer-less inverters, it is very critical to limit the leakage current for safety of the personnel and to comply with the power quality standards. HERIC inverter does that effectively by keeping the switching node voltage constant in all modes of operation and hence, eliminates the leakage current. In addition to zero leakage current, this inverter only requires only two additional switching devices as compared to a standard full bridge inverter. Publications on this topic are summarized in Chapter 2.

In the next part of this research work, the impact of application of WBG devices on EMI emissions of the converter has been studied. The application of these switching devices introduces high $\frac{dv}{dt}$ and $\frac{di}{dt}$ in the circuit, which increases the EMI emissions of the converter. Higher EMI emissions will require bigger and heavier EMI filters for the converter to comply with power quality standards. This negates one of the main purposes of the application of WBG devices, i.e. high power density. In addition to faster switching time of WBG devices, parasitic elements in the converter also facilitate the propagation of the high-frequency emissions. Multiple existing studies have discussed various methods to measure or calculate the values of these parasitic elements for a two winding inductor. However, detailed modelling of capacitive and inductive parasitic elements of a multi-winding inductor structure ($N > 2$) is still needed to be addressed. Hence, in this part of the research work, an inductive and capacitive high-frequency model of multi-winding coupled inductor for high voltage gain DC-DC converter is presented. Along with the model, a parametric extraction technique to accurately measure these parasitic elements has also been implemented. Selected converter topology has the ability to provide higher
voltage gain as compared to standard boost converter without requiring extra switching devices. All publications on this topic are summarized in Chapter 3.

In the future, most of the mechanically operated auxiliary functions in an aircraft are to be performed by electrical energy. Due to the attraction of low fuel consumption and space limitation in an aircraft, high power density and efficiency are essential parameters for aircraft’s power converters. Hence, WBG switching devices are the perfect candidates for these converters. In this part of the research work, a thorough design methodology of a 3-phase AC/DC power supply for 400 Hz operation has been presented. In addition to this, practical challenges faced during implementation of GaN based converters and their possible solutions have also been presented. All publications on this topic are summarized in Chapter 4.

Finally, based on the analysis and results presented in all previous chapters, conclusions of this research work are drawn in Chapter 5.

1.3 Contribution of Each Publication

This dissertation provides the summary of ten publications. Key scientific contributions of those publications are summarized in this section.

Publication [I]

In this publication a detailed Spice based model of the HERIC inverter with GaN HEMTs is developed. Performance of the inverter is evaluated in terms of the input power quality with the application of conventional and modified uni-polar PWM schemes.

Publication [II]

This publication highlighted the impact of high reverse conduction losses of the GaN HEMTs on overall efficiency of the HERIC inverter. Two modifications in PWM schemes are proposed to reduce those losses.

Publication [III]

This publication summarizes the results of Publication I and Publication II. Based on those results detailed mathematical modelling of the conduction losses in HERIC inverter is developed. Analysis is also extended to other existing uni-polar PWM schemes for HERIC inverter.
Publication [IV]

In this publication practical challenges in development of a high-frequency high voltage gain DC-DC converter are presented. Effect of parasitic elements on the converter operation is also addressed.

Publication [V]

This publication provided EMI analysis of the high step up converter. High-frequency noise emissions of the converter are presented in terms of its switching frequency and modes of operations.

Publication [VI]

This publication provides a FEA based optimization tool to minimize the parasitic elements in multi-winding coupled inductor.

Publication [VII]

In this publication, a detailed model of multi-winding coupled inductor is presented. It provides a measurement methodology and optimization of the parasitic elements in the inductor structure.

Publication [VIII]

This publication evaluates the Swiss rectifier for its application in aircraft’s power converters. It highlights the impact of 400 Hz operation on the power quality of the rectifier and its compliance with EMI standards.

Publication [IX]

This publication introduces an iterative optimization tool for the design of an efficient and power dense isolation transformer.

Publication [X]

This publication highlights the challenges in the practical implementation of the high-frequency converter. Multiple techniques to optimize the converter layout and magnetic components is presented.

Fig. 1.1 shows the relevance of publications to the main title of the thesis.
1.4 **Major Scientific Contributions of the Thesis**

As presented in section 1.2, in this research work, applications of GaN switching devices are explored in three different applications, namely DC/AC inverter, DC/DC high voltage gain converter and AC/DC power supply. Key scientific contributions from the work done on each selected application are summarized below.

Conversion efficiency of power electronics converters is a key parameter in photo-voltaic applications. Efficiency of solar inverters can be enhanced tremendously by the application of GaN switching devices. However, these devices add up the total cost of the converter. To justify the increase in cost, losses in the device have to be modelled accurately to assure the increase in efficiency. Hence, in the first portion of the study, losses in GaN HEMTs were modelled for the grid connected photo-voltaic inverter. HERIC topology was chosen to implement this study. Results obtained from mathematical and simulation models showed that with application of GaN switches, reverse conduction losses are increased as compared to Si switches. To reduce these losses, a modified version of unipolar-PWM scheme is introduced in this part of the work that successfully reduced the reverse conduction losses in GaN HEMTs based HERIC inverter by more than 50%.

In the second part of the work, role of parasitic elements in high frequency high voltage gain DC/DC converter was researched. It was shown that with the application of GaN switches, converter can indeed be oper-
ated at higher switching frequencies. However, with increase in switching frequency influence of parasitic elements on the converter operation is also enhanced. Chosen topology of high voltage gain converter requires a multi-winding coupled inductor and to accurately model the parasitic elements in the converter, an accurate high frequency model of the inductor with its parasitic capacitances was developed. Parametric extraction technique was utilized to measure these parasitic capacitances. With the aid of introduced modelling technique, conducted emissions of the converter were successfully reduced by reducing the size of parasitic capacitances in the inductor structure. Most important take away from this part of the research work was that in addition to miniaturization of magnetic components with the application GaN switches, it is critical to pay attention to the adverse affect of increase in parasitic elements for overall optimized performance of the converter.

With the application of GaN HEMTs, weight of the power converters in an aircraft can be reduced which will ultimately result in lower fuel consumption and lesser CO$_2$ emissions. As electric grid in an aircraft operates at 400 Hz fundamental frequency, it is important to identify the converter topologies that could operate at this frequency and also comply with more strict EMI standards for the aircraft applications. Two topologies for three-phase AC/DC rectifier namely, the Swiss rectifier and the Delta rectifier, were studied in the third part of the study. Results of the simulation model pointed out the fact that owing to low frequency (at each phase crossing of a three phase voltage) glitches in Swiss rectifier, it does not comply with EMI standards for aircraft applications. It must be noted that THD and high frequency (>10 kHz) emissions were below the standard limits. Following the rectifier, a DC/DC converter is required for isolation and DC voltage regulation. An iterative tool to optimize the design of isolation transformer of the converter was developed. Since, the parasitic elements were not considered in the design tool, similar transformer design with thin copper foil winding and Litz wire winding were implemented to study the effect of parasitic capacitance on converter operation. Results obtained from practical tests showed that the inter-winding capacitance of the foil based converter introduces high ringing and ultimately converter failure due to the fast voltage transition of GaN switches. Ringing was significantly improved by employing a solution with less parasitic capacitance i.e. Litz wire based transformer. This part of the study also pointed out the fact that for the design of GaN based converters, parasitic elements must be considered in the optimization procedure for stable and efficient operation of the converter.
2. Transformer-less DC/AC Solar Inverter

Depleting fossils fuel and reduction in per watt price of photo-voltaic (PV) modules has shifted much attention towards grid-tied PV systems [20, 21]. A power electronic converter is employed to convert DC voltage from PV modules to AC voltage for grid synchronization. These converters utilize a low-frequency transformer for electrical isolation in between PV arrays and grid. Half of the total losses in the converter occur in this isolation transformer. Since a highly efficient power electronic converter is vital for an overall efficient solar powered electrical system, it is desirable to remove this transformer from the system and increase the overall power density and conversion efficiency [22, 23]. However, due to the absence of an isolation transformer, leakage current flowing via high parasitic capacitance between PV panels and the ground becomes very critical for the safety of personnel and reliability of the whole system [24]. Hence, to comply with strict leakage current standards [25] and safety issues, it is vital to eliminate or reduce the leakage current below standard limits.

2.1 Transformer-less Solar Inverter

A conventional full-bridge inverter is shown in Fig. 2.1.

![Full bridge inverter topology](image)

Figure 2.1. Full bridge inverter topology

$C_{P1}$ and $C_{P2}$ represent parasitic capacitance between a PV array and
Transformer-less DC/AC Solar Inverter

To limit the current flowing through these parasitic capacitances for the safety concerns of the personnel, common mode (CM) voltage of the inverter which is defined as

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2}$$

(2.1)

has to be kept constant. \(V_{AN}\) and \(V_{BN}\) are the switching node voltages of the inverter (c.f. Fig. 2.1).

However, when a uni-polar (UP) PWM scheme is employed with this inverter topology, CM voltage varies with switching frequency, which generates high leakage currents through the parasitic capacitances to the ground \[26\]. To achieve low leakage current with high power density while maintaining high conversion efficiency with UP PWM scheme, conventional full bridge DC-AC inverter needs to be modified. Various techniques have been reported in literature to eliminate the leakage current \[27,28\] which also includes decoupling of DC and AC sides during zero voltage vector state. E.g. H5 inverter \[29\], H6 inverter family \[30–33\] and HERIC inverter \[34\]. Among various transformer-less solar inverter topologies discussed in literature, HERIC inverter shown in Fig. 2.2a is considered as a good candidate owing to its simpler structure, high efficiency and low leakage current \[35–39\].

![HERIC inverter topology](image)

**Figure 2.2. HERIC Inverter and UP PWM Scheme**

### 2.1.1 HERIC Inverter

As shown in Fig. 2.2a, this inverter topology consists of six active switches in comparison to four active switches in a h-bridge inverter (c.f. Fig. 2.1), where \(Q_1\), \(Q_2\), \(Q_3\) and \(Q_4\) forms a full bridge circuit while \(Q_5\) and \(Q_6\) along with \(D_1\) and \(D_2\) are used as by-pass switches to generate a zero voltage vector. \(C_{DC}\) represents the input DC capacitor, while \(C_{P1}\) and \(C_{P2}\) are the parasitic capacitances from solar panels to ground. While \(L_f\) is the AC grid side filter with \(V_g\) representing the grid voltage. For ideal resistive loads, HERIC inverter has four operation modes shown in Fig. 2.3.
Figure 2.3. HERIC inverter operation modes

**Mode Z₁ & Z₃**
During positive half cycle, switches \( Q₂, Q₃ \) and \( Q₆ \) are kept switched OFF, while \( Q₁ \) and \( Q₄ \) are switched at the switching frequency and \( Q₅ \) is continuously kept on as shown in Fig. 2.2b. During operation mode \( Z₁ \), \( Q₁ \) and \( Q₄ \) are switched on and current flows from DC side to AC side. While during operation mode \( Z₃ \), AC side is short circuited through \( Q₅ \) and \( D₁ \) to generate a zero voltage vector.

**Mode Z₂ & Z₄**
During negative half cycle, switches \( Q₁, Q₄ \) and \( Q₅ \) are kept switched OFF, while \( Q₂ \) and \( Q₃ \) are switched at the switching frequency and \( Q₆ \) is continuously kept on as shown in Fig. 2.2b. Current flows from DC to AC side via \( Q₂ \) and \( Q₄ \), while zero voltage at AC side is generated by \( Q₆ \) and \( D₂ \).

CM voltages (c.f. (2.1)) for all operation modes are summarized in Table 2.1. Since CM voltage remains constant \((V_{DC}/2)\) in all operating modes, leakage current through the parasitic capacitance is eliminated.

Table 2.1. CM Voltages HERIC Inverter

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>( V_{AN} )</th>
<th>( V_{BN} )</th>
<th>( V_{CM} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Z₁ )</td>
<td>( V_{DC} )</td>
<td>0</td>
<td>( V_{DC}/2 )</td>
</tr>
<tr>
<td>( Z₂ )</td>
<td>( V_{DC}/2 )</td>
<td>( V_{DC}/2 )</td>
<td>( V_{DC}/2 )</td>
</tr>
<tr>
<td>( Z₃ )</td>
<td>0</td>
<td>( V_{DC} )</td>
<td>( V_{DC}/2 )</td>
</tr>
<tr>
<td>( Z₄ )</td>
<td>( V_{DC}/2 )</td>
<td>( V_{DC}/2 )</td>
<td>( V_{DC}/2 )</td>
</tr>
</tbody>
</table>
2.2 HERIC Inverter with Reactive Power

With non-unity load, either a resistive and inductive load or resistive and capacitive load, AC side current lags and leads the grid voltage respectively. Fig. 2.4 shows the differential mode (DM) AC side voltage \( v_{DM} \) and grid current \( i_g \) of the inverter with conventional UP PWM scheme. \( v_c \) is the carrier sinusoidal signal to generate sine wave PWM pulses while \( i_{gref} \) is the reference current waveform that is delayed by an angle \( \phi \) from the sinusoidal carrier waveform.

![Figure 2.4. HERIC inverter with inductive load - Conventional UP PWM](image)

For the duration \([0, \phi]\), \( v_c > 0 \) but \( i_{gref} < 0 \), since, \( Q_6 \) is turned off, there is no path for negative AC side free-wheeling current. Hence, for this duration AC side is connected to DC side via body diodes of switches \( Q_1 \) and \( Q_4 \), which results in sharp decay in grid current \( i_g \). Similarly, for the duration \([\pi, \pi + \phi]\), \( v_c < 0 \) but \( i_{gref} > 0 \) and positive freewheeling current will flow through the body diodes of \( Q_2 \) and \( Q_3 \). These two operation modes are shown as \( Z_5 \) and \( Z_6 \) in Fig. 2.5.

![Figure 2.5. HERIC Inverter and UP PWM Scheme](image)

These distortions in the grid current deteriorate the power factor, which makes this UP-PWM scheme unsuitable for grid tied applications.
2.2.1 Modified PWM

A modified UP-PWM scheme shown in Fig. 2.6 has been discussed in Publication I to supply reactive power with HERIC inverter. This modified UP-PWM provides an alternative path to freewheeling current during negative power duration (i.e. \([0, \phi]\) & \([\pi, \pi + \phi]\)).

Figure 2.6. HERIC inverter with inductive load - Modified UP-PWM

The significant difference between modified PWM scheme and conventional PWM is switching of \(Q_5\) and \(Q_6\) at carrier frequency for the small transition period (i.e. negative power duration). However, this interval will vary depending on the requirement of reactive power by the load. For inductive loads, when the current is lagging the voltage, modified PWM signals can be generated by following the output current.

To evaluate the effect of these modifications on the performance of the inverter, total harmonic distortion (THD) of grid current is measured by performing LTspice based simulations. THD is mathematically represented in (2.2).

\[
THD = \sqrt{\sum_{n=2}^{\infty} \frac{I_{n,rms}^2}{I_{1,rms}^2}}. \tag{2.2}
\]

\(I_{1,rms}\) represents the RMS value of the fundamental component of the load current and \(I_{n,rms}\) is the RMS values of higher order components. The value of each component has been estimated using Fast Fourier Transform of the output current waveform for both modified and conventional PWM and the resultant THD values for various load angles (\(\phi\)) are presented in Fig. 2.7. These results show that the THD is improved significantly by the application of modified UP-PWM scheme.
2.3 Efficiency Optimization of HERIC Inverter

Efficiency and the power density of the inverter can be further increased by the application gallium nitride (GaN) switches [40]. It is shown in [41] that by the application of cascode GaN HEMTs efficiency of 99% can be obtained from HERIC inverter. However, cascode GaN HEMTs suffer from high parasitic inductance owing to its packaging [42]. Alternatively, enhancement-mode (e-mode) GaN HEMT has much smaller package inductance which makes it possible to operate at even higher switching frequencies for higher power density [43,44].

Unlike silicon (Si) MOSFETs, GaN HEMTs have much higher reverse conduction losses [12]. Since, during the negative power duration current will flow through body diodes of MOSFETs, it increases the conduction losses. Therefore, it is critical to include reverse conduction duration for accurate estimation of conduction losses. However, in literature only switching losses are evaluated and conduction losses are ignored while comparing the performance of HERIC inverter with these modified PWM schemes.

2.3.1 Reverse Conduction Losses

In Publication II reverse conduction losses of GaN HEMT based HERIC inverter are evaluated by performing LTspice based simulations. For accurate estimation of the losses, spice models of the switches and the circuit parasitic elements are included in the simulation model. Reverse conduction losses normalized with total conduction losses for both conventional UP-PWM and modified UP-PWM schemes are shown in Fig.2.8a and Fig.2.8b respectively.

It can be seen that at load angle of approximately 60°, with conventional
Transformer-less DC/AC Solar Inverter

(a) Conventional UP-PWM  

(b) Modified UP-PWM

**Figure 2.8.** Reverse conduction losses normalized with total conduction losses

UP PWM, reverse conduction losses constitutes upto 68% of total conduction losses in comparison to almost 8% with modified UP PWM (c.f. Publication I).

### 2.3.2 Mathematical Model for Different PWM Schemes

To supply reactive power by HERIC inverter, in addition to modified UP-PWM (c.f. Publication I & Publication II), two more modified UP PWM schemes have been discussed in literature: UP PWM with dead time shown in Fig. 2.9 and Hybrid UP PWM shown in Fig. 2.10.

**Figure 2.9.** UP PWM with dead time

As it has been discussed in previous sections, with GaN HEMTs it is critical for inverter design optimization to accurately compute the reverse conduction losses of switches for all PWM schemes in addition to their switching losses. Hence, in Publication III mathematical models of conduction losses including dead-time and reverse conduction for each PWM scheme are developed for their comparison. Since conventional UP PWM cannot supply reactive power, only modified UP PWM, UP PWM with dead time and hybrid UP PWM are considered. All the equations below are derived for switch $Q_2$ and $Q_6$. Similar concepts can be applied to all other switches in the circuit.
Modified UP-PWM

For modified UP-PWM scheme shown in Fig. 2.6, switch channel conduction and reverse conduction losses of bridge switch can be calculated by (2.3) and (2.4) respectively. While channel conduction losses of by-pass switch can be calculated by (2.5),

\[ P_C = \frac{1}{2\pi} \int_{\pi+\phi}^{2\pi} F(\alpha) \, d(\alpha) \]

\[ F(\alpha) = M \sin(\alpha - \phi - \pi) \hat{I}^2 \sin^2(\alpha - \phi - \pi) R_{ds} \quad (2.3) \]

\[ P_{RC} = \frac{1}{2\pi} \int_{\pi}^{\pi+\phi} F(\alpha) \, d(\alpha) \]

\[ F(\alpha) = M \sin(\alpha - \phi) \hat{I}^2 \sin^2(\alpha - \phi) R_{ds} \quad (2.4) \]

\[ P_{C,FW} = \frac{1}{2\pi} \left[ \int_{0}^{\phi} F(\alpha) \, d(\alpha) + \int_{\pi+\phi}^{2\pi} G(\alpha) \, d(\alpha) \right] \]

\[ F(\alpha) = (1 - M \sin(\alpha)) \hat{I}^2 \sin^2(\phi - \alpha) R_{ds} \]

\[ G(\alpha) = (1 - M \sin(\alpha - \pi)) \hat{I}^2 \sin^2(\alpha - \phi - \pi) R_{ds} \quad (2.5) \]

where \( M \) is the modulation index and \( R_{ds} \) is the drain to source resistance of the switch while it is in ON state, \( \hat{I} \) is the peak of grid current and \( \phi \) represents the load angle.

UP PWM with dead time

In this PWM scheme (c.f. Fig. 2.9), by-pass switches \( Q_5 \) and \( Q_6 \) are switched continuously in complimentary to bridge switches. Hence, to avoid short circuiting, a deadtime is introduced in between bridge and by-pass switches.
During the deadtime duration, bridge switches will conduct in reverse direction which will add up the reverse conduction losses. Channel conduction losses and reverse conduction losses including the affect of deadtime can be estimated by (2.6) and (2.7) respectively. While conduction losses for by-pass switches can be estimated by (2.8).

\[
P_C = \frac{1}{2\pi} \int_{\pi}^{2\pi} F(\alpha) d(\alpha)
\]

\[
F(\alpha)= (M \sin(\alpha - \pi) - 2t_d f_{sw}) (I^2 \sin^2(\alpha - \phi - \pi) R_{ds}).
\]  

(2.6)

\[
P_{RC} = \frac{1}{2\pi} \int_{\pi}^{\pi + \phi} F(\alpha) d(\alpha)
\]

\[
F(\alpha)= 2t_d f_{sw} V_{d} I \sin(\alpha - \phi)
\]  

(2.7)

\[
P_{C,FW} = \frac{1}{\pi} \int_{0}^{\pi} F(\alpha) d(\alpha)
\]

\[
F(\alpha)= (1 - D_{eq}) I^2 \sin^2(\alpha - \phi) R_{ds},
\]  

(2.8)

where $D_{eq}$ is the equivalent duty ratio that includes the affect of dead time on channel losses, $V_d$ represents the voltage drop across the body diode of the switch and $t_d$ is the deadtime duration.

**Hybrid UP-PWM**

This PWM scheme shown in Fig. 2.10 is almost similar to modified UP PWM (c.f. Fig. 2.6), except for the negative power duration. In this PWM scheme bridge switches are kept permanently off during negative power duration. Hence, the channel conduction losses of bridge switches and by-pass switches can be estimated by (2.3) and (2.5) respectively. While reverse conduction losses can be estimated by (2.9).

\[
P_{RC} = \frac{1}{2\pi} \int_{\pi}^{\pi + \phi} F(\alpha) d(\alpha)
\]

\[
F(\alpha)= V_d M \sin(\alpha - \phi) I \sin(\alpha - \phi)
\]  

(2.9)

More detailed analysis and comparison of these PWM schemes can be found in Publication III.

**Model Verification**

PLECs and MATLAB based simulations are made to verify the mathematical equations developed to calculate the conduction losses. A 650 V, 15 A
GaN HEMT "GS66504B" from GaN systems has been chosen. To emulate a non-unity load, a RL load is connected on the AC side of the inverter. Key simulation parameters are given in Table 2.2.

Table 2.2. Simulation parameters for HERIC inverter

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DC}$</td>
<td>DC Bus Voltage</td>
<td>200 V</td>
</tr>
<tr>
<td>$f$</td>
<td>Fundamental Frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Switching Frequency</td>
<td>100 kHz</td>
</tr>
<tr>
<td>$M$</td>
<td>Modulation Index</td>
<td>0.9</td>
</tr>
<tr>
<td>$t_d$</td>
<td>Dead Time</td>
<td>50 ns</td>
</tr>
<tr>
<td>$\phi$</td>
<td>Load Angle</td>
<td>19°</td>
</tr>
<tr>
<td>$R_L$</td>
<td>Load Resistance</td>
<td>20 Ω</td>
</tr>
<tr>
<td>$L_f$</td>
<td>AC Side Inductance</td>
<td>23 mH</td>
</tr>
<tr>
<td>$V_d$</td>
<td>Body Diode Voltage Drop @ $V_{gs} = -3$ V</td>
<td>4.5 V</td>
</tr>
</tbody>
</table>

Average conduction losses calculated from derived mathematical equations and simulations are compared in Fig. 2.11. $P_{RC}$ and $P_C$ are the average reverse conduction and channel conduction losses respectively. It can be seen that the developed mathematical models can accurately estimate the conduction losses including the affect of dead time and reverse conduction. Hybrid UP-PWM and modified UP-PWM schemes are similar to each other except during the negative power duration, hence, results for only hybrid UP-PWM are shown in Fig. 2.11.

Comparison of conduction losses with hybrid UP PWM (c.f. Fig. 2.10) and modified UP PWM scheme (c.f. Fig. 2.6) is shown in Fig. 2.12. These losses are calculated with the application of mathematical model that were presented in previous sections.

Channel conduction losses ($P_C$) remain same in both PWM schemes, however reverse conduction losses ($P_{RC}$) with hybrid UP PWM scheme
increased exponentially due to high voltage drop across the body diode of the bridge switch (Q2).

2.3.3 Experimental Validation

A practical prototype of HERIC inverter is designed and implemented for validation of the mathematical models presented in the previous sections. The prototype is shown Fig. 2.13, where each switch along with its gate driving circuit is marked. It must be noted that the switches Q3 and Q4 are soldered directly beneath their respective gate driving circuits to reduce the parasitic loop inductance.

An isolated integrated circuit (IC) from Silicon labs (Si8271x) has been selected as a gate driver. A major criterion for selecting this IC was its high common-mode transient immunity (CMTI) of 200 kV/\mu s. Since these GaN switches can turn-on and turn-off in tens of nano-seconds, it is very critical that the isolation barrier of gate driving circuit has high CMTI to reject the
CM noise from switches to pollute the operation of digital-signal-processor (DSP).

Selected gate driver IC is powered up by a circuit shown in Fig. 2.14. An isolated DC/DC converter is used to boost up the 5 V from auxiliary supply to 9 V. With the application of a zener diode, the output voltage of the converter is split to generate 6 V turn-on voltage and 3 V turn-off voltage. In Fig. 2.14, $V_{DD}$ and $V_{EE}$ represent the positive and negative power terminal of the gate driver IC respectively. While, 'S' shows the source terminal of the switch. Similar to CMTI of an isolated gate driver IC, a high CM noise rejection ratio is also required for isolated DC/DC converter. An isolated DC/DC converter with low isolation capacitance (high isolation barrier [5]) of 20 pF to 75 pF from RECOM power has been selected.

\[ \text{Figure 2.14. Circuit to generate negative bias for gate driving circuit} \]

For the initial design, a 20Ω turn-on resistor and 2Ω turn-off resistor have been selected. UP-PWM scheme with dead-time (c.f. Fig. 2.9) is generated by TMS320F28388D, a 32-bit micro-controller from Texas Instrument. Fig. 2.15 shows the measured output voltage and current of the HERIC inverter. Output voltage changes it polarity during the deadtime in between bridge and free-wheeling switches. This can be clearly seen during the positive and negative half-cycle in Fig. 2.15.

Initial tests were done at DC-bus voltage of 25 V and 1 A pk AC side load. However, the inverter did not work as it was intended to operate. There was high-frequency high-voltage noise present during the positive half cycle. To debug the possible cause of this phenomena, drain to source voltages of all four bridge switches were measured and their zoomed in versions are shown in Fig. 2.16.

During positive half cycle, when $Q_1$ and $Q_4$ are switched-off and before the free-wheeling switches $Q_5$ and $Q_6$ are switched-on, current will flow from AC side to DC side through the switches $Q_2$ and $Q_3$. During this duration, drain to source voltage of reverse conducting switches are clamped to $-4\,V$ (as can be seen in Fig. 2.16b and Fig. 2.16c). Similarly, before the $Q_1$ and $Q_4$ are switched-on, $Q_2$ and $Q_3$ conduct in reverse direction during the deadtime. As the DC voltage is increased beyond 25 V, the inverter starts behaving haphazardly and ends in blowing up the switches. To investigate
Figure 2.15. Measured output voltage and current of HERIC inverter (CH3 - Purple $V_{AC} : 25 \text{ V/Div}$, CH4 - Green $i_g : 1 \text{ A/Div}$)

(a) $Q_1$

(b) $Q_2$

(c) $Q_3$

(d) $Q_4$

Figure 2.16. Drain to source voltages of HERIC inverter switches during positive half-cycle - Marked switching transitions to show the switching imbalance (CH1 $V_{DS} : 5 \text{ V/Div}$)

the cause of this behaviour, tests were conducted at multiple switching frequencies ($10 \text{ kHz} - 100 \text{ kHz}$) and dead-times ($50 \text{ ns} - 100 \text{ ns}$), but it did not affect this phenomena. However, upon increasing turn-on resistance ($10 \Omega - 50 \Omega$) inverter did work beyond $25 V_{DC}$, but failed around $50 V_{DC}$. For all these tests, DC bus capacitance was kept constant ($20 \text{ uF}$ film...
capacitors and 4 $uF$ ceramic capacitors).

Upon careful observation of switching waveforms shown in Fig. 2.16, it can be seen that switching speed of one half-bridge (consists of $Q_3$ and $Q_4$) is slower than the other half-bridge (constitutes $Q_1$ and $Q_2$). When switches are switched-off, $Q_1$ switches-off faster than $Q_4$ and also reverse conduction via $Q_2$ starts faster than $Q_3$. This switching imbalance could be the possible cause of inverter failure. Since, $Q_3$ and $Q_1$ were not placed on the same PCB layer as their gate driving circuits, additional inductance of PCB vias could be the possible culprit of this phenomena. Moreover, current layout is also not balanced in terms of distance between bridge switches and free-wheeling switches (c.f. Fig. 2.13). It is very critical for GaN based inverters to minimize this distance [5]. Multiple versions of the prototype with various layout techniques are under design at the moment and results will be reported in the future publications.
3. High Voltage Gain DC-DC Converter

A high voltage gain boost converter also known as high step up (HSU) converter is an essential part of various applications including uninterruptible power supplies (UPS), electrical vehicles (EV) and renewable energy systems [45, 46]. Usually such converters require a multi-phase coupled inductor [47] and with the application of GaN devices, design of such magnetic components can be further optimized. Hence, in this chapter a HSU converter introduced in [48] has been discussed in detail and the design of its required inductor structure is optimized for high-frequency operation with GaN devices.

3.1 HSU Converter Topology

In this section, operation principle of selected HSU converter topology shown in Fig. 3.1a is discussed. This converter has a magnetic coupled-inductor, composed of three windings installed only in one core as shown in Fig. 3.1b.

(a) HSU Converter Topology  (b) Three-Winding Coupled Inductor

Figure 3.1. Selected HSU converter

To achieve this specific magnetic integration, a three-leg magnetic structure is used. Such structure can be achieved with EI, EE, EER, EC core shapes. In these shapes, each winding is possible to be installed in each leg of the core. The external windings are directly coupled and an air-gap may
be installed in each external leg in order to suppress DC flux induction. Moreover, each external winding, \( L_1 \) and \( L_2 \), is connected to the power source, and the central winding \( L_C \) is located between the cathodes of \( D_1 \) and \( D_2 \). Both switches \( S_1 \) and \( S_2 \) are switched at high frequency with gate pulses shifted by \( 180^\circ \) from each other. Fig. 3.2 demonstrates different operating modes of the converter. Detailed analysis of each mode can be studied from Publication IV.

Mathematical expressions for voltage gain calculation of the converter for duty ratio less than 0.5 and greater than 0.5 are given in (3.1) and (3.2) respectively.

\[
M_{D<0.5} = \frac{1 + N}{(1 + N) - D(1 + 2N) + \frac{R_L(1+N)(1+N)}{2R_o(1-D)}} \tag{3.1}
\]

\[
M_{D>0.5} = \frac{1 + N}{(1 - D) + \frac{R_L(1+N)(1+N)}{2R_o(1-D)}} \tag{3.2}
\]

Where \( N \) represents the turns ratio between central winding \( (L_C) \) and external winding \( (L_1 \) or \( L_2 \)) of the inductor. \( D \) is duty ratio of switches while \( R_L \) and \( R_o \) represents series winding resistance and output load resistance respectively. As voltage gain \( (M) \) of the converter is directly proportional to the winding turn ratio \( (N) \), hence gain can increased by increased the number of turns of central winding \( (L_C) \). However, the number of turns are restricted by the available window space in magnetic core.
3.1.1 Practical Performance of Converter

To evaluate the performance of the converter with GaN devices a practical prototype is implemented with parameters presented in Table 3.1.

Table 3.1. HSU converter prototype parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_o$</td>
<td>Output power</td>
<td>200 W</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Switching frequency</td>
<td>50 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>150 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>200 kHz</td>
</tr>
<tr>
<td>$d$</td>
<td>Duty Ratio</td>
<td>0.3 - 0.7</td>
</tr>
<tr>
<td>$L_1 = L_2$</td>
<td>Inductance external legs</td>
<td>302 μH</td>
</tr>
<tr>
<td>$L_C$</td>
<td>Inductance central leg</td>
<td>2.22 mH</td>
</tr>
<tr>
<td>$N$</td>
<td>Turns ratio</td>
<td>2</td>
</tr>
<tr>
<td>$R_L$</td>
<td>Winding resistance</td>
<td>1.10 Ω</td>
</tr>
<tr>
<td>$R_O$</td>
<td>Load resistance</td>
<td>1.60 Ω</td>
</tr>
</tbody>
</table>

PWM signals for both switching devices are generated by a digital signal processor from Texas Instrument (F28388D). A wire wound variable resistance box is used as a load and table top variable DC supply is employed to supply the input power. Two true RMS multi-meters from Fluke are connected in series with the converter to measure the input and output current and two more similar multi-meters are used to measure the input and output voltages. These measured currents and voltages are used to calculate the efficiency of the converter. Gain of the converter is varied by changing the duty ratio of the PWM signals generated by the digital signal processor. Complete model numbers of the equipment used during this testing is given in Appendix I. Converter prototype along with multi-winding coupled inductor and efficiency results are shown Fig. 3.3a and Fig.3.3b respectively.

The results revealed that due to presence of parasitic elements in the converter, voltage gain and efficiency of the converter drops as the switching frequency is increased. Hence, to avail the benefits of GaN devices at higher switching frequencies, it is critical to have an accurate high-frequency model of the converter.
In addition to affecting performance of the converter, parasitic elements also worsen its high-frequency electrical noise emissions. Especially, with faster transition times, characteristic of GaN devices, result in a higher commutation $\frac{dv}{dt}$ and $\frac{di}{dt}$ at switching nodes that increase the electromagnetic interference (EMI) generation in power converters [6,49]. Multiple studies including [6,13,14,49,50] have reached the conclusion that WBG devices based power converters do require extra measures to mitigate EMI.

To develop a high-frequency model of the converter, noise sources along with possible parasitic elements in HSU converter are shown in Fig. 3.4.

Major noise sources in the converter that includes high-frequency switches $S_1$ and $S_2$ are replaced with equivalent voltage sources $V_{S1}$ and $V_{S2}$. Similarly, high-frequency ripple voltage across the input and output capacitance is represented by $V_{IN}$ and $V_{CO}$ respectively, whereas the noise generated by reverse recovery current and charge stored in parasitic capacitance
of the diode is represented by equivalent current sources \(I_{D1}, \ldots I_{D4}\). By principle of superposition, an equivalent impedance network for each noise source can be formed to analyze and reduce its emissions.

Conducted emissions of the converter are measured with different switching transition times at constant switching frequency (300 kHz) to show that switching devices (GaN HEMTs) are indeed the major source of high-frequency noise in a power converter. Measurement results are shown in Fig. 3.5. It can be seen that when the turn on time of the switches is reduced from 14 ns to 11.2 ns, conducted emissions peaks over 1 MHz frequency spectrum are increased. This switching transition times are changed by reducing the gate source resistance of the switches from 20 \(\Omega\) to 10 \(\Omega\). For more details on this topic, please refer to Publication V.

Parasitic elements in the converter, especially equivalent parasitic capacitance (EPC) of inductor windings, provide a propagation path to the high-frequency noise. Hence, by reducing the parasitic capacitance of the inductor, over all high-frequency noise can be reduced [15, 51–55]. The magnitude of this capacitance depends on the physical structure and winding configuration of an inductive component [53, 56–58].

### 3.3 Comprehensive Model of Three-Winding Coupled Inductor

Multiple studies [54, 59–65] have presented various modelling techniques including reluctance models, inductance dual models, gyrator-capacitor models, and extended cantilever to model the inductances in a n-winding coupled inductor. However, parasitic capacitance in these n-winding models have not been considered. An extensive model of a two-winding coupled toroidal CM choke including parasitic capacitances has been presented in [66, 67]. This model was based on theoretical and experimental parame-
However, an extensive model with inductances and parasitic capacitances for a multi-winding (> 2) coupled inductor is still needed to be addressed. In a three-winding HSU inductor, there can be fifteen equivalent stray capacitances including three EPC and twelve inter-winding capacitances as illustrated in Fig. 3.6.

![Figure 3.6. Stray Capacitances in Three-Winding HSU Inductor](image)

In this figure, winding terminals are labeled as j and j'; j=1,2,3 and the respective parasitic capacitances between each terminal are indicated with subscripts. The most significant contributions for the lowest self-resonance frequency arises from EPC i.e., $C_{11'}, C_{22'}, C_{33'}$ (c.f. Fig. 3.6) [68]. The value of EPC ($C_P$) is determined by the summation of intra-winding capacitance ($C_C$) and capacitances between winding to core parts ($C_W$), which can be expressed as in 3.3.

$$C_P = C_W + C_C$$ (3.3)

The intra-winding capacitance ($C_W$) and capacitances between winding to core parts ($C_C$) can be calculated using effective parallel plate model by mathematical equations 3.4 and 3.5 respectively [68].

$$C_W = \alpha_w \epsilon_w \frac{2\pi h_w}{ln(1 + d_w/r)}$$ (3.4)

$$C_C = \alpha_c \epsilon_c \frac{A_c}{d_c}$$ (3.5)

where $\epsilon_w$ and $\epsilon_c$ are the effective permittivity, $h$ and $r$ are height and the radius of the winding, respectively, $d_w$ and $d_c$ are the effective distances between two turns and core plates, respectively, $A_c$ is the area of the plate, and $\alpha_{w,c}$ is the weighting factor.

In the subsequent sections, a comprehensive model of HSU inductor structure including high-frequency parasitic elements is presented by the application of finite element analysis (FEA) simulations and experimental parameter extraction technique.
3.3.1 FEA Model

With the application of FEA simulations, self-resonance frequency of the inductor can be estimated by computing its high-frequency impedance. Self-resonance frequency of the winding is given by

$$f_R = \frac{1}{2\pi \sqrt{LC}}. \quad (3.6)$$

Where $L$ is the self-inductance and $C$ is parasitic capacitance (EPC) of the coil.

If the number of turns are increased while keeping the self-inductance of the winding constant, EPC of inductor winding will increase, which will in turn reduce the self-resonance frequency. Hence, to evaluate the effect of the core size and number of turns on parasitic capacitance, the self-resonance frequency of the HSU inductor is computed while keeping the inductance constant. To perform FEM simulations, a 3D model of the inductor shown in Fig. 3.7 is designed in COMSOL.

![Figure 3.7. Inductor 3-D Model](image)

FEM simulations are performed on HSU inductors with three different core sizes while keeping the self-inductance constant. Magneto-static simulations are performed to calculate the number of turns required for each core to achieve similar self-inductance value. Detailed criteria for core selection and their parameters can be found in Publication VI. Reactance curves obtained from simulations for external and central windings are shown in Fig. 3.8a and Fig. 3.8b respectively.

Since both external windings ($L_1, L_2$) have identical design and impedance characteristics, reactance curves for only one winding are shown. The central winding has twice the number of turns than external windings, thus resulting in higher parasitic capacitance and lower self-resonance frequency (c.f. Fig. 3.8b). As the core size is reduced from EC-120 to EC-70, resonance frequency has been reduced from 7 MHz to 5 MHz for external winding while it reduced from 3.5 MHz to 2.5 MHz for central winding.

Simulation results obtained from this model emphasis the need of an
detailed high-frequency model of a multi-winding \((N > 2)\) transformer and a procedure to accurately measure the values of these parasitic elements. Hence, the study is further continued and an experimentally extracted model is presented in the following section. That model is validated by measuring the conducted emissions of the converter. To validate the generalization of the presented methodology and model, tests are conducted with two different inductor prototypes and three different switching frequencies.

### 3.3.2 Experimental Parameter Extraction

For clarity of terminal notations used in this section and subsequent subsections, a 3-winding coupled inductor using an E-core is shown in Fig. 3.9a. Note that the terminals of the three windings are named as \(i_{a,b}\), where \(i\) is winding number (1, 2, or 3) and subscript \(a\) (or \(b\)) represents the same polarity in all windings. The equivalent circuit of the high-frequency model of a 3-winding inductor is shown in Fig. 3.9b, where self-inductances of the windings \(L_i\) \((i \in 1, 2, 3)\) and mutual-inductances between windings \(M_{ij}\) \((i, j \in 1, 2, 3)\) represent the magnetic interactions between coils. Twelve intra-winding capacitances Fig. 3.6 are lumped into three capacitances and are represented as \(C_{ij}\) \((i, j \in 1, 2, 3)\).

This proposed parameter extraction method is divided into two parts: low-frequency model and high-frequency models. When the frequency is much less than the minimum resonance frequency considering any inductance and capacitance combination, then the impedance of all the capacitances are much larger than that of the inductor. Therefore, all the parasitic capacitances can be considered as open-circuited. Therefore, in low-frequency range only the self-inductances and mutual inductances for the model are considered. On the other hand, when the frequency is high, both inductances and parasitic capacitances should be taken into account. It should also be noted that all the circuit parameters are assumed to be...
dispersion-less (i.e., the variation of parameter value with respect to the frequency is negligible).

**Low-Frequency Model**
Self-inductances of each windings are measured at low frequency while all the other windings are kept open. As the measurement frequency is much less than the resonant frequency, all the windings other than the measured one will have negligibly small coil currents, which makes the effects of parasitic capacitances and mutual inductances negligible at the measured frequency. Next, for mutual inductance measurement, four different measurements (namely, test cases a–d) are made with series connected windings, as illustrated in Fig. 3.10. Note that the direction of the flux generated by each winding is illustrated with red and blue arrows.

\[
\begin{align*}
L_a &= (L_1 + L_2 + L_3) - 2(M_{12} + M_{13} + M_{23}) \\
L_b &= (L_1 + L_2 + L_3) - 2(-M_{12} - M_{13} + M_{23}) \\
L_c &= (L_1 + L_2 + L_3) - 2(-M_{12} + M_{13} - M_{23}) \\
L_d &= (L_1 + L_2 + L_3) - 2(M_{12} - M_{13} - M_{23})
\end{align*}
\] (3.7)
where \( L_{a,b,c,d} \) are measured equivalent inductances of four test cases a,b,c, and d, respectively. Mutual inductances between three windings (i.e., \( M_{12}, M_{13}, \) and \( M_{23} \)) can easily be calculated in terms of measured \( L_{a,b,c,d} \).

**High-Frequency Model**

Three types of impedance measurements are performed to compute the values of parasitic capacitances, namely parallel winding measurement (Fig. 3.11a), series winding measurement (Fig. 3.11b), and short-circuited winding measurement (Fig. 3.11c). In all the three types of measurements, at least one of the winding is short circuited, and the measurement leads are connected across the other two windings. The measurement cases are named with the winding numbers that are connected across the measurement leads, for example, \( m_{A,13} \) means the winding 2 is short circuited and winding 1 and 3 are connected to measurement leads (c.f. Fig. 3.11a).

![Figure 3.11. Test cases for high-frequency model](image)

For the subsequent impedance analysis, it is assumed that the parasitic effects from connecting wires and measurement leads are negligibly small.

All three test configurations shown in Fig. 3.11 can be simplified to parallel LC circuit. (3.8), (3.9) and (3.10) shows the mathematical expression for calculation of equivalent inductance and capacitance for test case \( m_A \) (c.f. Fig. 3.11a), \( m_B \) (c.f. Fig. 3.11b) and \( m_C \) (c.f. Fig. 3.11c) respectively. It must be noted that in test case \( m_C \), all windings are short circuited and hence inductance would be negligible. That is why (3.10) does not include an inductance term.

\[
\begin{align*}
L_{A-ij} &= \frac{L_iL_j - M_{ij}^2}{L_i + L_j + 2M_{ij}} \\
C_{A-ij} &= C_{pi} + C_{pj} + C_{ij} + \frac{C_{ik}C_{jk}}{C_{ik} + C_{jk}}
\end{align*}
\]  

(3.8)
High Voltage Gain DC-DC Converter

\[
L_{B-ij} = \frac{L_i L_j - M_{ij}^2}{L_i + L_j - 2M_{ij}}
\]

\[
C_{B-ij} = C_{ij} + \frac{C_{ik}C_{jk}}{C_{ik} + C_{jk}} + \frac{C_{pi}C_{pj}}{C_{pi} + C_{pj}}
\]  \hspace{1cm} (3.9)

\[
C_{C-ij} = C_{ij} + \frac{C_{ik}C_{jk}}{C_{ik} + C_{jk}}
\]  \hspace{1cm} (3.10)

Values of these equivalent inductances and capacitances are calculated by using the curve fitting tool box in MATLAB, and then the value of each EPC $C_{pi}$ and inter-winding capacitance $C_{ij}$ where $(i, j \in 1, 2, 3)$ is calculated by solving these equations. Further details on calculation of capacitance values can be found in Publication VII.

**Design Example**

To demonstrate the application of modelling technique introduced in the previous section, two HSU inductor structures with identical magnetic properties but different physical designs are constructed. Both inductor prototypes are shown in Fig. 3.12.

![HSU inductor prototypes](image)

*Figure 3.12. HSU inductor prototypes*

Design "a" has a larger magnetic core (ETD-59) as compared to design "b" (ETD-49) and hence to achieve same inductance from both prototypes, design "a" will require lesser number of turns as compared to design "b". After performing both low-frequency and high-frequency test cases on both prototypes, their parameters are summarized in Table 3.2.

As EPC of the winding increases with increase in number of turns, it can be seen from Table 3.2 that design "b" indeed has higher EPC than design "a".

**Model Validation**

As high-frequency emissions of a converter depend on the magnitude of the parasitic elements of the inductor [58]. Hence, to demonstrate the
application of this modelling technique, conducted emissions of a HSU converter (c.f. Section 3.1) with both inductor designs (ETD49, ETD59) and with three different switching frequencies (500 kHz, 750 kHz, 1 MHz) are measured. The test setup is shown in Fig. 3.13. A 5 μH line impedance stabilization network (LISN) with 50Ω output impedance and a spectrum analyzer are utilized to view the frequency spectrum of conducted noise. Operation parameters of HSU converter are kept same for all the test cases and are summarized in Table 3.3.

The frequency range of 150kHz to 50MHz for emissions measurement is selected, as the purpose of noise measurements is not to check the compliance with certain EMI standard but to demonstrate the effect of inductor parasitics on noise peaks. A 20dbm attenuator is used in all measurements at the input of spectrum analyzer for its channel protection.

To help visualize the results, converter emissions with inductor ETD59
Table 3.3. HSU Converter Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>40 VDC</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>200 VDC</td>
</tr>
<tr>
<td>Output Power ($P_o$)</td>
<td>50 W</td>
</tr>
<tr>
<td>Duty Ratio ($d$)</td>
<td>42 %</td>
</tr>
<tr>
<td>Switching Frequency ($f_{sw}$)</td>
<td>500 kHz</td>
</tr>
<tr>
<td></td>
<td>750 kHz</td>
</tr>
<tr>
<td></td>
<td>1 MHz</td>
</tr>
<tr>
<td>Input Current Ripple ($\Delta I_L$)</td>
<td>20% $I_{in}$</td>
</tr>
<tr>
<td>Required Inductance @ 500 kHz ($L$)</td>
<td>246 $\mu$H</td>
</tr>
<tr>
<td>Load Resistance ($R_L$)</td>
<td>800$\Omega$</td>
</tr>
<tr>
<td>Switching Device - GaN HEMT</td>
<td>GS66508B</td>
</tr>
<tr>
<td>SiC Diodes</td>
<td>VS-30ETH06S-M3</td>
</tr>
</tbody>
</table>

(c.f. Fig. 3.12(a)) are subtracted from emissions with inductor ETD49 (c.f. Fig. 3.12(b)) and are presented in Fig. 3.14.

![Graph showing emissions difference between converters with inductors ETD49 and ETD59](image)

**Figure 3.14.** Difference between emissions of converter with inductor ETD49 & ETD59

Since ETD49 has higher EPC than ETD59 (c.f. Table 3.2), it can be seen that it also has higher noise peaks. Especially beyond the frequency range of 20MHz, the difference between their noise peaks becomes more evident. It can also be seen that as the switching frequency in increased from 500kHz to 1MHz, the difference in between noise peaks of two inductors is also increased. Especially around the frequency range of 40MHz in Fig. 3.14 noise difference has been increased form almost 15dB$\mu$V at switching frequency of 500kHz to 20dB$\mu$V at switching frequency of 1MHz.
4. AC/DC Power Supply

In futuristic more electric aircraft (MEA), most of the auxiliary functions are to be performed by electric machines controlled by power electronics converters to reduce the weight of the aircraft, this resulting in decreased fuel consumption and CO$_2$ emissions [69, 70]. Since most of these auxiliary loads are operated by DC voltage, a power supply is required to convert three-phase AC voltage from the aircraft’s grid to DC. A typical two-stage power supply is shown in Fig. 4.1.

![Figure 4.1. Two stage AC/DC power supply](image)

The aircraft’s grid is rated at 115 V$_{\text{RMS}}$ and 400 Hz fundamental frequency while auxiliary loads are mostly rated at 28 V$_{\text{DC}}$ or 270 V$_{\text{DC}}$ [71]. Since power supplies operate at high switching frequencies, to fulfil power quality standards, a filter is employed in between the grid and the power supply. A three-phase power factor correction (PFC) circuit converts three-phase AC voltage to DC voltage while maintaining unity power factor at the input. An isolated DC/DC converter follows after the PFC circuit to regulate the DC voltage level and also to provide electrical isolation in between AC grid and DC loads.

In this chapter, a selection of a rectifier topology based on its compliance with military power quality standards (MIL-STD-461G) [72], design of isolation transformer for DC/DC converter and practical issues in implementation of GaN based power supply will be discussed. All the results and analyses presented in this chapter are taken from Publication VIII, Publication IX and Publication X.
4.1 Three-Phase PFC Topology Selection

Owing to its ability to comply with military power quality standards, a twelve-pulse rectifier topology is usually employed in conventional aircraft’s electrical system of aircrafts [73]. However, it requires a low-frequency (400 Hz) interphase transformer which adds up the volume and weight of the power supply. Hence, to improve the power density of the system by removing the low-frequency transformer, an active PFC topology would be required.

An active PFC circuit can be a buck-type or a boost-type, a uni-directional or a bi-directional topology [74, 75]. Since in this application, a unidirectional flow of power is required, bi-directional three-phase PFC topologies are not considered. In buck-type uni-directional PFC topology family, a six-switch PFC rectifier [76], a nine-switch buck type PFC rectifier [77], delta-type current source PFC rectifier [78] and a Swiss rectifier [79] seem good candidates for this application. However, owing to the simple control implementation, high efficiency and high power-density, Swiss rectifier topology (as shown in Fig. 4.2) has been chosen.

In boost-type uni-directional PFC topology family, Delta rectifier (a two level PFC topology) and Vienna rectifier (a three level PFC topology) provide an efficient and power-dense solution for MEA application [80]. Since a multi-level rectifier topology (Vienna rectifier) is advantageous for applications with high DC bus voltage ($V_{DC} > 600$ V), [80] Delta rectifier, shown in Fig. 4.7 is chosen for this study.

These topologies have already been proven in literature to be efficient and power-dense solutions for aircraft applications [80, 81]; hence, the loss model of these topologies will not be discussed here. However, a study on Swiss rectifier [81] was made for applications with fundamental frequency of 50 Hz and does not include analysis for 400 Hz applications. Furthermore, conducted emissions of Delta rectifier for 400 Hz applications were computed for frequency ranges of 150 kHz – 30 MHz [80]. However, for complete compliance with MIL-STD-461G, it is necessary to evaluate and restrict the low-frequency harmonics (800 Hz – 10 kHz) in addition to high-frequency (10 kHz – 30 MHz) harmonics. Hence, for selection of an appropriate topology for this application, PLECS and MATLAB based simulations of both chosen rectifier topologies are made to evaluate their power quality of mains currents for 400 Hz systems.

4.1.1 Swiss Rectifier Topology

Swiss rectifier shown in Fig. 4.2 also consists of a three-phase bridge to convert 3-phase AC voltage into DC pulsating voltage.

Three bi-directional bi-polar switches ($S_{IA}, S_{IB}, S_{IC}$) are used for the third harmonic injection to achieve unity power factor. These switches operate...
at twice the fundamental frequency (i.e. 800 Hz) and their switching state depends on the operation sector of three-phase input voltage. Each bi-directional switch is switched ON when its corresponding phase ($S_{IA} \rightarrow V_{AN}, S_{IB} \rightarrow V_{BN}, S_{IC} \rightarrow V_{CN}$) (c.f. Fig. 4.2) has the medium value. As in sector 1, phase $V_{AN}$ has maximum and phase $V_{BN}$ has minimum value, hence switch $S_{IC}$ is kept ON throughout this sector.

Switches $S_+$ and $S_-$ are high-frequency switches forming two buck-converters for output voltage regulation. The fact that this topology has only two high-frequency switches makes it a suitable candidate for high efficiency applications. Required duty ratio of these switches can be calculated by (4.1) and (4.2).

\[
d_{S+} = \frac{2V_{DC}}{3\hat{V}_{PH}^2} \max(V_{AN}, V_{BN}, V_{CN}) \tag{4.1}
\]
\[
d_{S-} = \frac{2V_{DC}}{3\hat{V}_{PH}^2} \min(V_{AN}, V_{BN}, V_{CN}) \tag{4.2}
\]

where $V_{DC}$ is output DC bus voltage, $\hat{V}_{PH}$ is the peak value of phase voltage, functions $\max(V_{AN}, V_{BN}, V_{CN})$ and $\min(V_{AN}, V_{BN}, V_{CN})$ represent the maximum and minimum value respectively from all three phases at each instant. Detailed operation principle of this topology can be found in Publication VIII.

**Simulation Design**

To develop an accurate simulation model, a high-frequency input filter is designed. This filter is required to remove the high-frequency ripple component from input current for perfectly sinusoidal current and EMI standard compliance. Size of the filter magnetic components depend on attenuation required for switching frequency harmonic. If the whole attenuation is to be provided by a single stage filter, it will require a low cut-off frequency and hence large filter components. This can be improved by using cascaded designing with two or more stages of LC filters with appropriate damping which will result in smaller filter magnetic components. A multi-stage LC filter with parallel RL damper shown in Fig. 4.3 is selected for this design. $L_f$ and $C_f$ represents the filter inductance and capacitance respectively.
tively. $L_d$ and $R_d$, in turn, represent the damping inductance and resistance respectively. Values of filter components are calculated by computing the required attenuation for switching frequency component in grid current to comply with military EMI standards.

**Figure 4.3.** Two-stage LC filter

**Results**
To check the compliance of designed rectifier with EMI standards, simulations are performed with the parameters summarized in Table 4.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase voltage</td>
<td>$V_{PH}$</td>
<td>115 V RMS</td>
</tr>
<tr>
<td>Fundamental frequency</td>
<td>$f_N$</td>
<td>400 Hz</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_{SW}$</td>
<td>100 kHz</td>
</tr>
<tr>
<td>DC bus voltage</td>
<td>$V_{DC}$</td>
<td>150 V</td>
</tr>
<tr>
<td>DC side inductance</td>
<td>$L_{DC}$</td>
<td>50 μH</td>
</tr>
<tr>
<td>DC side capacitance</td>
<td>$C_{DC}$</td>
<td>10 μF</td>
</tr>
</tbody>
</table>

To compute the low-frequency (800 Hz – 10 kHz) harmonics, the grid current is measured and exported to MATLAB to perform FFT. For high-frequency (10 kHz – 30 MHz) harmonics, a line impedance stabilization network (LISN) is added in between the grid and filter block and voltage is measured across its 50 Ω output impedance. Parasitic elements are also included in the LISN model for accuracy. Resultant low-frequency and high-frequency emissions along with standard limits are shown in Fig. 4.4a and Fig. 4.4b respectively.

By the application of the designed filter, high-frequency emissions shown in Fig. 4.4b are successfully attenuated below the standard limit. However, in low-frequency spectrum (c.f. Fig. 4.4a), few noise peaks around 8 kHz – 10 kHz are above the standard limit. These noise peaks in low-frequency range in this rectifier originates from the glitches in current waveform at phase crossings as shown in Fig. 4.5.

Although THD of the current is less than 5%, this rectifier is not suitable
for aircraft applications until it complies with low-frequency military EMI standards. Hence, to further analyze these harmonics, simulations are repeated with different values of filter capacitances and switching frequencies and the results are shown in Fig. 4.6a and Fig. 4.6b respectively.

These glitches in current waveform originate due to high-frequency voltage ripple across the filter capacitance. It can be seen in Fig. 4.6a and Fig. 4.6b that increasing the filter capacitance and switching frequency reduces these noise peaks but few peaks are still above the standard limit. Since filter capacitance is limited by its required reactive power and switching frequency by the switching losses, they can’t be increased indefinitely. Hence, for this study, Swiss rectifier is not considered anymore. Further work can be done to design a notch filter or closed loop control system to attenuate the harmonics in narrow frequency band of 8 kHz – 10 kHz.
4.1.2 Delta Rectifier Topology

Second topology that was selected for further analysis was Delta Rectifier topology which is shown in Fig. 4.7.

This rectifier is a boost type PFC which consists of a three-phase bridge to convert AC voltage into pulsating DC voltage and three bi-directional bi-polar third-harmonic injection switches. However, unlike in Swiss rectifier, these switches are switched at high frequency. The switching pattern for switches $S_{AB}$ and $S_{BA}$ is shown in Fig. 4.8.
Sectors in Fig. 4.8 are defined based on line-line voltages. Switches $S_{AB}$ and $S_{BA}$ are only switched when their corresponding line-line voltage $V_{AB}$ has either maximum or minimum value. When $V_{AB}$ has maximum value switch $S_{AB}$ is switched at high frequency while $S_{BA}$ is kept permanently on. Similarly when $V_{AB}$ has minimum value, $S_{BA}$ is switched at high frequency while $S_{BA}$ is kept permanently on. The switching pattern of the remaining two switches is also controlled by following the same principle.

**Simulation Design**

A closed loop control loop has been implemented to ensure the sinusoidal input grid currents and to maintain the output dc bus voltage to some reference value. A block diagram of the control loop is shown in Fig. 4.9.

A reference value of current $i_{N,ref}$ is generated by multiplying the instantaneous value of phase voltage $v_N$ by the transconductance $g_e$ which is the output of voltage control loop. Error from the current signal is eliminated by using a proportional resonant (PR) controller. The transfer function of
the controller is given in (4.3).

\[ G_c(z) = k_p \frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + 1} \]  

(4.3)

where \( a_2 = (1 + a_s/T_r) \), \( a_1 = b_1 \), \( a_0 = (1 - a_s/T_r) \) and \( b_1 = -2 \cos(w_g T_s) \). \( k_p \) and \( T_r \) are the proportional gain and the time constant of the controller respectively. And their values are computed by (4.4) and (4.5).

\[ k_p = \frac{\pi L}{6 T_s} \]  

(4.4)

\[ T_r = \frac{60 T_s}{\pi} \]  

(4.5)

where \( T_s \) and \( L \) are sampling time and input boost inductance values respectively. A detailed theoretical background and design procedure of resonant controller can be found in [82].

The voltage control loop is designed by following the methodology presented in [83]. If \( W \) is the actual energy stored in the output DC capacitance bank of the rectifier and \( W_{\text{ref}} \) is the required energy to be stored, in order to maintain the required DC bus voltage, then their transfer function can be represented by (4.6).

\[ \frac{W}{W_{\text{ref}}} = \frac{k p s + k i}{s^2 + k p s + k i} \]  

(4.6)

Controller gains are given as \( k_p = w_o^2 \), \( k_i = w_o \zeta \), where \( w_o \) is the natural frequency and \( \zeta \) is the damping ratio of the control loop.

**Results**

Following the equations presented in the previous subsection, both current loop and voltage loop are designed. Simulations with the parameters summarized in Table 4.2 are performed in PLECS and MATLAB.

**Table 4.2. Simulation parameters for Delta rectifier**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated power</td>
<td>( P )</td>
<td>5 ( kW )</td>
</tr>
<tr>
<td>Phase voltage</td>
<td>( V_{PH} )</td>
<td>115 ( V_{RMS} )</td>
</tr>
<tr>
<td>Fundamental frequency</td>
<td>( f_N )</td>
<td>400 Hz</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>( f_{SW} )</td>
<td>100 kHz</td>
</tr>
<tr>
<td>DC bus voltage</td>
<td>( V_{DC} )</td>
<td>400 V</td>
</tr>
<tr>
<td>Boost inductance</td>
<td>( L_N )</td>
<td>330 ( \mu H )</td>
</tr>
<tr>
<td>DC bus capacitance</td>
<td>( C_{DC} )</td>
<td>1 mF</td>
</tr>
</tbody>
</table>

Three-phase input grid currents and output DC voltage of Delta rectifier are shown in Fig.4.10.
It can be seen in Fig. 4.11 that Delta rectifier complies with both low-frequency and high-frequency emission standards.

This project is still in continuation and based on the results presented in this chapter so far, Delta rectifier is chosen as a front-end rectifier for practical implementation of three-phase AC to DC power supply for aircraft applications.

### 4.2 DC-DC Converter

An isolated DC-DC converter is employed after a front-end three-phase PFC circuit to provide a galvanic isolation between the AC grid and DC side, and also to regulate the output voltage level. Various topologies were considered for this application including: Full Bridge (FB) LLC Converter,
Phase Shifted Full Bridge (PSFB) Converter and Dual Active Bridge (DAB) Converter. FB LLC converter has complicated operation and EMI filter design owing to its variable frequency operation [84]. PSFB converter, in turn, operates at fixed frequency but it requires a secondary center tap transformer along with an additional inductor, which makes the circuit bulky [85]. However, DAB converter provides an efficient and power-dense solution with fixed-frequency operation [86]. Hence, DAB converter is selected for this application.

4.2.1 Dual Active Bridge Converter

DAB converter shown in Fig. 4.12, is an isolated bidirectional DC-DC converter topology.

\[ P = \frac{v_{in}v_{out}\phi(1 - \phi/\pi)n}{2\pi f L_{lk}} \]  

\( v_{in} \) and \( v_{out} \) are the input and output voltages of the converter. While \( \phi \) represents the phase shift between primary and secondary full-bridge modulation signals. \( f \) is the switching frequency and \( L_{lk} \) is the leakage inductance (this inductance could be the leakage inductance of the transformer or can be added externally in case higher inductance is needed for the converter operation).

In our application, only uni-directional power flow is needed. Hence, modulation signals of primary full-bridge will be leading the secondary
side signals. Multiple modulation schemes for this converter have been discussed in literature to further improve the performance of the converter [87]. However, the scope of this study has been kept limited to the design of optimized magnetic components and implementation of converter with GaN switching devices. Hence, the basic modulation scheme, i.e. fixed switching frequency and duty ratio (50%), will be considered for the rest of the study.

4.2.2 Design of an Isolation Transformer

In this section, an optimization tool for the design of a high-frequency, power-dense and efficient isolation transformer will be discussed. By using an iterative optimization algorithm, appropriate magnetic core material, core dimensions, winding wire thickness, required interleaving and optimal switching frequency are evaluated.

Transformer Loss Structure
Transformer losses can be categorized into two main categories; winding losses and core losses.

Losses that incur in the windings of the transformer depends on the DC resistance and AC resistance of the winding conductors. AC resistance accounts for the increase in effective resistance of the conductor due to skin and proximity effects [88]. Excluding high-frequency effects (skin effect and proximity effect), winding losses in terms of average current density "$J$" can be represented as in (4.8).

\[ P_{CU,DC} = \rho_{CU} \times V_{CU} \times J^2 \]  

(4.8)

Nevertheless, in reality the total winding losses are higher due to high-frequency effects. Effective increase in conductor’s resistance due to skin effect and proximity effect is presented by resistance factor \( F_R = \frac{R_{AC}}{R_{DC}} \). Hence, the total winding losses can be approximated by (4.9)

\[ P_{CU,tot} = F_R \times P_{CU,DC} \]  

(4.9)

Value of resistance factor \( F_R \) can be approximated by Dowell’s equation shown in (4.10).

\[ F_R = \frac{\phi \sinh 2\phi + \sin 2\phi}{\cosh 2\phi - \cos 2\phi} + \frac{2(m^2 - 1)}{3} \frac{\phi \sinh \phi - \sin \phi}{\cosh \phi + \cos \phi} \]  

(4.10)

Where \( \phi \) is a ratio between conductor thickness "$d$" and skin depth "$\delta$" at the given frequency \( \phi = \frac{d}{\delta} \). And \( m \) is the number of sheets of foil or litz wire turn on top of each other in the transformer winding.

Core losses of the transformer can be approximated by and defined by
Steinmetz equation described in (4.11)

\[ P_V = k \times f^a \times B^b \]  (4.11)

Where, \( P_V \) are the volumetric losses in the material and \( k, a, b \) are material dependent empirical coefficients, \( f \) is the frequency and peak flux density is represented by \( B \).

**Winding Losses Optimization**

As discussed in the previous section, high-frequency effects in transformers increase the effective resistance of its windings and hence hampers the overall efficiency of the converter. However, by opting thinner winding conductors and interleaving of turns, AC resistance can be reduced [89]. Fig. 4.13 and Fig. 4.14 shows the effect of conductor thickness and interleaving on resistance factor \( (F_R) \) respectively.

**Figure 4.13.** Resistance factor vs winding foil thickness

**Figure 4.14.** Resistance factor vs interleaving, foil thickness of 0.1 mm
It can be seen in Fig. 4.14 that the $F_R$ is improved massively with introduction of the interleaving. $M$ in this figure represents the number of intersections between the primary and secondary windings. As the interleaving is increased, the improvement in $F_R$ becomes smaller, while the complexity and engineering cost of transformer fabrication increases. Hence, for this design, interleaving is restricted to $M = 3$ with winding foil thickness of 0.1 mm.

**Core Losses Optimization**

With an increase in operating frequency, the power density of the magnetic components is increased but core losses (eddy current losses) are also increased. Hence, in order to find an optimal solution, a comprehensive table of available materials from Ferroxcube, TDK, Mag-Inc and Vitroperm was created. To compare the different designs, a quality function $Q = \eta/W$ is defined, where $\eta$ is the efficiency and $W$ is the weight of the transformer. Fig. 4.15 shows the variation of quality function of each selected magnetic material with frequency.

![Figure 4.15. Quality function ($\eta / W$) for selection of magnetic-core material](image)

Based on these results, magnetic material and operation frequency range is selected.

**Design Flow**

An iterative tool is designed to optimize the design of transformer. Flow chart of the algorithm is shown in Fig. 4.16. After initial design parameters and limitations are given, the algorithm estimates the initial size of the magnetic core by equating core and winding losses. Then the required surface area of the magnetic core to dissipate losses is calculated [90]. This process is iterative and the initial losses and core size might be far from optimal. As the algorithm constantly improves the winding structure (by changing number of turns) to minimize both core and winding losses in each step, the end result is the smallest possible losses for a
given transformer size. After single loop, results are stored in a table. The algorithm repeats the design process for given range of operating frequencies and transformer sizes. At the end, the best possible design is selected on the basis of quality function "Q".

**Figure 4.16.** Flow diagram for transformer design

Following the design procedure explained so far and with the aid of
the optimization tool, a transformer is designed with the parameters as summarized in Table 4.3.

**Table 4.3.** Design parameters of high-frequency isolation transformer

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetic Material</td>
<td>3C95</td>
</tr>
<tr>
<td>Core Volume</td>
<td>5.2 cm³</td>
</tr>
<tr>
<td>Core Area</td>
<td>4.2 cm²</td>
</tr>
<tr>
<td>Winding foil thickness</td>
<td>0.05 mm</td>
</tr>
<tr>
<td>Primary voltage</td>
<td>400 V</td>
</tr>
<tr>
<td>Secondary voltage</td>
<td>270 V</td>
</tr>
<tr>
<td>Operation frequency</td>
<td>250 kHz</td>
</tr>
<tr>
<td>Current density</td>
<td>3.3 A/mm²</td>
</tr>
<tr>
<td>Interleaving M</td>
<td>3</td>
</tr>
</tbody>
</table>

It must be noted that in Fig. 4.15, nano-crystalline magnetic material VP500F from Vacuumschmelze has the best quality factor throughout the frequency range. However, in practical design (c.f. Table 4.3), ferrite material 3C95 from Ferroxcube has been used. The reason for this is the unavailability of VP500F magnetic cores in required EE or EI shape. In the future with the availability of these nano-crystalline magnetic cores in more practical shapes will further enhance the performance of the converter.

### 4.2.3 Practical Implementation of DAB Converter

After the fabrication of the designed transformer, DAB converter prototype is built following a modular approach. The same printed circuit board (PCB) design is used for both the full bridges and an additional third board is added for magnetic components (External inductance "Llk" and transformer). Resultant assembly is shown in Fig. 4.17.

![Figure 4.17. DAB converter practical prototype](image)

Converter is designed to deliver the peak power of 5 kW at 400 VDC input voltage. Top cooled GaN HEMTs from GaN systems are chosen as the
switching device for the converter. Maximum switching current (secondary side current) of the converter would be 18 A, hence GS66508T rated at 30 A is the appropriate choice for our design. However, GS66516T rated at 60 A has half the $R_{ds,ON}$ of GS66508T and hence half the conduction losses. Since one of the main motivations of this project is to obtain ultra-high conversion efficiency, GS66516T is selected as the switching device for both primary and secondary side of the converter. A copper foil-based transformer has a very low leakage inductance ($L_{lk} = 500 \text{nH} @ 100 \text{kHz}$). Hence, an additional 4.7 $\mu$H external inductor is added in series with the transformer.

**Practical Evaluation**

Upon practical evaluation of the converter with purely resistive load, at 35 VDC input voltage and 60 W input power, the circuit behaved in a haphazard manner as can be seen in Fig. 4.18.

![Figure 4.18. High-frequency noise during DAB operation](image)

Voltage at the switching nodes on the primary side on channel 1 (yellow) has a peak to peak value of 374 VDC while on the secondary on channel 2 (green) has 251 VDC. This behavior of the converter at such low input voltages led to catastrophic failures at even slightly higher operating parameters. The noise overshoot and ringing penetrate the gate to source of the GaN device on channel 4 (pink) and leading to higher voltage stresses on the device at gate-to-source as well as drain-to-source junctions which cause device failures.

**Converter Debugging**

Upon careful observation, apart from switching frequency, two ringing frequencies (21.2 MHz and 4.2 MHz) were prominent in the switching waveforms. This ringing is caused by the energy stored in parasitic inductance and capacitances in the circuit and to eliminate it, it is critical to identify these parasitic elements. Drain to source capacitance of the selected switch is $C_{DS} = 120 \text{ pF}$ while inter-winding capacitance of
the transformer is $C_{\text{inter}} = 4 \text{ nF}$. Upon calculation, the resonance frequency of $C_{\text{DS}}$ and $C_{\text{inter}}$ with the measured leakage inductance of the transformer ($L_{lk} = 500 \text{ nH @ 100 kHz}$) comes out to be 20.5 MHz and 3.6 MHz respectively. Additionally, the external inductance has also a self-resonance at 20 MHz which also contributed in sustained ringing.

Apart from parasitic elements of magnetic components, parasitic inductances of the PCB have also a significant impact on the converter operation. With the application of mathematical equations explained in [91], parasitic inductances of PCB are calculated and shown in Fig. 4.19.

![Figure 4.19. Parasitic inductances of the PCB tracks](image)

**Design Modification**

The first prototype resulted in failures and no significant testing in terms of the rated power and voltage could be achieved. Thus, to reduce the parasitic inductances in the layout, a more compact prototype is designed and implemented. The revised version has a single PCB assembly with identical layouts for both the full bridges and is shown in Fig. 4.20.

![Figure 4.20. Improved DAB layout design](image)

In the improved layout design, inductance between top and bottom switch of a half-bridge has been reduced from 5 nH to 1 nH. By placing the transformer on the same board, added inductance of external wires has also been removed.

**Practical Evaluation of Improved Design**

The improved layout was tested at switching frequency of 100 kHz, input DC bus voltage of 100 V, while 850 W of power being delivered. Fig. 4.21
shows the voltage across the GaN device on channel 1 (blue) and current in the device on channel 4 (green).

![AC/DC Power Supply](image)

**Figure 4.21.** Switching waveforms of DAB with improved layout design

Ringing in the current sustains for multiple cycles which increases the losses across the switching device and hampers the overall efficiency of the converter. One possible source of this ringing could be the parasitic capacitance of copper foil-based isolation transformer. To reduce this capacitance, copper foil is replaced with multi-stranded litz wire with a diameter of 0.05 mm (similar to copper foil thickness used in first design). With this design improvement, inter-winding capacitance is reduced from 4 nF to 500 pF. However, leakage inductance of Litz wire based transformer is increased to 870 nH from 500 nH. This increase in leakage inductance can be compensated by reducing the value of external inductance.

To evaluate the effectiveness of reduced parasitic elements in layout and isolation transformer, DAB converter with Litz wire-based transformer was tested at multiple switching frequencies (100 kHz - 300 kHz). Fig. 4.22 shows the switching waveforms of DAB converter at multiple switching frequencies.

It can be seen that by reducing the parasitic elements in layout and transformer, ringing has been reduced significantly, and increasing the switching frequency (upto 300 kHz) does not affect the switching performance of the converter. These results show the significance of optimization of parasitic elements in GaN based power electronics converters. Impact of these parasitic elements on over-all efficiency of the converter are presented in Publication X.
Figure 4.22. Switching waveforms of DAB converter at multiple switching frequencies (Ch1 (Navy Blue): Voltage across Secondary side Device, Ch2 (Sky Blue): Current through Secondary side Device, Ch3 (Pink): Output Current, Ch4 (Green): Voltage across External Leakage Inductor).
5. Conclusion

The application of GaN switching devices makes it possible to enhance the power density and conversion efficiency of the power electronics converter. However, these devices also introduce new challenges, and for an over-all optimized system, it is very critical to address and solve those challenges.

In the first part of this research work, the application of GaN switches in the single-phase solar inverters was discussed. HERIC inverter from the family of transformer-less solar inverters was selected for further study. A major criterion of selection of this topology was its ability to maintain constant CM voltage at switching node and high-efficiency operation. With the aid of SPICE simulations and mathematical modelling, it was shown that for grid-connected applications with $pf = 0.85$, almost $50\%$ of the total conduction losses in the inverter with GaN switches comes from reverse conduction losses when the conventional UP-PWM scheme is employed. These losses were reduced to a mere $6\%$ of the total conduction losses with the application of modified UP-PWM. Although the practical prototype did not work for the intended purpose, it aided in reaching to the conclusion that balanced PCB layout is very significant for the successful implementation of the GaN-based inverter.

A non-isolated DC-DC converter with high voltage gain and power density was selected for the second portion of this research work. This converter produces high voltage gain with the application of three-winding coupled inductor. Upon the practical implementation of the converter with GaN devices, it was shown that the converter performance and voltage gain of the converter is greatly influenced by the parasitic elements of the inductor. This gave motivation for developing a detailed model of the inductor including its parasitic capacitances. The value of these parasitic capacitances were calculated first by performing FEA on 3-D model of the inductor and later by using parametric extraction technique on inductor prototype. For verification of the results, conducted emissions of a HSU converter with GaN switching devices were measured. The measurement results showed that when the inductor with smaller size magnetic core and higher EPC is employed, the converter has higher noise peaks as compared to the
Conclusion

larger inductor but lesser winding EPC. The difference between the noise emissions gets even larger when the switching frequency of the converter is increased, which will result in larger EMI filter requirements to comply with standards. This section provided key insights on the significance of the parasitic elements of the magnetic components.

GaN HEMTs are the suitable candidates for switching devices in power converters for the modernized, more electric aircrafts. Hence, in the third portion of this work, design challenges of an isolated 3-phase AC-DC power supply for 400 Hz operation were presented. For the selection of front-end 3-phase AC to DC rectifier, owing to the low number of high-frequency switches, two topologies namely, the Swiss rectifier and the Delta rectifier, were considered. Simulation models of both the rectifier topologies, including LISN and high-frequency filter were developed to check their compliance with military EMI standards. Based on the results, Delta rectifier topology was selected. For DC-DC converter stage, DAB topology was chosen and an iterative tool was developed to optimize the isolation transformer in terms of its weight and efficiency. High-frequency losses were optimized by interleaving of winding turns and opting a thin copper foil as a winding material. However, during the practical evaluation of the converter, excessive ringing was observed at switching nodes. The source of this ringing was the resonance between the transformer’s inter-winding capacitance and added external inductance. To reduce this inter-winding capacitance, copper foil-based transformer was replaced with litz wire-based transformer, which resulted in significant reduction in ringing. Hence, it is critical to include the parasitic elements of the transformer in the optimization tool in addition to its efficiency and power density.

5.1 Possible Future Continuations

This research work has successfully addressed multiple challenges in the implementation of high-frequency and highly efficient GaN based power electronics converters. It also opened doors to various new research questions related to the system level optimization of these converters.

First part of the work established the fact that mere replacement of Si switches with GaN switches is not enough. A modification in modulation scheme or converter control is often required for overall optimized system performance. However in addition to the modifications in control, optimization of circuit board layouts for high $dv/dt$ operation is still an open challenge. During the whole duration of this research work, it has been observed that specially with non-linear loads high $dv/dt$ introduces significant ringing in switching voltages which often ends up in device failure. Hence, in future, prototyping with GaN switches could be further explored for layout optimization to enhance the reliability of the system.
Second part of the research work concluded that miniaturization of the converters with the aid of high switching GaN devices could possibly worsen the EMI of the converter. Hence, to achieve an overall optimized system a very special attention has to be paid to the increase in parasitics of the magnetic components. This part of the work can be possibly extended to the common mode filters. Since an increase in parasitic capacitance of DM filter will have a direct affect on the required CM filter, it would be of significant value to develop a multi-variant optimization tool for the design of power dense and efficient filtering.

In third part of this work, design challenges of a 400 Hz three-phase AC/DC isolated power supply for aircraft applications has been discussed. A front end three phase AC/DC PFC rectifier is critical for maintaining the grid side power quality and comply with strict military power quality standards. It was concluded that buck type Swiss rectifier in open loop operation does not comply with power quality standards at 400 Hz fundamental frequency. In future conventional or model predictive based closed loop control of this topology can be explored to improve its power quality for possible application in futuristic air-crafts. A boost type delta rectifier with conventional closed loop control is found suitable for this application. However, effect of source impedance is not considered in design of control loop. This could be the future direction of this work. It was also shown that the presence of high parasitic capacitance in isolation transformer of the DC/DC converter stage could result in converter failure. A transformer with copper foil based windings had to be replaced with Litz wire based transformer due to the presence of high parasitic capacitance in the foil based design. This foil based design is preferable due to its low resistive losses. Hence, in future this could be further explored to reduce these parasitic capacitances for its possible application in high frequency and high $dv/dt$ GaN switches.

Even with all these challenges, GaN devices have initiated a new wave of innovation in the field of technology. And in future its impact will be visible in most of the power electronics applications.
References


[31] Bo Yang, Wuhua Li, Yunjie Gu, Wenfeng Cui, and Xiangning He. Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system. IEEE transactions on power electronics, 27(2):752–762, 2011.


References


6. Appendices

6.1 Appendix I

List of the lab equipment that were used during the lab testing.

Table 6.1. Lab equipment used for testing

<table>
<thead>
<tr>
<th>Equipment</th>
<th>Manufacturer</th>
<th>Model Number</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP</td>
<td>Texas Instrument</td>
<td>F28388D</td>
<td>32 – bit</td>
</tr>
<tr>
<td>Load Resistor</td>
<td>Terco</td>
<td>MV1100</td>
<td>3.3 kW</td>
</tr>
<tr>
<td>DC Power Supply</td>
<td>Hewlett Packard</td>
<td>6030A</td>
<td>1 kW</td>
</tr>
<tr>
<td>Multi-meter</td>
<td>Fluke</td>
<td>28II</td>
<td>1 kV 10 A</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>Tektronix</td>
<td>MDO4104C</td>
<td>1 GHz 1 GS/s</td>
</tr>
<tr>
<td>Current Probe</td>
<td>Hioki</td>
<td>3276</td>
<td>100 MHz 30 A</td>
</tr>
<tr>
<td>Soldering Station</td>
<td>JBC</td>
<td>DDE − 2C</td>
<td>450 °C</td>
</tr>
</tbody>
</table>
Since the inception of the first silicon (Si) transistor from Bell Labs in 1948, it has been the most widely used switching device in power electronics converters. However, due to the intrinsic properties of Si material, these devices exhibit limitations in terms of blocking voltage, thermal management, and switching speeds. Gallium nitride (GaN) semiconductor material-based switching devices show superior properties over Si devices. The application of these switching devices has made it possible to achieve ultra-highly efficient and power-dense power converters. However, these devices also give rise to new challenges.

This thesis takes a deep dive into tackling the challenges that are faced during the practical implementation of GaN-based converters. The main contributions of this thesis include: A modified PWM scheme for DC/AC solar inverter to reduce reverse conduction losses and improve its power quality, A high-frequency parasitic model of multi-winding coupled inductor for DC/DC converter to reduce EMI, An iterative tool to optimize the design of magnetic components for a 3-phase isolated AC/DC power supply for aircraft applications.